MAX20471, MAX20472, MAX20472B

Low Voltage Synchronous Boost Converter

General Description

The MAX20471, MAX20472, and MAX20472B are high-efficiency low-voltage DC-DC converters that boost a 3.0V to 4.0V input supply to between 3.8V and 5.25V (factory-configurable) at 500mA or 1A. The boost converters achieve ±1.5% output error over load, line, and temperature range.

The devices feature a 2.2MHz (2.0MHz for MAX20472B) fixed-frequency PWM mode for better noise immunity and load-transient response, and a pulse-frequency modulation mode (skip) for increased efficiency during light-load operation. The 2.2MHz/2.0MHz frequency operation allows for the use of all ceramic capacitors and minimizes external components. The programmable spread-spectrum frequency modulation minimizes radiated electromagnetic emissions. Integrated low-R_{DSON} switches improve efficiency at heavy loads and make the layout a much simpler task with respect to discrete solutions.

Other features include true shutdown, soft-start, overcurrent, and overtemperature protections.

Applications

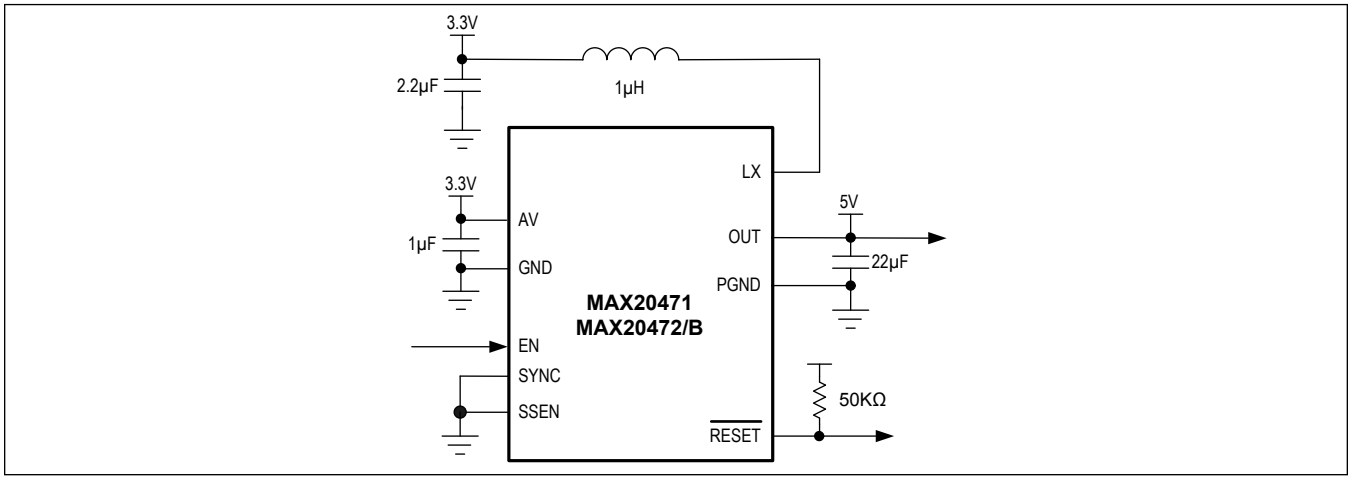
- Automotive Point of Load
- Automotive CAN Transceivers

Benefits and Features

- Multiple Functions for Small Size
  - Synchronous Boost Converter
    - 3.8V to 5.25V Factory-Preset Output in 50mV Steps
    - 500mA and 1A Options
  - 3V to 4V Operating Supply Voltage
  - True Output Shutdown
  - 2.2MHz Operation for the MAX20471, MAX20472
  - 2.0MHz Operation for the MAX20472B
  - Open-Drain Reset Output Pin ($\overline{RESET}$)
  - Spread-Spectrum Enable Pin (SSEN)
- High-Precision
  - ±1.5% Output Voltage Accuracy
  - 93 ±2% UV Monitoring
  - 107 ±2% OV Monitoring
  - Good Load-Transient Performance
- Robust for the Automotive Environment
  - Current-Mode, Forced-PWM and SKIP Operation
  - Overtemperature and Short-Circuit Protection
  - 12-Pin (3mm x 3mm) TDFN
  - 12-Pin (3mm x 3mm) SWTDFN
  - 8-Pin (0.150") SOIC (MAX20471 Only)
  - -40°C to +125°C Automotive Temperature Range

Ordering Information appears at end of datasheet.

Simplified Block Diagram



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Absolute Maximum Ratings

EN, SYNC to GND ..... -0.3V to 6V
AV to GND ..... -0.3V to 6V
RESET to GND ..... -0.3V to 6V
OUT to PGND ..... -0.3V to 6V
SSEN to GND ..... -0.3V to V_{AV}+0.3V
LX to PGND (Note 1) ..... -0.3V to VOUT+0.3V
GND to PGND ..... -0.3V to 0.3V
Maximum Continuous RMS Current 2.5A
Output Short-Circuit Duration ..... Continuous

Continuous Power Dissipation (Note 2)
12-Pin TDFN-EP (derate 24.4 mW/°C > 70°C) 1951mW
12-Pin SWTDFN-EP (derate 24.4 mW/°C > 70°C) 1951mW
8-Pin SOIC (derate 7.8mW/ºC > +70ºC) 623mW
Operating Temperature Range ..... -40°C to 125°C
Junction Temperature ..... +150°C
Storage Temperature Range ..... -65°C to +150°C
Soldering Temperature (reflow) ..... +300°C

Note 1: Self-protected from transient voltages exceeding these limits in circuit under normal operation.

Note 2: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to www.maximintegrated.com/thermal-tutorial.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

12 TDFN

Package Code	TD1233+2C
Outline Number	21-0664
Land Pattern Number	90-0397
Thermal Resistance, Four-Layer Board:	
Junction to Ambient (θ_{JA})	41 °C/W
Junction to Case (θ_{JC})	8.5 °C/W

12 SWTDFN

Package Code	TD1233Y+2C
Outline Number	21-100176
Land Pattern Number	90-100072
Thermal Resistance, Four-Layer Board:	
Junction to Ambient (θ_{JA})	41 °C/W
Junction to Case (θ_{JC})	8.5 °C/W

8 SOIC

Package Code	S8+2C
Outline Number	21-0041
Land Pattern Number	90-0096
Thermal Resistance, Four-Layer Board:	
Junction to Ambient (θ_{JA})	128.4 °C/W
Junction to Case (θ_{JC})	36 °C/W

For the latest package outline information and land patterns (footprints), go to *www.maximintegrated.com/packages*. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to *www.maximintegrated.com/thermal-tutorial*.

Electrical Characteristics

(V_{AV} = 3.3V, EN = 3.3V, T_A = T_J = -40°C to +125°C, unless otherwise noted., Typical values are at T_A = 25 °C under normal conditions unless otherwise noted. (Note 3))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage Range	V_{IN}		3		4	V
UVLO	V_{UVLOR}	Rising	2.48	2.55	2.65	V
	V_{UVLOF}	Falling		2.475		
Shutdown Supply Current	I_{SD}	EN = low		0.1	2	µA
Supply Current	I_{IN}	EN = high, I_{OUT} = 0mA, SYNC low		130		µA
PWM Switching Frequency	f_{SW}	Internally Generated	2	2.2	2.4	MHz
PWM Switching Frequency for MAX20472B	f_{SW}	Internally Generated	1.88	2.0	2.12	MHz
Spread Spectrum	SS	SSEN high		±3		%
OUT						
Voltage Accuracy	V_{OUT}	I_{LOAD} = 0A to I_{MAX}, 3V ≤ V_{AV} ≤ 4V	-1.5		+1.5	%
pMOS On-Resistance	R_{HS}	V_{AV} = 3.3V, I_{LX} = 0.18A		150		mΩ
nMOS On-Resistance	R_{LS}	V_{AV} = 3.3V, I_{LX} = 0.18A		100		mΩ
nMOS Current-Limit Threshold	I_{LIM1}	MAX20471	1.4	1.8	4	A
	I_{LIM2}	MAX20472/MAX20472B	2.8	4.2	7	
pMOS Turn Off Threshold	I_{ZX}			50		mA
LX Leakage Current	I_{LXLKG}	V_{AV} = 6V, LX = PGND or OUT, T_A = 25°C		0.1		µA
Maximum Duty Cycle	DC_{MAX}		90			%
OUT Discharge Resistance	R_{DISCH}	V_{EN} = 0V (connected to OUT)		300		Ω
SKIP Threshold	TH_{SKIP}	Percentage of nMOS current-limit threshold (MAX20471/MAX20472 only)		15		%
Soft-Start Time	t_{SS}			1.9		ms
THERMAL OVERLOAD						
Thermal Shutdown Temperature	T_{SHDN}	T_J rising		165		°C
Hysteresis	T_{HYST}			15		°C
RESET						
OV Threshold	OV_{ACC}	Rising, % of nominal output	105	107	109	%
UV Threshold	UV_{ACC}	Falling, % of nominal output	91	93	95	%

Electrical Characteristics (continued)

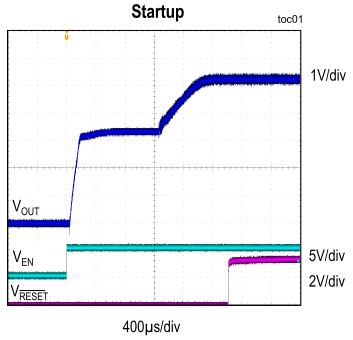
(V_{AV} = 3.3V, EN = 3.3V, T_A = T_J = -40°C to +125°C, unless otherwise noted., Typical values are at T_A = 25 °C under normal conditions unless otherwise noted. (Note 3))

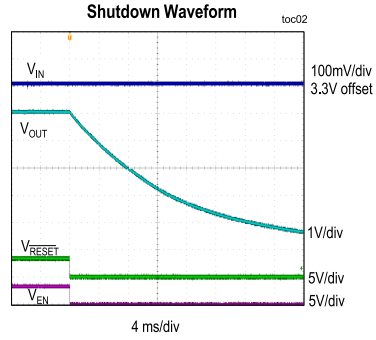
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Active Hold Period	t_{HOLD1}	Option 1 (default)		0.5		ms
	t_{HOLD2}	Option 2		3.7		
	t_{HOLD3}	Option 3		7.4		
	t_{HOLD4}	Option 4		14.8		
Delay Filter	t_{UVDEL}	10% below/above threshold		10		µs
Output-High Leakage Current	I_{RLKG}	T_A = 25°C	-0.5	0.1	+0.5	µA
Output Low Level	V_{ROL}	Sinking -2mA, 3V ≤ V_{AV} ≤ 4V			0.2	V
ENABLE AND SYNC INPUTS						
Input High Level	V_{IH}		1.5			V
Input Low Level	V_{IL}				0.5	V
Input Hysteresis	V_{HYST}			0.1		V
EN Pulldown Current	I_{ENPD}	V_{AV} = 3.3V	0.5	1	2	µA
SYNC Input Pulldown	R_{SYNCPD}	EN high		100		kΩ
SYNC Input Frequency Range	f_{SYNC}		1.7		2.6	MHz

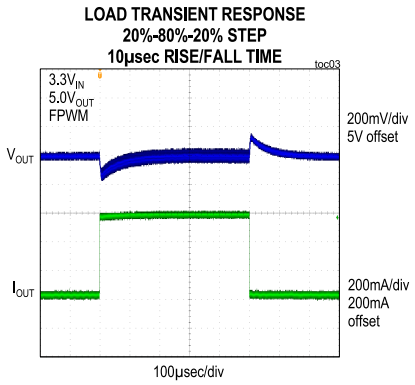
Note 3: All units are 100% production tested at +25˚C. All temperature limits are guaranteed by design and characterization.

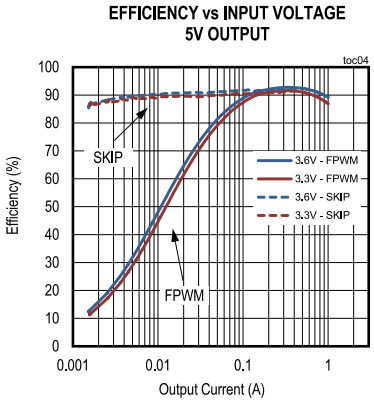
Typical Operating Characteristics

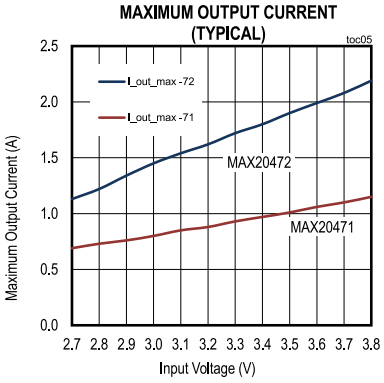
(AV_{VDD} = +3.3V, V_{DDIO} = +1.8V, V_{REFP} - V_{REFN} = V_{REF} = 2.5V; No Line-Frequency Rejection, Continuous-Conversion Mode, Internal Clock; T_A = T_{MIN} to T_{MAX} unless otherwise noted.)

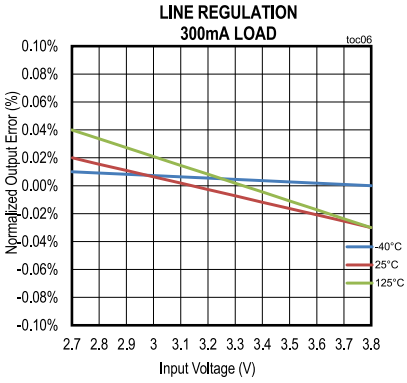






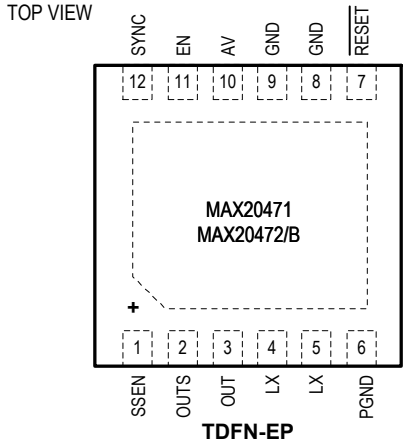






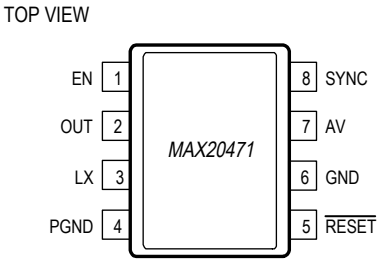
Pin Configurations

MAX20471/MAX20472/MAX20472B



TDFN-EP
SWTDFN-EP
3mm x 3mm

MAX20471



SOIC
(0.150")

Pin Description

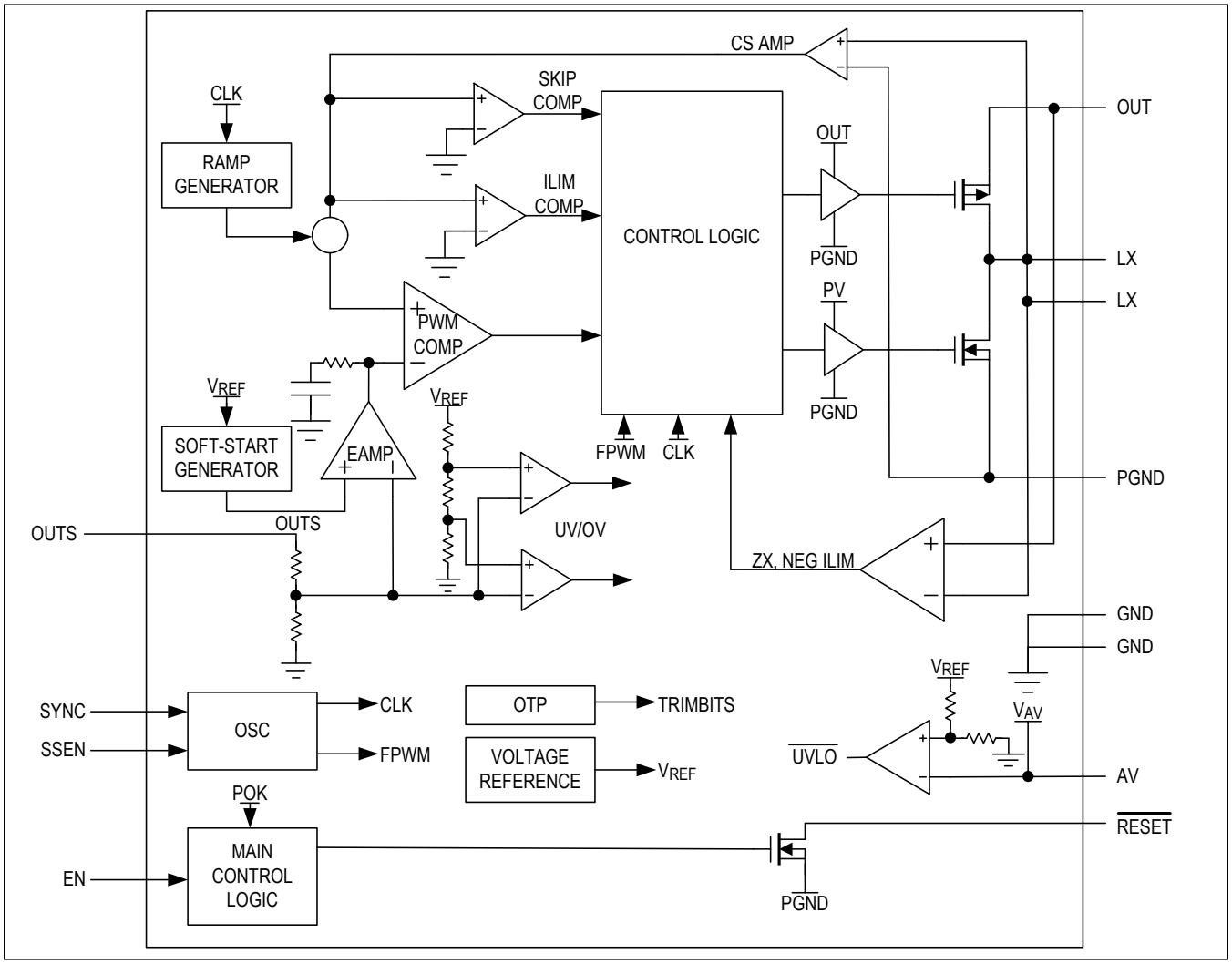
PIN		NAME	FUNCTION
MAX20471/ MAX20472/ MAX20472B	MAX20471		
1	—	SSEN	Spread Spectrum Enable. Connect to V_{AV} to enable spread spectrum.
2	—	OUTS	Output Voltage Feedback Pin. Connect this pin to the output capacitor.
3	2	OUT	Output Voltage.
4, 5	3	LX	Inductor Connection. Connect LX to the switched side of the inductor.
6	4	PGND	Power Ground.
7	5	$\overline{\text{RESET}}$	Open–Drain $\overline{\text{RESET}}$ Output. To obtain a logic signal, pull up $\overline{\text{RESET}}$ with an external resistor.
8	—	GND	Ground. Connect all ground pins to the EP.
9	6		Analog Ground. Connect all ground pins to the EP.

Pin Description (continued)

PIN		NAME	FUNCTION
MAX20471/ MAX20472/ MAX20472B	MAX20471		
10	7	AV	Analog Power Input Supply. Connect a 1µF ceramic capacitor from V_{AV} to GND.
11	1	EN	Active-High Enable. Drive EN HIGH for normal operation.
12	8	SYNC	SYNC Input. Connect SYNC to GND or leave unconnected to enable skip-mode operation under light loads. Connect SYNC to V_{AV} or an external clock to enable fixed-frequency forced-PWM-mode operation.
-	—	EP	Exposed Pad. Connect the exposed pad to ground. Connecting the exposed pad to ground does not remove the requirement for proper ground connections to PGND. The exposed pad is attached with epoxy to the substrate of the die, making it an excellent path to remove heat from the IC.

Functional Diagrams

Diagram 1



Detailed Description

The MAX20471, MAX20472, and MAX20472B are high-efficiency, low-voltage 500mA and 1A synchronous DC-DC boost converter ICs that boost the 3.0V to 4.0V input supply to a fixed output voltage between 3.8V and 5.25V. The boost converters have True Shutdown™, so the output voltage will be 0V when off. The ICs achieve ±1.5% output error over load, line, and temperature ranges.

The ICs feature either a 2.2MHz (MAX20471/MAX20472) or a 2.0MHz (MAX20472B) fixed-frequency FPWM mode for better noise immunity and load-transient response, as well as pulse-frequency operation that allows the use of all-ceramic capacitors, thus minimizing external components. The programmable spread-spectrum frequency modulation minimizes radiated electromagnetic emissions. The spread modulation is factory set to pseudorandom. Integrated low $R_{DS(ON)}$ switches improve efficiency at heavy loads, which makes the layout a much simpler task with respect to discrete solutions.

The ICs contain high-accuracy, factory-set OV/UV thresholds for each output mapped to the $\overline{RESET}$ pin. There are diagnostics on the $\overline{RESET}$ and OUT pins to guarantee high reliability and fail-safe operation. In light-load applications, a logic input (SYNC) allows the ICs to operate either in skip mode for reduced current consumption, or fixed-frequency FPWM mode to eliminate frequency variation and help minimize EMI.

Enable Input (EN)

The EN input activates the ICs' channels from their low-power shutdown state. EN has an input threshold of 1.0V (typ), with hysteresis of 100mV (typ). When EN goes high, the associated output voltage ramps up with the programmed soft-start time.

$\overline{RESET}$ Output

The device features individual open-drain, active-low reset outputs for each output that asserts low when the corresponding output voltage is outside of the UV/OV window. $\overline{RESET}$ remains asserted for a fixed timeout period after the output rises up to its regulated voltage. The fixed timeout period is selectable between 0.5ms, 3.7ms, 7.4ms, or 14.8ms (see the Selector Guide). To obtain a logic signal, place a resistor pullup between $\overline{RESET}$ pins to the system I/O voltage.

Internal Oscillator

The device has a spread-spectrum oscillator that varies the internal operating frequency up by ±3% relative to the internally generated typical operating frequency. This function does not apply to externally applied oscillation frequency. The spread frequency generated is pseudorandom with a repeat rate well below the audio band. Spread spectrum on MAX20471ASAA is enabled as an internal setting. Contact customer support for more details.

Synchronization (SYNC)

The ICs have an on-chip oscillator that provides a 2.2MHz/2.0MHz switching frequency. Depending on the condition of SYNC, two operation modes exist. If SYNC is unconnected or at GND and the load current is below the skip-mode current threshold, the ICs will operate in a highly efficient pulse-skipping mode. If the current is above the threshold, the ICs automatically change to FPWM mode. If SYNC is at V_{AV} or has a frequency applied to it, the ICs will always operate in FPWM mode. The ICs can be switched during operation between FPWM or skip mode by pulling SYNC up to V_{AV} or down to GND.

Soft-Start

The IC includes a fixed soft-start of 1.9ms. Soft-start time limits start-up inrush current by forcing the output voltage to ramp up towards its regulation point.

Current Limit / Short-Circuit Protection

The device features current limit that protects the device against short-circuit and overload conditions at the output. In

the event of a short-circuit or overload condition, the high-side MOSFET remains on until the inductor current reaches the high-side MOSFET's current-limit threshold. The converter then turns on the low-side MOSFET to allow the inductor current to ramp down. Once the inductor current crosses below the low-side MOSFET current-limit threshold, the converter turns on the high-side MOSFET again. This cycle repeats until the short or overload condition is removed.

PWM/SKIP Modes

The device features an input (SYNC) that puts the converter either in SKIP mode for forced PWM mode of operation. See *Pin Descriptions* for mode detail. In PWM mode of operation, the converter switches at a constant frequency with variable on-time. In SKIP mode of operation, the converter's switching frequency is load dependent until the output load reaches a certain threshold. At higher load current, the switching frequency does not change and the operating mode is similar to the PWM mode. SKIP mode helps improve efficiency in light-load applications by allowing the converter to turn on the high-side switch only when the output voltage falls below a set threshold. As such, the converter does not switch MOSFETs on and off as often as is the case in the PWM mode. Consequently, the gate charge and switching losses are much lower in SKIP mode.

Overtemperature Protection

Thermal overload protection limits the total power dissipation in the MAX20471, MAX20472, and MAX20472B. When the junction temperature exceeds 165°C (typ), an internal thermal sensor shuts down the internal bias regulator and the step-down controller, allowing the IC to cool. The thermal sensor turns on the IC again after the junction temperature cools by 15°C.

Boost Converter Short Protection

The boost has protection against startup into short and also protection against short/overload after startup.

Startup into Short

After the boost is enabled, the internal pMOS rectifier is configured as a 2A (typ) current source. This mode of operation is referred to as "charge mode" and is used to charge the output to within 600mV of the input. Under normal circumstances, charge mode is successful and the boost begins switching soft-start to 5.0V. If the output is shorted or overloaded, charge mode will be unable to charge the output to within 600mV of the input. If charge mode lasts for more than 1.9ms, the boost shuts off and automatically attempts restart after 120ms. This automatic restart is called "hiccup mode" and continues indefinitely. Disabling then reenabling the boost overrides the 120ms timer and retries immediately.

Short or Overload after Soft-Start

After soft-start is complete, the boost continues monitoring to ensure that the output is always greater than the 600mV input. If a short or overload condition pulls the output below the 600mV input, the boost stops switching and re-enters the charge-mode configuration. If the output continues to fall below 3.125V, independent of the input voltage, the boost shuts off and enters hiccup mode, as described above.

Applications Information

Input Capacitor

The input filter capacitor reduces peak currents drawn from the power source and reduces noise and voltage ripple on the input caused by the circuit's switching. A 2.2µF X7R ceramic capacitor is recommended for the DC-DC input. A 1µF X7R ceramic capacitor is recommended for the V_{AV} pin.

Inductor Selection

Use a 1µH inductor for MAX20472/MAX20471 and MAX20472B. For a ferrite core, the saturation current should be greater than the maximum current limit. For a soft-saturation core, the saturation current can be less than the maximum current limit as long as the inductance at the maximum current limit is greater than 50% of the nominal inductance.

Boost Output Capacitor

The MAX20471, MAX20472, and MAX20472B is designed to be stable with low-ESR ceramic capacitors. Other capacitor types are not recommended, as the ESR zero can affect stability of the device. The output-capacitor calculations below are guidelines based on nominal conditions. The phase margin must be measured on the final circuit to verify that proper stability is achieved.

$$C_{OUT\_MIN} = \frac{55\ \mu\ sec}{V_{OUT}}$$

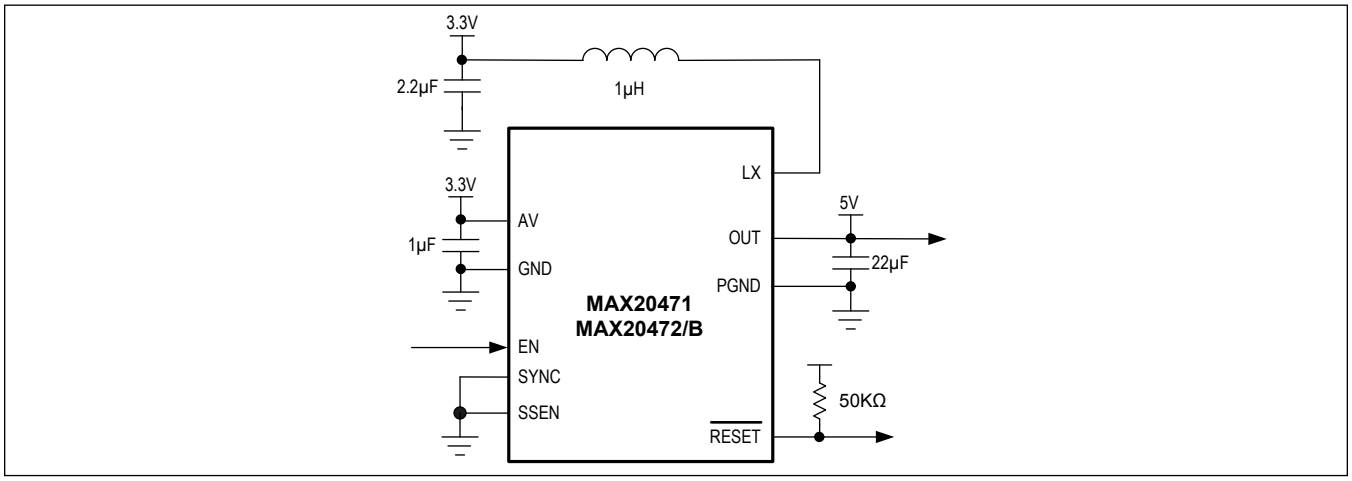
$$C_{OUT\_NOM} = \frac{110\ \mu\ sec}{V_{OUT}}$$

PCB Layout Guidelines

When laying out the PCB, keep the DC-DC power components close together and the routes short to minimize loop area. The output capacitor, power inductor, and input capacitor should be placed close to the IC package. The output capacitor experiences the greatest amount of ripple current, and should be placed closest to the IC. The higher current-carrying traces, such as the input (LX) and OUT, should be wide. Vias should connect the exposed pad of the ICs to provide optimal ground and thermal dissipation connections. A large ground plane should be placed directly below the power traces.

Typical Application Circuits

Circuit 1



Ordering Information

PART NUMBER	TEMP RANGE	PIN-PACKAGE	V_{OUT} (V)	INPUT CURRENT LIMIT (A)
MAX20471ATCA/V+	-40°C to +125°C	12 TDFN-EP*	5	1.8
MAX20471ATCB/V+	-40°C to +125°C	12 TDFN-EP*	5.15	1.8
MAX20471ATCA/VY+	-40°C to +125°C	12 SWTDFN-EP*	5	1.8
MAX20471ASAA/V+	-40°C to +125°C	8 SOIC	5	1.8
MAX20472ATCA/V+	-40°C to +125°C	12 TDFN-EP*	5	4.2
MAX20472ATCB/V+	-40°C to +125°C	12 TDFN-EP*	5.15	4.2
MAX20472ATCC/V+	-40°C to +125°C	12 TDFN-EP*	3.85	4.2
MAX20472ATCA/VY+	-40°C to +125°C	12 SWTDFN-EP*	5	4.2
MAX20472BATCC/V+	-40°C to +125°C	12 TDFN-EP*	3.85	4.2

Note: For variants with different options, contact factory.

/V Denotes an automotive qualified part.

Y Denotes side-wettable

+ Denotes a lead(Pb)-free/RoHS-compliant package.

T = Tape and reel

**EP = Exposed pad.*

***Future product—contact factory for availability*

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	9/17	Initial Release	-
1	1/18	Changed part in Ordering Information table from MAX20471ASA/V+** to MAX20471ASAA/V+** and removed future product status from MAX20472ATCA/V*	9
2	5/18	Updated Internal Oscillator section and added Boost Converter Short Protection, Startup into Short, and Short or Overload after Soft-Start sections	7, 8
3	6/18	Added MAX20472ATCB/V+** (future product) to Ordering Information table.	10
4	9/18	Removed all references to MAX20473 and 2A convertor operation; updated Pin Configuration; updated Functional Diagram; updated Inductor Selection and Output Capacitor sections; updated Typical Application Circuit; removed MAX20473ATCA/V+** and future-part designation for MAX20471ATCB/V+ from the Ordering Information table	1–11
5	11/18	Removed future-part designation for MAX20472ATCB/V+ from the Ordering Information table	11
6	12/18	Updated Package Information table	2
7	3/19	Added information for SWTDFN package to Benefits and Features, Absolute Maximum Ratings, Package Information, Pin Configurations, and Ordering Information; added MAX20472ATCC/V+** to Ordering Information	1, 2, 6, 11
8	6/19	Removed future-part designation from MAX20471ASAA/V+ in the Ordering Information table	11
9	8/19	Added notes to Ordering Information table	11
9.1		Corrected Revision Date for Rev 9 in Revision History	11
10	6/20	Added MAX20472B	1–14
11	8/20	Updated Package Information, Ordering Information	3, 14
12	9/20	Updated Benefits and Features, Absolute Maximum Ratings, Electrical Characteristics, Pin Description, Detailed Description, and Applications Information; removed future-product notation from MAX20471ATCA/VY+T in Ordering Information	1, 3, 4, 5, 7, 8, 10, 12, 13