swissbit®

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Product Data Sheet

Industrial M.2 SATA SSD

X-75m2 P Series

SATA Gen3 – 6.0 Gbit/s, 3D TLC

Commercial and Industrial Temperature Grade

Date: November 18, 2021
Revision: 1.00

Made in Germany

Contents

X-75m2 P Series – Industrial M.2 SATA Solid State Drive 240 GBytes up to 1920 GBytes (PCI Express™ M.2)

1. Product Summary

- **Capacities:** 240 GBytes, 480 GBytes, 960 GBytes, 1920 GBytes
- **Form Factor[1]:** 2280: PCI Express™ M.2 (2280) (80 mm x 22 mm x 3.58 mm)
- **Compliance:** SATA Gen3 – 6 Gbit/s (Gen2 – 3 Gbit/s and Gen1 – 1.5 Gbit/s backward compatible)
- **Command Sets:** Supports ATA/ATAPI-8 and ACS-2
- **Performance:**
  - Burst Transfer Rate: Up to 600 MBytes/s in SATA Gen3 – 6.0 Gbit/s
  - Read Performance: Sequential Read up to 560 MBytes/s, Random Read 4K up to 77,700 IOPS
  - Write Performance: Sequential Write up to 500 MBytes/s, Random Write 4K up to 71,200 IOPS
- **Operating Temperature Range[2]:**
  - Commercial: 0 °C to 70 °C
  - Industrial: -40°C to 85 °C
- **Storage Temperature Range:** -40 °C to 85 °C
- **Operating Voltage:** 3.3 V ± 5%
- **Power (Max):**
  - Read (Active): 1.7 W
  - Write (Active): 2.3 W
  - Idle: 365 mW
  - Partial: 130 mW
- **Data Retention:** 10 Years @ Life Begin / 1 Year @ Life End
- **Endurance in TeraBytes Written (TBW) @ Max Capacity[3]:**
  - Sequential Workload ≥ 6,485
  - Client Workload ≥ 730
  - Enterprise Workload ≥ 1,200
- **Shock/Vibration:** 1,500 *g* / 50 *g*
- **High-Performance 32-Bit Processor with Integrated, Parallel Flash Interface Engines:**
  - Triple-Level Cell (TLC) 3D NAND Flash
  - LDPC ECC with up to 165 bit correction per 1 KByte page (BCH equivalent)
- **High Reliability:**
  - Mean Time Between Failure (MTBF): > 2,000,000 hours
  - Data Reliability: < 1 non-recoverable error per 10^{16} bits read

[1] The verification of the host system and storage device compatibility is the customer's responsibility. Swissbit can provide guidance and support upon request.
[2] Adequate airflow is required to ensure the temperature, as reported in the S.M.A.R.T. data, does not exceed 110°C (industrial temperature drive) and 95°C (commercial temperature drive) respectively.
[3] According to JEDEC (JESD47I), the time to write the full TBW is a minimum of 18 months. Higher average daily data volume reduces the specified TBW. The values listed are estimates and are subject to change without notice.

2. Product Features

- Dynamic and Static Wear Leveling
- Subpage Mode Flash Translation Layer (FTL)
- Active Data Care Management: Adaptive Read Refresh
- Lifetime Enhancements
  - Dynamic Bad Block Remapping
  - Write Amplification Reduction
- On-Board Power Fail Protection
- TRIM and NCQ Support
- ATA Security Feature Set Support
- DEVSLP Compatible
- In-Field Firmware Update[4]
- Enterprise-Grade Self-Monitoring, Analysis, and Reporting Technology (S.M.A.R.T.)
- 30 µinch Gold-Plated Connector (IPC-6012B Class 2 Compliant)
- End-to-End (E2E) Data Protection
- powersafe™ Functionality
- AES256 Encryption (on request)
- TCG OPAL 2.0 Compliant (on request)
- Life Cycle Management
- Controlled "Locked" BOM
- RoHS-6 Compliant
- Swissbit Life Time Monitoring (SBLTM) Tool and SDK for SBLTM (on request)

[4] A host system that supports in-field firmware updates is recommended.

3. Ordering Information

Table 1: Standard Product List

Capacity	Part Number
240 GBytes	SFSA240GMxAK2TA-t-6B-5yB-STD
480 GBytes	SFSA480GMxAK4TA-t-6B-6yB-STD
960 GBytes	SFSA960GMxAK2TA-t-8C-5yB-STD
1920 GBytes	SFSA1T92MxAK4TA-t-8C-6yB-STD

x = product generation; t = temperature grade; y = firmware revision

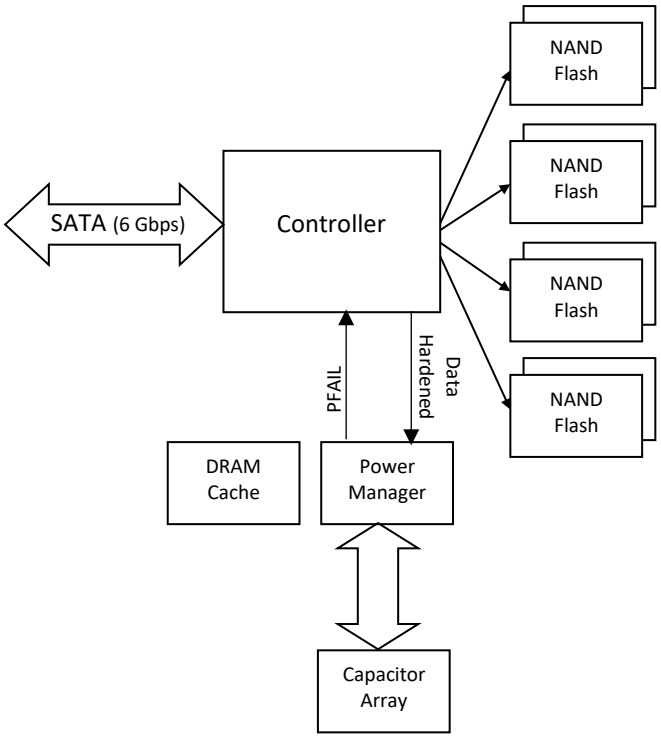
Table 2: Available Part Numbers

Capacity	Commercial Temperature	Industrial Temperature
240 GBytes	SFSA240GM2AK2TA-C-6B-51B-STD	SFSA240GM2AK2TA-I-6B-51B-STD
480 GBytes	SFSA480GM2AK4TA-C-6B-61B-STD	SFSA480GM2AK4TA-I-6B-61B-STD
960 GBytes	SFSA960GM2AK2TA-C-8C-51B-STD	SFSA960GM2AK2TA-I-8C-51B-STD
1920 GBytes	SFSA1T92M2AK4TA-C-8C-61B-STD	SFSA1T92M2AK4TA-I-8C-61B-STD

4. Product Description

The Swissbit X-75m2 P Solid State Drive (SSD) leverages the M.2 SATA industry-standard form factor and connectivity as well as support for AES encryption, E2E security and TCG OPAL standards. Combined with a SATA Gen3 controller and Triple-Level Cell (TLC) 3D NAND flash technology, the X-75m2 P realizes a robust non-volatile storage solution for today's embedded storage applications. The flash of the smaller capacity drives (≤ 120 GBytes) is managed using a mixture of storage as pseudo Single-Level Cell (pSLC) and TLC. This combination allows smaller drives, with fewer flash channels, to maintain a sufficient balance of endurance and performance. A functional block diagram of the X-75m2 P SSD is provided below in Figure 1.

Figure 1: X-75m2 P SATA Functional Block Diagram



The X-75m2 P SSD incorporates a 75-position edge connector with B and M keys to support host read/write, control, and power activity per the applicable JEDEC and SATA IO specifications[5].

The on-board SATA Gen3 controller manages the interface between the host and the non-volatile NAND flash memory array. The controller is designed to support SATA Gen3 (6 Gbit/s) interface speeds and is fully backward compatible with SATA Gen2 (3 Gbit/s) and SATA Gen1 (1.5 Gbit/s) to enable the broadest possible range of platform compatibility. The controller utilizes a high performance 32-bit RISC CPU, providing an optimum balance between read/write performance, Data Care Management and power fail protection.

Swissbit's X-75m2 P SSDs deliver an impressive IOPS rate and endurance by combining TLC 3D NAND flash technology with a high-end controller architecture, firmware and an optimized configuration. The SSDs are designed for applications requiring high data transfer rates (see Table 3: Read/Write Performance). This performance is achieved through an on-board DRAM cache and the 4-channel NAND flash controller interface that supports ONFI and Toggle 2 (400 MT/s) interface speeds. In addition, the X-75m2 P series features Swissbit's proven power fail safety and support for the ATA security feature set, NCQ, TRIM, advanced wear leveling, bad block management and in-field firmware updates.

5 SerialATA IO rev 3.2 Section 6.6, Aug 7, 2013
https://www.jedec.org/standards-documents/focus/flash/solid-state-drives
https://www.sata-io.org/sata-m2-card
http://pcisig.com/specifications, Nov 2013

An on-controller LDPC Error Correction Code (ECC) engine provides the X-75m2 P hardware ECC, which is capable of correcting up to 165 bits per 1 KByte page (BCH equivalent). This engine, combined with Swissbit's Data Care Management firmware, provides active data management strategies to ensure data integrity and extract the maximum possible endurance and reliability from the NAND flash array. These strategies include, but are not limited to, Global Wear Leveling, Adaptive Read Refresh and Dynamic Block Remapping.

The risk of data loss as a result of an unexpected power fail event is mitigated using a robust sequence of voltage regulators, capacitors and detectors designed to ensure a graceful shutdown of the controller and NAND flash array. The combination of hardware and firmware power fail features prevents the possibility of resident data being corrupted during an unexpected power failure.

The Swissbit X-75m2 P offers additional powersafe™ functionality. These drives contain an array of holdup capacitors designed to supply voltage to the controller long enough for data hardening to complete. If the voltage drops below a specified threshold, the PFAIL signal is asserted, notifying the controller of the voltage loss. The controller then begins the process of hardening data and switches the power supply to the power manager from the host to the capacitor array. This allows the controller to complete any writes that were in progress at the time of power loss.

Related Documentation

- Serial ATA International Organization Serial ATA Revision 3.0 (http://www.serialata.org)
- Serial Transport Protocols and Physical Interconnect (ATA/ATAPI-8) (http://www.t13.org)
- AT Attachment Interface Document, American National Standards Institute, X3.298-1997
- PCI Express M.2 standard – PCI Express M.2 Specification, Revision 1.1, December 9, 2016

4.1 Performance Specifications

The X-75m2 P read/write sequential and random CDM performance benchmarks are detailed in the following Table 3.

Table 3: Read/Write Performance[6]

Capacity	Sequential Read (MBPS)	Sequential Write (MBPS)	Random Read 4K (IOPS)	Random Write 4K (IOPS
240 GBytes	560	140	42,700	34,400
480 GBytes	560	305	75,400	71,200
960 GBytes	560	500	77,000	69,600
1920 GBytes	560	390	77,700	66,200

4.2 Current Consumption

The drive-level current consumption as a function of operating mode is shown in the following Table 4.

Table 4: Current Consumption[7]

Drive Capacity	Sequential Read	Sequential Write	Random Read	Random Write	Idle	Partial	Unit
240 GBytes	440	485	445	485	105	25	mA
480 GBytes	500	595	500	590	100	30	
960 GBytes	435	690	415	690	110	35	
1920 GBytes	450	635	350	635	105	40	

4.3 Environmental Specifications

4.3.1 Recommended Operating Conditions

The recommended operating conditions for the X-75m2 P SSD are provided in the following Table 5.

Table 5: Recommended Operating Conditions[8]

Parameter	Value
Commercial Operating Temperature	0 °C to 70 °C
Industrial Operating Temperature	-40 °C to 85 °C
Power Supply V_{CC} Voltage	3.3 V ± 5%

4.3.2 Recommended Storage Conditions

The recommended storage conditions are listed in the following Table 6.

Table 6: Recommended Storage Conditions

Parameter	Value
Commercial Storage Temperature	-40 °C to 85 °C
Industrial Storage Temperature	-40 °C to 85 °C

[6] The values are measured using Crystal Disk Mark 6.0.2. Performance depends on flash type and number, file/cluster size, and burst speed.
[7] All values are the maximum recorded running IOMeter script for Read/Write operations with 1MB transfer size in 1 minute intervals at 25 °C, with nominal supply voltage and SATA transfer rate 6Gb/s.
[8] Adequate airflow is required to ensure the temperature, as reported in the S.M.A.R.T. data, does not exceed 110°C (industrial temperature drive) and 95°C (commercial temperature drive) respectively.

4.3.3 Shock, Vibration and Humidity

The maximum shock, vibration and humidity conditions are listed in the following Table 7.

Table 7: Shock, Vibration and Humidity

Parameter	Value
Non-Operating Shock	1,500 *g*, 0.5 ms pulse duration, half-sine wave (IEC 60068-2-27 and JESD22-B110 cond. B)
Non-Operating Vibration	50 *g*, 80-2,000 Hz, 3 axes, 12 cycles (IEC 60068-2-6, MIL-STD-883 H Method 2007.3)
Humidity (Non-Condensing)	85% RH 85 °C, 1000 hrs, max. supply voltage (JESD22-A101B)

4.4 Regulatory Compliance

The X-75m2 P devices comply with the directives and standards listed in the following Table 8.

Table 8: Regulatory Compliance

Abbreviation	Regulation/ Standard
EMC	CE - 2014/30/EU FCC - 47 CFR Part 15 UKCA - S.I. 2016 No. 1091 and S.I. 2012 No. 3032
RoHS	2011/65/EU with 2015/863/EU and 2017/2102/EU
REACh	1907/2006/EU and 207/2011/EU
WEEE	2012/19/EU

4.5 Mechanical Specifications

The X-75m2 P SSD consists of a flash controller and NAND flash memory devices. The controller interfaces with a host system, allowing data to be written to and read from the flash memory array. The SSD has a PCIe mini connector with a SATA interface. Physical dimensions are detailed in the following Table 9. Figure 3 on page 11 illustrates the X-75m2 P dimensions.

Table 9: Physical Dimensions

Physical Dimensions		Unit
Length	80.00±0.15	mm
Width	22.00±0.15	
Thickness (Max)	4.00	
Weight (Max Capacity)	≤ 12	g

4.6 Reliability and Endurance

The Mean Time Between Failure (MTBF) is specified to exceed the value listed in the following Table 10. Data reliability with effective error tolerance and data retention at the beginning and end of life is also provided.

Table 10: Reliability

Parameter	Value
MTBF (at 25 °C)	> 2,000,000 hours
Data Reliability	< 1 Non-Recoverable Error per 10^{16} Bits Read
Data Retention (up to 40 °C)	10 Years at Start (JESD47), 1 Year at EOL

Endurance represented as both TeraBytes Written (TBW) and full Drive Writes Per Day (DWPD) for different application scenarios is provided in the following Table 11.

Table 11: Endurance[9, 10]

Drive Capacity	Sequential		Client[11]		Enterprise	
	TBW	DWPD[12]	TBW	DWPD[12]	TBW	DWPD[12]
240 GBytes	720	2.74	315	1.20	60	0.23
480 GBytes	1,544	2.94	531	1.01	287	0.55
960 GBytes	3,190	3.04	661	0.63	597	0.57
1920 GBytes	6,486	3.09	734	0.35	1,200	0.57

4.7 Drive Geometry Specification

The X-75m2 P drive geometry is set to report industry standard LBA settings per the IDEMA standard (LBA1-03). The values for each capacity are shown in the following Table 12.

Table 12: Drive Geometry

Raw Capacity	User Capacity[13]	Total LBA	User Addressable Bytes
		Decimal	(Unformatted)
256 GBytes	240 GBytes	468,862,128	240,057,409,536
512 GBytes	480 GBytes	937,703,088	480,103,981,056
1024 GBytes	960 GBytes	1,875,385,008	960,197,124,096
2048 GBytes	1920 GBytes	3,750,748,848	1,920,383,410,176

[9] Client and Enterprise workloads follow the JEDEC JESD219 standard. Enterprise workload values are measured on data storage area and based on 168 hours of runtime. 1 TByte = 10^{12} bytes

[10] According to JEDEC (JESD47I), the time to write the full TBW is a minimum of 18 months. Higher average daily data volume reduces the specified TBW. The values listed are estimates and are subject to change without notice.

[11] Because the JEDEC master trace file for the Client workload is designed for capacities ≥ 60 GBytes, the TBW and DWPD values for the capacities below 60 GBytes are estimates

[12] DWPD values are based on a service life of 3 years

[13] 1 GByte = 10^9 bytes

5. Electrical Interface

This 75-position M.2 connector incorporates both the B and M keys for Socket 2 SATA-based SSDs (Figure 2) and follows the applicable JEDEC specifications. M.2 SSDs follow the SATA I/O specification, offering a maximum performance of 6 Gbit/s. The signal/pin assignments and descriptions are listed in the following Table 13.

Figure 2: X-75m2 P SATA Electrical Interface

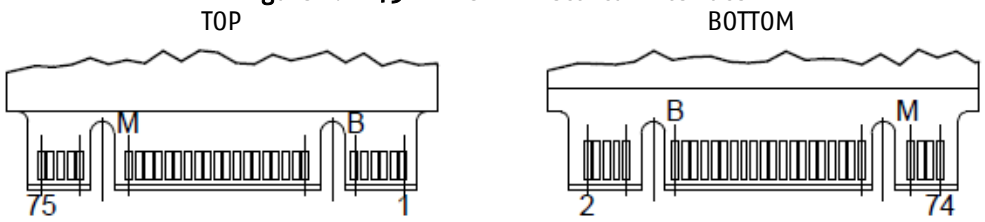


Table 13: Pin Assignment, Name and Description

Description	Assignment	Pin	Pin	Assignment	Description
Config_3	GND	1	2	+3.3V	3.3V Source
Ground	GND	3	4	+3.3V	3.3V Source
No Connect	NC	5	6	NC	No Connect
No Connect	NC	7	8	NC	No Connect
No Connect	NC	9	10	DAS/DSS	DEVACT Device Activity Signal
No Connect	NC	11	12-18	-	Mechanical Notch B
Mechanical Notch B	-	13-19	20	NC	Reserved[14]
Config_0	GND	21	22	NC	Reserved[15]
No Connect	NC	23	24	NC	Reserved
No Connect	NC	25	26	NC	Reserved[16]
Ground	GND	27	28	NC	No Connect
No Connect	NC	29	30	NC	No Connect
No Connect	NC	31	32	NC	No Connect
Ground	GND	33	34	NC	Reserved
No Connect	NC	35	36	NC	Reserved
No Connect	NC	37	38	DEVSLP	Device Sleep, Input
Ground	GND	39	40	NC	Reserved
+SATA Differential Transmit Signal*	B+	41	42	NC	Reserved
-SATA Differential Transmit Signal*	B-	43	44	NC	No Connect
Ground	GND	45	46	NC	Reserved
-SATA Differential Receive Signal*	A-	47	48	NC	Reserved
+SATA Differential Receive Signal*	A+	49	50	NC	No Connect
Ground	GND	51	52	NC	No Connect
No Connect	NC	53	54	NC	No Connect
No Connect	NC	55	56	NC	Reserved
Ground	GND	57	58	NC	Reserved
Mechanical Notch M	-	59-65	60-66	-	Mechanical Notch M
No Connect	NC	67	68	NC	No Connect
Config_1	GND	69	70	3.3V	Supply pin, 3.3V
Ground	GND	71	72	3.3V	Supply pin, 3.3V
Ground	GND	73	74	3.3V	Supply pin, 3.3V
Config_2	GND	75			

*TX (transmit) and RX (receive) pins are labeled from the SSD view and must be connected with the reversed RX and TX signals of the host (i.e., TX to RX and RX to TX).

[14] The write protect option is available on this pin upon request
[15] The quick erase option is available on this pin upon request
[16] The RESET# option is available on this pin upon request

6. Package Mechanical

Figure 3: X-75m2 P SATA SSD Dimensions in mm [in]

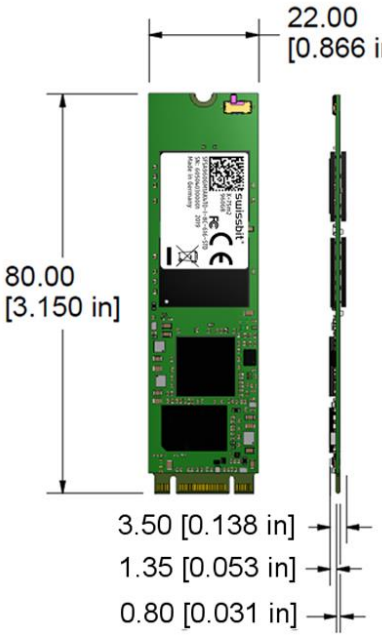
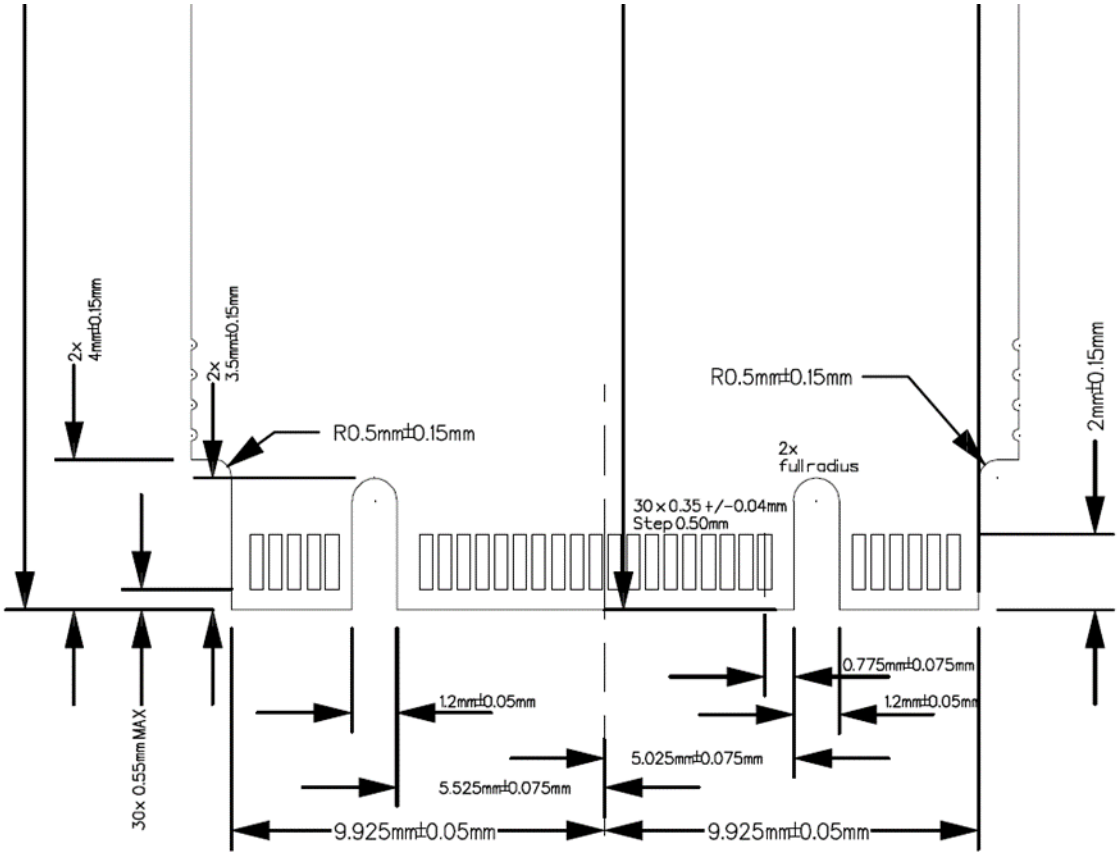


Figure 4: M.2 Connector Dimensions in mm



7. ATA Commands

This section provides information on the ATA commands supported by the SSD. The commands are issued to the device by loading the required registers in the command block with the supplied parameter and then writing the command code to the register. For backward compatibility, some commands are implemented as a "no operation". See the following Table 14 for a list of ATA commands the device supports. For details about setting up the command registers, see the latest ATA Specification.

Table 14: ATA Command Set

Command	Code	Protocol
General Feature Set		
Execute Device Diagnostic	90h	Execute Device Diagnostic
Flush Cache	E7h	Non-data
Identify Device	ECh	PIO data-in
Read DMA	C8h	DMA
Read Multiple	C4h	PIO data-in
Read Sector(s)	20h	PIO data-in
Read Verify Sector(s)	40h or 41h	Non-data
Set Feature	EFh	Non-data
Set Multiple Mode	C6h	Non-data
Write DMA	CAh	DMA
Write Multiple	C5h	PIO data-out
Write Sector(s)	30h	PIO data-out
NOP	00h	Non-data
Read Buffer	E4h	PIO data-in
Write Buffer	E8h	PIO data-out
Write Buffer DMA	E9h	DMA
Download Microcode	92h	PIO data-out
Download Microcode DMA	93h	DMA
Power Management Feature Set		
Check Power Mode	E5h	Non-data
Idle	E3h	Non-data
Idle Immediate	E1h	Non-data
Sleep	E6h	Non-data
Standby	E2h	Non-data
Standby Immediate	E0h	Non-data
Sanitize Feature Set		
Sanitize	B4h	Non-data
Security Mode Feature Set		
Security Set Password	F1h	PIO data-out
Security Unlock	F2h	PIO data-out
Security Erase Prepare	F3h	Non-data
Security Erase Unit	F4h	PIO data-out
Security Freeze Lock	F5h	Non-data
Security Disable Password	F6h	PIO data-out
S.M.A.R.T. Feature Set		
S.M.A.R.T. Disable Operations	B0h	Non-data
S.M.A.R.T. Enable/Disable Autosave	B0h	Non-data
S.M.A.R.T. Enable Operations	B0h	Non-data
S.M.A.R.T. Execute Off-Line Immediate	B0h	Non-data
S.M.A.R.T. Read Data	B0h	PIO data-in
S.M.A.R.T. Read Log	B0h	PIO data-in
S.M.A.R.T. Read Thresholds	B0h	PIO data-in
S.M.A.R.T. Return Status	B0h	Non-data

Command	Code	Protocol
S.M.A.R.T. Save Attribute Values	B0h	Non-data
S.M.A.R.T. Write Log	B0h	PIO data-out
S.M.A.R.T. Write Thresholds	B0h	PIO data-out
Host Protected Area Feature Set		
Read Native Max Address	F8h	Non-data
Set Max Address	F9h	Non-data
Set Max Set Password	F9h	PIO data-out
Set Max Lock	F9h	Non-data
Set Max Freeze Lock	F9h	Non-data
Set Max Unlock	F9h	PIO data-out
48-Bit Address Feature Set		
Flush Cache Ext	EAh	Non-data
Read Sector(s) Ext	24h	PIO data-in
Read DMA Ext	25h	DMA
Read Log Ext	2Fh	PIO data-in
Read Log DMA Ext	47h	DMA
Read Multiple Ext	29h	PIO data-in
Read Native Max Address Ext	27h	Non-data
Read Verify Sector(s) Ext	42h	Non-data
Set Max Address Ext	37h	Non-data
Write DMA Ext	35h	DMA
Write DMA FUA Ext	3Dh	DMA
Write Multiple Ext	39h	PIO data-out
Write Multiple FUA Ext	CEh	PIO data-out
Write Sector(s) Ext	34h	PIO data-out
NCQ Feature Set		
Read FPDMA Queued	60h	DMA Queued
Write FPDMA Queued	61h	DMA Queued
Trusted		
Trusted Send	5Eh	PIO data-out
Trusted Send DMA	5Fh	DMA
Trusted Receive	5Ch	PIO data-in
Trusted Receive DMA	5Dh	DMA
Trusted (Non-Data)	5Bh	Non-data
Others		
Data Set Management	06h	DMA
Seek	70h-7Fh	Non-data

8. Identify Device Information

The following Table 15 describes the 512 bytes of data the drive returns for the Identify Device command (ECh).

Table 15: Identify Device Information

Word(s)	Default Value	Total Bytes	Data Field Type Information
0	0040h*	2	Standard configuration (fixed)
1	3FFFh	2	Default number of cylinders
2	C837h	2	Specific configuration
3	0010h	2	Default number of heads
4-5	0000h	4	Obsolete
6	003Fh	2	Default number of sectors per track
7-8	0000h	4	Number of sectors per drive (Word 7 = MSW, Word 8 = LSW)
9	0000h	2	Obsolete
10-19	XXXX*	20	Serial number in ASCII (right-justified)
20-22	0000h	6	Obsolete
23-26	XXXX*	8	Firmware revision in ASCII (big-endian byte order in Word)
27-46	XXXX*	40	Model number in ASCII (left-justified)
47	8010h	2	Maximum number of sectors on Read/Write Multiple command
48	0400h	2	Trusted Computing feature set
49	2F00h*	2	Standby timer, DMA, LBA, IORDY supported
50	4000h	2	Capabilities
51	0000h	2	PIO data transfer cycle timing mode 0
52	0000h	2	Obsolete
53	0007h*	2	Words 88 and 64-70 valid
54	3FFFh	2	Current numbers of cylinders
55	0010h	2	Current numbers of heads
56	003Fh	2	Current sectors per track
57-58	XXXXh	4	Current capacity in LBAs (Word 57 = LSW, Word 58 = MSW)
59	B110h*	2	Sanitize and multiple sector setting (host changeable)
60-61	XXXXh	4	Total number of sectors addressable in LBA mode
62	0000h	2	Obsolete
63	0007h*	2	Multiword DMA transfer support modes 2, 1 and 0
64	0003h	2	Advanced PIO modes supported
65	0078h*	2	Minimum Multiword DMA transfer cycle time per Word
66	0078h*	2	Recommended Multiword DMA transfer cycle time
67	0078h*	2	Minimum PIO transfer cycle time without flow control
68	0078h*	2	Minimum PIO transfer cycle time with IORDY flow control
69	4D30h	2	CFast support
70-74	0000h	10	Reserved
75	001Fh	1	Queue depth
76	850Eh	2	SATA capabilities
77	0086h	2	Additional SATA capabilities
78	017Ch	2	SATA feature support
79	0040h*	2	SATA features enabled (host changeable)
80	07FCh	2	Major revision
81	FFFFh	2	Minor revision
82-84	746Bh* 7701h* 6163h*	6	Features/command sets supported
85-87	7469h* B401h* 6163h*	6	Features/command sets enabled (host changeable)
88	407F*	2	UDMA mode supported

Word(s)	Default Value	Total Bytes	Data Field Type Information
89	0002h*	2	Time for security erase unit completion
90	0001h*	4	Time for enhanced security erase completion
91	00FEh	2	Power Management
92	FFFEh*	2	Master password revision code
93–99	0000h*	14	Reserved
100–103	XXXXh	8	Max user LBA48 address feature set
104	0000h	2	Reserved
105	0008h	2	Maximum number of 512-bytes blocks per Data Set Management command
106	4000h	2	Sector size
107–118	0000h	24	Reserved (WWN)
119–120	401Ch 401Ch	4	Command set supported settings Command set features enabled (may change in operation)
121–127	0000h	14	Reserved
128	0021h*	2	Security status (may change in operation)
129–159	XXXXh	62	"Swissbit SSD"
160	84B0h*	2	Power requirement
161	8203h	2	CFast configuration
162	0000h	2	Management schemes
163	0000h	2	CF IDE Timing
164	0000h	2	CF Timing
165	8080h	2	CFast Operating Temperature Range
166–167	0000h	4	Reserved
168	0003h	2	Form Factor
169	0001h	2	Data Set Management supported
170–205	XXXXh	72	Reserved
206	003Dh	2	SCT Command Transport
207–208	0000h	4	Reserved
209	0400h	2	Logical block alignment
210–216	0000h	14	Reserved
217	0001h*	2	Nominal media rotation rate: Solid State Device
218–221	0000h	8	Reserved
222	10FFh	2	Transport major revision
223–233	0000h	22	Reserved
234	0002h	2	Minimum number of 512-byte units per segmented download
235	0400h	2	Maximum number of 512-byte units per segmented download
236–254	0000h	38	Reserved
255	XXXXh	2	Integrity Word

* Standard values for full functionality are listed. Values depend on device configuration.

9. S.M.A.R.T. Functionality

The X-75m2 P SSD fully supports the ATA Specification for Self-Monitoring, Analysis and Reporting Technology (S.M.A.R.T.).

9.1 S.M.A.R.T. Subcommands

The following Table 16 lists the supported S.M.A.R.T. subcommands and the Features register values.
The device aborts any S.M.A.R.T. subcommands with Features register values not listed in Table 16.

Table 16: S.M.A.R.T. Features Supported

Features	Operation
D0h	S.M.A.R.T. Read Data
D1h	S.M.A.R.T. Read Attribute Thresholds
D2h	S.M.A.R.T. Enable/Disable Autosave
D3h	S.M.A.R.T. Save Attribute Values
D4h	S.M.A.R.T. Execute Off-Line Immediate
D5h	S.M.A.R.T. Read Log
D6h	S.M.A.R.T. Write Log
D8h	S.M.A.R.T. Enable Operations
D9h	S.M.A.R.T. Disable Operations
DAh	S.M.A.R.T. Return Status

9.2 S.M.A.R.T. Read Data

When the drive receives the S.M.A.R.T. Read Data subcommand, it returns one sector (512 bytes) of data. See the following Table 17 for the data structure of this sector.

Table 17: S.M.A.R.T. Data Structure

Byte(s)	Value	Description
0-1	0100h	S.M.A.R.T. structure version
2-361	XXXXh	Attribute entries 1 to 30 (see Table 18)
362	00h	Off-line data collection status (no off-line data collection started)
363	00h	Self-test execution status byte (self-test completed)
364-365	0000h	Total time, in seconds, to complete off-line data collection
366	00h	Vendor specific
367	00h	Off-line data collection capability (no off-line data collection)
368-369	0003h	S.M.A.R.T. capabilities
370	01h	Error logging capability
371	00h	Vendor specific
372	01h	Short self-test routine recommended polling time, in minutes
373	02h	Extended self-test routine recommended polling time, in minutes
374	01h	Conveyance self-test routine recommended polling time, in minutes
375-510	XXXXh	Reserved (vendor specific)
511	XXh	Data structure checksum

9.3 S.M.A.R.T. Attribute Entry Structure

Each attribute entry consists of 12 bytes. See the following Table 18 for the data structure of each entry.

Table 18: Attribute Entry

Byte(s)	Value	Description
0	XXh	Attribute ID (see Table 19)
1-2	XXXXh	Flags (little-endian)
3	XXh	Attribute value as a percentage
4	XXh	Worst value as a percentage
5-11	XXXXh	Raw value (little-endian)

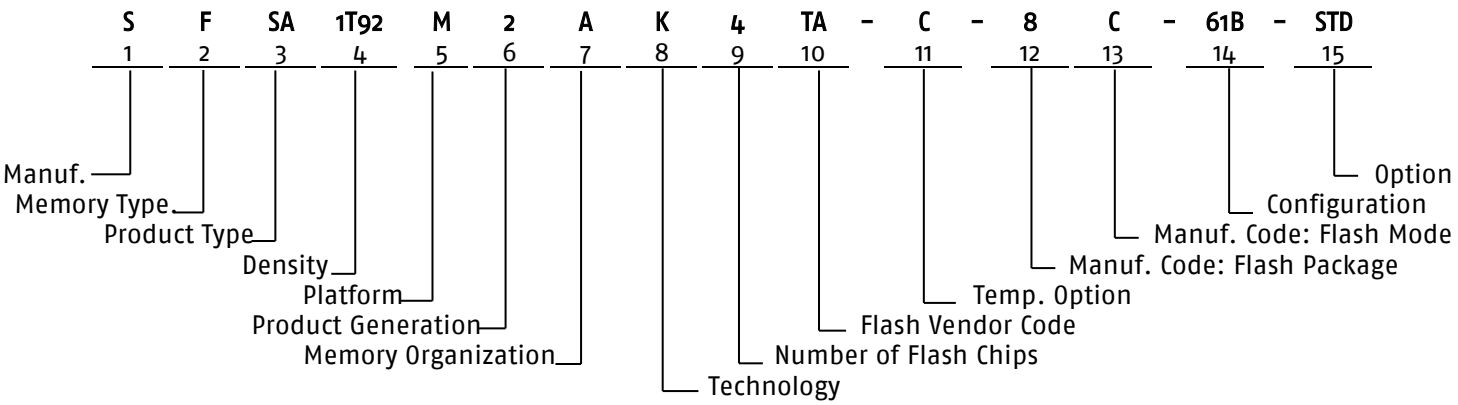
9.4 S.M.A.R.T. Attributes

The X-75m2 P drives support the S.M.A.R.T. attributes listed in the following Table 19.

Table 19: S.M.A.R.T. Attributes

ID	Threshold	Attribute	Description
0x01	0	Read Error Rate	CRC Error count/total LBAs read
0x05	0	Reallocated Sectors Count	Total number of runtime bad blocks (physical blocks)
0x09	0	Power On Hours	Total number of hours the device has been actively operating since the date of manufacture
0x0C	0	Power Cycle Count	Total number of power cycles the device encountered
0x10	1	Average Erase Count (pSLC)	Average Erase Count on pSLC blocks (raw capacities ≤ 128 GBytes only); Average Erase Count on system blocks (raw capacities ≥ 256 GBytes)
0x11	0	Rated Erase Count (pSLC)	Rated Erase Count on pSLC blocks (raw capacities ≤ 128 GBytes); Rated Erase Count on system blocks (raw capacities ≥ 256 GBytes)
0xA0	0	Uncorrectable Sector Count On Line	Read/Write Uncorrectable Sector Count
0xA1	0	Spare Block Count	Number of available spare blocks
0xA3	0	Number of Initial Invalid Blocks	Number of initial invalid blocks
0xA4	0	Total Erase Count	Total Erase Count on all blocks
0xA5	0	Maximum Erase Count	Maximum Erase Count on a single block
0xA6	0	Minimum Erase Count	Minimum Erase Count on a single block
0xA7	0	Average Erase Count	Average Erase Count on data storage blocks
0xA8	0	Rated Erase Count	Rated Erase Count on data storage blocks
0xA9	0	Power On Uncorrectable Error Count	Number of uncorrectable errors encountered during a power up event
0xAF	1	Power Loss Protection Holdup Cap Health	The status of the powersafe™ functionality after power up; the value of bit 31 (most significant bit) indicates the status; if 1, the voltage level is too low; if 0, the capacitors are fully charged
0xC1	0	Dynamic Remaps	Total number of remap operations
0xC2	0	Temperature	On-chip temperature sensor value (degrees Celsius)
0xC3	0	Flash ECC recovered	Total number of times the device required the read-retry process to recover data
0xC6	0	Reported Uncorrectable Errors	Total uncorrectable count when off-line
0xC7	0	SATA PHY CRC Error Count	Host Interface CRC Error
0xD7	0	TRIM Count	Total number of times the host has issued the TRIM command
0xE7	25	Life Remaining	Percentage of flash life remaining based on the number of spare blocks remaining
0xEB	0	Total Flash LBAs Written	Total number of flash sectors written (in 512-byte increments)
0xED	0	Total Flash LBAs Written, Expanded	Total number of flash sectors written, expanded (in 512-byte increments)
0xF1	0	Total Host LBAs Written	Total number of host sectors written (in 512-byte increments)
0xF2	0	Total Host LBAs Read	Total number of host sectors read (in 512-byte increments)
0xF3	0	Total Host LBAs Written, Expanded	The upper 5 bytes of the total number of host sectors written (in 512-byte increments)
0xF4	0	Total Host LBAs Read, Expanded	The upper 5 bytes of the total number of host sectors read (in 512-byte increments)
0xF8	1	SSD Remaining Life	Percent of flash life remaining based upon the number of P/E cycles consumed

10. Part Number Decoder



10.1 Manufacturer

Swissbit code	S

10.2 Memory Type

Flash	F

10.3 Product Type

SATA Interface	SA

10.4 Density

240 GBytes	240G
480 GBytes	480G
960 GBytes	960G
1920 GBytes	1T92

10.5 Platform

M.2 SSD	M

10.6 Product Generation

10.7 Memory Organization

x8	A

10.8 Technology

X-75m2 P Series	K

10.9 Number of Flash Chips

1 Flash	1
2 Flash	2
4 Flash	4

10.10 Flash Code

Toshiba / Kioxia Gen4	TA

10.11 Temperature Option

Commercial Temperature Range: 0 °C to 70 °C	C

Industrial Temperature Range: -40 °C to 85 °C	I

10.12 Die Classification

3D TLC MONO (single die package)	5
3D TLC DDP (dual die package)	6
3D TLC QDP (quad die package)	7
3D TLC ODP (octal die package)	8

10.13 Pin Mode

	TSOP	BGA
Single nCE and Single R/nB	S	A
Dual nCE and Dual R/nB	T	B
Quad nCE and Quad R/nB	U	C
Octal nCE and Octal R/nB	*	V
Sexdec nCE & Sexdec R/nB	*	W

*Not Available

10.14 Drive configuration XYZ

X = Dimension and Assembly

Dimension	Assembly	X
2280	Single-Sided	5
2280	Double-Sided	6

Y = Firmware Revision

FW Revision	Y
SBR13108	1

Z = Feature

Feature	Z
Powersafe	B

10.15 Option

Standard	STD

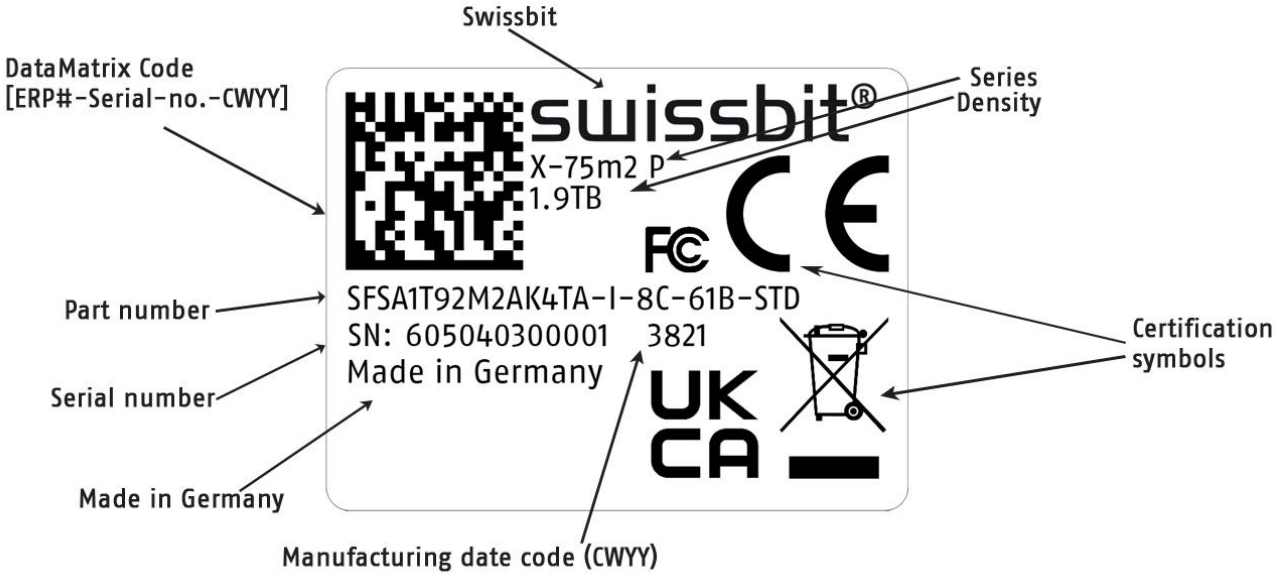
11. Swissbit M.2 SATA SSD Marking Specification

11.1 Top View

Figure 5: X-75m2 P 2280 top view (example)

11.2 Print on the label

Figure 6: X-75m2 P label details



12. Revision History

Table 20: Document Revision History

Date	Revision	Description	Revision Details
18-Aug-2021	0.90	Preliminary draft	Doc. req. no. 4800
18-Nov-2021	1.00	Initial release	Doc. req. no. 5145