HV2607/HV2707/HV2708

No High-Voltage Bias, Low Harmonic Distortion, 16-Channel, High-Voltage Analog Switch

Features

- 16-Channel High-Voltage Analog Switch
- Analog Signal Voltage Up to ±100V
- Only +5V Bias Supply Required
- 3.3V and 5V CMOS Input Logic Level
- 66 MHz Data Shift Clock Frequency
- Ultra-Low Quiescent Current < 10 µA
- Low Parasitic Capacitance
- Low Harmonic Distortion
- DC to 100 MHz Analog Small Signal Frequency
- 200 kHz to 50 MHz Large Signal Frequency
- -76 dB Typical Off Isolation at 5.0 MHz
- Excellent Noise Immunity
- Cascadable Serial Data Register with Latches
- Integrated Bleed Resistors on the Outputs (both sides for HV2707, one side for HV2708)

Application

- Medical Ultrasound Imaging
- Non-Destructive Testing (NDT) Metal Flaw Detection
- Piezoelectric Transducer Drivers
- Inkjet Printer Head
- Optical MEMS Module

General Description

HV2607/HV2707/HV2708 devices are low harmonic distortion, low charge injection, 16-channel, high-voltage analog switches without high-voltage supplies. They are intended for use in applications requiring high-voltage switching controlled by low-voltage control signals, such as medical ultrasound imaging, driving piezoelectric transducers and printers.

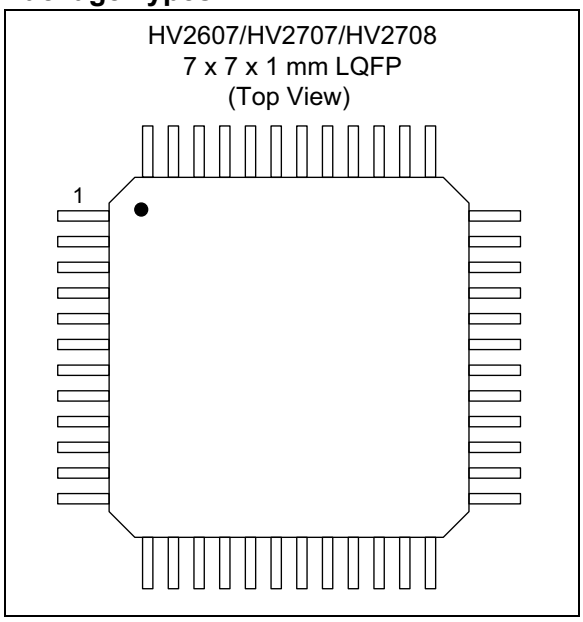
The HV2707 has integrated bleed resistors at both sides of the switches. The HV2708 has integrated bleed resistors at the SWA side only. The HV2607 has no bleed resistors. The bleed resistor eliminates voltage build up on capacitive loads, such as piezoelectric transducers.

The HV2607/HV2707/HV2708 devices require no high-voltage supplies and require only +5V or +6V bias supply. The analog input voltage range is up to ±100V, even though there are no high-voltage supplies.

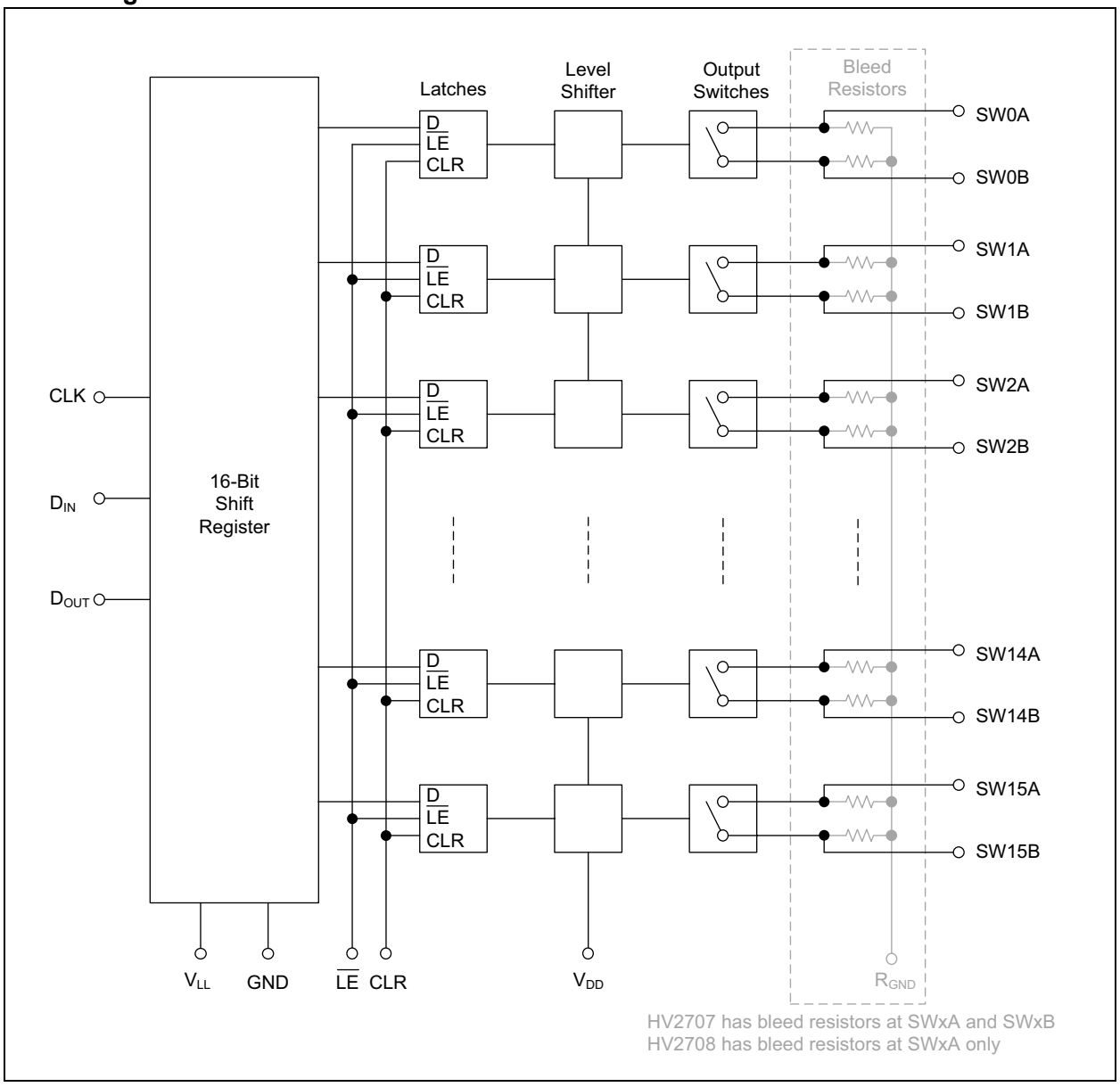
The HV2607/HV2707/HV2708 devices are offered in a 48-pin LQFP package, which is pin-to-pin compatible with HV2601/HV2701 and HV2605/HV2705 devices, except power supply pins.

Package Types

HV2607/HV2707/HV2708
7 x 7 x 1 mm LQFP
(Top View)



Block Diagram



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings†

Logic Supply Voltage (V_{LL}) ..... -0.5V to 6.6V
Positive Supply Voltage (V_{DD})..... -0.5V to 6.6V
Logic Input Voltage (V_{IN})..... -0.5V to V_{LL} + 0.3V
Analog Signal Range (V_{SIG})..... -110V to +110V
Peak Analog Signal Current/Channel (I_{PK}) 1.9A

† **Notice:** Stresses above those listed under “Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS(1,2,3)

Parameter	Sym.	Min.	Typ.	Max.	Units	Conditions
Logic Supply Voltage	V_{LL}	3	—	5.5	V	
Positive Supply Voltage	V_{DD}	4.5	—	6.3	V	
High-Level Input Voltage	V_{IH}	0.9 V_{LL}	—	V_{LL}	V	
Low-Level Input Voltage	V_{IL}	0	—	0.1 V_{LL}	V	
Analog Signal Voltage Peak-to-Peak	V_{SIG}	-100	—	100	V	

Note 1: Power-up sequence is V_{LL} first and then V_{DD}. Power-down sequence is the reverse of power-up.
2: V_{SIG} must be GND ≤ V_{SIG} ≤ V_{DD} or floating during power-up/down transition.
3: Rise and fall times of power supplies, V_{LL} and V_{DD}, should be greater than 1.0 ms.

DC ELECTRICAL CHARACTERISTICS

Unless otherwise specified, V_{LL} = +5V, V_{DD} = +5V, T_A = +25°C.
Boldface specifications apply over the full operating temperature range.

Parameter	Sym.	Min.	Typ.	Max.	Units	Conditions/Comments
Small Signal Switch On-Resistance	R_{ONS}	—	14	**23**	Ω	I_{SIG} = 5 mA
		—	14.5	**23**	Ω	I_{SIG} = 200 mA
Small Signal Switch On-Resistance Matching	ΔR_{ONS}	—	5	**20**	%	I_{SIG} = 5 mA
Large Signal Switch On-Resistance	R_{ONL}	—	12	—	Ω	V_{SIG} = 90V, R_{LOAD} = 70Ω **(Note 1)**
Value of Output Bleed Resistor (HV2707/HV2708 only)	R_{INT}	20	35	50	kΩ	I_{RINT} = 0.1 mA
Switch Off Leakage per Switch	I_{SOL}	—	—	**10**	µA	V_{SIG} = +100V, 500 µs pulse, see Figure 3-1
		—	—	**10**	µA	V_{SIG} = -100V, 100 µs pulse, see Figure 3-1 **(Note 1)**
HV2607						
Switch Off Bias per Switch	I_{SOB}	—	—	**3**	µA	V_{SIG} = +100V, 500 µs pulse, see Figure 3-2
		—	—	**100**	µA	V_{SIG} = -100V, 100 µs pulse, see Figure 3-2 **(Note 1)**
HV2707						
Switch Off Bias of All SWA and SWB Switches	I_{SOB}	—	—	**3**	µA	V_{SIG} = +100V, 500 µs pulse, see Figure 3-2
		—	—	**3**	mA	V_{SIG} = -100V, 100 µs pulse, see Figure 3-2 **(Note 1)**
HV2708						
Switch Off Bias of All SWA (with Bleed Resistor) Switches	I_{SOB}	—	—	**3**	µA	V_{SIG} = +100V, 500 µs pulse, see Figure 3-2
		—	—	**1.5**	mA	V_{SIG} = -100V, 100 µs pulse, see Figure 3-2 **(Note 1)**
Switch Off Bias per SWB (without Bleed Resistor) Switch		—	—	**3**	µA	V_{SIG} = +100V, 500 µs pulse, see Figure 3-2
		—	—	**100**	µA	V_{SIG} = -100V, 100 µs pulse, see Figure 3-2 **(Note 1)**
Switch Off DC Offset	V_{OS}	—	1	**10**	mV	R_{LOAD} = 25 kΩ (HV2607)/50 kΩ (HV2708), no load (HV2707), see Figure 3-3 **(Note 1)**
Switch On DC Offset		—	1	**10**		
Quiescent V_{DD} Supply Current	I_{DDQ}	—	—	**10**	µA	All switches off
		—	—	**10**		All switches on, V_{SW} = 1V
Quiescent V_{LL} Supply Current	I_{LLQ}	—	1	**10**	µA	All logic inputs are GND
Switch Output Peak Current	I_{SW}	1.3	1.9	—	A	V_{SIG} duty cycle < 0.1% **(Note 1)**
Output Switching Frequency	f_{SW}	—	—	**50**	kHz	Duty cycle = 50% **(Note 1)**
Average V_{DD} Supply Current	I_{DD}	—	3.7	**6**	mA	All output switches are turning on and off at 50 kHz with no load
Average V_{LL} Supply Current	I_{LL}	—	0.3	**0.5**	mA	f_{CLK} = 5.0 MHz, f_{DIN} = 2.5 MHz
Data Out Source Current	I_{SOR}	**10**	—	—	mA	$V_{OUT} = V_{LL} - 0.7V$
Data Out Sink Current	I_{SINK}	**10**	—	—	mA	V_{OUT} = 0.7V
Logic Input Capacitance	C_{IN}	—	8	—	pF	**Note 2**

Note 1: Specification is obtained by characterization and is not 100% tested.

2: Design guidance only.

AC ELECTRICAL CHARACTERISTICS

Unless otherwise specified, V_{LL} = +5V, V_{DD} = +5V, t_R= t_F ≤ 5.0 ns, 50% duty cycle, T_A = +25°C.
Boldface specifications apply over the full operating temperature range.

Parameter	Sym.	Min.	Typ.	Max.	Units	Conditions/Comments
Setup Time Before $\overline{LE}$ Rises	t_{SD}	**25**	—	—	ns	**Note 1**
Time Width of $\overline{LE}$	t_{WLE}	**12**	—	—	ns	**Note 1**
Clock Delay Time to Data Out	t_{DO}	—	—	**13.5**	ns	
Time Width of CLR	t_{WCLR}	**55**	—	—	ns	**Note 1**
Setup Time Data to Clock	t_{SU}	**1.5**	—	—	ns	**Note 1**
Hold Time Data from Clock	t_H	**1.5**	—	—	ns	**Note 1**
Clock Frequency	f_{CLK}	—	—	**66**	MHz	50% duty cycle, f_{DIN} = (1/2)f_{CLK}, C_{DOUT} = 20 pF **(Note 1)**
Clock Rise and Fall Times	t_R, t_F	—	—	**50**	ns	
Turn-On Time	t_{ON}	—	—	**5**	µs	V_{SIG} = 5V, R_{LOAD} = 550Ω, see Figure 3-4
Turn-Off Time	t_{OFF}	—	—	**5**	µs	V_{SIG} = 5V, R_{LOAD} = 550Ω, see Figure 3-4
Input Large Signal Pulse Width	t_{PW}	—	—	**2.5**	µs	V_{PULSE} = 0V to ±100V, measured at 90% amplitude, see Figure 3-5 **(Note 1)**
Maximum V_{SIG} Slew Rate	dV/dt	—	—	20	V/ns	**Note 1**
Analog Small Signal Frequency	f_{BWS}	—	100	—	MHz	**Note 1**
Off Isolation	K_O	—	-64	-60	dB	f = 5.0 MHz,1.0 kΩ//15 pF load, see Figure 3-6 **(Note 1)**
		—	-76	-70	dB	f = 5.0 MHz, 50Ω load, see Figure 3-6 **(Note 1)**
Switch Crosstalk	K_{CR}	—	-70	-60	dB	f = 5.0 MHz, 50Ω load, see Figure 3-7 **(Note 1)**
Off Capacitance SW to GND	$C_{SG(OFF)}$	—	9	—	pF	V_{SIG} = 50 mV @1 MHz, no load **(Note 1)**
On Capacitance SW to GND	$C_{SG(ON)}$	—	17	—	pF	V_{SIG} = 50 mV @ 1 MHz, no load **(Note 1)**
Output Voltage Spike at SWA, SWB	$+V_{SPK}$	—	—	40	mV	R_{LOAD} = 50Ω, see Figure 3-8 **(Note 1)**
	$-V_{SPK}$	-10	—	—	mV	
Charge Injection	QC	—	110	—	pC	See Figure 3-8 **(Note 1)**
Second Harmonic Distortion	HD2	—	-64	—	dBc	V_{SIG} = 1.5V @ 5 MHz, 50Ω load **(Note 1)**
		—	-60	—	dBc	V_{SIG} = 1.5V @ 5 MHz, 1 kΩ//15 pF load **(Note 1)**

Note 1: Specification is obtained by characterization and is not 100% tested.

TEMPERATURE SPECIFICATION

Parameters	Sym	Min	Typ	Max	Units	Conditions
Temperature Range						
Operating Temperature	T_A	0	—	+70	°C	
Storage Temperature	T_S	-65	—	+150	°C	
Maximum Junction Temperature	T_J	—	—	+125	°C	
Package Thermal Resistance						
Thermal Resistance, LQFP	Θ_{JA}	—	52	—	°C/W	

TABLE 1-1: TRUTH TABLE(1,2,3,4,5,6)

D0	D1	...	D7	D8	...	D15	$\overline{LE}$	CLR	SW0	SW1	...	SW7	SW8	...	SW15
L	—		—	—		—	L	L	OFF	—		—	—		—
H	—		—	—		—	L	L	ON	—		—	—		—
—	L		—	—		—	L	L	—	OFF		—	—		—
—	H		—	—		—	L	L	—	ON		—	—		—
—	—		—	—		—	L	L	—	—		—	—		—
—	—		—	—		—	L	L	—	—		—	—		—
—	—		L	-		—	L	L	—	—		OFF	—		—
—	—	...	H	-	...	—	L	L	—	—	...	ON	—	...	—
—	—		—	L		—	L	L	—	—		—	OFF		—
—	—		—	H		—	L	L	—	—		—	ON		—
—	—		—	—		—	L	L	—	—		—	—		—
—	—		—	—		—	L	L	—	—		—	—		—
—	—		—	—		L	L	L	—	—		—	—		OFF
—	—		—	—		H	L	L	—	—		—	—		ON
X	X	X	X	X	X	X	H	L	HOLD PREVIOUS STATE						
X	X	X	X	X	X	X	X	H	ALL SWITCHES OFF						

Note 1: The 16 switches operate independently.

2: Serial data are clocked in on the L to H transition of the CLK.

3: All 16 switches go to a state retaining their latched condition at the rising edge of $\overline{LE}$. When $\overline{LE}$ is low, the shift registers' data flow through the latch.

4: D_{OUT} is high when the data in Register 15 are high.

5: Shift register clocking has no effect on the switch states if $\overline{LE}$ is high.

6: The CLR (clear) input overrides all of the inputs.

1.1 Typical Timing Diagram

Figure 1-1 shows the timing of AC characteristic parameters graphically.

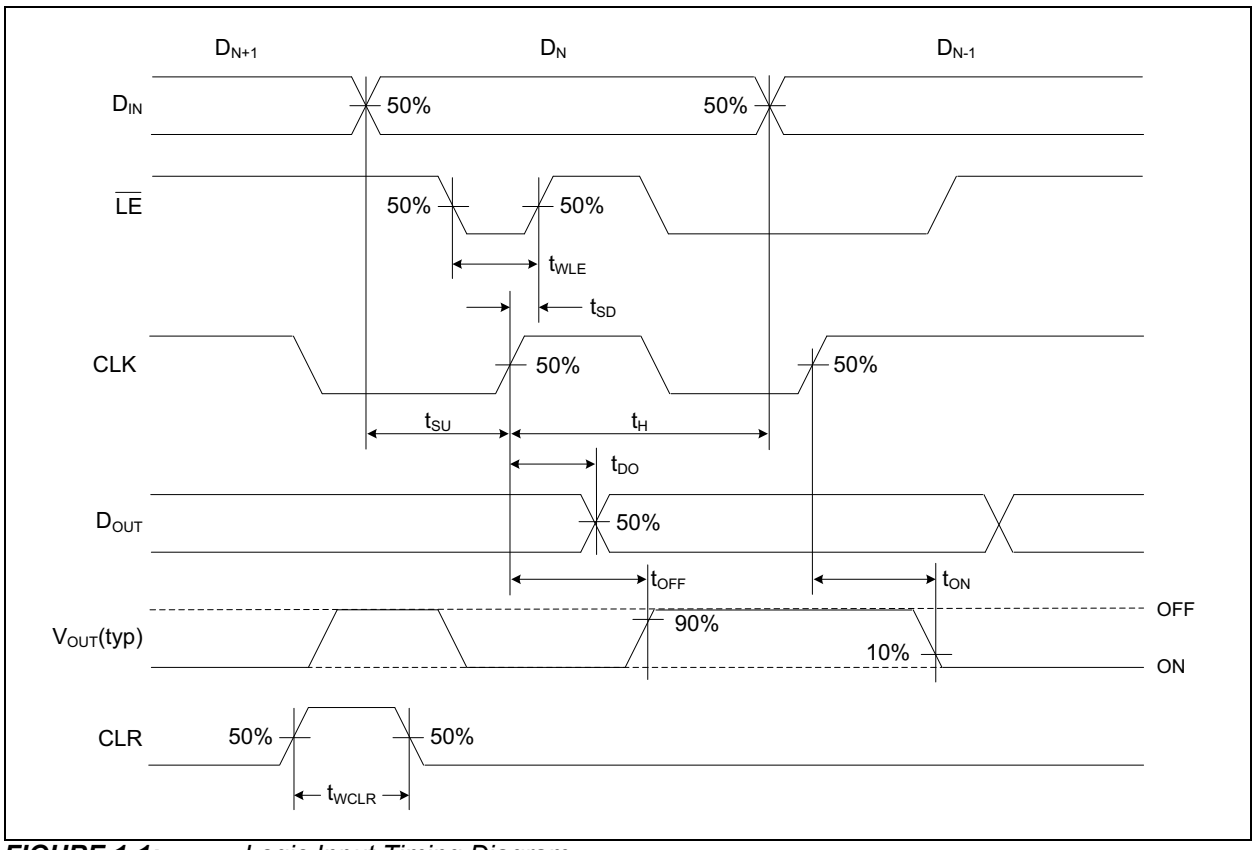


FIGURE 1-1: *Logic Input Timing Diagram.*

2.0 PIN DESCRIPTION

This section details the pin description for the 48-Lead LQFP package (Figure 2-1). The descriptions of the pins are listed in Table 2-1.

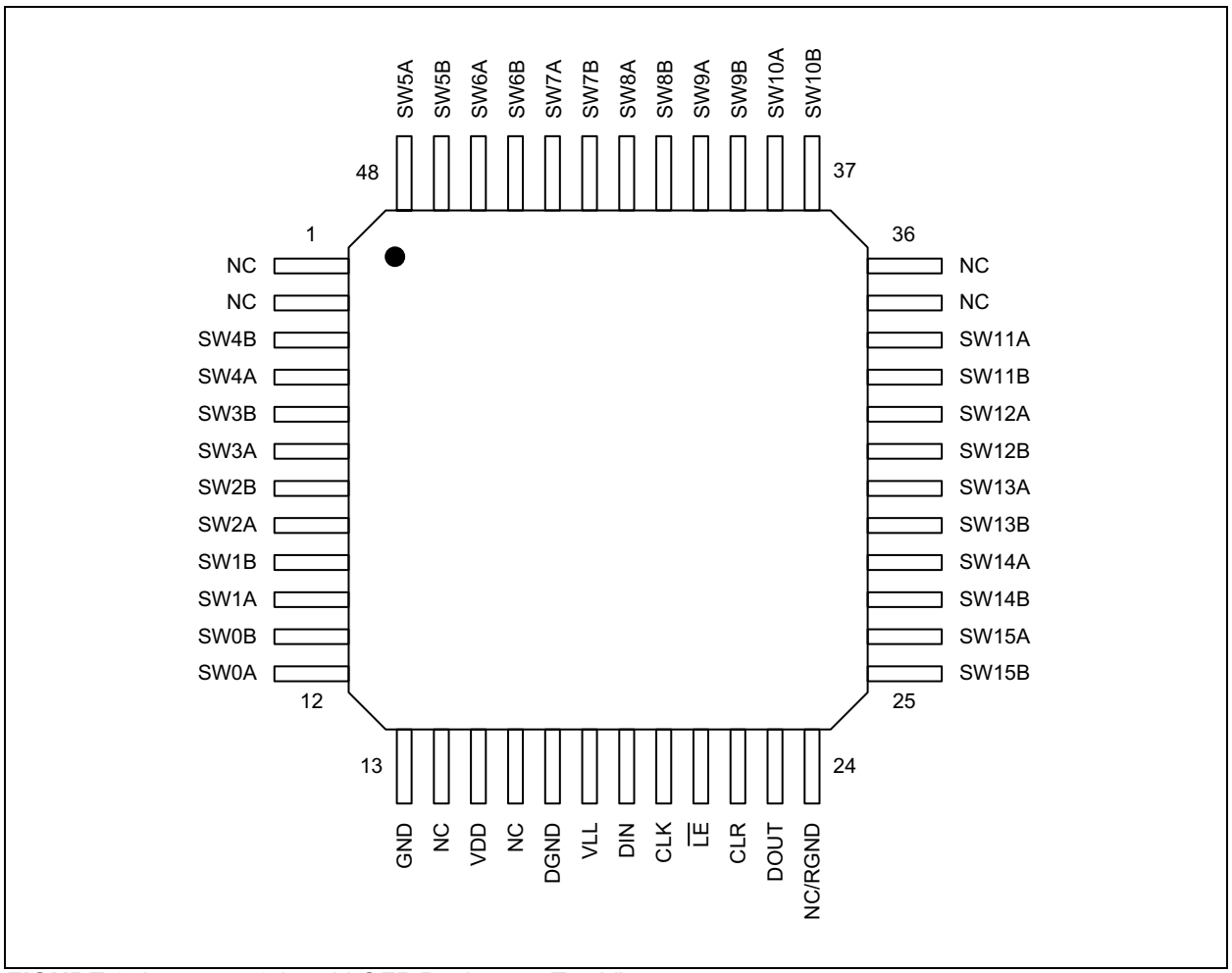


FIGURE 2-1: *48-Lead LQFP Package – Top View.*

TABLE 2-1: PIN FUNCTION TABLE

Pin Number	Symbol		Description
	HV2607	HV2707/HV2708	
1	NC	NC	No Connection
2	NC	NC	No Connection
3	SW4B	SW4B	Analog Switch 4 Terminal B
4	SW4A	SW4A	Analog Switch 4 Terminal A
5	SW3B	SW3B	Analog Switch 3 Terminal B
6	SW3A	SW3A	Analog Switch 3 Terminal A
7	SW2B	SW2B	Analog Switch 2 terminal B
8	SW2A	SW2A	Analog Switch 2 Terminal A
9	SW1B	SW1B	Analog Switch 1 Terminal B
10	SW1A	SW1A	Analog Switch 1 Terminal A
11	SW0B	SW0B	Analog Switch 0 Terminal B
12	SW0A	SW0A	Analog Switch 0 Terminal A
13	GND	GND	Ground
14	NC	NC	No Connection
15	V_{DD}	V_{DD}	Positive Supply Voltage
16	NC	NC	No Connection
17	DGND	DGND	Digital Ground
18	V_{LL}	V_{LL}	Logic Supply Voltage
19	D_{IN}	D_{IN}	Data In Logic Input
20	CLK	CLK	Clock Logic Input for Shift Register
21	$\overline{LE}$	$\overline{LE}$	Latch Enable Logic Input, Low Active
22	CLR	CLR	Latch Clear Logic Input
23	D_{OUT}	D_{OUT}	Data Out Logic Output
24	NC	RGND	No Connection/Ground for Bleed Resistor
25	SW15B	SW15B	Analog Switch 15 Terminal B
26	SW15A	SW15A	Analog Switch 15 Terminal A
27	SW14B	SW14B	Analog Switch 14 Terminal B
28	SW14A	SW14A	Analog Switch 14 Terminal A
29	SW13B	SW13B	Analog Switch 13 Terminal B
30	SW13A	SW13A	Analog Switch 13 Terminal A
31	SW12B	SW12B	Analog Switch 12 Terminal B
32	SW12A	SW12A	Analog Switch 12 Terminal A
33	SW11B	SW11B	Analog Switch 11 Terminal B
34	SW11A	SW11A	Analog Switch 11 Terminal A
35	NC	NC	No Connection
36	NC	NC	No Connection
37	SW10B	SW10B	Analog Switch 10 Terminal B
38	SW10A	SW10A	Analog Switch 10 Terminal A
39	SW9B	SW9B	Analog Switch 9 Terminal B
40	SW9A	SW9A	Analog Switch 9 Terminal A
41	SW8B	SW8B	Analog Switch 8 Terminal B
42	SW8A	SW8A	Analog Switch 8 Terminal A
43	SW7B	SW7B	Analog Switch 7 Terminal B
44	SW7A	SW7A	Analog Switch 7 Terminal A
45	SW6B	SW6B	Analog Switch 6 Terminal B
46	SW6A	SW6A	Analog Switch 6 Terminal A
47	SW5B	SW5B	Analog Switch 5 Terminal B
48	SW5A	SW5A	Analog Switch 5 Terminal A

3.0 TEST CIRCUIT EXAMPLES

This section details a few examples of test circuits.

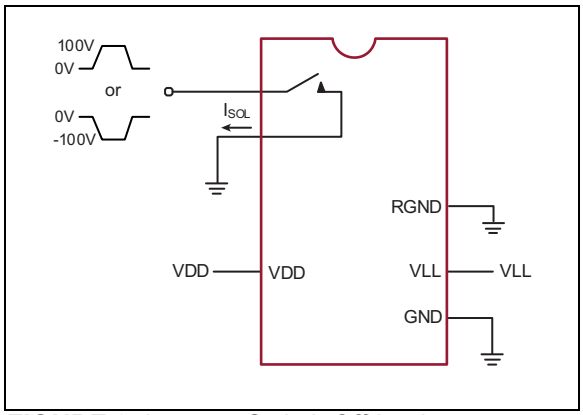


FIGURE 3-1: *Switch Off Leakage per Switch.*

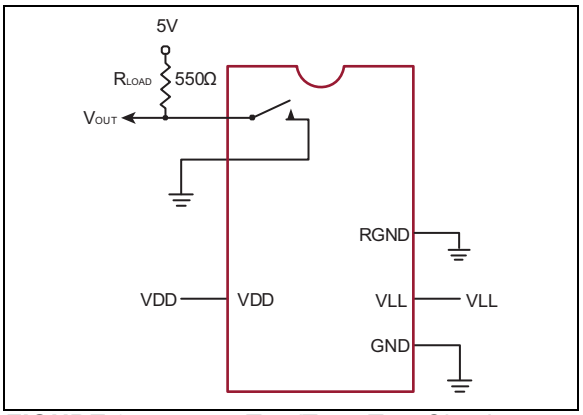


FIGURE 3-4: *T_{ON}/T_{OFF} Test Circuit.*

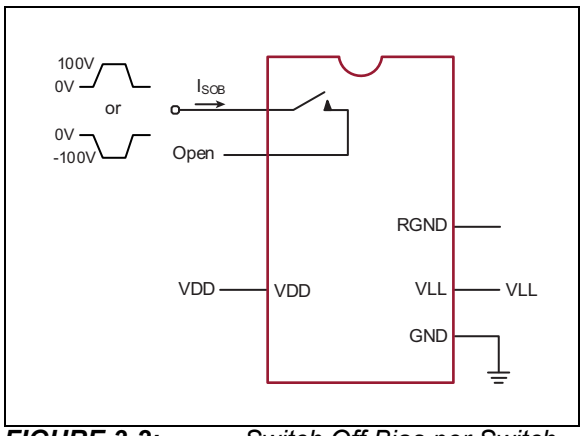


FIGURE 3-2: *Switch Off Bias per Switch.*

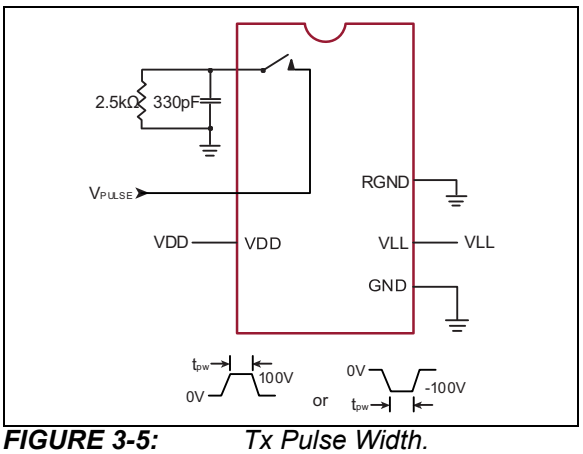


FIGURE 3-5: *Tx Pulse Width.*

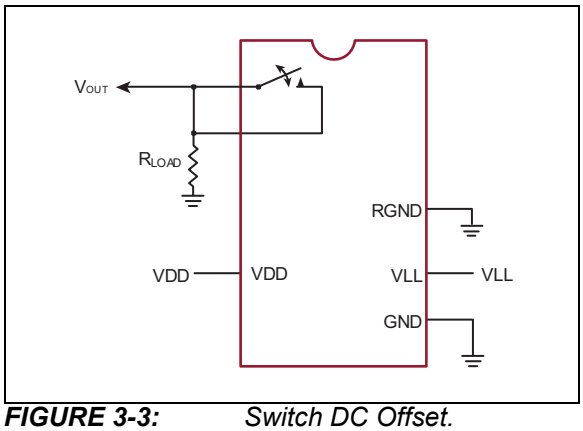


FIGURE 3-3: *Switch DC Offset.*

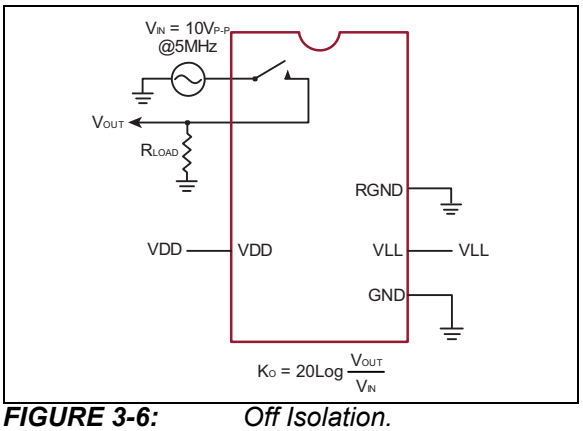


FIGURE 3-6: *Off Isolation.*

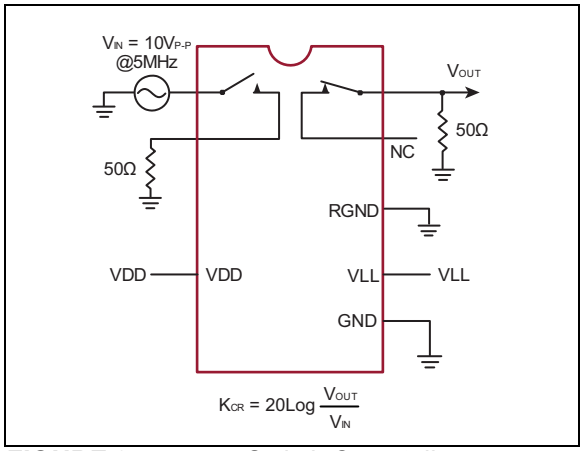


FIGURE 3-7: *Switch Crosstalk.*

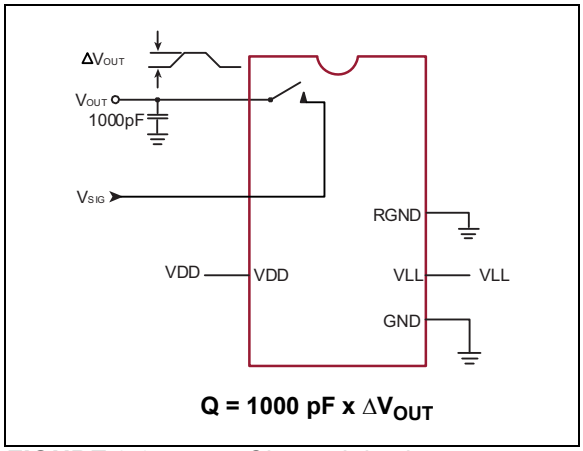


FIGURE 3-9: *Charge Injection.*

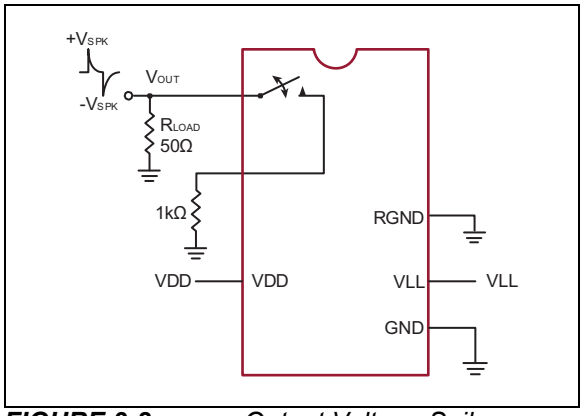


FIGURE 3-8: *Output Voltage Spike.*

4.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise specified, V_{LL} = +5V, V_{DD} = +5V, T_A = +25°C.

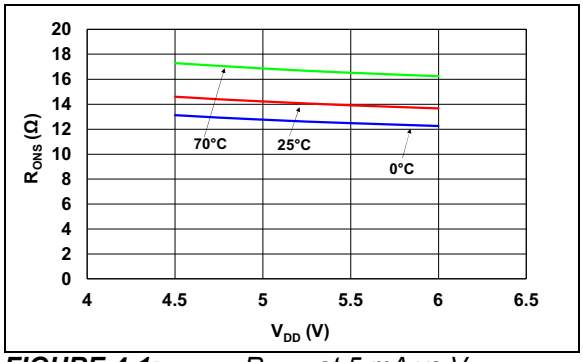


FIGURE 4-1: *R_{ONS} at 5 mA vs V_{DD}.*

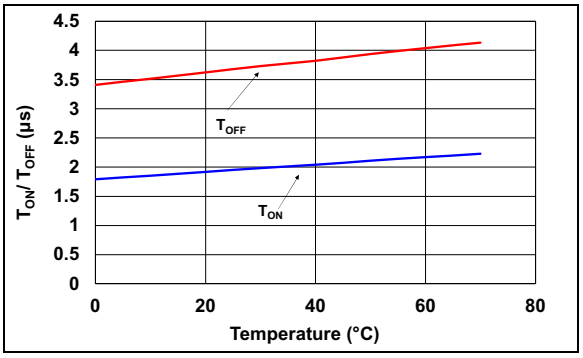


FIGURE 4-4: *T_{ON}/T_{OFF} vs. Temperature.*

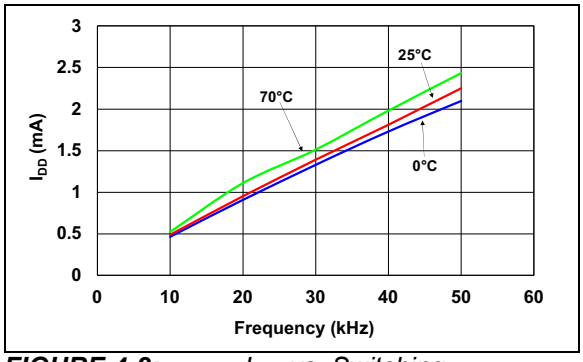


FIGURE 4-2: *I_{DD} vs. Switching Frequency.*

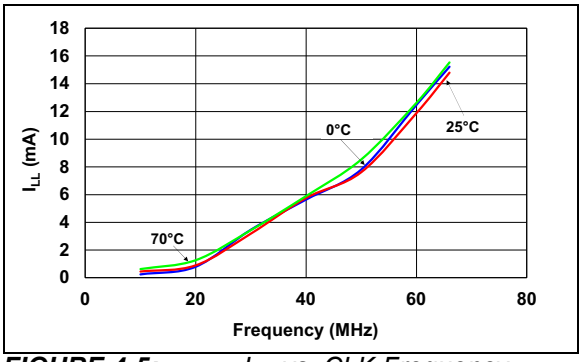


FIGURE 4-5: *I_{LL} vs. CLK Frequency.*

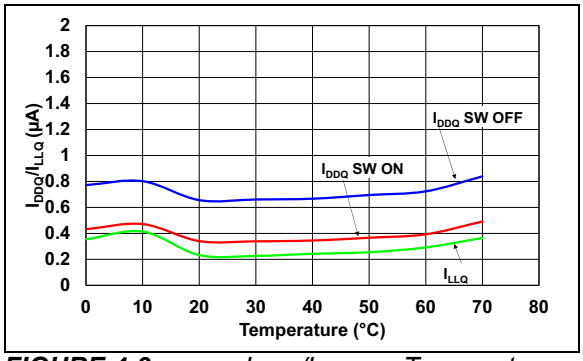


FIGURE 4-3: *I_{DDQ}/I_{LLQ} vs. Temperature.*

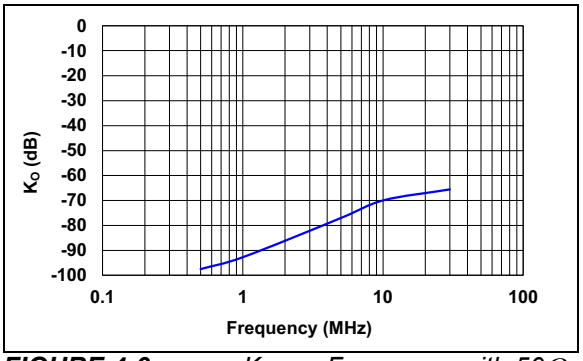


FIGURE 4-6: *K_O vs. Frequency with 50Ω Load.*

5.0 DETAILED DESCRIPTION AND APPLICATION INFORMATION

5.1 Device Overview

The HV2607/HV2707/HV2708 devices are low harmonic distortion, low charge injection, 16-channel, high-voltage analog switches without high-voltage supplies. The high-voltage analog switches are used for multiplexing a piezoelectric transducer array in a probe to multiple channel transmitter (Tx) arrays in a medical ultrasound system.

The HV2607/HV2707/HV2708 devices are distinguished by bleed resistors that eliminate voltage build-up in capacitance load, such as piezoelectric transducers. These devices can pass ±100V high-voltage pulses without high-voltage bias, such as ±100V. These devices have typical 14Ω on-resistance and 100 MHz bandwidth for small signals.

Figure 5-1 shows a typical medical ultrasound image system consisting of 64 channels of transmit pulsers, 64 channels of receivers (LNA and ADC) and 64 channels of T/R switches connecting to 192 elements of an ultrasound probe via a HV2XXX high-voltage analog switch array.

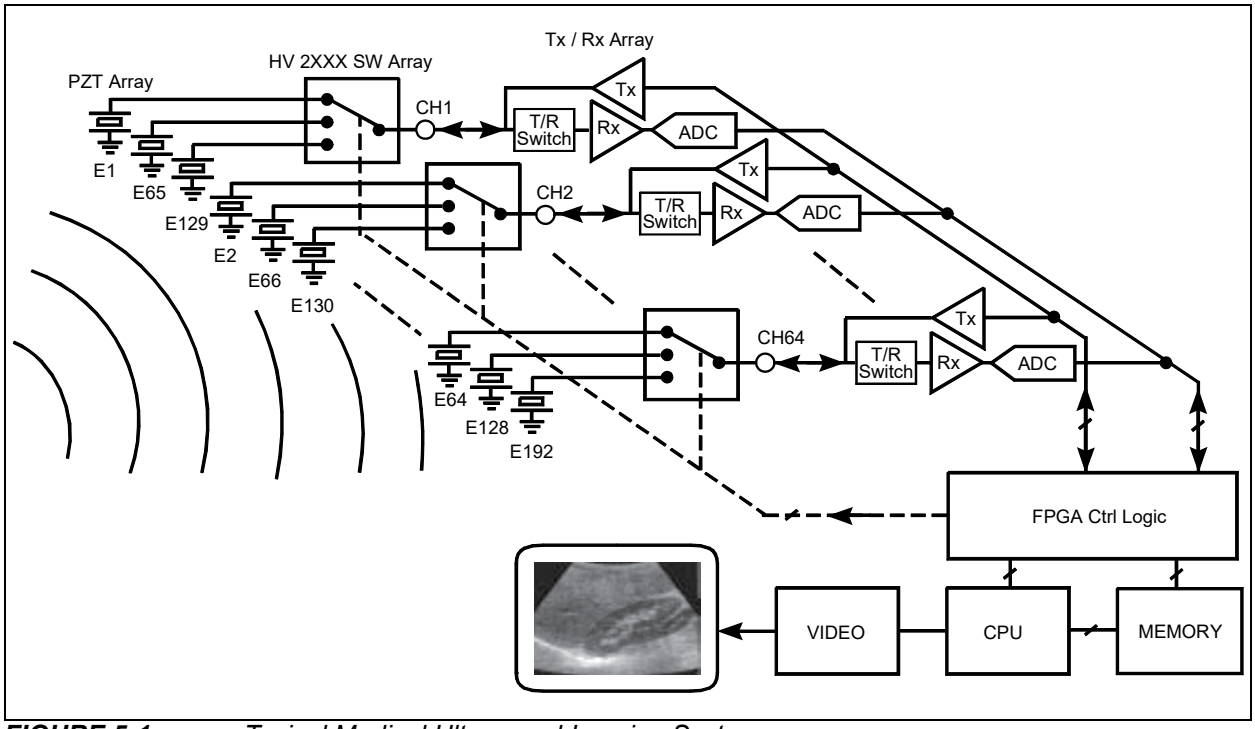


FIGURE 5-1: *Typical Medical Ultrasound Imaging System.*

5.2 Logic Input Timing

The HV2607/HV2707/HV2708 devices have a digital serial interface consisting of Data In (D_{IN}), Clock (CLK), Data Out (D_{OUT}), Latch Enable ($\overline{LE}$) and Clear (CLR) to control 16 switches individually. The digital circuits are supplied by V_{LL} and connected to DGND. The serial clock frequency is up to 66 MHz.

The switch state configuration data are shifted into the shift registers on the rising edge (low-to-high transition) of the clock. The switch Configuration bit of SW15 is shifted in first and the Configuration bit of SW0 is shifted in last. To change all the switch states at the same time, the Latch Enable ($\overline{LE}$) input should remain high while the 16-bit Data In signal is shifted into the 16-bit register. After the valid 16-bit data complete shifting into the shift registers, the high-to-low transition of the $\overline{LE}$ signal transfers the contents of the shift registers into the latches. Finally, setting the $\overline{LE}$ high again allows all the latches to keep the current state, while new data can now be shifted into the shift registers without disturbing the latches.

It is recommended to change all the latch states at the same time through this method to avoid possible clock feed through noise (see Figure 5-2 for details).

When the CLR input is set high, it resets the data of all 16 latches to low. Consequently, all the high-voltage switches are set to the OFF state. However, the CLR signal does not affect the contents of the shift register, so the shift register can operate independently of the CLR signal. Therefore, when the CLR input is low, the shift register still retains the previous data.

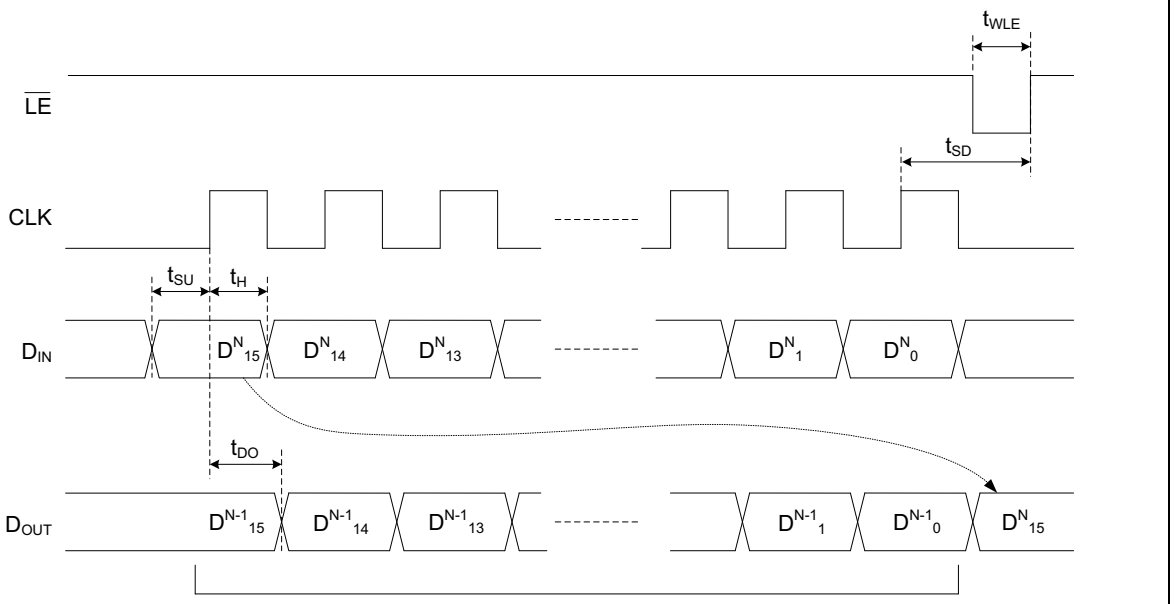


FIGURE 5-2: *Latch Enable Timing Diagram.*

5.3 Multiple Devices Connection

The serial input interface of the HV2607/HV2707/HV2708 allows multiple devices to daisy-chain together. In this configuration, the D_{OUT} of a device is connected to the D_{IN} of the subsequent device, and so forth. The last D_{OUT} of the daisy-chained HV2607/HV2707/HV2708 can either be floating or fed back to an FPGA to check the previously stored shift register data.

To control all the high-voltage analog switch states in daisy-chained N devices, N-times 16 clocks and N-times 16 bits of data are shifted into shift registers, while $\overline{LE}$ remains high and CLR remains low. After all the data finish shifting in, one single negative pulse of $\overline{LE}$ transfers the data from all shift registers to all the latches simultaneously. Consequently, all N-times 16 high-voltage analog switches change states simultaneously.

5.4 Power-up/Down Sequence and Decoupling Capacitor

The recommended power-up sequence of the HV2607/HV2707/HV2708 is V_{LL} first, then V_{DD}. The power-down sequence is in reverse order of power-up. During the power-up/down period, all the analog switch inputs should be within V_{DD} and GND or floating.

5.5 Layout Considerations

The HV2607/HV2707/HV2708 devices have two separate ground connections. DGND is the ground connection for digital circuitry and GND is the ground connection for substrate and analog switches. Since the analog switch passes large transient current from the pulser, the GND should be shared with the pulser output stage ground. It is important to have a good PCB layout which minimizes noise and ground bounce. It is recommended to use two separate ground planes in the PCB, connected together at the return terminal of the input power line, as shown in Figure 5-3. It is recommended that 0.1 µF or larger ceramic decoupling capacitors with low-ESR (Equivalent Series Resistance) and appropriate voltage ratings be connected between ground and power supplies, as shown in Figure 5-3. The decoupling capacitor of V_{LL} and V_{DD} should be connected to DGND. These decoupling capacitors should be placed as close as possible to the device.

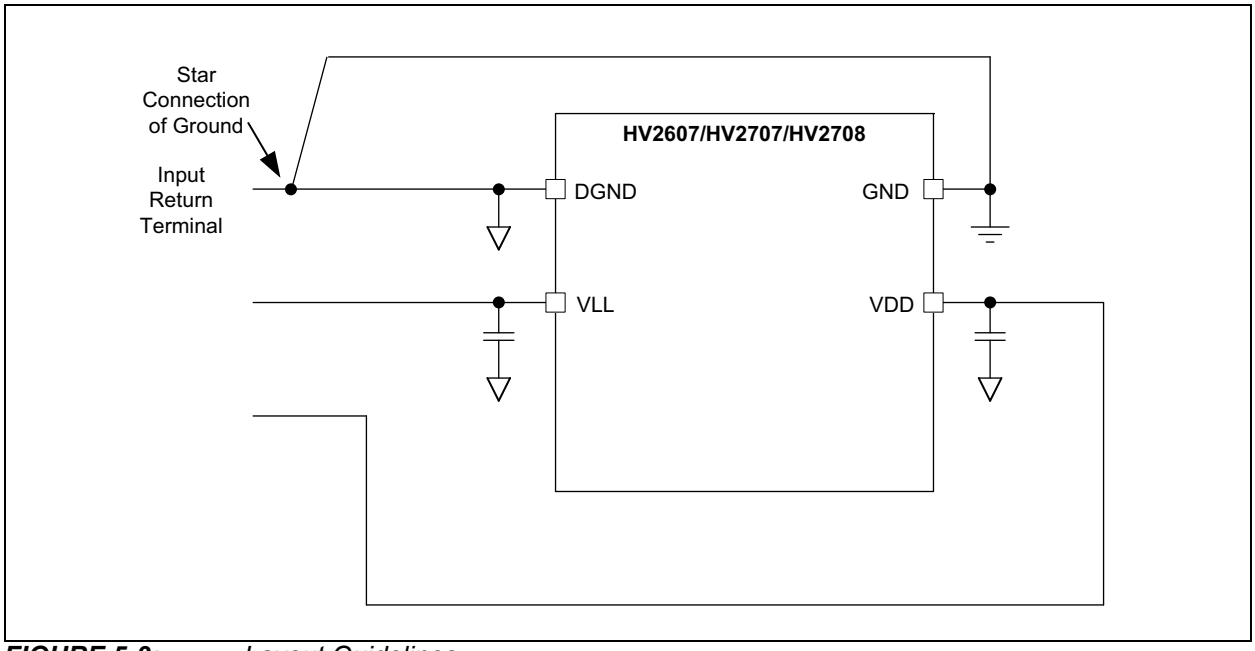
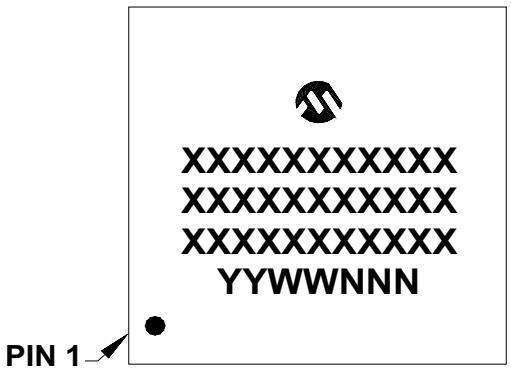


FIGURE 5-3: *Layout Guidelines.*

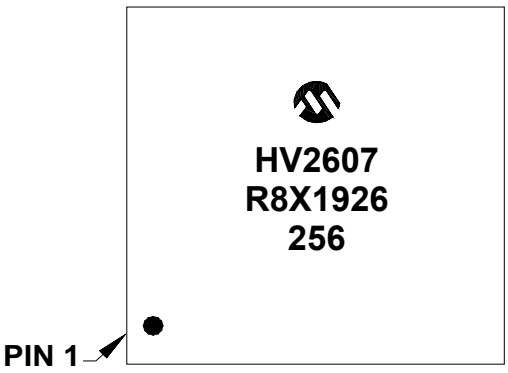
6.0 PACKAGING INFORMATION

6.1 Package Marking Information

48-Lead LQFP



Example

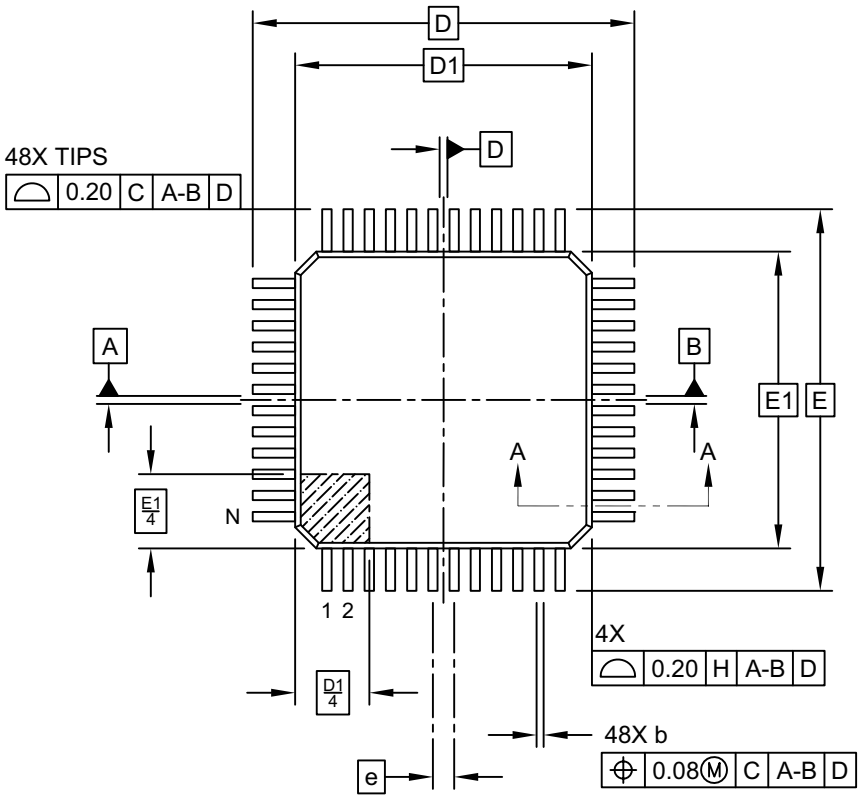


Legend:	XX...X	Product Code or Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
		can be found on the outer packaging for this package.

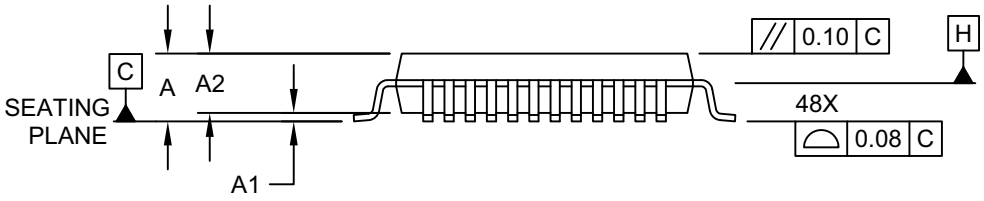
Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or may not include the corporate logo.

48-Lead Low-profile Plastic Quad Flat Pack Package (R8) -7x7 mm Body [LQFP]
Supertex Legacy Package

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



TOP VIEW

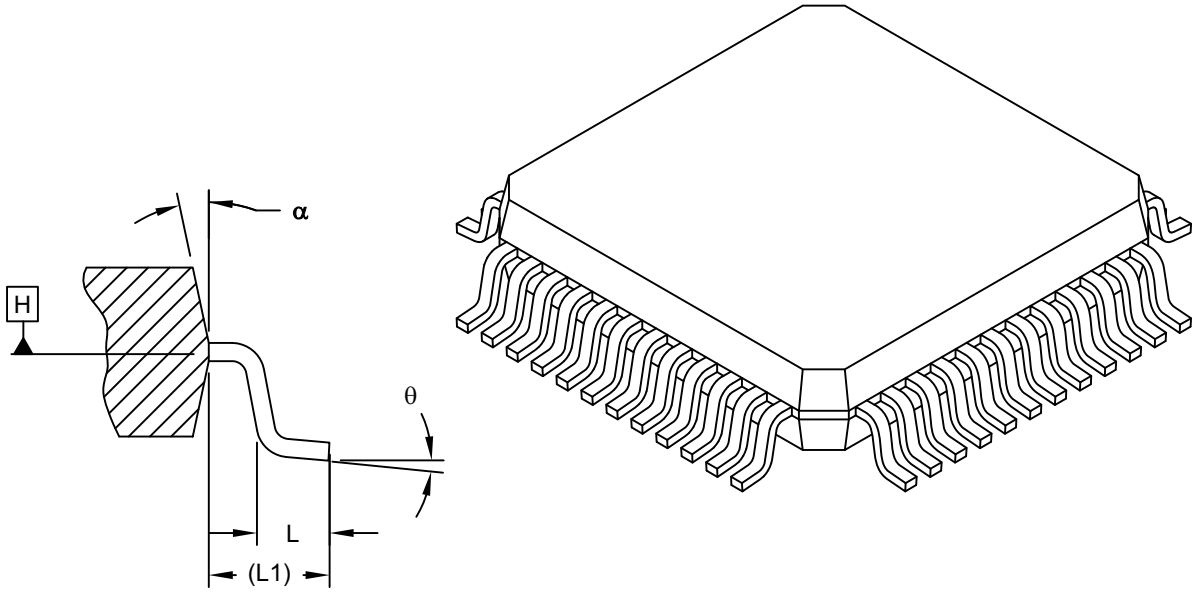


SIDE VIEW

Microchip Technology Drawing C04-278 Rev A Sheet 1 of 2

48-Lead Low-profile Plastic Quad Flat Pack Package (R8) -7x7 mm Body [LQFP] Supertex Legacy Package

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



SECTION A-A

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Leads	N		48	
Lead Pitch	e		0.50 BSC	
Overall Height	A	1.40	1.50	1.60
Standoff	A1	0.05	0.10	0.15
Molded Package Thickness	A2	1.35	1.40	1.45
Foot Length	L	0.45	0.60	0.75
Footprint	L1		1.00 REF	
Foot Angle	θ	0°	3.5°	7°
Overall Width	E		9.00 BSC	
Overall Length	D		9.00 BSC	
Molded Package Width	E1		7.00 BSC	
Molded Package Length	D1		7.00 BSC	
Lead Width	b	0.17	0.22	0.27
Mold Draft Angle Top	α	11°	12°	13°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensioning and tolerancing per ASME Y14.5M

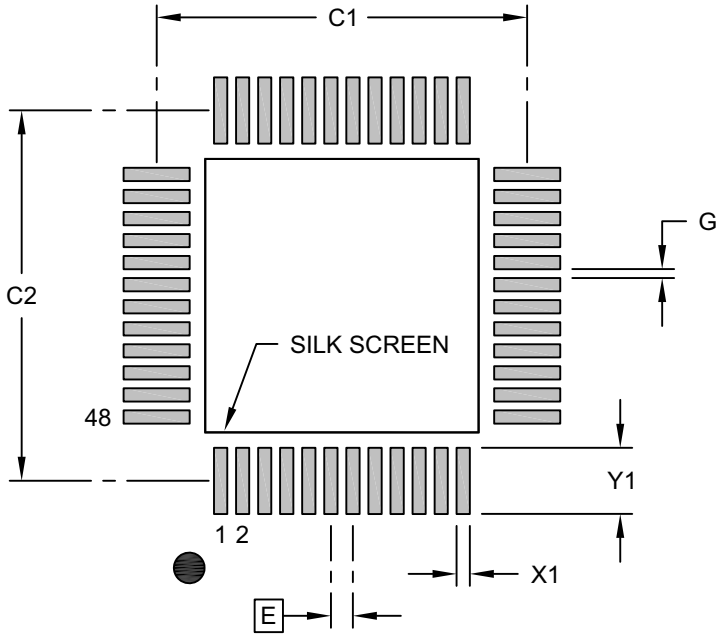
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-278 Rev A Sheet 2 of 2

48-Lead Low-profile Plastic Quad Flat Pack Package (R8) -7x7 mm Body [LQFP] Supertex Legacy Package

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.50 BSC		
Contact Pad Spacing	C1		8.40	
Contact Pad Spacing	C2		8.40	
Contact Pad Width (X48)	X1			0.30
Contact Pad Length (X48)	Y1			1.50
Contact Pad to Contact Pad (X44)	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-2278 Rev A

NOTES:

APPENDIX A: REVISION HISTORY

Revision A (July 2020)

- Original Release of this Document.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	X	-X	/XX
Device	Tape and Reel	Environmental	Package

Device:	HV2607:	No High-Voltage Bias, 16-Channel High-Voltage Analog Switch (Tape and Reel)
	HV2707:	No High-Voltage Bias, 16-Channel High-Voltage Analog Switch with Bleed Resistor at Both Sides of Switch (Tape and Reel)
	HV2708:	No High-Voltage Bias, 16-Channel High-Voltage Analog Switch with Bleed Resistor at One Side of Switch (Tape and Reel)
Environmental:	C =	Lead (Pb)-Free/ROHS-Compliant Package
Package:	R8X =	Low Profile Plastic Quad Flat Pack Package, 7x7 mm Body, 48-Lead (LQFP)

Examples:

a) HV2607T-C/R8X: No High-Voltage Bias, 16-Channel High-Voltage Analog Switch, 48-Lead LQFP package.

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

NOTES:

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- Microchip is willing to work with the customer who is concerned about the integrity of their code.
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