Product Change Notification / SYST-10QRAR381

Date:

16-Feb-2021

Product Category:

8-bit Microcontrollers

PCN Type:

Document Change

Notification Subject:

ERRATA - ATmega4808/4809 Silicon Errata and Data Sheet Clarification

Affected CPNs:

SYST-10QRAR381_Affected_CPN_02162021.pdf
SYST-10QRAR381_Affected_CPN_02162021.csv

Notification Text:

SYST-10QRAR381

Microchip has released a new Product Documents for the ATmega4808/4809 Silicon Errata and Data Sheet Clarification of devices. If you are using one of these devices please read the document located at ATmega4808/4809 Silicon Errata and Data Sheet Clarification.

Notification Status: Final

Description of Change:1) Added new errata:
- – Device: 2.2.1 Writing the OSCLOCK Fuse in FUSE.OSCCFG to '1' Prevents Automatic Loading of Calibration Values
- – TCA: 2.8.1 Restart Will Reset Counter Direction in NORMAL and FRQ Mode
- – TCB: 2.9.3 CCMP and CNT Registers Operate as 16-Bit Registers in 8-Bit PWM Mode
- – USART:
  - 2.10.2 Open-Drain Mode Does Not Work When TXD is Configured as Output
  - 2.10.3 Start-of-Frame Detection Can Unintentionally Be Triggered in Active Mode

2) New hold place for CPUINT errata: After Device errata

Impacts to Data Sheet: None

Reason for Change: To Improve Productivity

Change Implementation Status: Complete

Date Document Changes Effective: 16 Feb 2021

NOTE: Please be advised that this is a change to the document only the product has not been changed.

Markings to Distinguish Revised from Unrevised Devices: N/A

Attachments:

ATmega4808/4809 Silicon Errata and Data Sheet Clarification

Please contact your local Microchip sales office with questions or concerns regarding this notification.

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Affected Catalog Part Numbers (CPN)

ATMEGA4809-AFR-VAO
ATMEGA4809-AU
ATMEGA4809-AUR
ATMEGA4809-MF
ATMEGA4809-MF-VAO
ATMEGA4809-MFR
ATMEGA4809-MFR-VAO
ATMEGA4809-MU
ATMEGA4809-MUR
ATMEGA4809-PF
ATMEGA4809-XPRO
ATMEGA4808-AF
ATMEGA4808-AFR
ATMEGA4808-AFR-VAO
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ATMEGA4808-MFR-VAO
ATMEGA4808-MU
ATMEGA4808-MUR
ATMEGA4808-XF
ATMEGA4808-XFR
ATMEGA4808-XFR-VAO
ATMEGA4808-XU
ATMEGA4808-XUR
ATMEGA4809-AF
ATMEGA4809-AF-VAO
ATMEGA4809-AFR
ATMEGA4809-AFR-V01

ATmega4808/4809 Silicon Errata and Data Sheet Clarification

ATmega4808/4809 Silicon Errata and Data Sheet Clarification

The ATmega4808/4809 devices of the megaAVR® 0-series you have received conform functionally to the current device data sheet (www.microchip.com/DS40002173), except for the anomalies described in this document. The errata described in this document will likely be addressed in future revisions of the ATmega4808/4809 devices.

Notes:

- This document summarizes all the silicon errata issues from all revisions of silicon, previous as well as current
- Refer to the Device/Revision ID section in the current device data sheet (www.microchip.com/DS40002173) for more detailed information on Device Identification and Revision IDs for your specific device, or contact your local Microchip sales office for assistance

1. Silicon Issue Summary

Legend

- **-** Erratum is not applicable.
- **X** Erratum is applicable.

Errata Overview

Peripheral	Short Description	Valid for Silicon Revision
		Rev. B(1)
DEVICE	2.2.1 Writing the OSCLOCK Fuse in FUSE.OSCCFG to '1' Prevents Automatic Loading of Calibration Values	X
CPUINT	2.3.1 Interrupt Level 1 Does Not Work	X
PORTMUX	2.4.1 SPI SS Pin is Connected to Pin Even if SPI is Configured to Have No Port Connection	X
ADC	2.5.1 One Extra Measurement Performed After Disabling ADC Free-Running Mode	X
	2.5.2 Pending Event Stuck When Disabling the ADC	X
	2.5.3 ADC Functionality Cannot be Ensured with CLKADC Above 1.5 MHz and a Setting of 25% Duty Cycle	X
	2.5.4 ADC Performance Degrades with CLKADC Above 1.5 MHz and VDD < 2.7V	X
CCL	2.6.1 D-latch is Not Functional	X
RTC	2.7.1 Any Write to the RTC.CTRLA Register Resets the RTC and PIT Prescaler	X
TCA	2.8.1 Restart Will Reset Counter Direction in NORMAL and FRQ Mode	X
TCB	2.9.1 The TCA Restart Command Does Not Force a Restart of TCB	X
	2.9.2 Minimum Event Duration Must Exceed the Selected Clock Period	X
	2.9.3 CCMP and CNT Registers Operate as 16-Bit Registers in 8-Bit PWM Mode	X
USART	2.10.1 TXD Pin Override Not Released When Disabling the Transmitter	X
	2.10.2 Open-Drain Mode Does Not Work When TXD is Configured as Output	X
	2.10.3 Start-of-Frame Detection Can Unintentionally Be Triggered in Active Mode	X

Note:

1. This revision is the initial release of the silicon.

2. Silicon Errata

2.1 Errata Details

-	Erratum is not applicable.
X	Erratum is applicable.

2.2 Device

2.2.1 Writing the OSCLOCK Fuse in FUSE.OSCCFG to '1' Prevents Automatic Loading of Calibration Values

Writing the OSCLOCK fuse in FUSE.OSCCFG to '1' prevents the automatic loading of calibration values from the signature row. The device will run with an uncalibrated OSC20M oscillator.

Work Around

Do not use OSCLOCK for locking the oscillator calibration value. The oscillator calibration value can be locked by writing LOCK in CLKCTRL.OSC20MCALIBB to '1'.

Affected Silicon Revisions

Rev. B
X

2.3 CPUINT

2.3.1 Interrupt Level 1 Does Not Work

Interrupt Level 1 may fail to execute correctly by executing the Reset vector rather than the intended interrupt vector. This only applies to the following products and is limited to date codes older than 1914 (week 14 of 2019).

- ATMEGA4809-AF
- ATMEGA4809-AFR
- ATMEGA4809-AU
- ATMEGA4809-AUR
- ATMEGA4809-MF
- ATMEGA4809-MFR
- ATMEGA4809-MU
- ATMEGA4809-MUR
- ATMEGA4809-PF

Work Around

Use Interrupt Level 0 instead of Interrupt Level 1.

Affected Silicon Revisions

Rev. B
X

2.4 PORTMUX

2.4.1 SPI $\overline{SS}$ Pin is Connected to Pin Even if SPI is Configured to Have No Port Connection

The SPIn $\overline{SS}$ pin is connected even if NONE is selected in the SPIn field in PORTMUX.TWISPIROUTE. If SPIn is operating in Host mode and the $\overline{SS}$ pin goes low, or input is disabled, the SPIn will exit Host mode.

Work around
Write the SSD bit in SPIn.CTRLB to '1' to ignore the $\overline{SS}$ signal.

Affected Silicon Revisions

Rev. B
X

2.5 ADC

2.5.1 One Extra Measurement Performed After Disabling ADC Free-Running Mode

The ADC may perform one additional measurement after clearing ADCn.CTRLA.FREERUN.

Work Around
Write ADCn.CTRLA.ENABLE to '0' to stop the Free-Running mode immediately.

Affected Silicon Revisions

Rev. B
X

2.5.2 Pending Event Stuck When Disabling the ADC

If the ADC is disabled during an event-triggered conversion, the event will not be cleared.

Work Around
Clear ADC.EVCTRL.STARTEI and wait for the conversion to complete before disabling the ADC.

Affected Silicon Revisions

Rev. B
X

2.5.3 ADC Functionality Cannot be Ensured with CLK_{ADC} Above 1.5 MHz and a Setting of 25% Duty Cycle

The ADC functionality cannot be ensured if CLK_{ADC} > 1.5 MHz with ADCn.CALIB.DUTYCYC set to '1'.

Work around
If ADC is operated with CLK_{ADC} > 1.5 MHz, ADCn.CALIB.DUTYCYC must be set to '0' (50% duty cycle).

Affected Silicon Revisions

Rev. B

X

2.5.4 ADC Performance Degrades with CLK_{ADC} Above 1.5 MHz and V_{DD} < 2.7V

The ADC INL performance degrades if CLK_{ADC} > 1.5 MHz and ADCn.CALIB.DUTYCYC set to '0' for V_{DD} < 2.7V.

Work Around
None.

Affected Silicon Revisions

Rev. B
X

2.6 CCL

2.6.1 D-latch is Not Functional

The CCL D-latch is not functional.

Work Around
None.

Affected Silicon Revisions

Rev. B
X

2.7 RTC

2.7.1 Any Write to the RTC.CTRLA Register Resets the RTC and PIT Prescaler

Any write to the RTC.CTRLA register resets the 15-bit prescaler resulting in a longer period on the current count or period.

Work Around
None.

Affected Silicon Revisions

Rev. B
X

2.8 TCA

2.8.1 Restart Will Reset Counter Direction in NORMAL and FRQ Mode

When the TCA is configured to the NORMAL or FRQ mode (WGMODE in TCAn.CTRLB is '0x0' or '0x1'), a RESTART command or Restart event will reset direction to default. The default is counting upwards.

Work Around
None.

Affected Silicon Revisions

Rev. B
X

2.9 TCB

2.9.1 The TCA Restart Command Does Not Force a Restart of TCB

The TCA restart command does not force restarting the TCB when TCB is running in SYNCUPD mode. TCB is restarted only after a TCA OVF.

Work Around

None.

Affected Silicon Revisions

Rev. B
X

2.9.2 Minimum Event Duration Must Exceed the Selected Clock Period

Event detection will fail if TCBn receives an input event with a high/low period shorter than the period of the selected clock source (CLKSEL in TCBn.CTRLA). This applies to the TCB modes (CNTMODE in TCBn.CTRLB) *Time-Out Check* and *Input Capture Frequency and Pulse-Width Measurement* mode.

Work Around

Ensure that the high/low period of input events is equal to or longer than the selected clock source (CLKSEL in TCBn.CTRLA) period.

Affected Silicon Revisions

Rev. B
X

2.9.3 CCMP and CNT Registers Operate as 16-Bit Registers in 8-Bit PWM Mode

When the TCB operates in 8-bit PWM mode (CNTMODE in TCBn.CTRLB is '0x7'), the low and high bytes for the CNT and CCMP registers operate as 16-bit registers for read and write. They cannot be read or written independently.

Work Around

Use 16-bit register access. Refer to the data sheet for further information.

Affected Silicon Revisions

Rev. A4	Rev. A5
X	X

2.10 USART

2.10.1 TXD Pin Override Not Released When Disabling the Transmitter

The USART will not release the TXD pin override if:

- The USART transmitter is disabled by writing the TXEN bit in USART.CTRLB to '0' while the USART receiver is disabled (RXEN in USART.CTRLB is '0')
- Both the USART transmitter and receiver are disabled at the same time by writing the TXEN and RXEN bits in USART.CTRLB to '0'

Work Around
There are two possible work arounds:

- Make sure the receiver is enabled (RXEN in USART.CTRLB is '1') while disabling the transmitter (writing TXEN in USART.CTRLB to '0')
- Writing to any register in the USART after disabling the transmitter will start the USART for long enough to release the pin override of the TXD pin

Affected Silicon Revisions

Rev. B
X

2.10.2 Open-Drain Mode Does Not Work When TXD is Configured as Output

When the USART TXD pin is configured as an output, it can drive the pin high regardless of whether the Open-Drain mode is enabled or not.

Work Around
Configure the TXD pin as an input by writing the corresponding bit in PORTx.DIR to '0' when using Open-Drain mode.

Affected Silicon Revisions

Rev. B
X

2.10.3 Start-of-Frame Detection Can Unintentionally Be Triggered in Active Mode

The Start-of-Frame Detection feature enables the USART to wake up from Standby sleep mode upon data reception.

The Start-of-Frame Detector can unintentionally be triggered when the Start-of-Frame Detection Enable (SFDEN) bit in the USART Control B (USARTn.CTRLB) register is set, and the device is in Active mode. If the Receive Data (RXDATA) registers are read while receiving new data, the Receive Complete Interrupt Flag (RXCIF) in the USARTn.STATUS register is cleared. This results in the Start-of-Frame Detector being triggered and falsely detecting the following falling edge as a start bit. When the Start-of-Frame Detector detects a start condition, the frame reception is restarted, resulting in corrupt received data.

Note that the USART Receive Start Interrupt Flag (RXSIF) always is '0' when in Active mode. No interrupt will be triggered.

Work Around
Disable Start-of-Frame Detection by writing '0' to the Start-of-Frame Detection Enable (SFDEN) bit in the USART Control B (USARTn.CTRLB) register when the device is in Active mode. Enable it again by writing the bit to '1' before transitioning to Standby sleep mode. This work around depends on a protocol preventing a new incoming frame when re-enabling Start-of-Frame Detection. Re-enabling Start-of-Frame Detection, while a new frame is already incoming, will result in corrupted received data.

Affected Silicon Revisions

Rev. B
X

3. Data Sheet Clarifications

None.

4. Document Revision History

Note: The document revision is independent of the silicon revision.

4.1 Revision History

Doc Rev.	Date	Comments
B	02/2021	• Added new errata: – Device: 2.2.1 Writing the OSCLOCK Fuse in FUSE.OSCCFG to '1' Prevents Automatic Loading of Calibration Values – TCA: 2.8.1 Restart Will Reset Counter Direction in NORMAL and FRQ Mode – TCB: 2.9.3 CCMP and CNT Registers Operate as 16-Bit Registers in 8-Bit PWM Mode – USART: • 2.10.2 Open-Drain Mode Does Not Work When TXD is Configured as Output • 2.10.3 Start-of-Frame Detection Can Unintentionally Be Triggered in Active Mode • New hold place for CPUINT errata: After Device errata
A	01/2020	• Document – Change document structure from one document for the entire megaAVR 0-series to one document per data sheet: • from: megaAVR-0-series-Errata-and-Clarification-80000777C.pdf • to: ATmega4808_4809-Errata-and-Clarification-DS80000867A.pdf – Updated document template • Errata – The ADC errata, ADC Functionality Cannot be Ensured with ADCCLK Above 1.5 MHz for All Conditions, has been split into two separate erratas and rewritten

4.2 Appendix - Obsolete Revision History

Note: Due to document structure change from a single megaAVR 0-series to one document per data sheet, the following history from www.microchip.com/DS80000777 is provided as reference.

Doc Rev.	Date	Comments
C	08/2019	• New Errata: – CPUINT: Interrupt Level 1 Does Not Work **Note:** Only applicable to ATmega4808/4809 for specific date codes.

.....continued

Doc Rev.	Date	Comments
B	07/2019	• Document – Adding variants with 16 KB and 8 KB Flash – Adding 40-pin variant of ATmega4809 – Changing document title – Adding section "Data Sheet Clarifications" • New Errata: – PORTMUX: SPI SS is Connected to Pin Even if SPI is Configured to Have No Port Connection – TCB: Minimum Event Duration Must Exceed Selected Clock Period – USART: TXD Pin Override Not Released When Disabling the Transmitter • Erratum for TCA removed: Issuing a restart will clear the direction bit - the data sheet is describing this correctly.
A	02/2018	• Initial document release.

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