

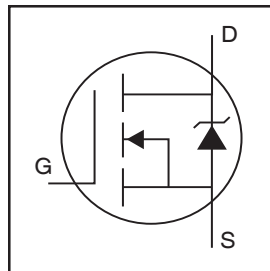
- Surface Mount (IRLR120N)
- Straight Lead (IRLU120N)
- Advanced Process Technology
- Fast Switching
- Fully Avalanche Rated
- Lead-Free

Description

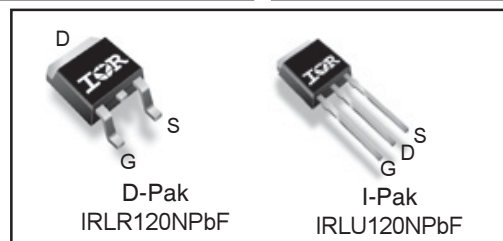
Fifth Generation HEXFETs from International Rectifier utilize advanced processing techniques to achieve the lowest possible on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that HEXFET Power MOSFETs are well known for, provides the designer with an extremely efficient device for use in a wide variety of applications.

The D-PAK is designed for surface mounting using vapor phase, infrared, or wave soldering techniques. The straight lead version (IRFU series) is for through-hole mounting applications. Power dissipation levels up to 1.5 watts are possible in typical surface mount applications.

HEXFET® Power MOSFET



| |
|----------------------------|
| $V_{DSS} = 100V$ |
| $R_{DS(on)} = 0.185\Omega$ |
| $I_D = 10A$ |



| Base Part Number | Package Type | Standard Pack | | Orderable Part Number | Note |
|------------------|--------------|---------------------|----------|-----------------------|------------------|
| | | Form | Quantity | | |
| IRLR120NPbF | D-Pak | Tube | 75 | IRLR120NPbF | |
| | | Tape and Reel | 2000 | IRLR120NTRPbF | |
| | | Tape and Reel Left | 3000 | IRLR120NTRLpbF | |
| | | Tape and Reel Right | 3000 | IRLR120NTRRPbF | EOL notice # 289 |
| IRLU120NPbF | IPak | Tube | 75 | IRLU120NPbF | |

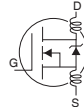
Absolute Maximum Ratings

| | Parameter | Max. | Units |
|---------------------------|--|--------------|-------|
| $I_D @ T_C = 25^\circ C$ | Continuous Drain Current, $V_{GS} @ 10V$ | 10 | A |
| $I_D @ T_C = 100^\circ C$ | Continuous Drain Current, $V_{GS} @ 10V$ | 7.0 | |
| I_{DM} | Pulsed Drain Current ①⑥ | 35 | |
| $P_D @ T_C = 25^\circ C$ | Power Dissipation | 48 | W |
| | Linear Derating Factor | 0.32 | W/°C |
| V_{GS} | Gate-to-Source Voltage | ± 16 | V |
| E_{AS} | Single Pulse Avalanche Energy②⑥ | 85 | mJ |
| I_{AR} | Avalanche Current①⑥ | 6.0 | A |
| E_{AR} | Repetitive Avalanche Energy①⑥ | 4.8 | mJ |
| dv/dt | Peak Diode Recovery dv/dt ③ | 5.0 | V/ns |
| T_J | Operating Junction and Storage Temperature Range | -55 to + 175 | °C |
| T_{STG} | | | |

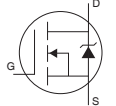
Thermal Resistance

| | Parameter | Typ. | Max. | Units |
|-----------------|------------------------------------|------|------|-------|
| $R_{\theta JC}$ | Junction-to-Case | — | 3.1 | °C/W |
| $R_{\theta JA}$ | Junction-to-Ambient (PCB mount) ** | — | 50 | |
| $R_{\theta JA}$ | Junction-to-Ambient | — | 110 | |

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

| | Parameter | Min. | Typ. | Max. | Units | Conditions |
|--|--------------------------------------|------|------|-------|-------|--|
| V _{(BR)DSS} | Drain-to-Source Breakdown Voltage | 100 | — | — | V | V _{GS} = 0V, I _D = 250μA |
| ΔV _{(BR)DSS} /ΔT _J | Breakdown Voltage Temp. Coefficient | — | 0.12 | — | V/°C | Reference to 25°C, I _D = 1mA |
| R _{DS(on)} | Static Drain-to-Source On-Resistance | — | — | 0.185 | Ω | V _{GS} = 10V, I _D = 6.0A ④ |
| | | — | — | 0.225 | | V _{GS} = 5.0V, I _D = 6.0A ④ |
| | | — | — | 0.265 | | V _{GS} = 4.0V, I _D = 5.0A ④ |
| V _{GS(th)} | Gate Threshold Voltage | 1.0 | — | 2.0 | V | V _{DS} = V _{GS} , I _D = 250μA |
| g _{fs} | Forward Transconductance | 3.1 | — | — | S | V _{DS} = 25V, I _D = 6.0A ⑥ |
| I _{DSS} | Drain-to-Source Leakage Current | — | — | 25 | μA | V _{DS} = 100V, V _{GS} = 0V |
| | | — | — | 250 | | V _{DS} = 80V, V _{GS} = 0V, T _J = 150°C |
| I _{GSS} | Gate-to-Source Forward Leakage | — | — | 100 | nA | V _{GS} = 16V |
| | Gate-to-Source Reverse Leakage | — | — | -100 | | V _{GS} = -16V |
| Q _g | Total Gate Charge | — | — | 20 | nC | I _D = 6.0A |
| Q _{gs} | Gate-to-Source Charge | — | — | 4.6 | | V _{DS} = 80V |
| Q _{gd} | Gate-to-Drain ("Miller") Charge | — | — | 10 | | V _{GS} = 5.0V, See Fig. 6 and 13 ④ ⑥ |
| t _{d(on)} | Turn-On Delay Time | — | 4.0 | — | ns | V _{DD} = 50V |
| t _r | Rise Time | — | 35 | — | | I _D = 6.0A |
| t _{d(off)} | Turn-Off Delay Time | — | 23 | — | | R _G = 11Ω, V _{GS} = 5.0V |
| t _f | Fall Time | — | 22 | — | | R _D = 8.2Ω, See Fig. 10 ④ ⑥ |
| L _D | Internal Drain Inductance | — | 4.5 | — | nH | Between lead, 6mm (0.25in.) from package and center of die contact ③ |
| L _S | Internal Source Inductance | — | 7.5 | — | |  |
| C _{iss} | Input Capacitance | — | 440 | — | pF | V _{GS} = 0V |
| C _{oss} | Output Capacitance | — | 97 | — | | V _{DS} = 25V |
| C _{rss} | Reverse Transfer Capacitance | — | 50 | — | | f = 1.0MHz, See Fig. 5 ⑥ |

Source-Drain Ratings and Characteristics

| | Parameter | Min. | Typ. | Max. | Units | Conditions |
|-----------------|---|--|------|------|-------|--|
| I _S | Continuous Source Current (Body Diode) | — | — | 10 | A | MOSFET symbol showing the integral reverse p-n junction diode.  |
| I _{SM} | Pulsed Source Current (Body Diode) ① ⑥ | — | — | 35 | | |
| V _{SD} | Diode Forward Voltage | — | — | 1.3 | V | T _J = 25°C, I _S = 6.0A, V _{GS} = 0V ④ |
| t _{rr} | Reverse Recovery Time | — | 110 | 160 | ns | T _J = 25°C, I _F = 6.0A |
| Q _{rr} | Reverse Recovery Charge | — | 410 | 620 | nC | di/dt = 100A/μs ④ ⑥ |
| t _{on} | Forward Turn-On Time | Intrinsic turn-on time is negligible (turn-on is dominated by L _S +L _D) | | | | |

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11) ④ Pulse width ≤ 300μs; duty cycle ≤ 2%.
- ② V_{DD} = 25V, starting T_J = 25°C, L = 4.7mH ⑤ This is applied for I-PAK, L_S of D-PAK is measured between lead and center of die contact
- ③ I_{SD} ≤ 6.0A, di/dt ≤ 340A/μs, V_{DD} ≤ V_{(BR)DSS}, T_J ≤ 175°C ⑥ Uses IRL520N data and test conditions.

** When mounted on 1" square PCB (FR-4 or G-10 Material) .
For recommended footprint and soldering techniques refer to application note #AN-994

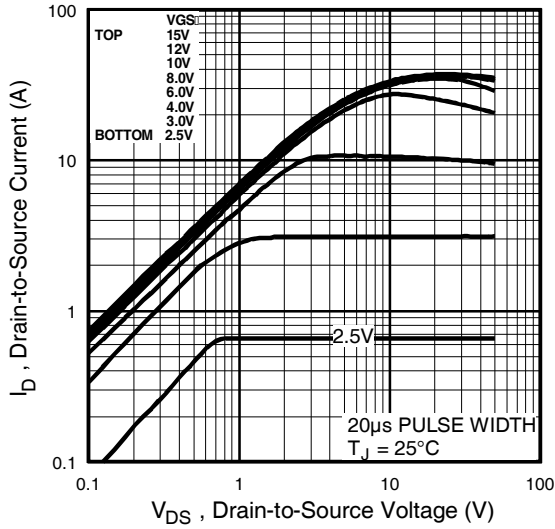


Fig 1. Typical Output Characteristics

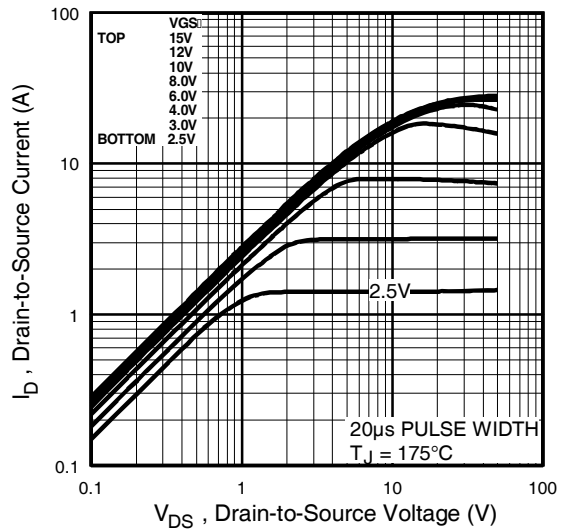


Fig 2. Typical Output Characteristics

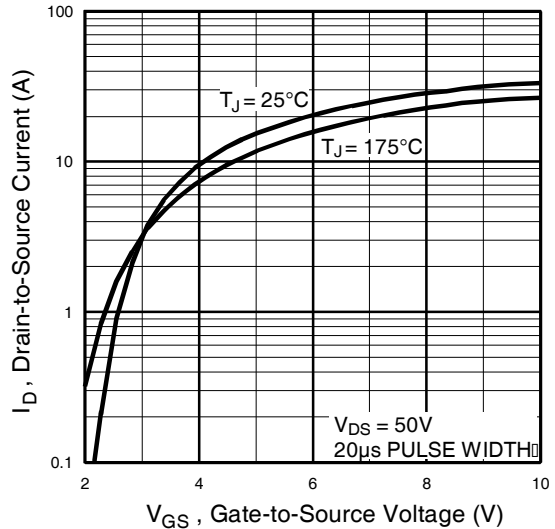


Fig 3. Typical Transfer Characteristics

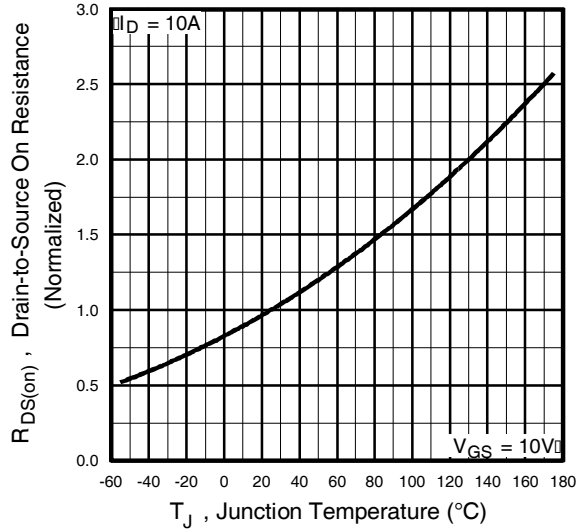


Fig 4. Normalized On-Resistance Vs. Temperature

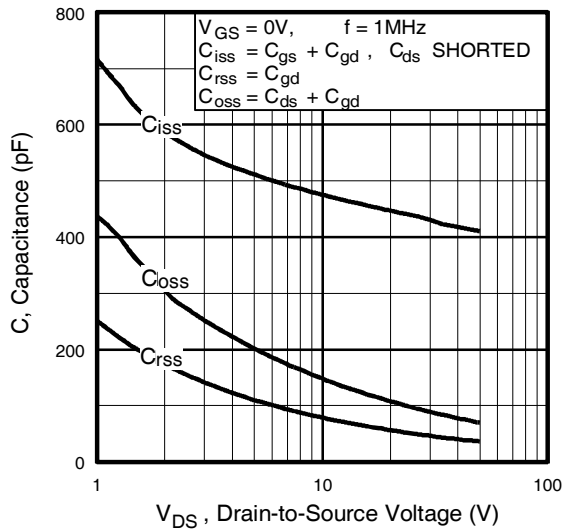


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

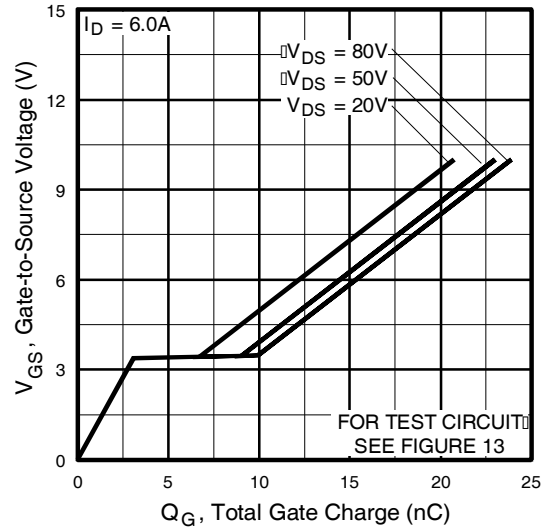


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

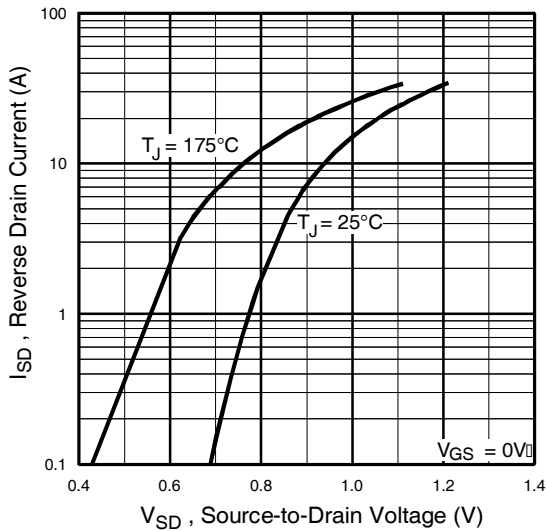


Fig 7. Typical Source-Drain Diode Forward Voltage

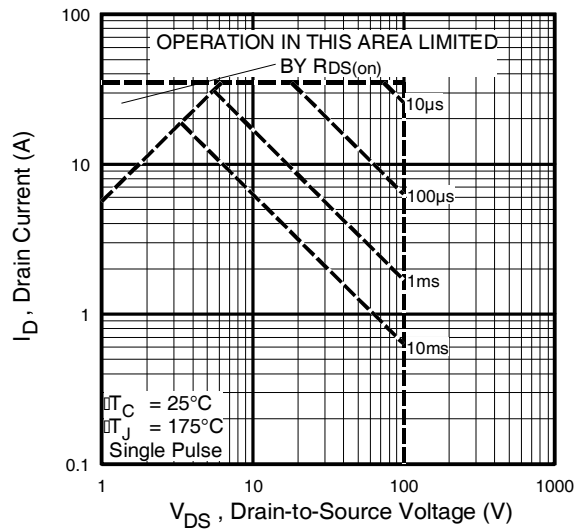


Fig 8. Maximum Safe Operating Area

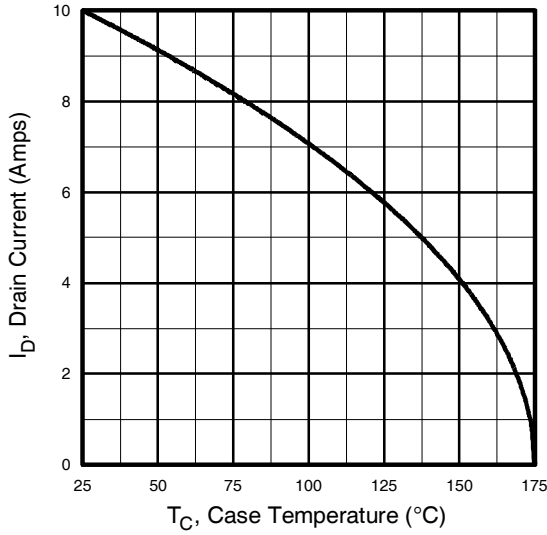


Fig 9. Maximum Drain Current Vs. Case Temperature

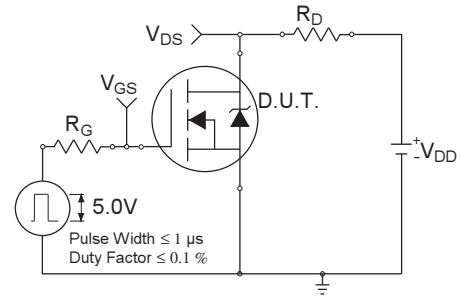


Fig 10a. Switching Time Test Circuit

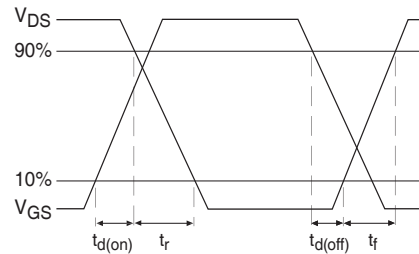


Fig 10b. Switching Time Waveforms

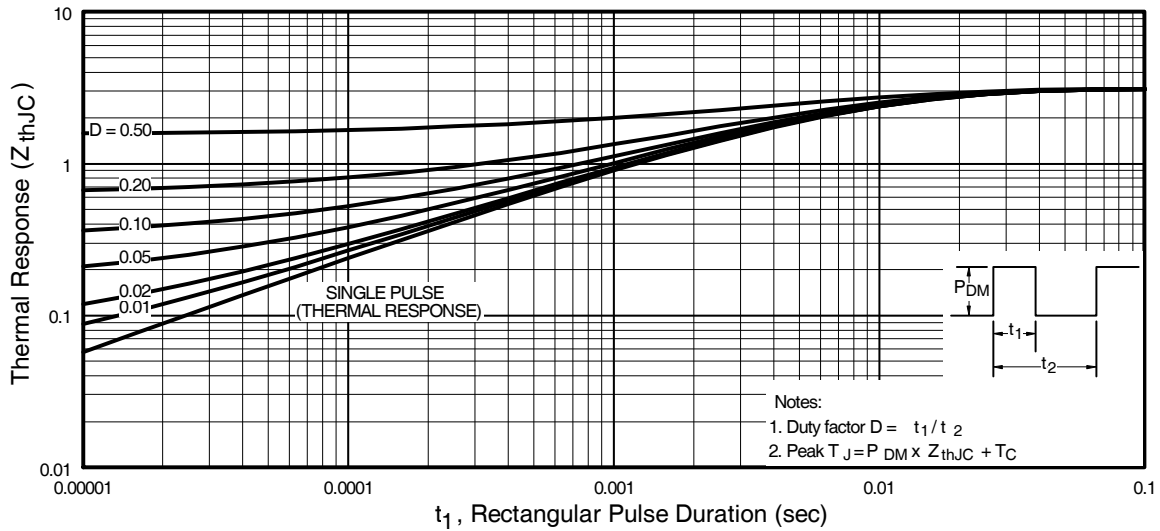
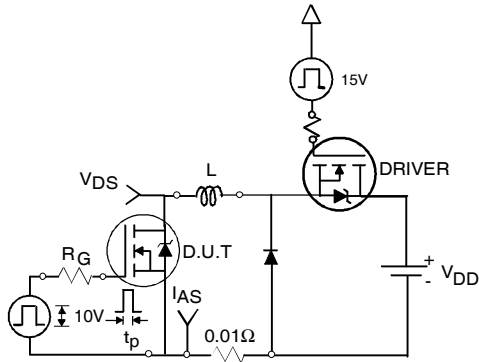
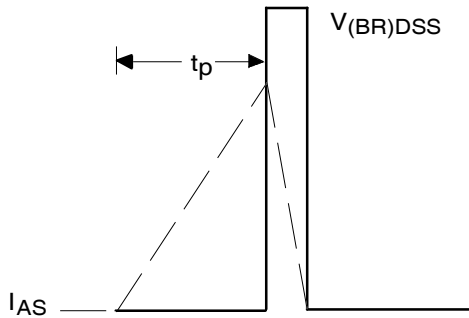
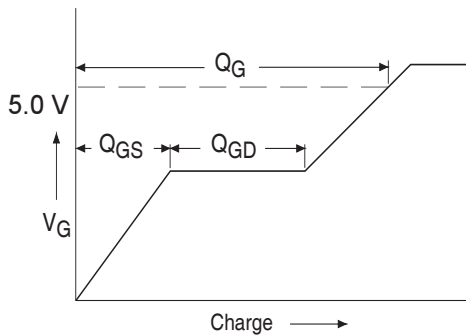
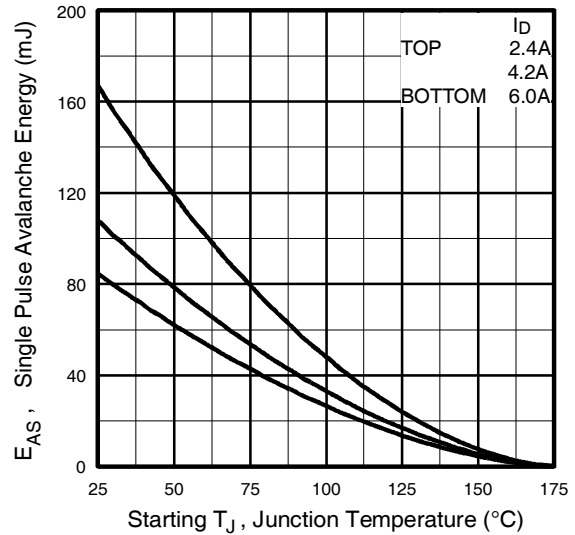
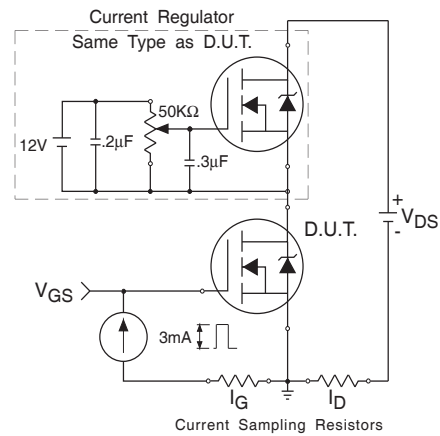
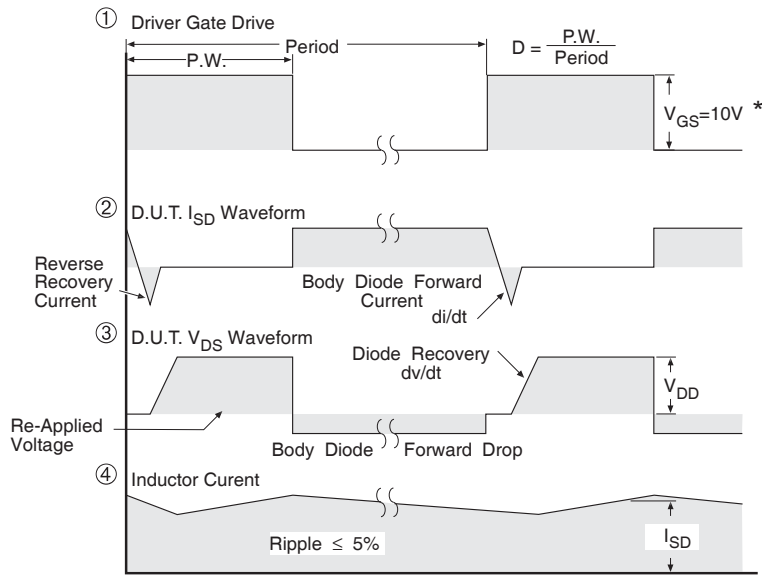
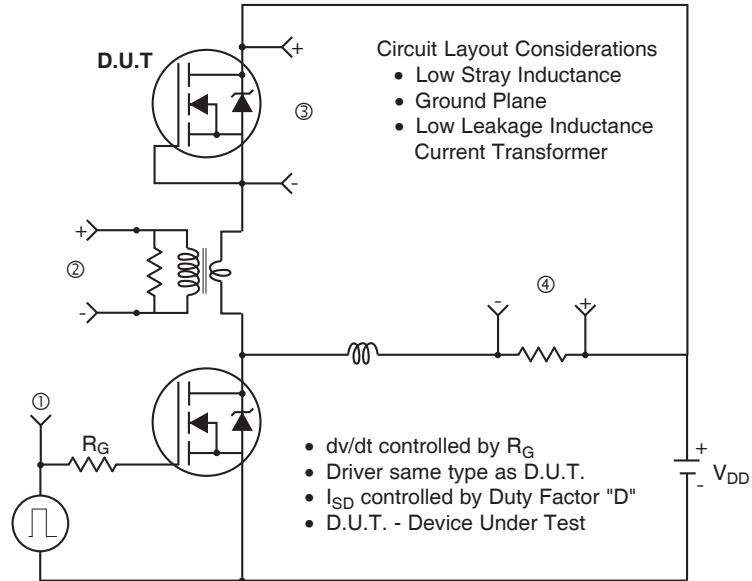


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case


Fig 12a. Unclamped Inductive Test Circuit

Fig 12b. Unclamped Inductive Waveforms

Fig 13a. Basic Gate Charge Waveform

Fig 12c. Maximum Avalanche Energy Vs. Drain Current

Fig 13b. Gate Charge Test Circuit

Peak Diode Recovery dv/dt Test Circuit

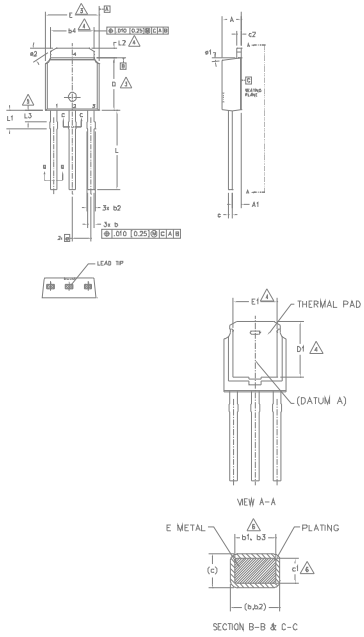


* $V_{GS} = 5V$ for Logic Level Devices

Fig 14. For N-Channel HEXFETS

I-Pak (TO-251AA) Package Outline

Dimensions are shown in millimeters (inches)



- NOTES:
- 1.- DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
 - 2.- DIMENSION ARE SHOWN IN INCHES [MILLIMETERS]
 - 3.- DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005 [0.13] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY.
 - 4.- THERMAL PAD CONTOUR OPTION WITHIN DIMENSION b4, L2, E1 & D1.
 - 5.- LEAD DIMENSION UNCONTROLLED IN L3.
 - 6.- DIMENSION b1, b3 & c1 APPLY TO BASE METAL ONLY.
 - 7.- OUTLINE CONFORMS TO JEDEC OUTLINE TO-251AA (Date 06/02).
 - 8.- CONTROLLING DIMENSION : INCHES.

| SYMBOL | DIMENSIONS | | | | NOTES |
|--------|-------------|------|--------|------|-------|
| | MILLIMETERS | | INCHES | | |
| | MIN. | MAX. | MIN. | MAX. | |
| A | 2.18 | 2.39 | .086 | .094 | |
| A1 | 0.89 | 1.14 | .035 | .045 | |
| b | 0.64 | 0.89 | .025 | .035 | |
| b1 | 0.65 | 0.79 | .025 | .031 | 6 |
| b2 | 0.76 | 1.14 | .030 | .045 | |
| b3 | 0.76 | 1.04 | .030 | .041 | 6 |
| b4 | 4.95 | 5.46 | .195 | .215 | 4 |
| c | 0.46 | 0.61 | .018 | .024 | |
| c1 | 0.41 | 0.56 | .016 | .022 | 6 |
| c2 | 0.46 | 0.89 | .018 | .035 | |
| D | 5.97 | 6.22 | .235 | .245 | 3 |
| D1 | 5.21 | - | .205 | - | 4 |
| E | 6.35 | 6.73 | .250 | .265 | 3 |
| E1 | 4.32 | - | .170 | - | 4 |
| e | 2.29 | BSC | .090 | BSC | |
| L | 8.89 | 9.65 | .350 | .380 | |
| L1 | 1.91 | 2.29 | .045 | .090 | |
| L2 | 0.89 | 1.27 | .035 | .050 | 4 |
| L3 | 0.89 | 1.52 | .035 | .060 | 5 |
| ø1 | 0" | 15" | 0" | 15" | |
| ø2 | 25" | 35" | 25" | 35" | |

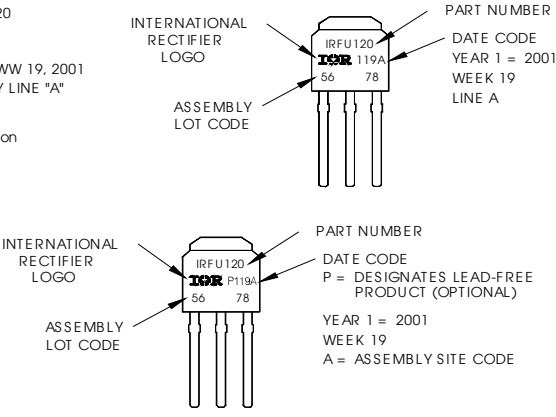
- LEAD ASSIGNMENTS
- HEXFET
- 1.- GATE
 - 2.- DRAIN
 - 3.- SOURCE
 - 4.- DRAIN

I-Pak (TO-251AA) Part Marking Information

EXAMPLE: THIS IS AN IRFU120 WITH ASSEMBLY LOT CODE 5678 ASSEMBLED ON WW 19, 2001 IN THE ASSEMBLY LINE "A"

Note: "P" in assembly line position indicates Lead-Free"

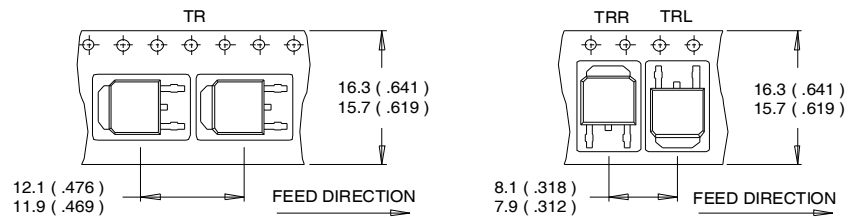
OR



Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

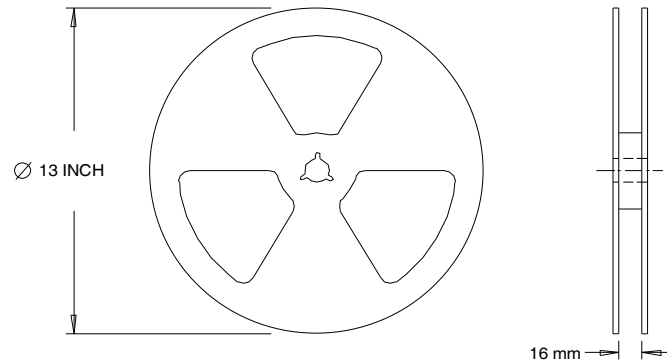
D-Pak (TO-252AA) Tape & Reel Information

Dimensions are shown in millimeters (inches)



NOTES :

1. CONTROLLING DIMENSION : MILLIMETER.
2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).
3. OUTLINE CONFORMS TO EIA-481 & EIA-541.



NOTES :

1. OUTLINE CONFORMS TO EIA-481.

Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

Qualification information[†]

| | | |
|----------------------------|--|------|
| Qualification level | Industrial (per JEDEC JESD47F ^{††} guidelines) | |
| Moisture Sensitivity Level | D-Pak | MSL1 |
| | I-Pak | |
| RoHS compliant | Yes | |

[†] Qualification standards can be found at International Rectifier's web site: <http://www.irf.com/product-info/reliability>

^{††} Applicable version of JEDEC standard at the time of product release

Revision History

| Date | Comment |
|----------|---|
| 7/9/2014 | <ul style="list-style-type: none"> • Updated Electrical parameter table typo on R_{dson} units from "W" to "Ω" on page2. • Updated Package outline on page 8 & page 9. • Added Orderable table on page1. • Updated datasheet with IR corporate template. • Updated ordering information to reflect the End-Of-life (EOL notice #289) • Added Qualification table on page10. |

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