AN-Power stage of 48V BSG inverter

Reference design with TOLL & TOLG MOSFET

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About this document

Scope and purpose

The power stage was developed to support customers during their first steps in designing 48V inverter for Belt-driven Starter Generator (BSG) application. The document provides a detailed description of the main components and their functionality. This information is intended to enable the customers to re-use and modify the original design and qualify their own design for the production, according to their own specific requirements.

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1 Introduction

The power stage shown in Figure 1 was developed to support customers during their first steps in designing 48V inverter for BSG applications. A logic board with driver circuit is necessary for evaluation. The following chapters provide a detailed description of the main components and their functionality. This information is intended to enable the customers to re-use and modify the original design and qualify their own design for the production, according to their own specific requirements.

The boards provided by Infineon Technologies are subjected to functional testing only.

The current implementation of the design is for reference only! It does not cover in general all application specific requirements. For specific recommendations on how to implement designs with TOLL MOSFET, please contact your local Infineon sales partner. More information is available on www.infineon.com.

Due to their purpose the system is not subjected to the same procedures regarding Returned Material Analysis (RMA), Process Change Notification (PCN) and Product Withdraw (PWD) as regular products.

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Figure 1 **Overview of the power stage**

Introduction

Belt-driven Starter Generator (BSG) is used as a motor in the Micro-Hybrid vehicle to enhance the output torque of the engine. Inverter of BSG need compactly mounted on the bottom of motor. The power supply is DC 48V. The peak power is 12kW. The power stage including paralleled MOSFET should be assigned on a round shape to fit the shape of the motor. The output current will be up to 400Arms. More than 550W power loss would be generated. The challenge is to get 3 key performances in 150mm diameter round space. The performances are: well-balanced current in the paralleled MOSFET, low V_{DS} spike at switching off, low R_{th} of heatsink system.

Using customized MOSFET module is the state of art. The outline of the module is fixed by specific motor. It's not easy to reuse in other project. So that different customer should customize different module. Even the same customer should customize several modules for different vehicle platform.

This reference design is a solution of discrete MOSFET with IMS board. It is very easy to reuse and modify for customer to adapt their system. The scalability and feasibility are the strength of this reference design. Customer can change the R_{DSon} with same package to get different power capability. And reduce the number of paralleling MOSFET is another good choice for tuning the size and the power capability. The current are well balanced so that the temperature deference could be down to 2°C. The V_{DS} spike of switching off 570A current is only 19V at 48V DC bus. R_{th} of junction to coolant could be around 2 K/W.

Note: A logic board with driver circuit is necessary for evaluation.

2 Quick Start Guide

The power stage should be used with heatsink and be connected with power cable and signal cable. Chapter 2.1 shows the block diagram of BSG inverter. Chapter 2.2 shows the heatsink. Chapter 2.3 shows the signal connector. Chapter 2.4 shows the power terminals.

2.1 Block Diagram

Figure 2 shows the block diagram of the inverter. The parts in red rectangle are the power stage including MOSFETs and DC bus capacitor bank. Four MOSFET paralleled as a switch.

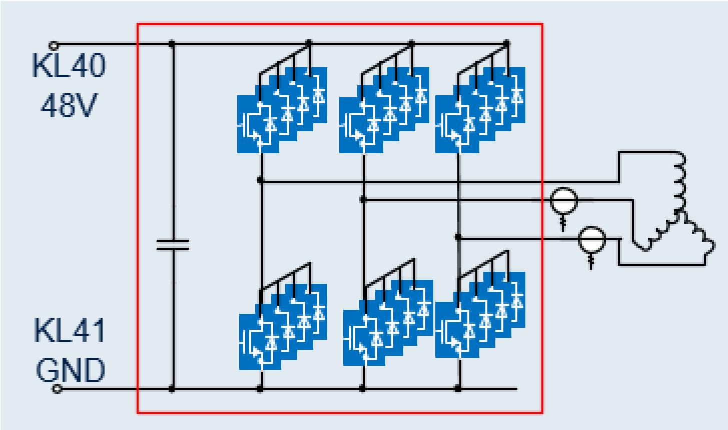


Figure 2 Block diagram of the inverter

2.2 System with heatsink

The power stage can be mounted on the rear of the target motor. For lab test, it should be mounted on a water or air cooling heatsink with thermal grease. Less than 5A can be handled in 5 minutes without heatsink. Thermal grease should be used between heatsink and the IMS board. There should be a groove on the heatsink for the capacitors terminal on the bottom of bus bar as show in Figure 3. The depth of the groove is 3mm. The Figure 4 shows the power stage with water cooling for lab test.

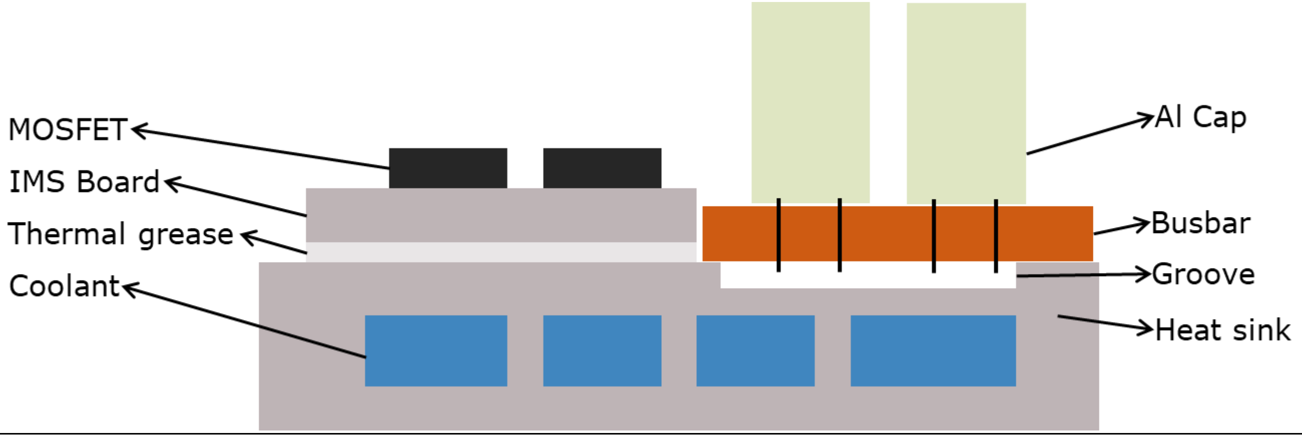


Figure 3 Assembly structure with the groove on the Heat sink

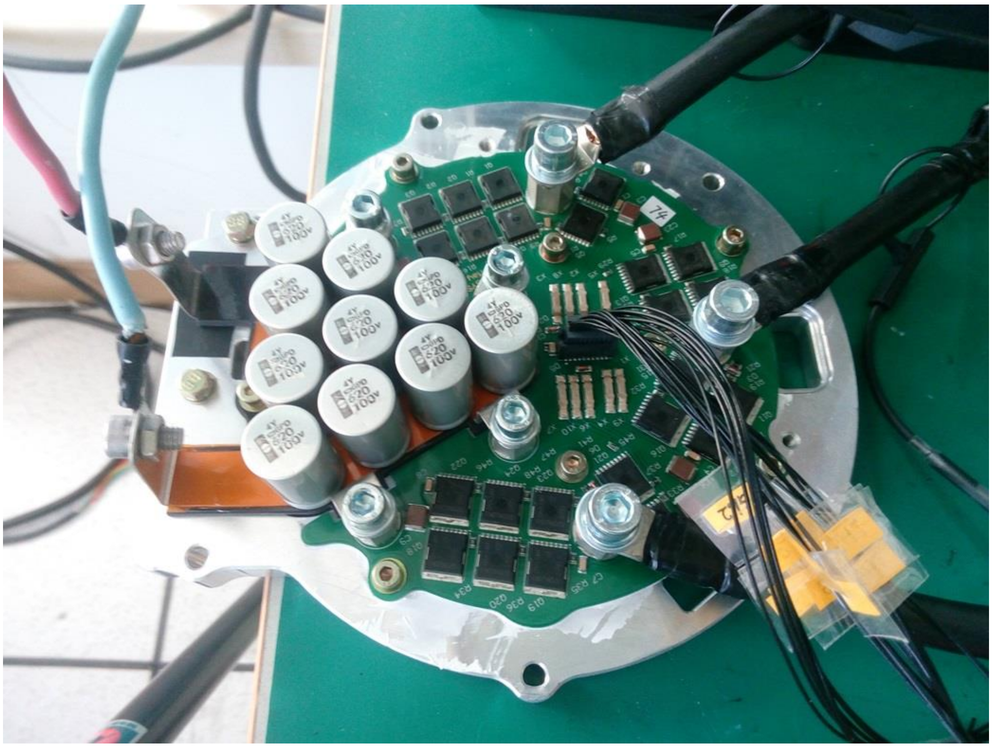


Figure 4 Power stage with water cooling heatsink for lab test

2.3 Connector

There is only one connector for all the gate driving signals. The part number of the connector is TFM110-22-S-D-P from Samtec. User needs Samtec SFSD-10-28-G as corresponding connector.

Table 1 and Figure 5 show the Pin Assignment of the connector.

Table 1 Connector description

Pin Number	**Name**	**Description**
1	T1	Terminal 1 of NTC
2	T2	Terminal 2 of NTC
3	P_GND	Ground for GL3
4	P_GND	Ground for GL1
5	GL3	Low side gate 3, voltage level 5~15V
6	GL1	Low side gate 1, voltage level 5~15V
7	SH3	High side source 3
8	SH1	High side source 1
9	GH3	High side gate 3, voltage level 5~15V
10	GH1	High side gate 1, voltage level 5~15V
11	NC	Not connected
12	NC	Not connected
13	P_GND	Ground
14	P_GND	Ground for GL2

Pin Number	**Name**	**Description**
15	GH2	High side gate 2, voltage level 5~15V
16	GL2	Low side gate 2, voltage level 5~15V
17	SH2	High side source 2
18	P_GND	Ground
19	NC	Not connected
20	NC	Not connected

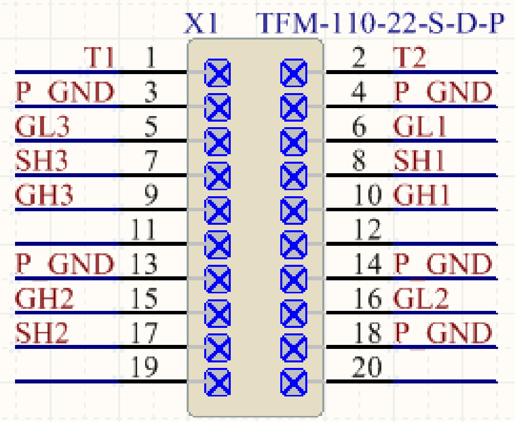


Figure 5 Pin Assignment of connector

Please check layout of connector in Figure 6 to make sure the correct connection.

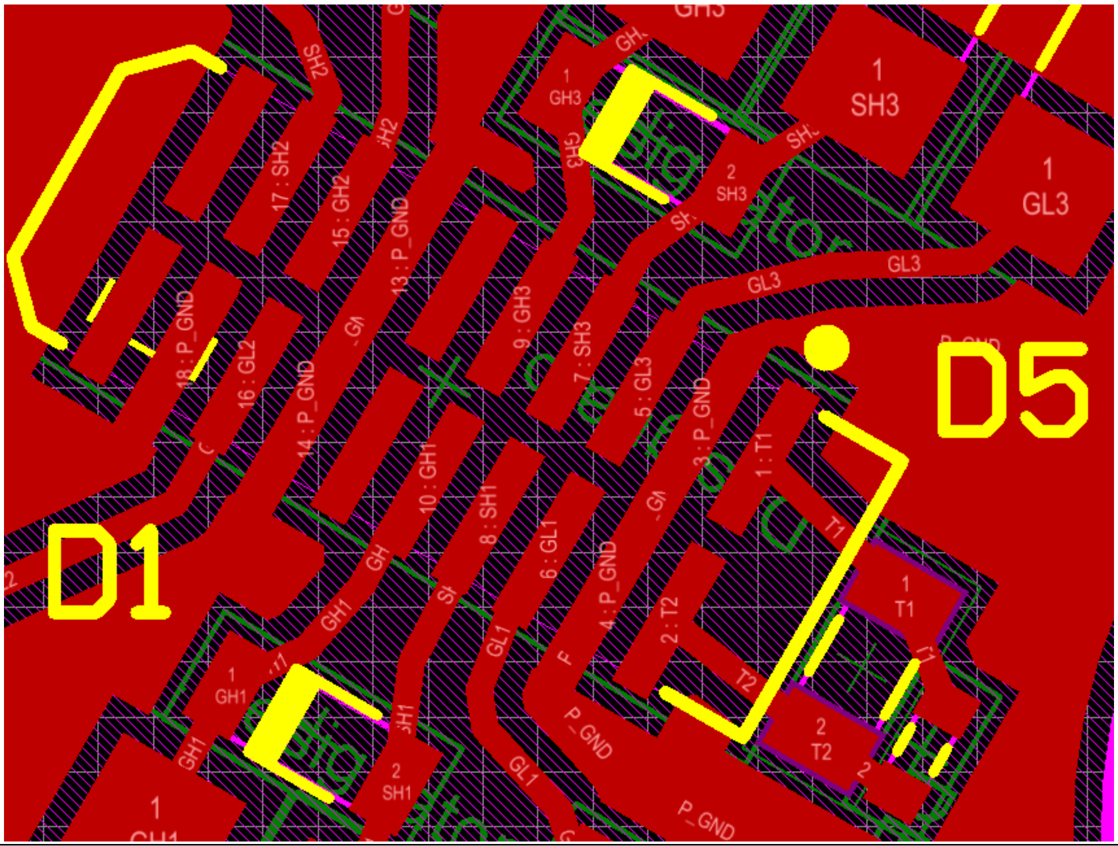


Figure 6 Layout of the Connector

2.4 Power Terminals

As shown in Figure 7, there are 5 power terminals. The DC+ and DC- connect to 48V power supply. The M8 screw U,V,W connect to the 3 phase motor.

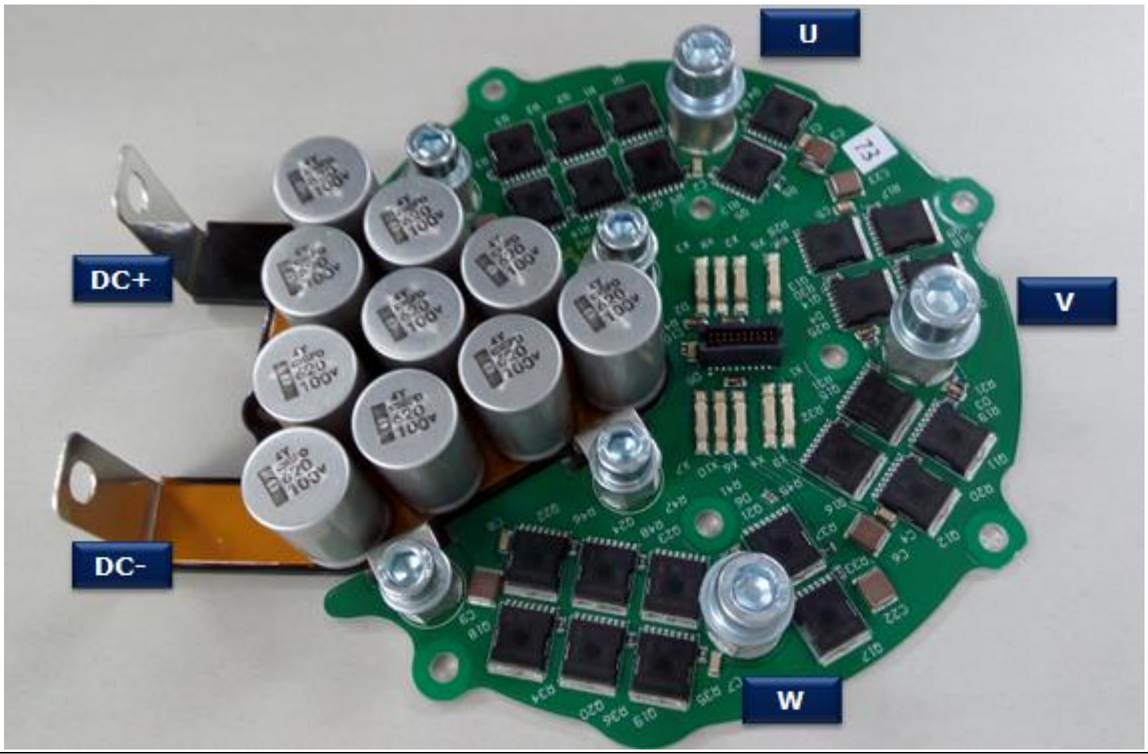


Figure 7 Power Terminals

3 Design Features

3.1 Inverter specification

The inverter specification describes the working condition of the power stage as shown in Table 2. This specification is not directly limited by the power stage. The power stage is designed for such inverter and motor system. The target motor is Permanent Magnet Synchronous Motor (PMSM). The most critical specification for power stage is the peak phase current.

Table 2

Name	**Min.**	**Typ.**	**Max.**	**Unit**	**Description**
VDC_motoring	36	48	52	V	Motoring mode DC bus voltage
VDC_generating	36	48	54	V	Generating mode DC bus voltage
Output Power_motoring		3.8		kW	Motoring mode output power at 48V
Output Power_generating		2.6		kW	Generating mode output power at 48V
Peak Power_motoring		11.3		kW	Motoring mode peak power at 48V 10 sec
Peak Power_generating		12.8		kW	Generating mode peak power at 48V 10 sec
Iout_con		160		Arms	Motoring mode continuous phase current
Iout_max1		400		Arms	Motoring mode peak phase current 10sec
Iout_max1		500		Arms	Motoring mode peak phase current 0.5sec
Igen_con		160		Arms	Generating mode continuous phase current
Igen_max		400		Arms	Generating mode peak phase current 10sec
Fsw	5	10		kHz	Switching frequency
Motoring frequency			1000	Hz	
Generating frequency			1000	Hz	
Coolant Temperature		65	95	°C	

3.2 Key components

3.2.1 Bus bar and capacitors

Ten aluminum capacitors soldered on the bus bar as shown in Figure 8. The part number of the capacitor is EGPD101ELL621MM30H from Chemi-Con. Table 3 shows the key features of the capacitor. Additionally if the max BEMF of the motor is lower than 80V, the 80V 820uF capacitor is a better choice. The part number is EGVD800ELL821MM30H. It has higher vibration resistance by GPD series (acceleration 392m/s2, 40G).

Table 3 Key feature of ALUMINUM ELECTROLYTIC CAPACITORS

	Rated ripple current	**Temperature Range**	**DC Voltage**	**Capacitance**
EGPD101ELL621MM30H	3.92A	-40°C to 135°C	100V	620uF
EGVD800ELL821MM30H	3.93A	-40°C to 135°C	80V	820uF

The DC+_A and DC-_A terminals connect to the power supply. The DC+_B and DC-_B connect to the power board with M6 screw as shown in Figure 8.

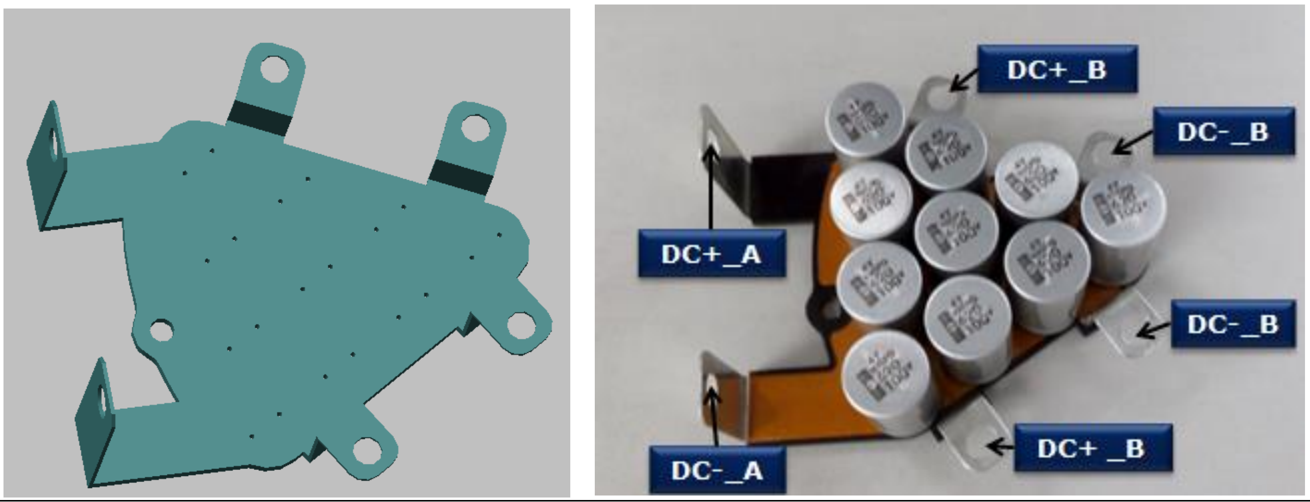


Figure 8 **Bus bar and capacitors overview**

3.2.2 Power Board

There are four M6 screws and three M8 screws on the power board as shown in Figure 9. M6 screws in left connect to the capacitor bank. M8 screws connect to the phase of the motor.

The Insulated Metal Substrate (IMS) material is used. The detail of IMS board is shown in Table 4.

The thickness of the copper is 3oz (0.105mm), it helps to handle 400A~500Arms while the width of copper plane is around 10mm.

The thickness of the Aluminum substrate is 2mm which handle the dynamic thermal behavior, for example start the engine in 300ms with 500Arms output current.

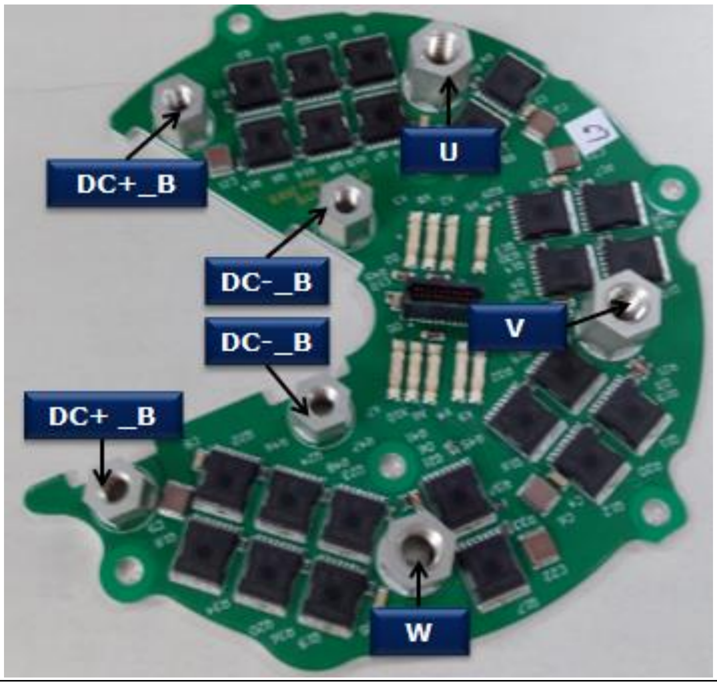


Figure 9 **Power board overview**

Table 4 IMS board material

Items	**Features**
Board type	Thermal Clad HT04503
Copper thickness	3oz (105um)
Aluminum carrier thickness	2mm
Insulator layer thickness	76um

3.2.3 TOLL & TOLG MOSFET

The TO-Leadless (TOLL) is a molded package optimized for high power high reliability applications. Its small mechanical dimensions allow really compact designs and the high current capability combined with the low Thermal Resistance (R_{thJC}), resulting in lower chip temperatures enables the designer to go for higher power density and higher reliability.

Furthermore, Infineon investigated a derivate of the TOLL to improve thermal cycling on board (TCoB) performance on Al-core IMS board. It is called TO-Leaded with Gullwing geometry (TOLG). The footprint of TOLG could be compatible with TOLL.

Compared to the commonly used D2PAK or D2PAK 7Pin the TOLL & TOLG has a smaller footprint. The size of TOLL and TOLG are 11.7mm * 9.9mm * 2.3mm and 11.7mm * 9.75mm * 2.3mm comparing to the 15.0mm * 10.0mm * 4.4mm of the D2PAK (7Pin) as shown in Figure 10. This leads to a 30% smaller footprint and a 60% smaller space.

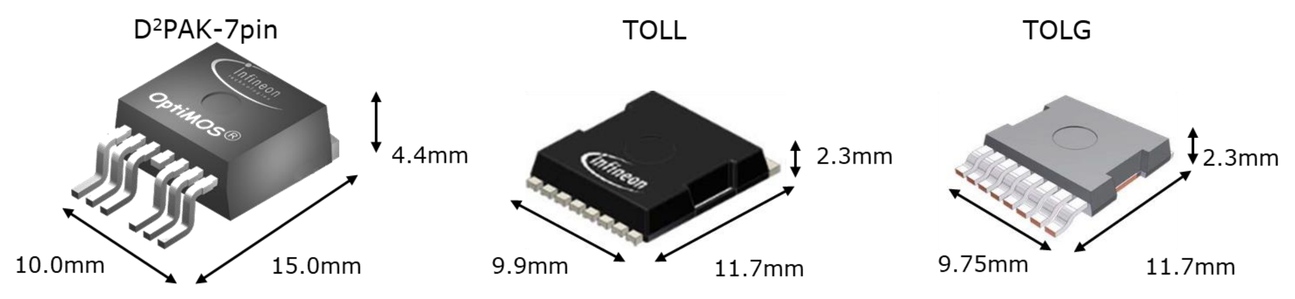


Figure 10 Space reduction of TOLL & TOLG compared to D2PAK 7Pin

Figure 11 shows the calculated typical $Z_{th\text{-}JC}$ of junction to case of D2PAK, TOLL and TOLG package. The 0.1K/W reduction of thermal resistance makes no sense to a normal board level thermal system, as the total R_{thJA} from junction to ambient could be about 40K/W. But it’s worth to use the reduction in a well cooling system. For example, the IMS board with water cooling system has very low total R_{thCA} from junction to coolant like 2K/W.

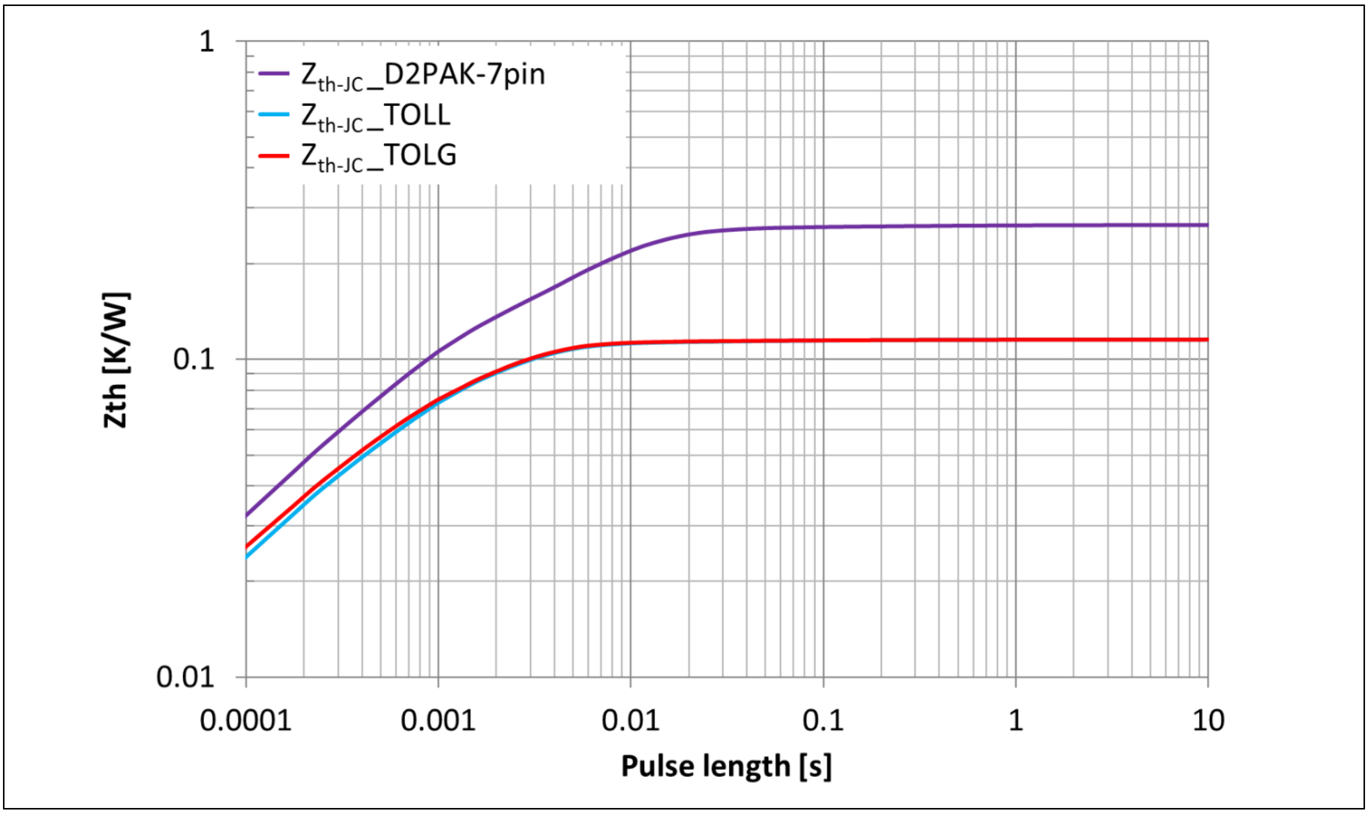


Figure 11 ZthJC (calculated) of D2PAK 7Pin, TOLL and TOLG

AEC-Q101 qualified TOLL & TOLG MOSFETs are available for automotive application as shown in Table 5.

Table 5 Key feature of TOLL & TOLG MOSFET

Part NO. of TOLL	Part NO. of TOLG	V_{DS}	$R_{DSon,max}$	$I_{D,nom}$	**Operating Temp.**
IAUT165N08S5N029	IAUS165N08S5N029	80V	2.9mohm	165A	-55°C~175°C
IAUT200N08S5N023		80V	2.3mohm	200A	-55°C~175°C
IAUT240N08S5N019	IAUS240N08S5N019	80V	1.9mohm	240A	-55°C~175°C
IAUT300N08S5N014		80V	1.4mohm	300A	-55°C~175°C
IAUT300N08S5N012	IAUS300N08S5N012	80V	1.2mohm	300A	-55°C~175°C
IAUT165N10S5N035		100V	3.5mohm	165A	-55°C~175°C
IAUT300N10S5N015		100V	1.5mohm	300A	-55°C~175°C

4 Function description and design implementation

4.1 Power loss Calculation

The power loss calculation in Ref. [2] is used for thermal estimation. There are four MOSFETs in paralleled as a switch. Assuming the current of MOSFET is well balanced. The formulas are using for the power loss calculation of the MOSFET.

The total power losses are divided as MOSFET power loss (P_M) and Diode power loss (P_D). P_M is divided as conduction loss (P_{CM}) and switching loss (P_{SWM}). P_D is divided as conduction loss (P_{CD}) and switching loss (P_{SWD}) as well.

$$P_M = P_{CM} + P_{swM} = R_{DSon} \cdot I_{Drms}^2 + (E_{onM} + E_{offM}) \cdot f_{sw}$$

$$P_D = P_{CD} + P_{swD} = u_{D0} \cdot I_{Fav} + R_D \cdot I_{Frms}^2 + E_{onD} \cdot f_{sw}$$

The conduction loss could be calculated using an MOSFET-approximation with the drain-source on-state resistance (R_{DSon}). The conduction losses of the body diode can be estimated using a diode approximation with a series connection of DC voltage source (u_{D0}) representing diode on-state zero-current voltage and a diode on-state resistance (R_D).

$$P_{CM} = R_{DSon} \cdot I_{Drms}^2 = R_{DSon} \cdot I_o^2 \cdot (\frac{1}{8} + \frac{m_a \cdot \cos\phi}{3\pi})$$

$$P_{CD} = u_{D0} \cdot I_{Fav} + R_D \cdot I_{Frms}^2 = u_{D0} \cdot I_o \cdot \left(\frac{1}{2\pi} - \frac{m_a \cdot \cos\phi}{8}\right) + R_D \cdot I_o^2 \cdot (\frac{1}{8} - \frac{m_a \cdot \cos\phi}{3\pi})$$

The switching power loss could be calculated from the switching energy and switching frequency (f_{sw}). The switching energy could be calculated from parameters in the Datasheet refer to Ref. [1].

$$E_{onM} = E_{onMi} + E_{onMrr} = U_{DD} \cdot I_{Doff} \cdot \frac{tri + tfu}{2} + Q_{rr} \cdot U_{DD}$$

$$E_{offM} = U_{DD} \cdot I_{Doff} \cdot \frac{tru + tfi}{2}$$

$$E_{onD} \approx E_{onDrr} = \frac{1}{4} \cdot Q_{rr} \cdot U_{DD}$$

The input values are shown in Table 6. The value of R1 and R2 are explained in Chapter 4.3.

Table 6 **Input parameters**

Parameters	**Value**	**Unit**
fsw	10000	hz
Iload	40, 100, 125	Arms
VDS	48	V
m	0.85	
phi	0.555	rad
V_plateau	4.3	V
Vdr	12	V
Vth	2	V
Rhi	0.03	ohm
Rg	0	ohm
Rg_internal	1.9	ohm
Ciss	11200	pF
Crss	69	pF
rdson	0.0033	ohm
rfdiode	0.003535	ohm
Vfo	0.4	V
Qrr	232	nC
Cgd1	70	pF
Cgd2	1100	pF
tri0	58	ns
tfi0	18	ns
R1	5.1	ohm
R2	15	ohm
Vf_D1	0.3	V

The results of power loss are shown in Table 7. 5.38W was used for steady state thermal simulation. The power loss of 23.3W in 10 seconds and 34.3W in 0.5 second could be used in dynamic thermal simulation.

Table 7 **Power loss calculation result**

Phase Current	**Current of each MOSFET**	**Power loss of each MOSFET with body diode**
160Arms	40Arms	5.38W
400Arms	100Arms	23.3W
500Arms	125Arms	34.3W

4.2 Thermal Estimation

4.2.1 Cooling structure

Figure 12 shows the cooling structure of power stage. Please refer Figure 12 as an example. The MOSFETs were soldered on the IMS board. The IMS board has copper layer, dielectric layer and aluminum layer. The IMS board was mounted on a water cooling heatsink with thermal grease.

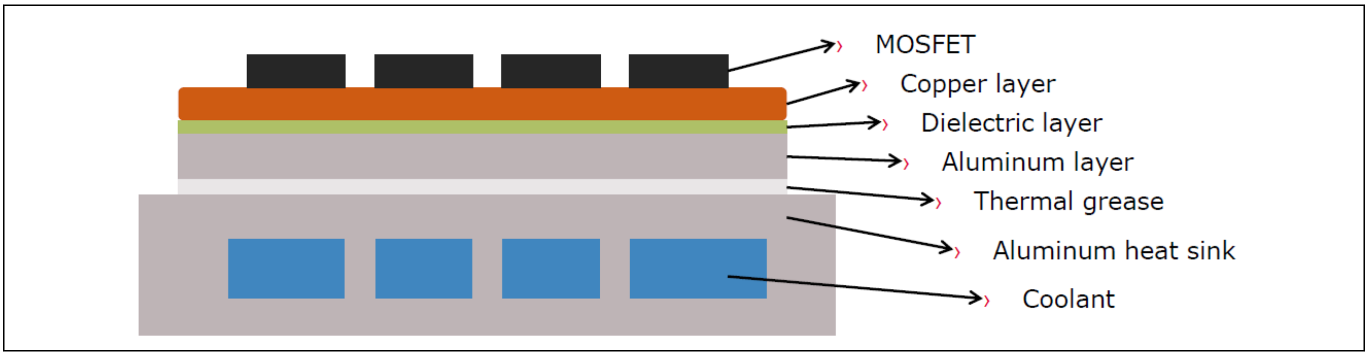


Figure 12 **Cooling structure of power stage**

4.2.2 Temperature rise estimation

During design phase the temperature rise of steady state could be estimated from power loss multiplying thermal resistance.

$$\Delta T_j = P \times R_{th\_JA}$$

The thermal resistance junction to case is 0.4K/W. The thermal resistance of IMS board is 0.45K/W. The thermal resistance of thermal grease could be estimated as 1K/W. The total thermal resistance is estimated as 2K/W.

The temperature rise of steady state could be estimated as

ΔTj = 5.38W * 2K/W = 10.76°C

4.2.3 Thermal simulation

Figure 13 shows the thermal simulation with ideal environment.

Ambient temperature is 45°C. The thickness of thermal grease is TP-1500 with 0.25mm thickness and 10psi pressure. Power loss of MOSFET is 5.38W. MOSFETs are placed on the IMS board with an ideal heatsink and cooling by water at 65°C. The simulation result of temperature plane in top layer give draft understanding of thermal distribution and thermal coupling of the design.

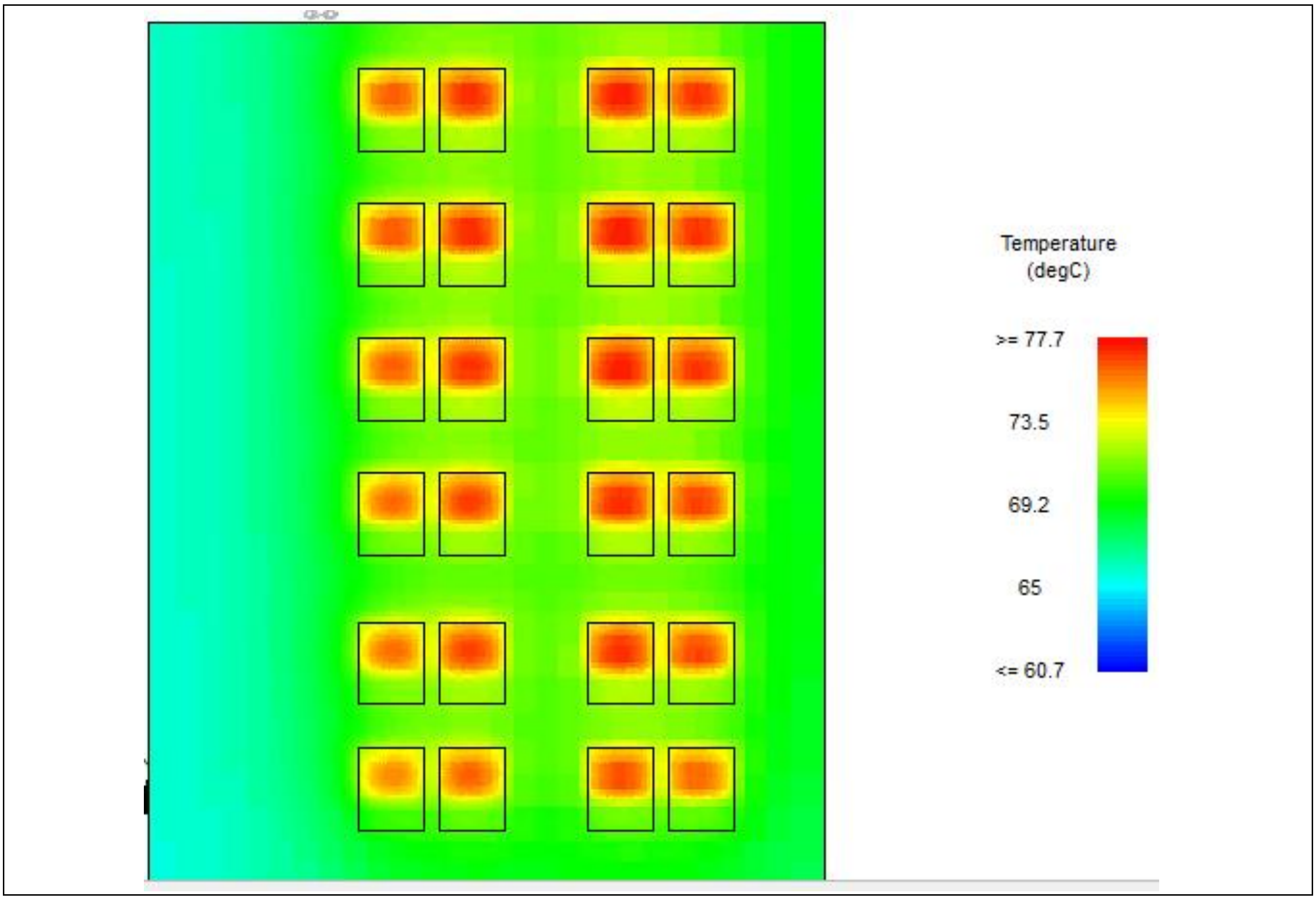


Figure 13 Thermal Estimation of MOSFET on IMS board

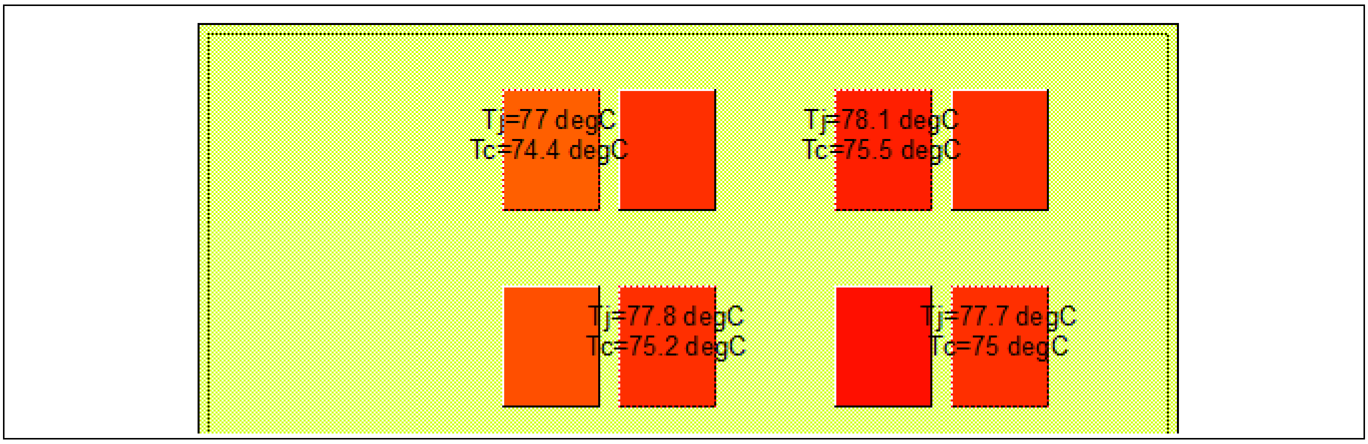


Figure 14 Temperature difference between junction and case

Chapter 4.1 shows the power loss of MOSFET in three conditions. It is acceptable that the temperature rise of junction at 160Arms would be around 10 degrees from simulation and estimation.

Furthermore it is shown in Figure 14 that the temperature difference between junction and case of MOSFET was about 2.6°C. The main part of power loss sink through bottom side to the water cooling heatsink. The case temperature could be easily measured by a thermal camera. The junction temperature could be calculated with the simulation result.

The temperature rise of junction at 400Arms and 500Arms is a dynamic value in this application. The 500Arms phase current is additional requirement as cold start mode in BSG. These data are measured on test bench and verified in Chapter 5.3. Further simulation shows that the dynamic temperature difference between junction and case of MOSFET could be 20°C. It is necessary to consider the margin at dynamic state.

4.2.4 Copper based IMS board thermal consideration

Due to different thermal expansion coefficients (CTE) between FR4 and Al, Al-based IMS substrate (CTE~25.5 ppm/K) is much stiffer than usual FR4 boards (CTE~14-16 ppm/K). Therefore, there is much more strain on the soldering material between pins and IMS Substrate. More detail was described in Ref. [3].

On Al-IMS, as compared to the FR4, lifetime of solder material is significantly lower for TOLL packages. This phenomenon is independent on the MOSFET or IMS provider. Packages with gullwing-type leads still achieve high lifetime.

Another possible workaround is usage of Cu-based IMS (CTE~17 ppm/K) which has same results as FR4. Copper has better performance in thermal perspective. Table 8 shows the comparison between the copper and aluminum.

Table 8 Comparison between copper and aluminum

	Copper	Aluminum
Thermal conductivity	401 W/(mK)	237 W/(mK)
Specific heat capacity	0.385 J/(g °C)	0.902 J/(g °C)
Density	8.96 g/cm^3	2.70 g/cm^3
Heat capacity in same volume	3.45 J / (cm^3 °C)	2.44 J / (cm^3 °C)

The copper has 70% better thermal conductivity than aluminum. That means the thermal resistance of the metal layer will be 70% better when copper was used. Notice that the Rth of the metal layer is not the main part of the Rth between junction and coolant.

The steady state simulation result with copper based IMS board was shown in Figure 15. It shows that the temperature rise will be 5% lower than aluminum based IMS in Figure 14.

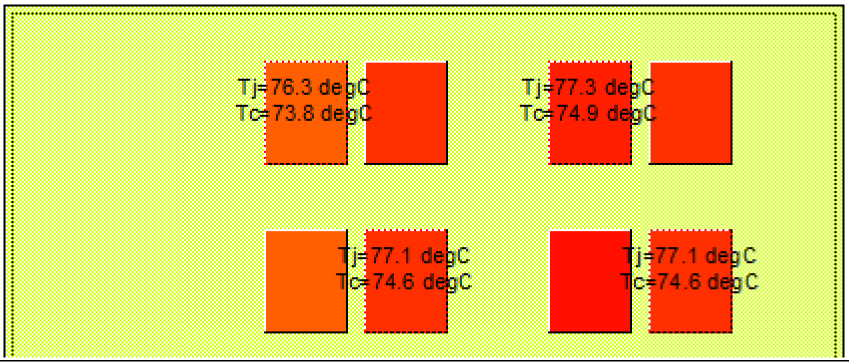


Figure 15 Temperature of junction and case on copper based IMS board

The copper has 40% more thermal storage capacity than aluminum. If the 2mm aluminum layer is replaced by 1.6mm thickness copper, the thermal storage capacity of copper will be 13% better than aluminum. This helps the dynamic thermal performance of the MOSFET. Furthermore the steady state 1.6mm Cu based thermal performance was simulated. The three scenarios are compared in Figure 16.

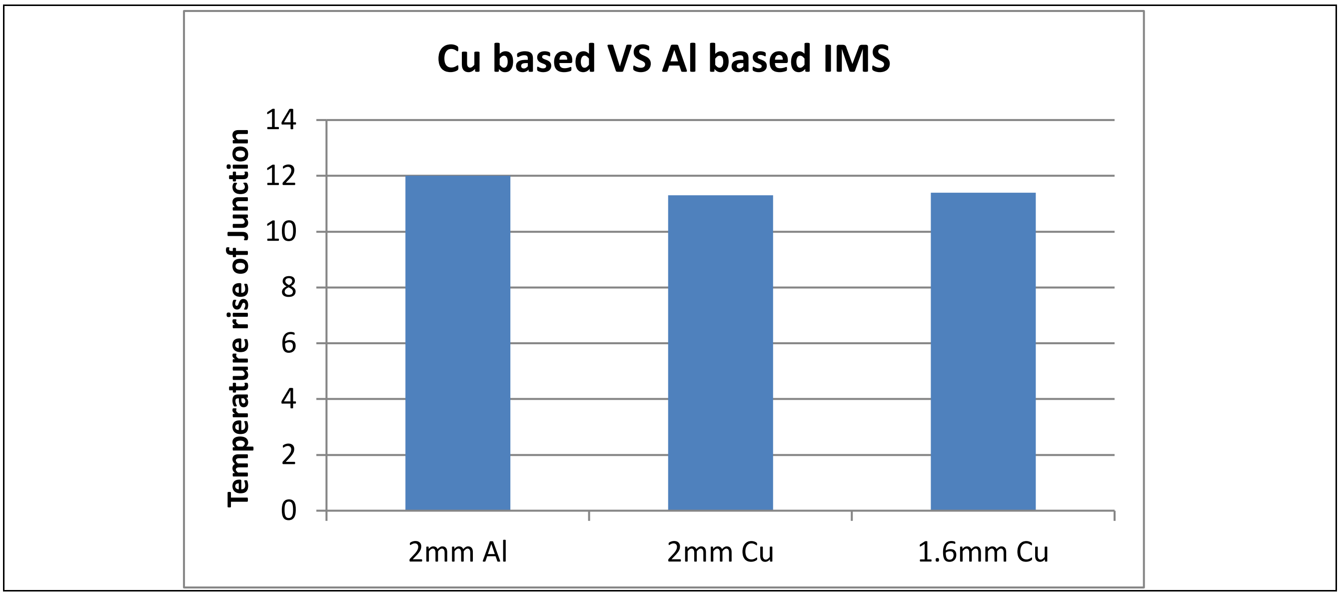


Figure 16 Comparison of junction temperature rise

The solution with 1.6mm copper layer will be slightly better than 2mm aluminum. The reliability of thermal shock is the main motivation to do this analysis.

4.2.5 TOLG MOSFET for Al based IMS board

The TOLG package MOSFET is recommended for all users who intend to use Al-based IMS board. The performance of new package TOLG is much better than TOLL on the AL based IMS board under same condition, although the TOLL fulfills the standard TCoB requirements as shown in Figure 17 . The reason for better performance is the flexibility of the gullwing leads.

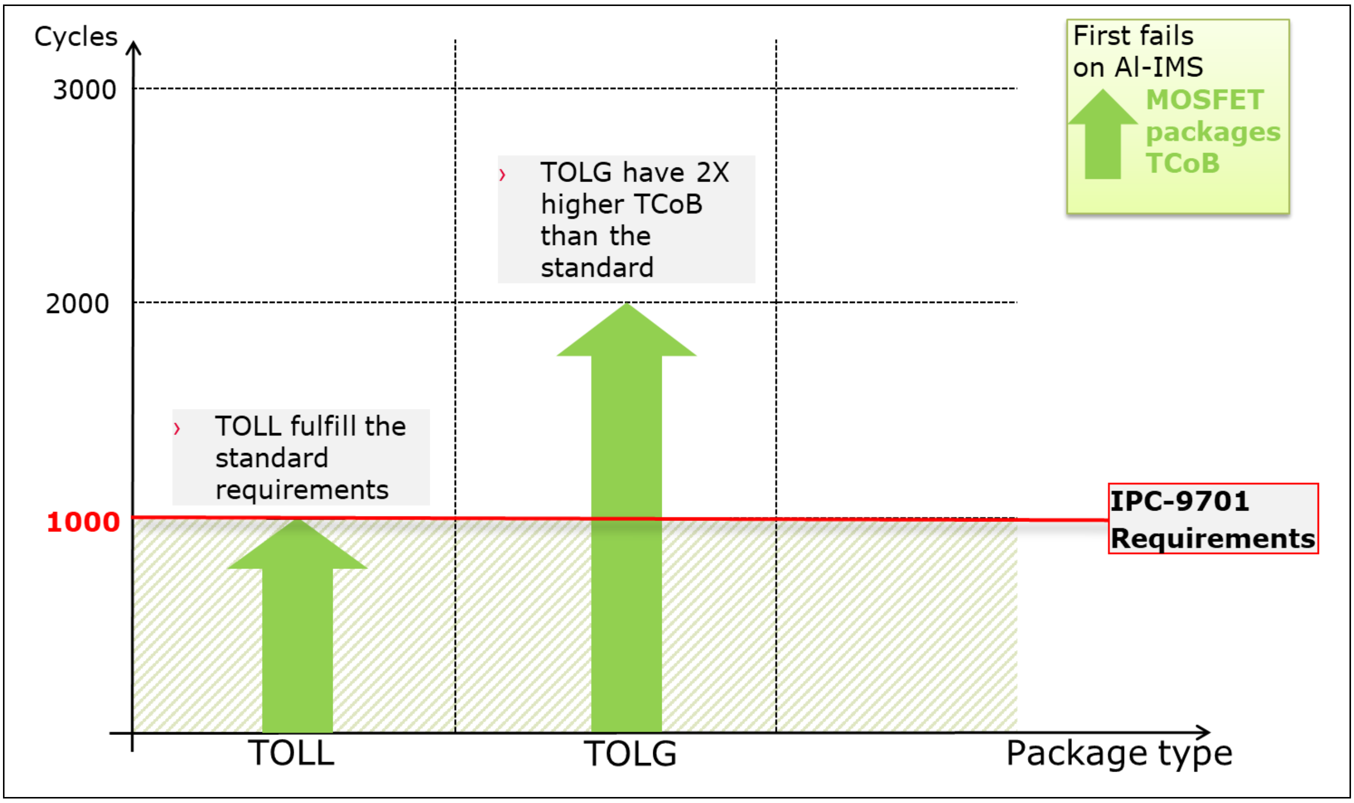


Figure 17 Comparison of TOLL and TOLG under TCoB test

4.3 Driver IC and circuit analysis

Driver IC consideration: The MOSFET has very low resistance but the gate charge is high. Four MOSFET in parallel has maximum 828nC gate charge totally. It’s better to design a 10mA charge pump circuit for high side switch. The bootstrap circuit could be not enough for high side power supply.

If the switching on and switching off circuit needs to be optimized separately on trade off on EMI and thermal perspective, the circuit in Figure 18 is proposed. The R1 and R2 are mentioned in the Table 6 for power loss calculation. R1 and Schottky diode D1 are on the driver board and R2 are on the IMS board as separate gate resistors. D1 help to switch off faster as clamping diode.

The comparison between using and not using the D1 and R1 is shown in Table 9. It shows that the peak current of gate is reduced and the switching off voltage threshold is lower with the same power loss.

Table 9

	Without R1 and D1	**With R1 and D1**
Ig_on max	1.82A	0.82A
Ig_off max	1.01A	0.95A
Voff threshold	3.92V	3.85V
Power loss per MOS @500A	57.9W	57.5W

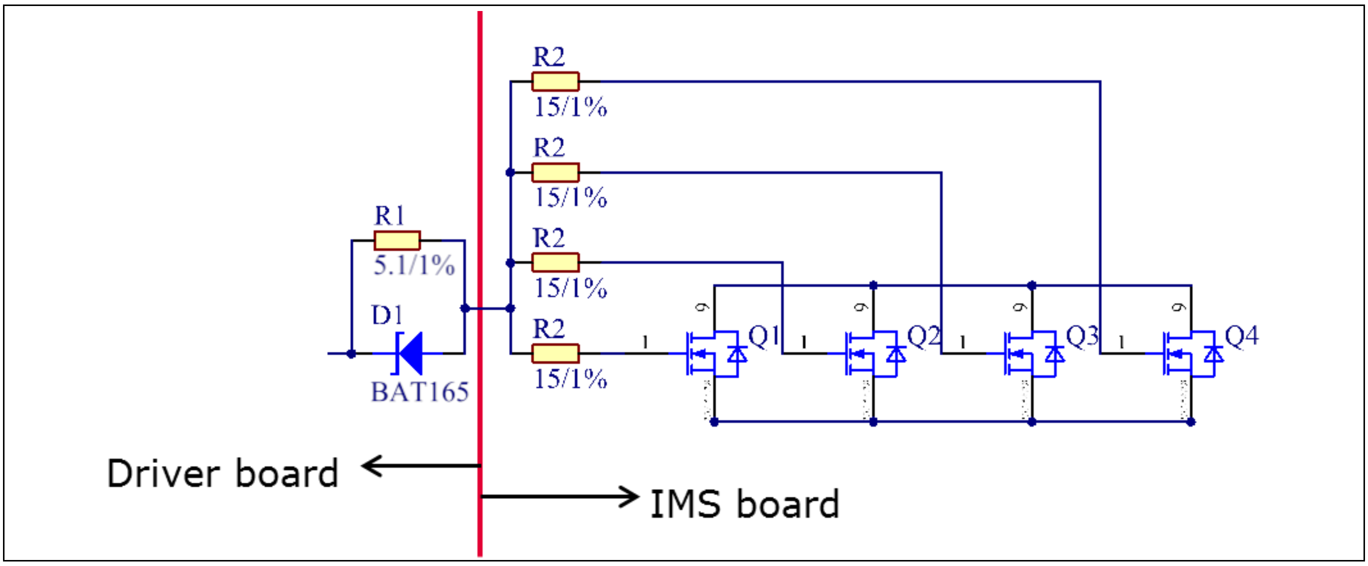


Figure 18 Driver circuit of paralleling MOSFET

4.4 Schematic

The schematic of the IMS board are shown in Figure 19 to Figure 22.

Each MOSFET has separated gate resistor (e.g. R1~R4). Four MOSFET in parallel has a common pull down resister (e.g. R5) and common Zener (e.g. D1). The jumpers (e.g. X2) make the layout to be possible on a single copper layer. The 100nF capacitors parallel with the MOSFET as a snubber circuit (e.g. C1, C2). R49 is a NTC resister for temperature measurement. C3, C6, C9, C21, C22, C23 are 4.7uF 100V MLCC which close to each half bridge.

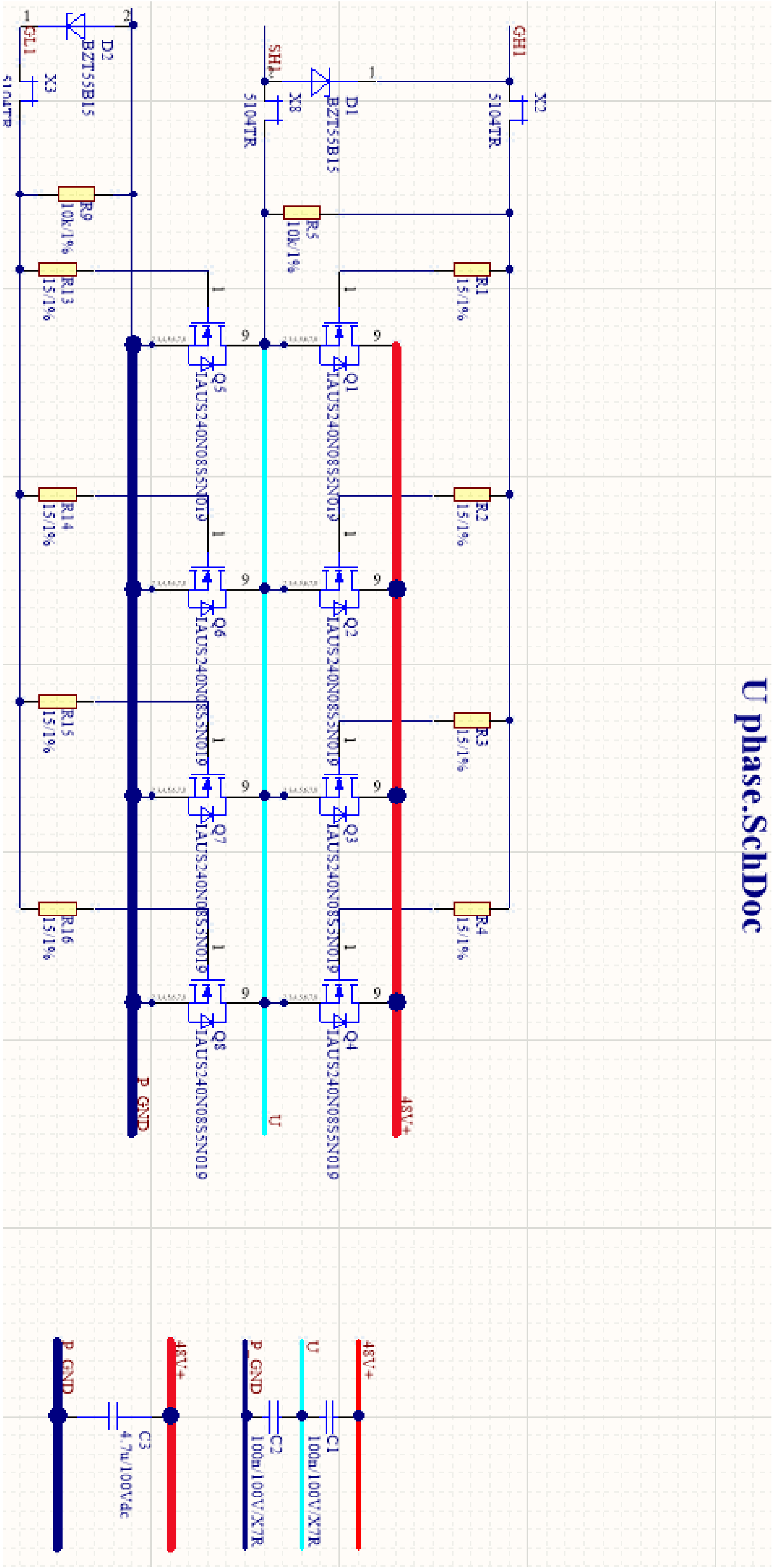


Figure 19 Schematic U phase

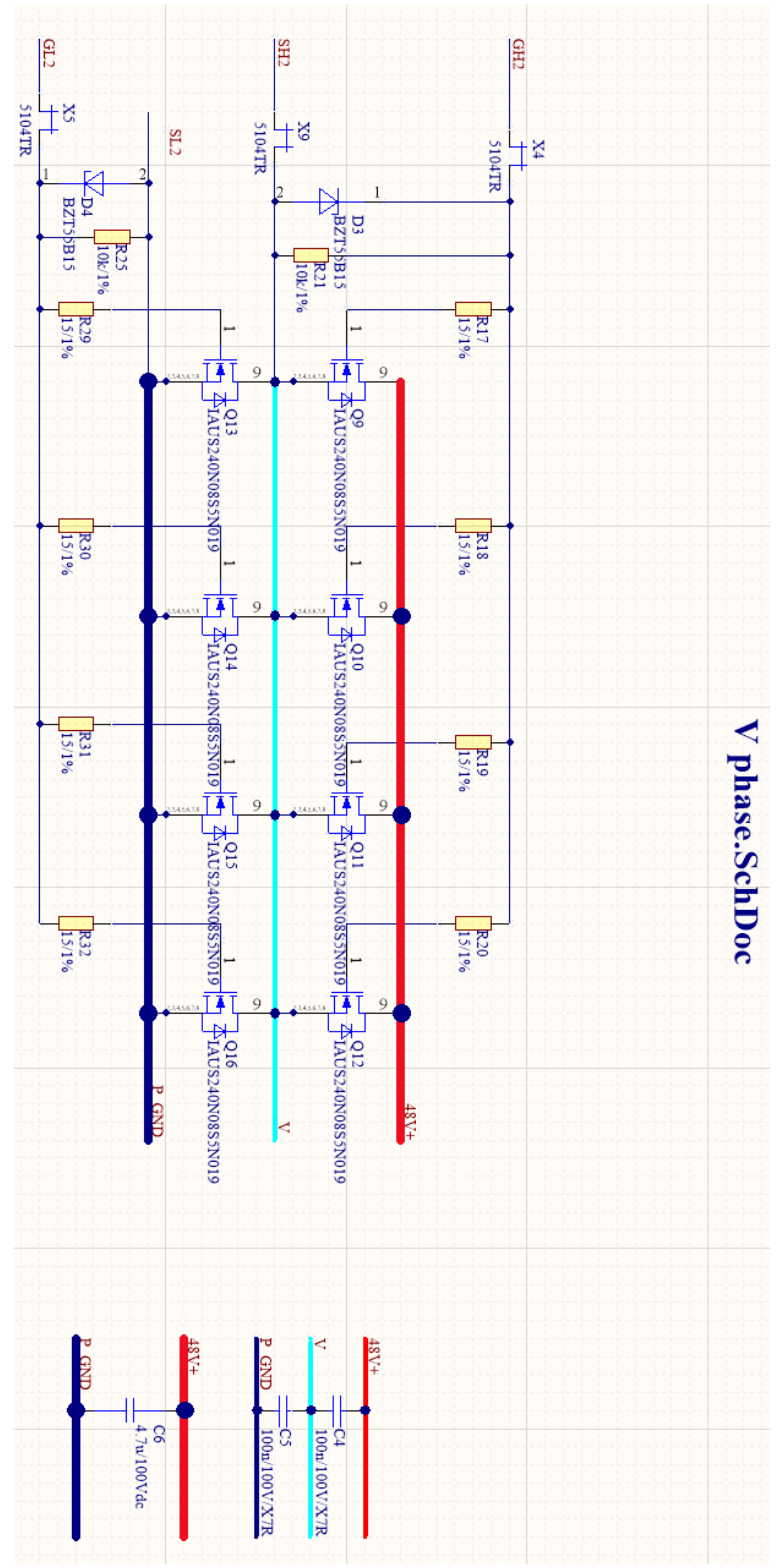


Figure 20 Schematic V phase

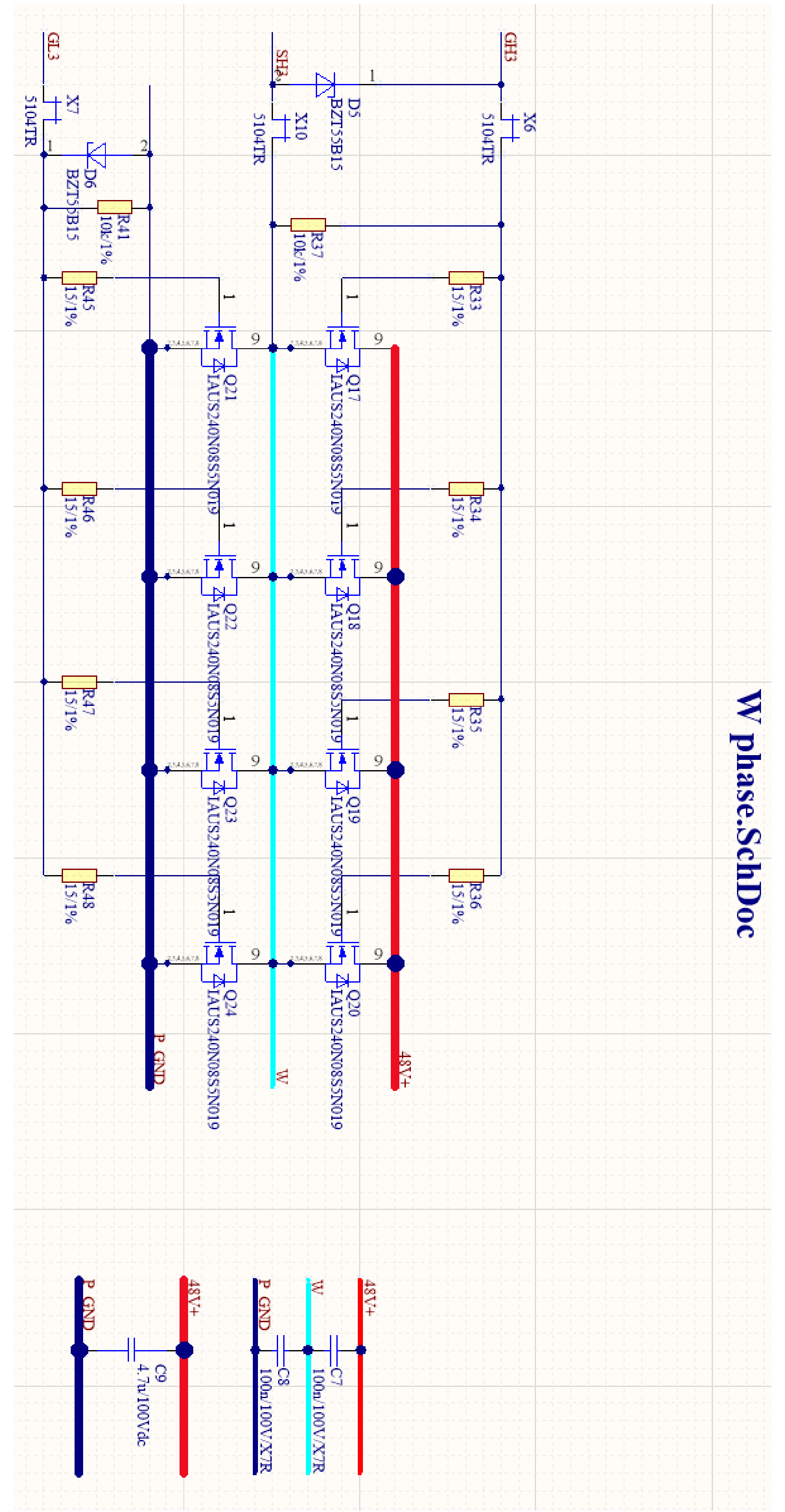


Figure 21 Schematic W phase

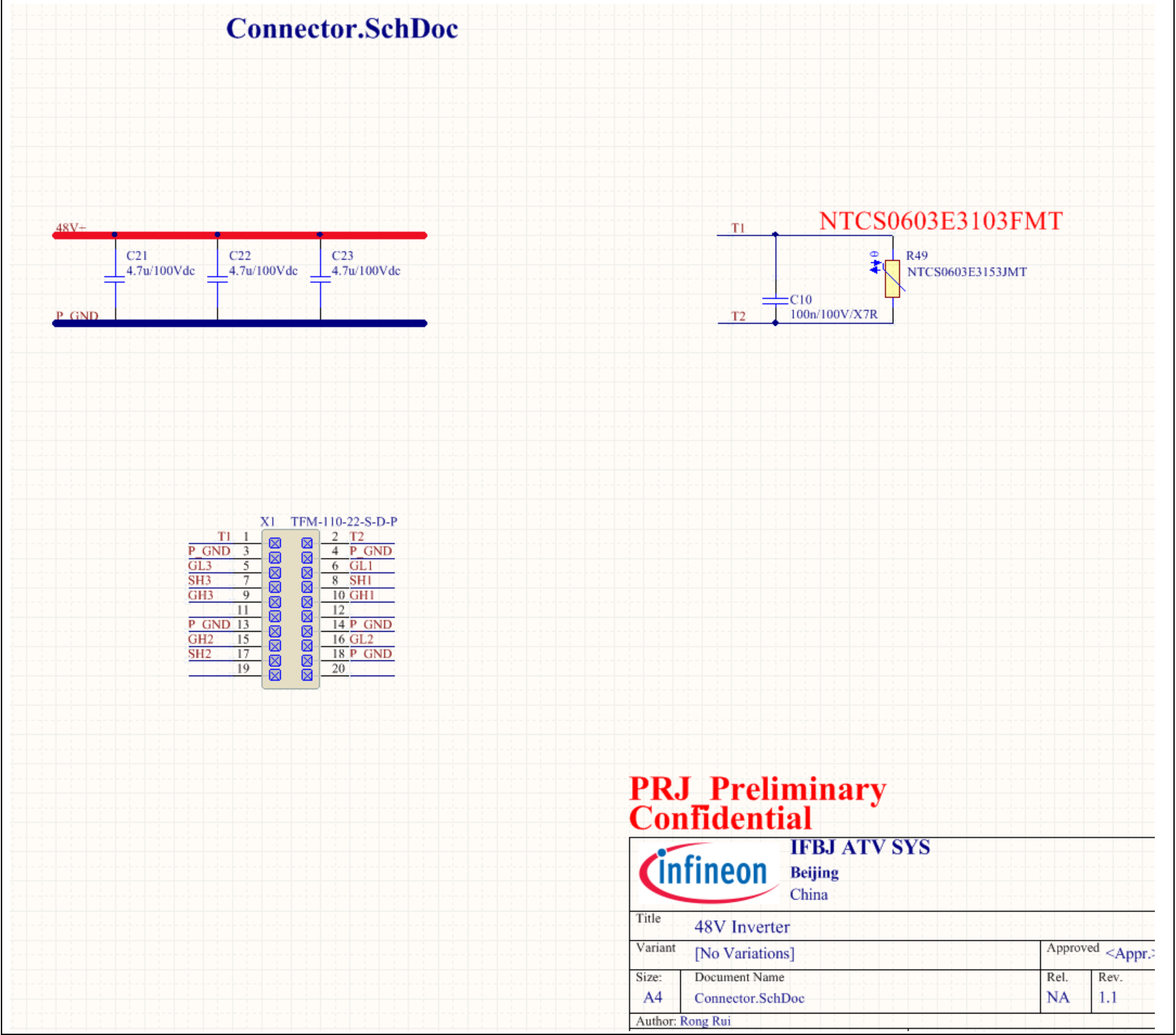


Figure 22 **Schematic Connector, NTC resistor and snubber**

4.5 Mechanical boundary

The power stage should be mounted at the end of the motor, so that there is mechanical boundary of the design. The diameter of the motor is 170mm. There should be place for current sensor and power terminal connecting. The diameter of power stage is defined as 145mm and the height is less than 40mm.

Furthermore, the space above the power stage would be occupied by control board with microcontroller and driver circuit. The components placement should take account of the control board.

4.6 Stray inductance consideration

When the MOSFET switch off with high current, the V_{DS} spike should be analyzed to avoid avalanche of MOSFET.

The switching-off voltage spike is determined by the stray inductance of the system and the change rate of turn-off current, which is calculated according to the following formula:

Vs=Ls * di/dt

Ls indicates stray inductance of the system, di/dt indicates the change rate of current. Figure 23 shows the overshoot of V_{DS} waveform.

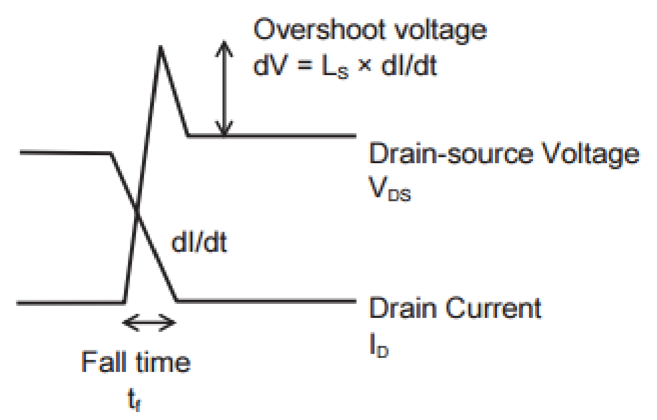


Figure 23 V_{DS} overshoot cause by stray inductance and switching off speed

The laminated busbar was used to minimize the stray inductance of the busbar.

The stray inductance of the PCB layout should be calculated as a microstrip line as shown in Figure 24.

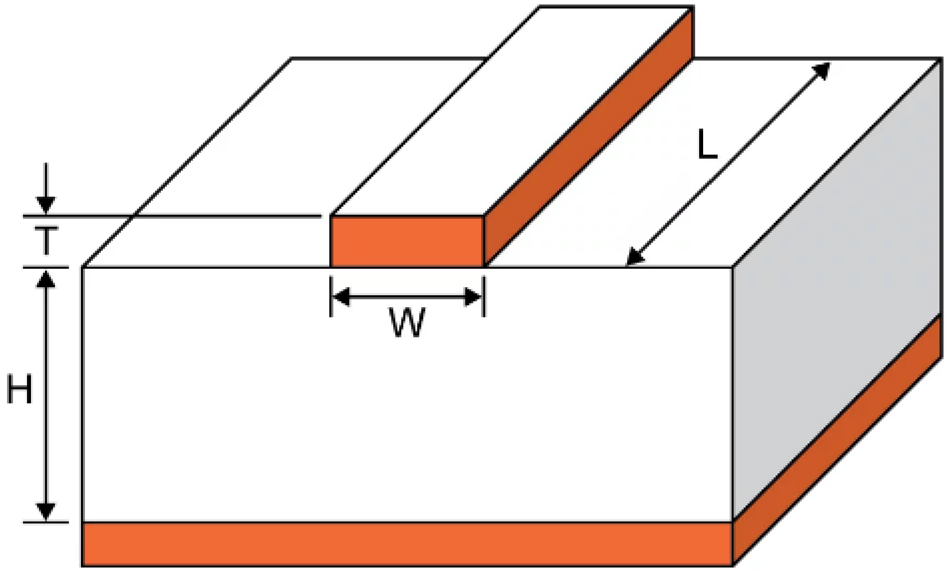


Figure 24 Microstrip line structure

The inductance of microstrip line could be calculated as following equation:

$$L_{microstrip} = 2 \times L \times [\ln\left(\frac{2L}{W+H}\right) + 0.5 + 0.2235 \times \frac{(W+H)}{L}]$$

Lmicrostrip means inductance of the microstrip line in nH

W means width of the microstrip line in cm

L means length of the microstrip line in cm

H means distance between the microstrip line and ground in cm

If the width is 1cm and the length is 10cm, the inductance is about 70nH. The inductance with different length and width are shown in Figure 25 and Figure 26. The length of the trace should be as short as possible, but the width is not critical especially when the width is wider than 10mm.

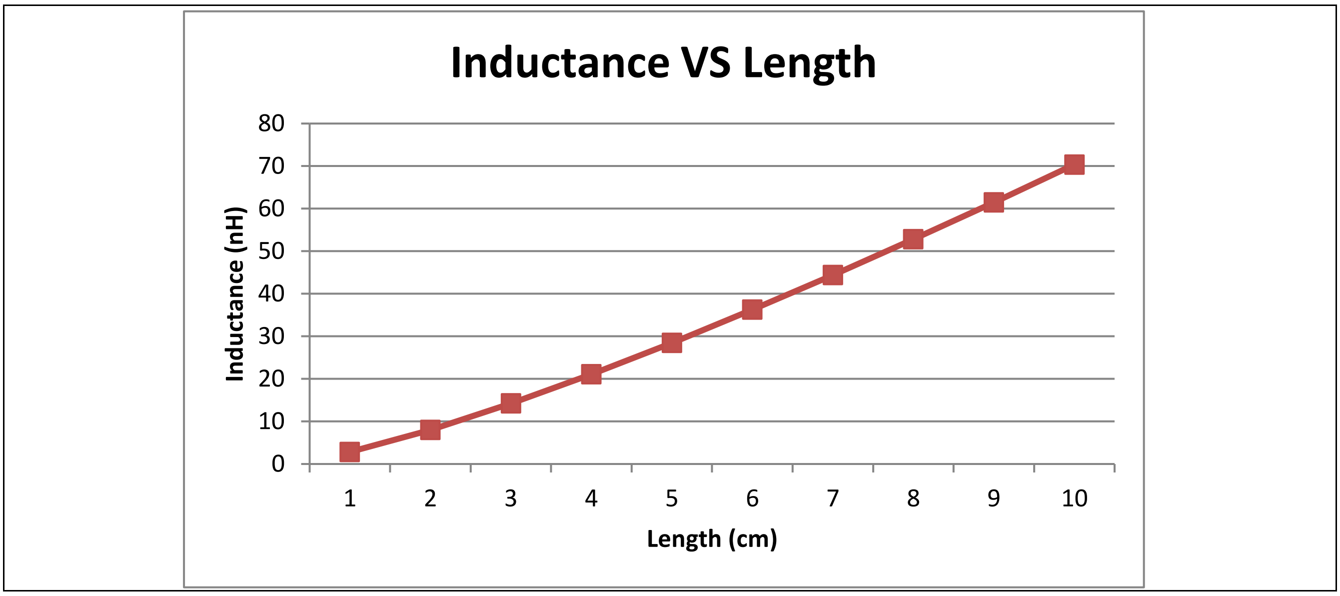


Figure 25 Microstrip line inductance VS Length. The width is fixed at 10mm.

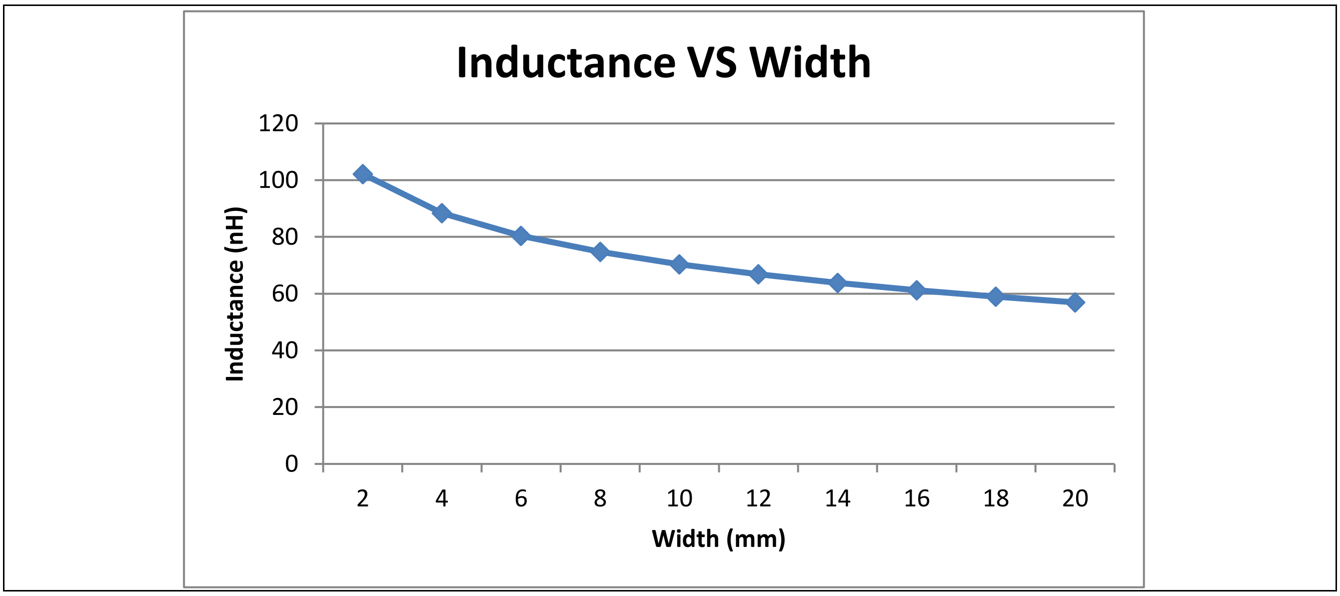


Figure 26 Microstrip line inductance VS Width. The length is fixed at 5cm.

4.7 Components Arrangement and Layout

Figure 27 shows the components arrangement of the IMS board.

Each MOSFET has its own gate resistor. The gate resistor is left side of the MOSFET and close to gate pin. The distance between each paralleled MOSFET is about 2mm which help to decouple the thermal effect. The MOSFET are around the phase output terminal so that the current and the thermal are well distributed.

The connector in the middle connects to six gate and source signals with jumpers.

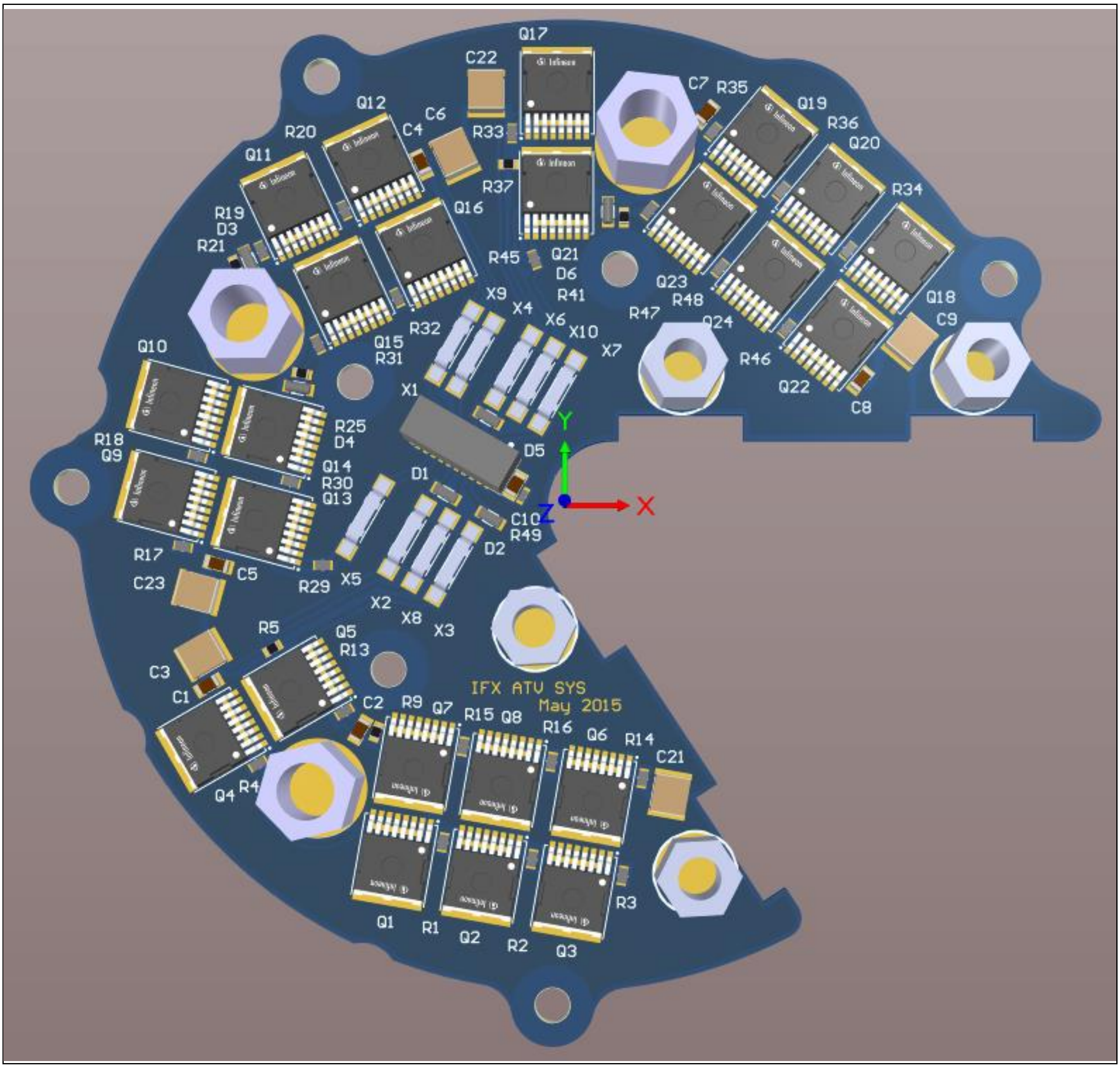


Figure 27 Components arrangement

Figure 28 shows the layout of copper layer on the IMS board. Copper plane of DC+ is placed in the form of circle; it connects the bus bar at the end, and connects drain of 12 high-side MOSFETs. The copper plane of each phase is placed in the middle of the circle as shown in Figure 28. The copper plane of DC- is placed in the center of the circle. Notice that the NTC resister for temperature measurement cannot measure the package temperature or junction temperature as it is far away from the MOSFET. It shows the board temperature which is related to the coolant temperature.

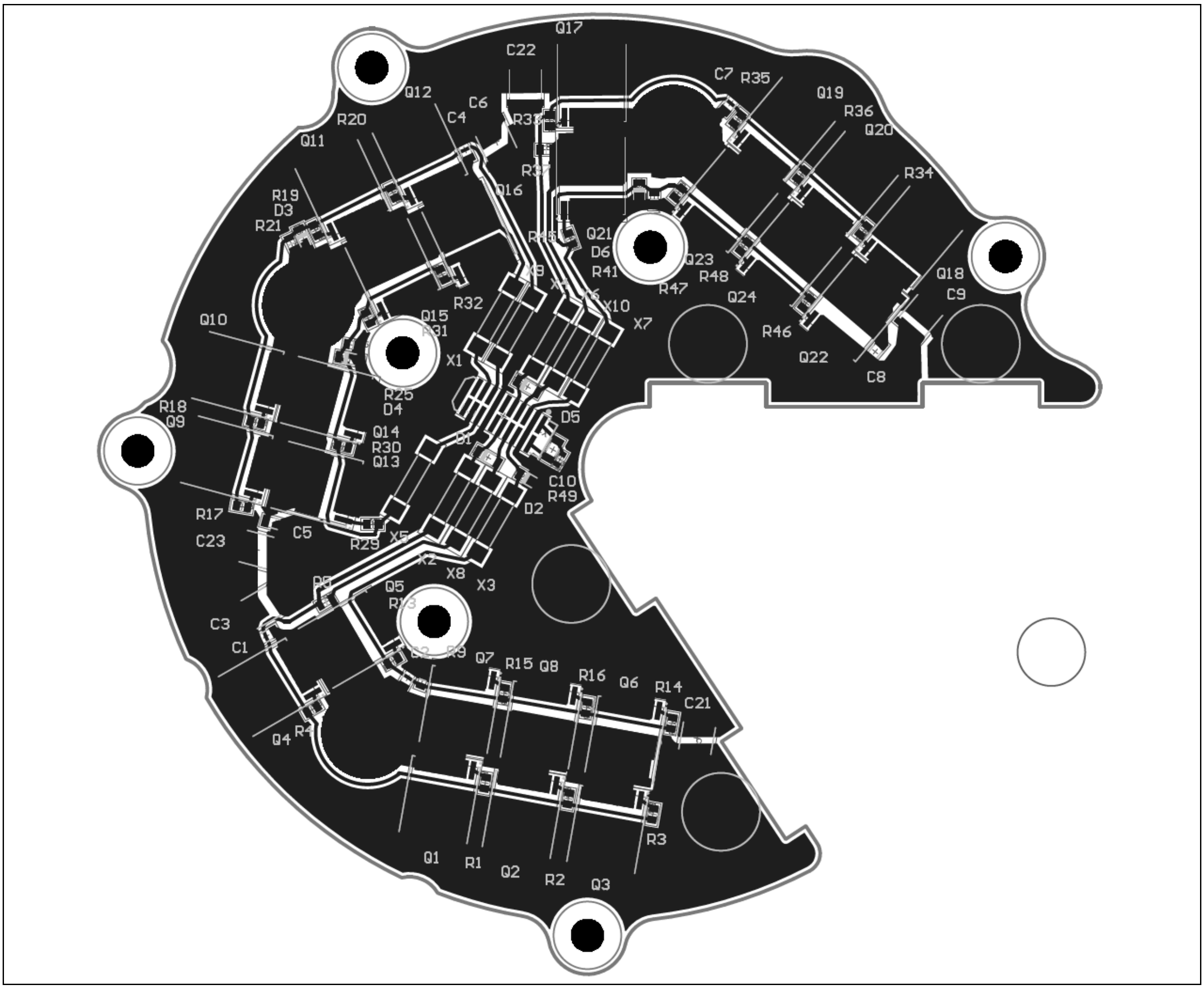


Figure 28 The layout of the copper layer

4.8 Bill of materials

Table 10 shows the BOM of the power board excluding the dc-link capacitors, bus bar, screws and nuts.

Table 10 Bill of materials

#	Qty.	Designator	Manufacturer	Part Number	Description
1	7	C1, C2, C4, C5, C7, C8, C10	AVX	12061C104K4Z2A	100n/100V/X7R
2	6	C3, C6, C9, C21, C22, C23	TDK	C5750X7R2A475K230KA	4.7uF/100V/10%/X7R/125°C
3	6	D1, D2, D3, D4, D5, D6	Vishay	BZT55B15	Zener Diode/15V
4	24	Q1, Q2, Q3, Q4, Q5, Q6, Q7, Q8, Q9, Q10, Q11, Q12, Q13, Q14, Q15, Q16, Q17, Q18, Q19, Q20, Q21, Q22, Q23, Q24	Infineon Technologies	IAUS240N08S5N019	1.9mohm 80V N-channel MOSFET
5	24	R1, R2, R3, R4, R13, R14, R15, R16, R17, R18, R19, R20, R29, R30, R31, R32, R33, R34, R35, R36, R45, R46, R47, R48	Yageo /Phycomp	AC0805FR-0715RL	15/150V/1%
6	6	R5, R9, R21, R25, R37, R41	Vishay	CRCW080510K0FKEA	10k/150V/1%
7	1	R49	Vishay	NTCS0603E3103FMT	NTC resistor 10k/1%/0603
8	1	X1	Samtec	TFM-110-22-S-D-P	SMT connector
9	9	X2, X3, X4, X5, X6, X7, X8, X9, X10	Keystone Electronics	5104TR	Silver Plate SMD Jumper

5 Measurement results

Table 11 shows the summary of tests.

Table 11

Test item	**Result**
X-ray check	Air bubbles under MOSFET
Switching behavior	V_{DS} 65V at V_{DC} 46V
Thermal distribution	Thermal resistance is about 2K/W. The junction temperature is 150°C at the most critical transient working condition.
Torque Speed characteristics	Meet the design target at motoring mode and generating mode
Voltage ripple	Meet VDA320

5.1 X-ray check

Equipment: X-ray

Description: Check if there are bubbles under 24pcs MOSFET

Result & Analysis:

The air bubbles area is 40~50% as shown in Figure 29 to Figure 30.

Calculation was done as follow to estimate the influence:

Thickness of solder:	0.05mm
Thermal conductivity of solder:	60 W/mK
Area of pad:	50mm^2
Rth of solder:	0.05*1E-3 / 60 / 50*1E-6 = 0.017 K/W

If contact area decrease to 50%, Rth would be 0.035K/W.

It cause 0.4°C temperature rise when power is 23W corresponding 400Arms output. It cannot be accepted from the quality perspective, but it could be used for thermal evaluation and lab test.

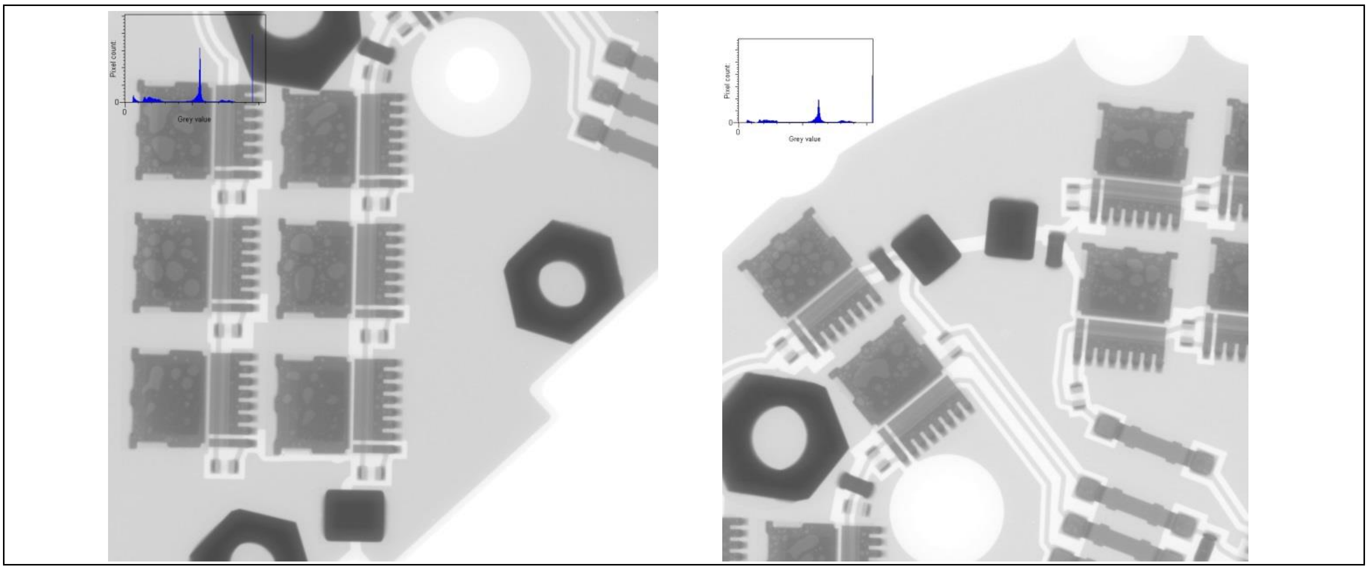


Figure 29 X-ray picture 1

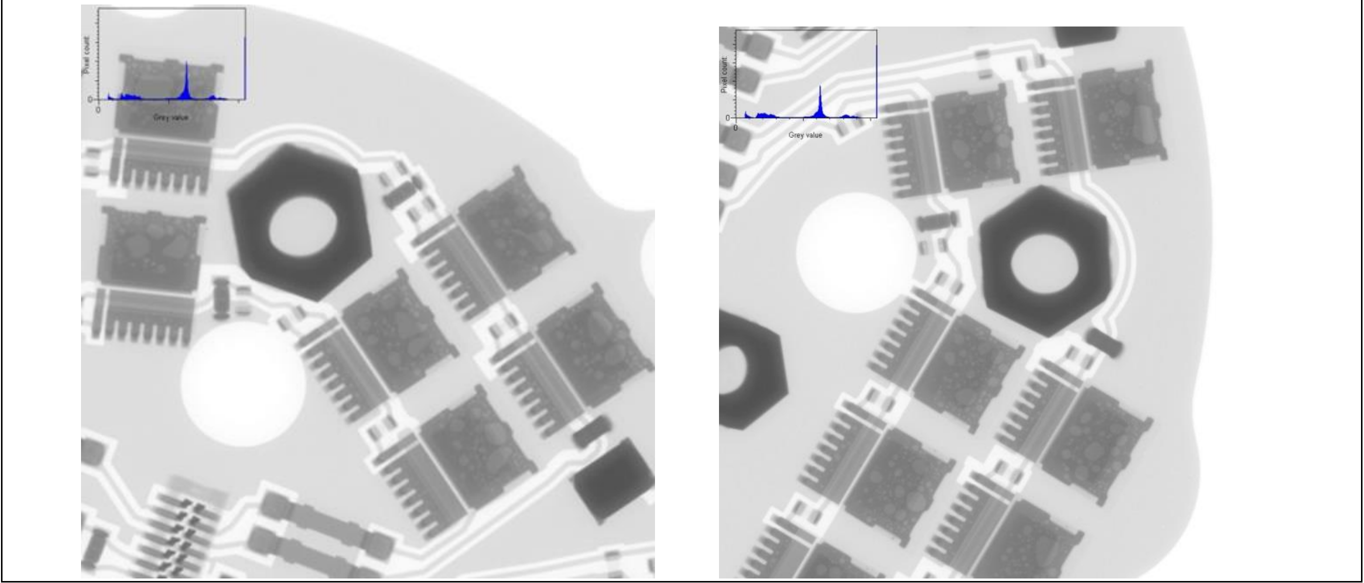


Figure 30 X-ray picture 2

5.2 Switching behavior

Switching behavior test shows the over voltage of the V_{DS} at switching off. Figure 31 is the waveform of 570A switching off. C1 is the V_{GS} signal. C2 is the V_{DS} of the four paralleled MOSFET. C3 and C4 is the current on the two DC- screws measuring by ultra mini rogowski coil referring Figure 8 and Figure 9. C3+C4 are total I_D current. The V_{DS} peak value is 65V when the V_{DC} is 46V. The voltage spike is 17V.

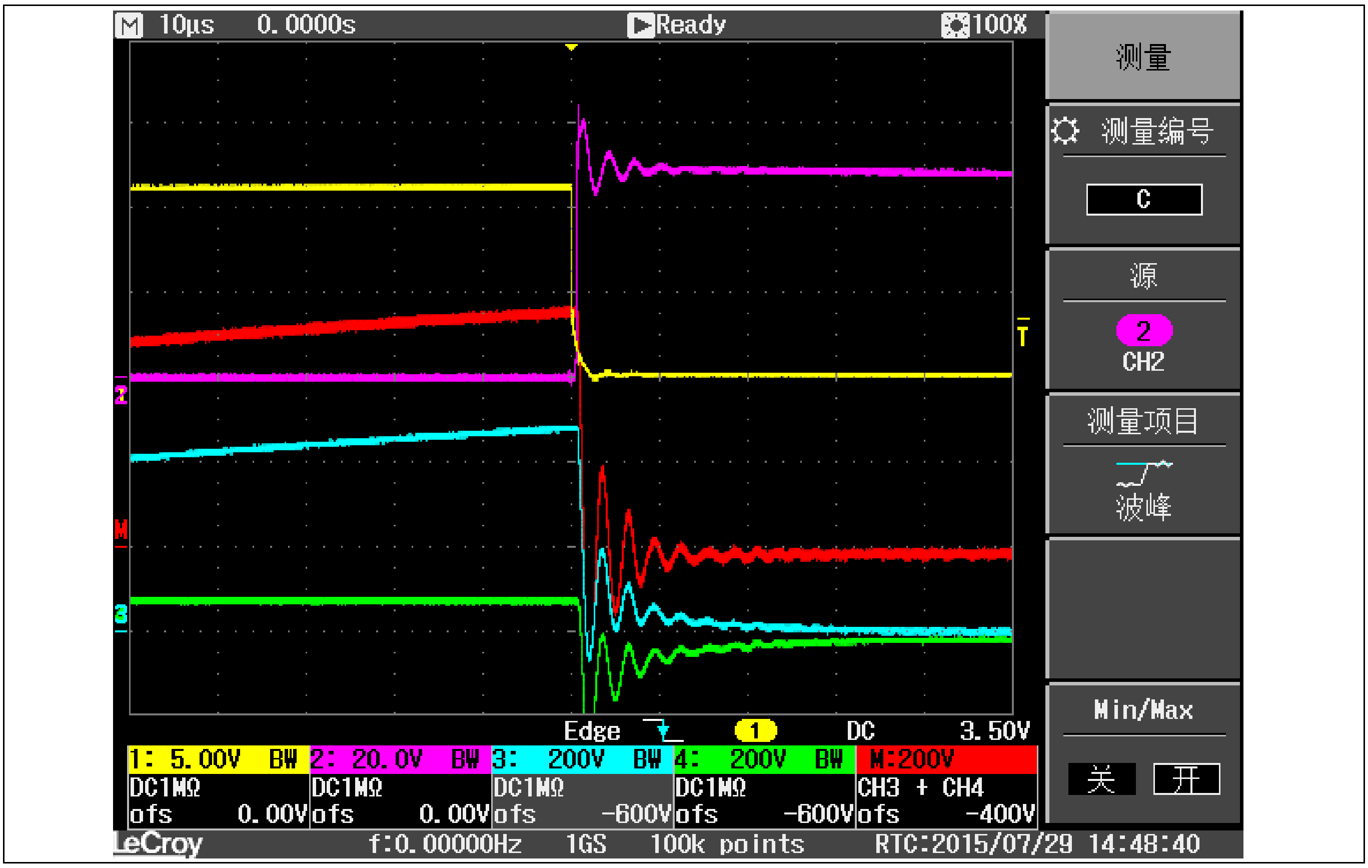


Figure 31 V_{DS} waveform of 570A switching off

C1 (yellow): V_{DC}, C2 (purple): V_{DS}, C3 (blue): I_{D1}, C4 (green): I_{D2}, Math (red): $I_{D1}+I_{D2}$

5.3 Thermal distribution

Thermal distribution test shows the thermal performance of the MOSFET and DC-link capacitors.

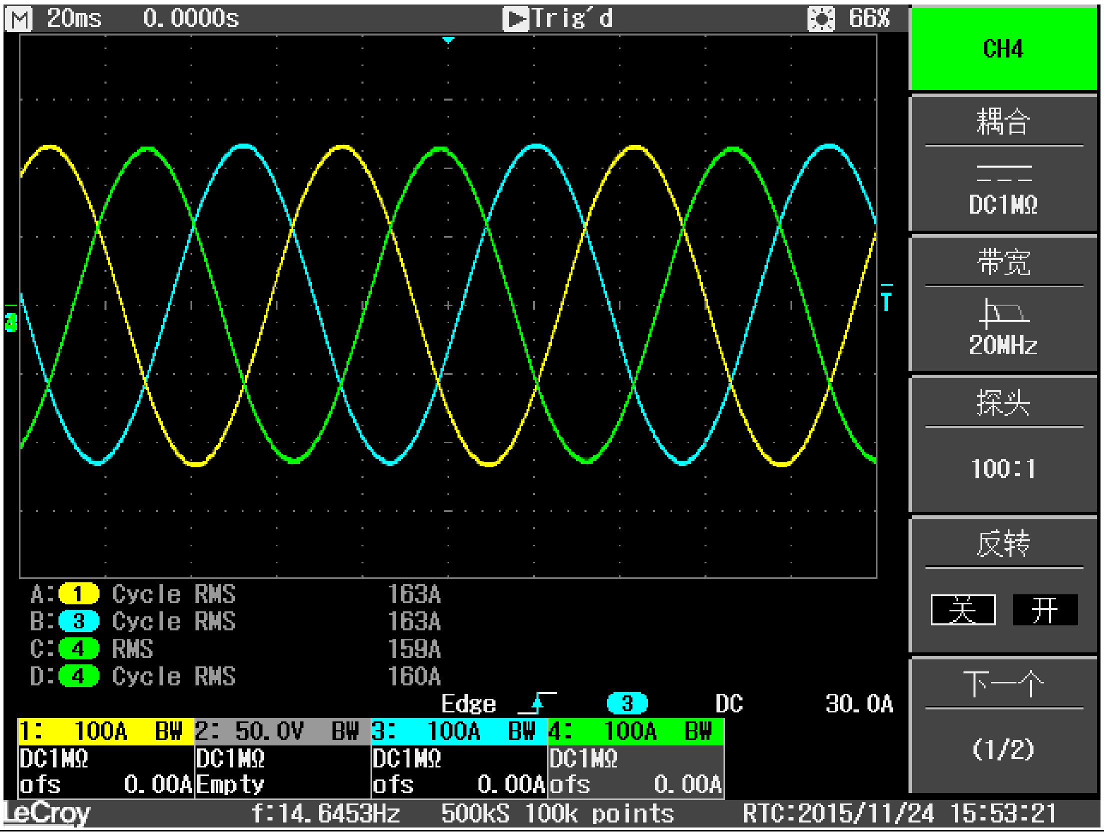
5.3.1 Static state thermal distribution

The static state thermal test is critical for the DC-link capacitors.

Test condition is shown as follow:

V_{DC}:	48V
Load type:	Inductor load
T_{water}:	18.8°C
Electrical frequency:	15Hz
Liquid flow:	13L/min
Duration:	15min
I_{phase}:	160A

Figure 32 shows the three phase current waveform at 160Arms.



```
20ms     0.0000s                    Trig'd                 66%
A: 1 Cycle RMS          163A
B: 3 Cycle RMS          163A
C: 4 RMS                159A
D: 4 Cycle RMS          160A
                    Edge        3         DC        30.0A
1:   100A   BW 2: 50.0V   BW 3:   100A   BW 4:   100A   BW
DC1MΩ          DC1MΩ          DC1MΩ          DC1MΩ
ofs       0.00A Empty         ofs       0.00A ofs       0.00A
           f:14.6453Hz    500kS 100k points    RTC:2015/11/24 15:53:21
```

Figure 32 160Arms three phase current wave form

Figure 33 shows V_{GS} waveform at 160Arms. The green line is high side V_{GS} of W phase. The orange line is low side V_{GS} of low side.

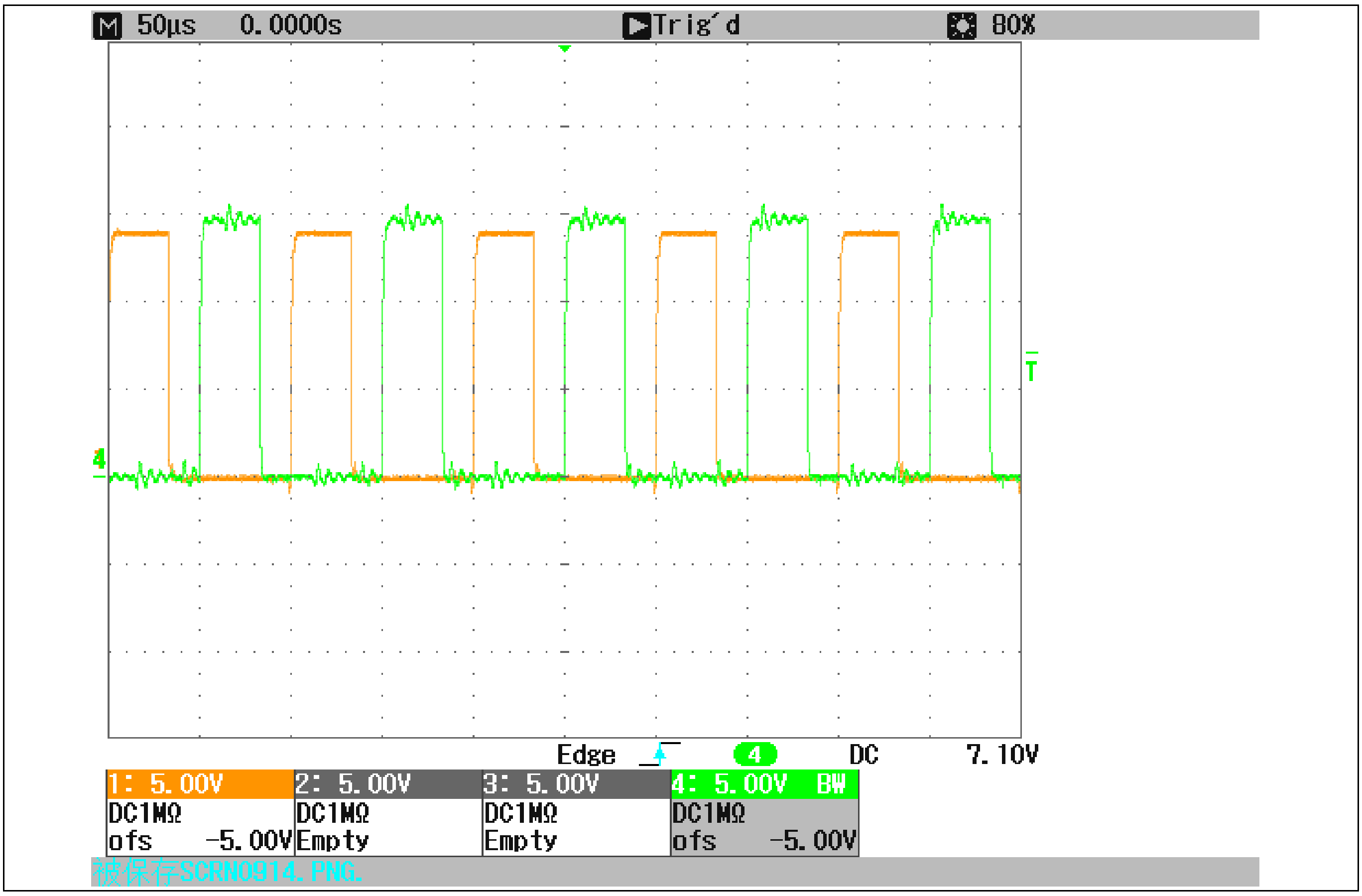


Figure 33 V_{GS} at 160Arms output.

Figure 34 shows the thermal distribution. The MOSFETs were well cooling by the liquid cooling heatsink and reach static state in several minutes. It shows that there is 10°C temperature rise on MOSFET. R_{thCA} of case to coolant was calculated as about 2K/W. The junction temperature would be several degrees higher than case at continuous working condition. The temperature of DC-Link capacitors was up to 40°C. The DC-link capacitors were cooling by still air. It shows that the DC-link capacitors need external heat sink to handle the thermal at continuous condition.

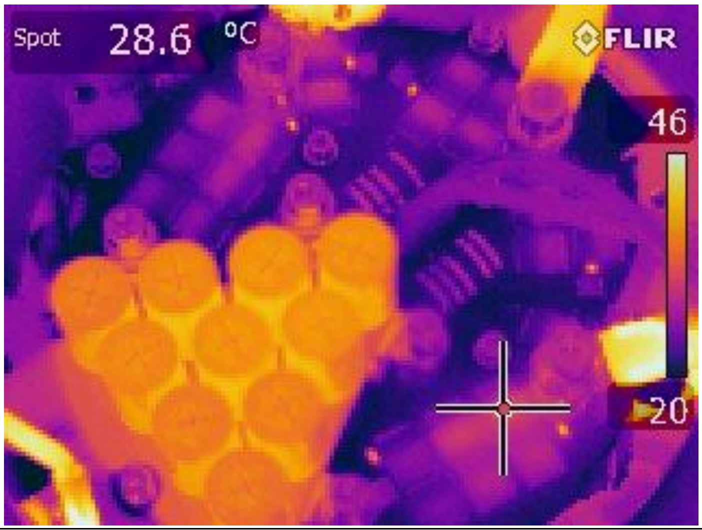


Figure 34 Steady state thermal distribution of the power stage @160Arms

5.3.2 Dynamic thermal distribution

The dynamic thermal test is critical for the MOSFETs. Three dynamic thermal tests were done.

The first one is lab test with 400Arms output of inductor load. The second one is bench test with 40Nm load. The third one is bench test with 50Nm load.

5.3.2.1 Lab Test with 400Arms output of inductor load

Equipment:

Inductor load

Driver board

SVPWM generator

Cooling System

48V Power Supply

Thermal Camera

Description:

48V 400Arms with inductor load

Check V_{DS} and V_{GS} PWM signal

Thermal of Tc

Test condition：

V_{DC}: 48V

Load type: Inductor

I_{phase}: 404Arms

T_{water}: 18.6°C

Duration: 10sec

Test result:

Tcase of MOSFET: 45.9°C

Figure 35 shows the thermal distribution of power stage at 400Arms output with 10sec duration. The maximum temperature rise was 45.9°C - 18.6°C = 27.3°C. As mention in 4.2.3, the junction temperature rise could be 47.3°C. When the temperature of coolant is 95°C, the junction temperature could be 142.3°C.

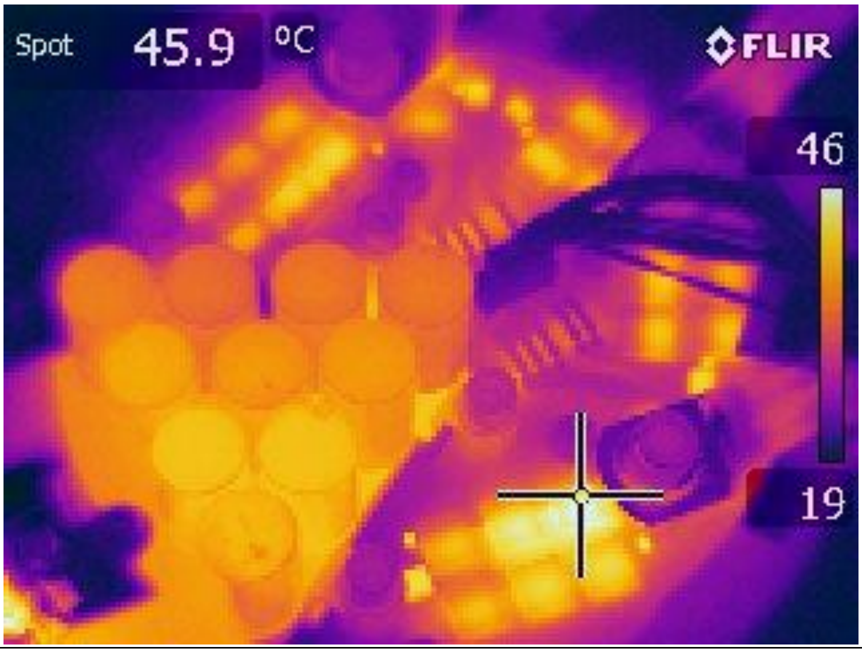


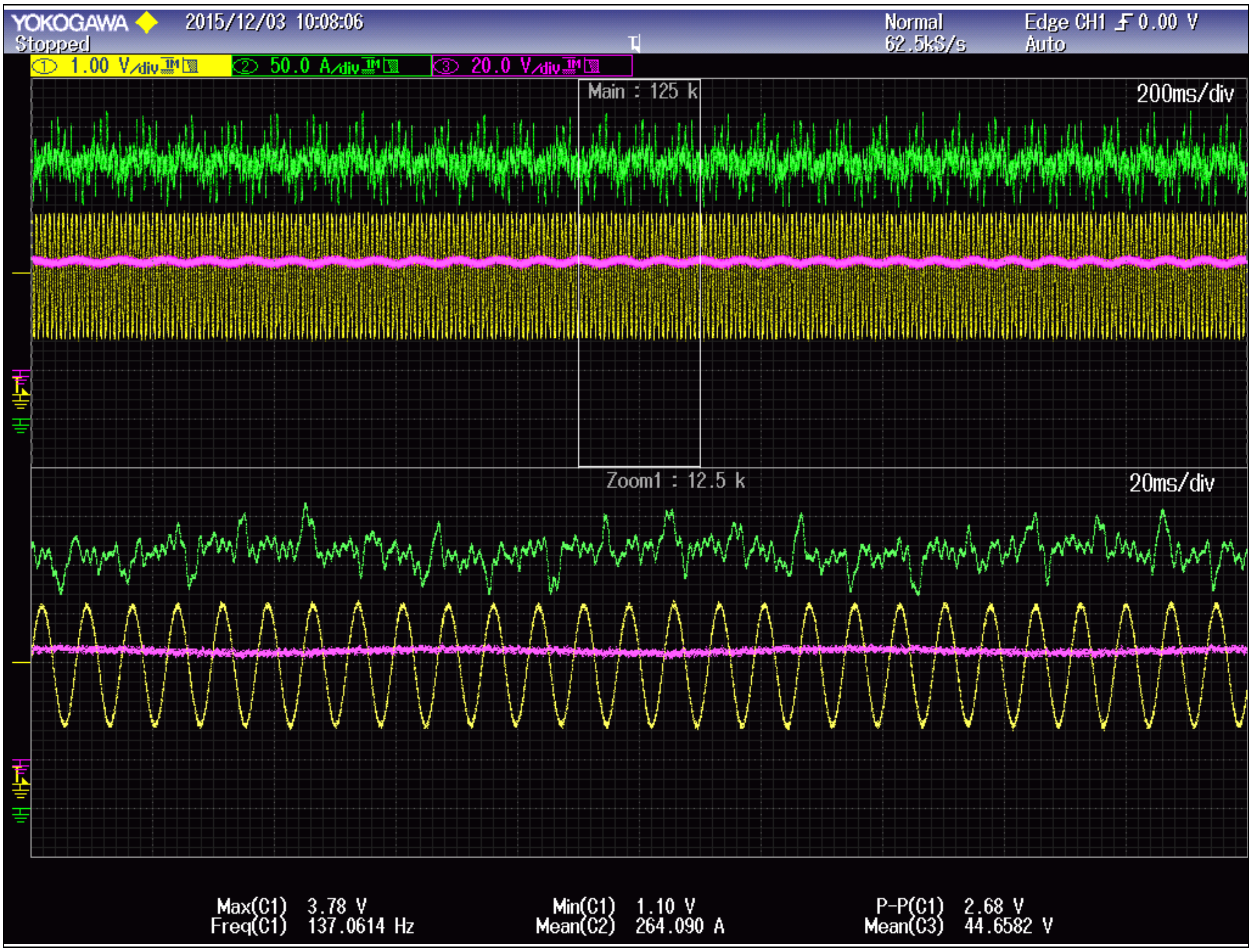
Figure 35 Dynamic thermal distribution of the power stage @400Arms 10s

5.3.2.2 Bench test with 40Nm load

Test condition is shown as follow:

Vdc: 44.6V
Load type: PMSM motor
Twater: 20°C
Motor Speed: 2000rpm
Torque: Motoring 40Nm
Liquid flow: 15L/min
Duration: 10 seconds
Idc: 264A
Iphase: 339Arms

Figure 36 shows the related wave form of dynamic thermal distribution. DC voltage, DC current and phase current could be read from the wave form.



Max(C1) 3.78 V
Freq(C1) 137.0614 Hz
Min(C1) 1.10 V
Mean(C2) 264.090 A
P-P(C1) 2.68 V
Mean(C3) 44.6582 V

Figure 36 Test wave form of dynamic thermal distribution 40Nm motoring

C1: phase current signal from LEM sensor. C2: DC current. C3: DC voltage.

Figure 37 shows the result of dynamic thermal distribution at the end of test period. The positions of measurement points SP1, SP2, SP3 SP4 are shown in Figure 37. SP1 is the highest temperature point of W phase MOSFET. SP2 is the highest temperature point of V phase MOSFET. SP3 is the highest temperature point of U phase MOSFET. SP4 is the temperature of DC-Link cap.

Note: the highest temperature point in the Figure 37 is the power terminal on the top left side. The reason is that the power terminal surface is not smooth. The contact resistance is very high, but it wouldn’t influence the measurement of MOSFET and DC-link capacitor.

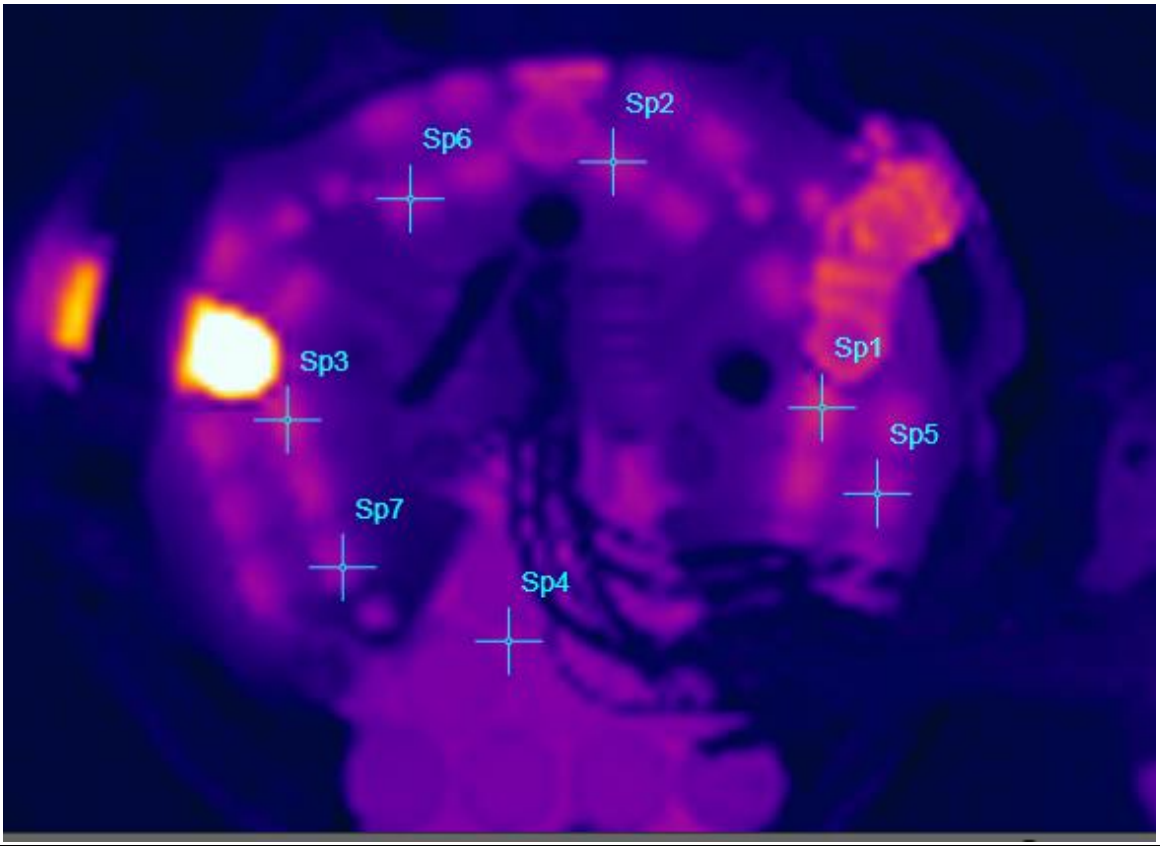


Figure 37 Dynamic thermal distribution of power stage 40Nm motoring

Figure 38 shows the dynamic behavior of the MOSFET and DC-link capacitor. The system started at 45 second. It reached 40Nm at 1min05sec and kept to 1min15sec. At beginning the MOSFETs temperature is close to coolant temperature, and the DC-link capacitor temperature is close to ambient temperature. The maximum temperature rise of MOSFET case (ΔTc) is 24°C. The experimental analysis shows that the junction temperature would be 20°C higher than top case temperature. When the coolant temperature is 95°C, the junction temperature of MOSFET could be 140°C. This approximate equivalent meets the requirement. The DC-link capacitor is quiet cool in this test because the thermal storage capacity is enough to handle the dynamic thermal.

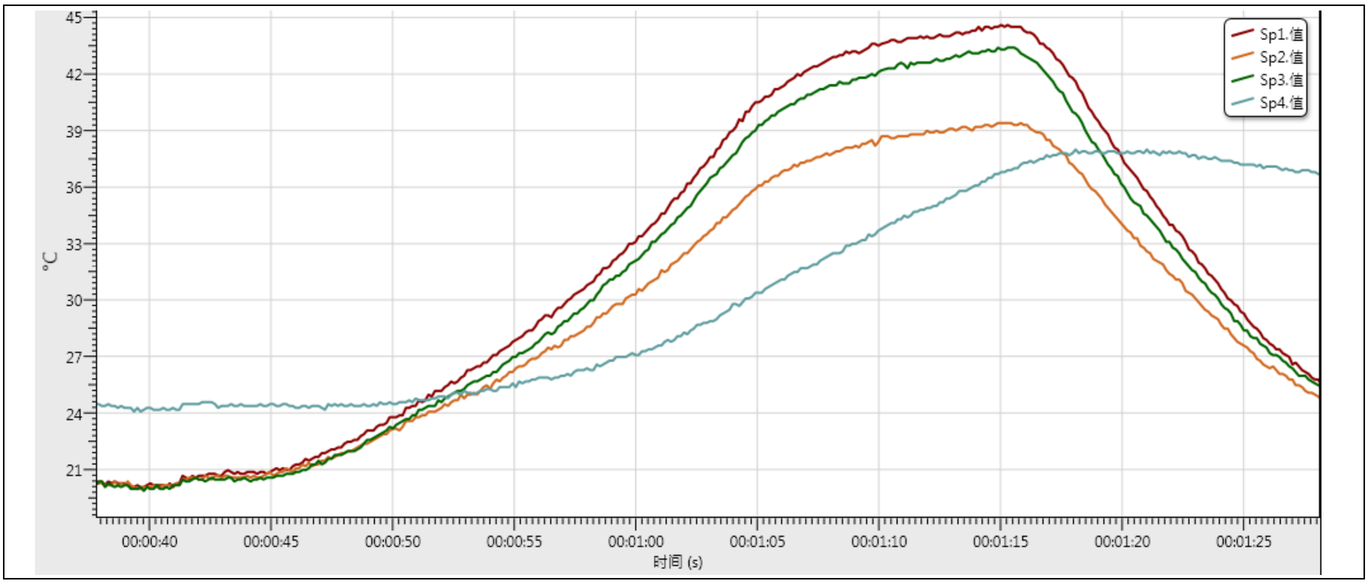


Figure 38 **Dynamic thermal behavior of the MOSFET and DC-link capacitor 40Nm motoring**

5.3.2.3 Bench Test with 50Nm load

Test condition:

Vdc: 44.6V

Load type: PMSM motor

Twater: 20°C

Motor Speed: 2000rpm

Torque: Motoring 50Nm

Liquid speed: 15L/min

Current Sensor: Panasonic +/-800A corresponding 0.5~4.5V

Duration: 0.5 seconds

Idc: 264A

Iphase: 480Arms

Figure 39 shows the related wave form of dynamic thermal distribution. DC voltage, DC current and phase current could be read from the wave form.

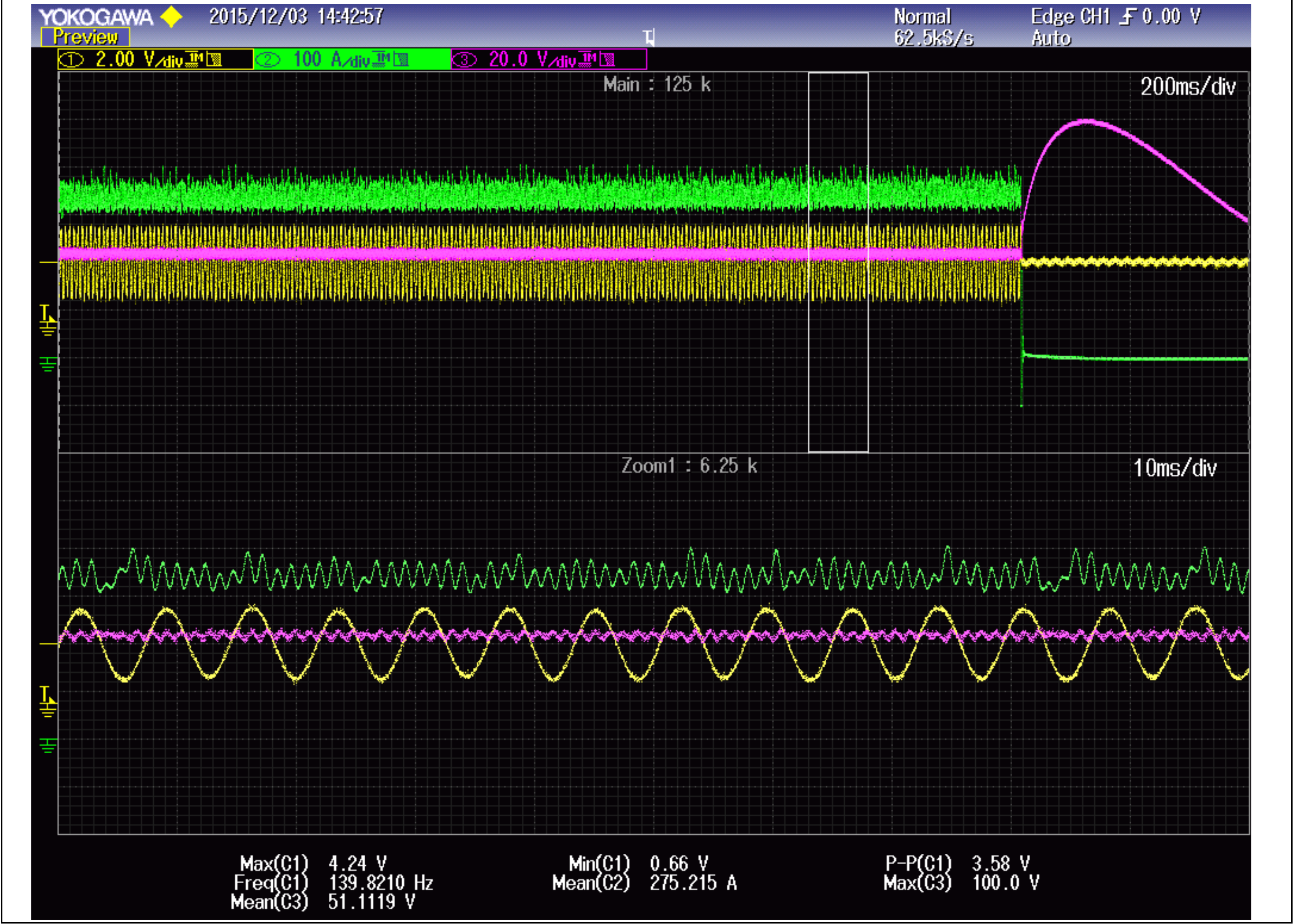


Figure 39 Test wave form of dynamic thermal distribution 50Nm motoring

C1: Phase current of current sensor (Yellow)

C2: DC current (Green)

C3: DC bus voltage (Purple)

Figure 40 shows the result of dynamic thermal distribution at the end of test period. The positions of measurement points SP1 to SP7 are shown in Figure 40. SP1 is the highest temperature point of W phase MOSFET. SP2 is the lowest temperature point of V phase MOSFET. SP3 is the highest temperature point of V phase MOSFET. SP4 is the lowest temperature point of V phase MOSFET.SP5 is the highest temperature point of U phase MOSFET. SP6 is the lowest temperature point of U phase MOSFET. SP7 is the temperature of DC-Link cap.

Note: the highest temperature point in the Figure 40 is the power terminal on the top left side. The reason is that the power terminal surface is not smooth. The contact resistance is very high, but it wouldn’t influence the measurement of MOSFET and DC-link capacitor.

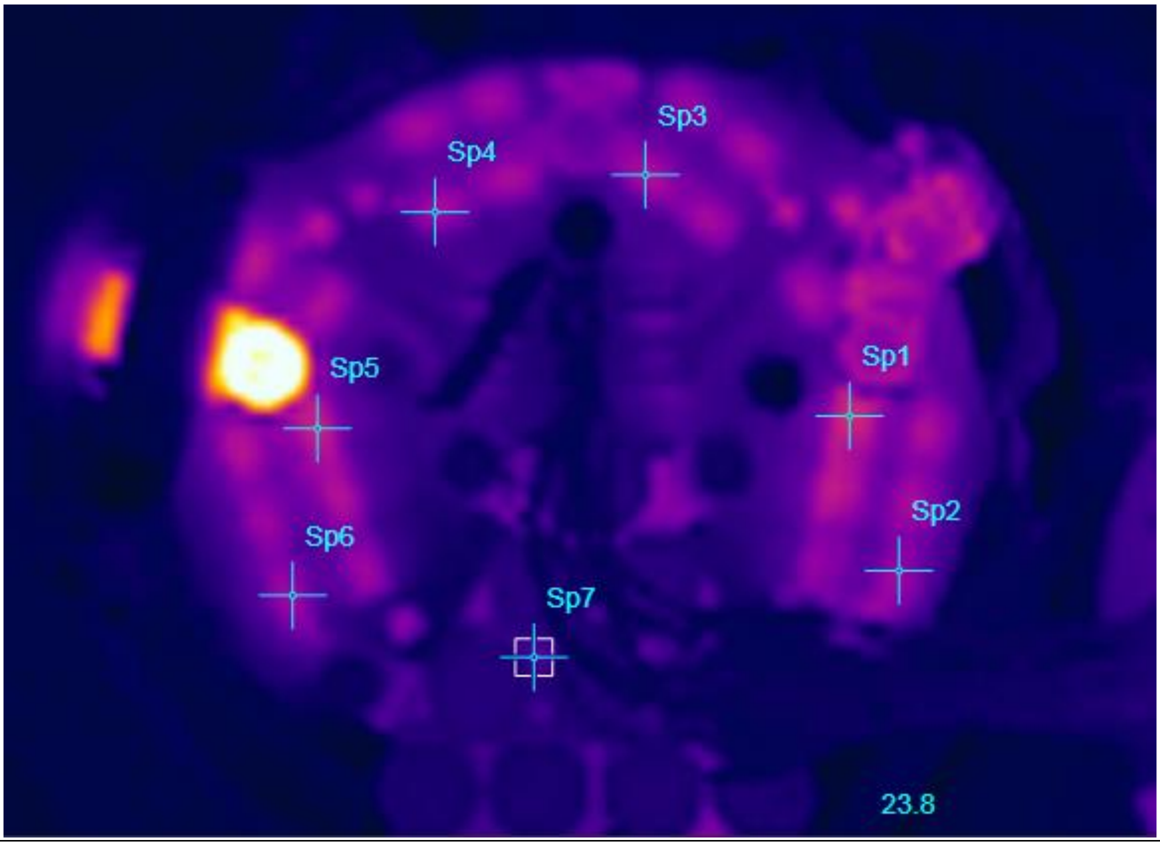


Figure 40 Dynamic thermal behavior of the MOSFET and DC-link capacitor 50Nm mortoring

Sp1 Tmax of W Phase MOSFET, Sp2 Tmin of W Phase MOSFET, Sp3 Tmax of V Phase MOSFET

Sp4 Tmin of V Phase MOSFET, Sp5 Tmax of U Phase MOSFET, Sp6 Tmin of U Phase MOSFET

Sp7 Tmax of DC link capacitors

Figure 41 shows the dynamic behavior of the MOSFET and DC-link capacitor. The system started at 1min30second. It reached 50Nm at 2min03sec and shunt down immediately. At beginning the MOSFETs temperature is close to coolant temperature, and the DC-link capacitor temperature is close to ambient temperature. The maximum temperature rise of MOSFET case (ΔTc) is 30°C. The experimental analysis shows that the junction temperature would be 20°C higher than top case temperature. When the coolant temperature is 95°C, the junction temperature of MOSFET could be 145°C. This approximate equivalent meets the requirement. The DC-link capacitor is quiet cool in this test because the thermal storage capacity is enough to handle the dynamic thermal.

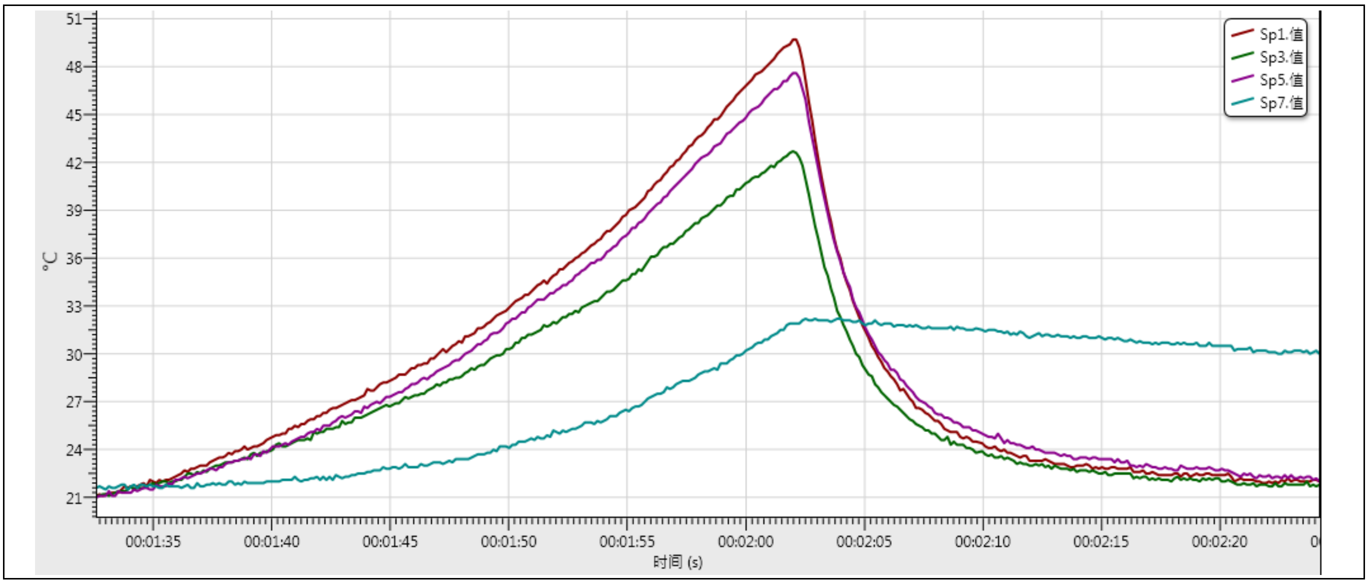


Figure 41 Dynamic thermal behavior of the MOSFET and DC-link capacitor 50Nm motoring

5.4 Torque Speed characteristics

The inverter plus motor can reach the torque speed characteristics on the test bench as shown in Table 12 and Table 13. It shows the BSG system capability. It is not directly limited by the power stage.

Table 12 Motoring characteristics

Motoring Speed (RPM)	**Torque Reference (Nm)**	**Torque measurement (Nm)**
500	40	39.44
1000	40	39.24
1500	40	39.20
2000	40	39.08
2500	34	33.00
3000	29	25.84
3500	25	21.72
4000	21	18.16
4500	19	15.76
5000	17	13.84
5500	16	12.28
6000	14	11.08
6500	13	11.64

Table 13 Generating characteristics

Generating Speed (RPM)	**Torque Reference (Nm)**	**Torque measurement (Nm)**
500	40	40.28
1000	40	40.24
1500	40	40.24
2000	40	40.16
2500	40	40.16
3000	40	40.20
3500	40	37.28
4000	36	30.32

Generating Speed (RPM)	**Torque Reference (Nm)**	**Torque measurement (Nm)**
4500	32	24.72
5000	29	20.48
5500	26	17.40
6000	24	14.08

5.5 Voltage ripple

The voltage ripple measured at 1750rpm of motor speed. The ripple is not the key parameter for Aluminum DC link capacitors. If film cap is used for DC-link capacitor, the capacitance will significantly reduce. Then the voltage ripple should be concerned. This test is archived for comparing with film cap.

Figure 42 to Figure 45 show the voltage ripple on DC bus as purple line C3 channel.

Table 14

Mode	**Torque**	**Target Phase Current**	**Voltage ripple**	**Percentage**
Motoring	16.5Nm	160Arms	1.63V	3.4%
Motoring	40.0Nm	400Arms	3.73V	7.8%
Generating	16.5Nm	160Arms	1.79V	3.7%
Generating	40.0Nm	400Arms	3.40V	7.1%

Figure 42 Voltage ripple waveform @ motoring 16.5Nm

C1 and C2: V_{DS} waveform of certain phase. C3: Voltage ripple of DC bus.

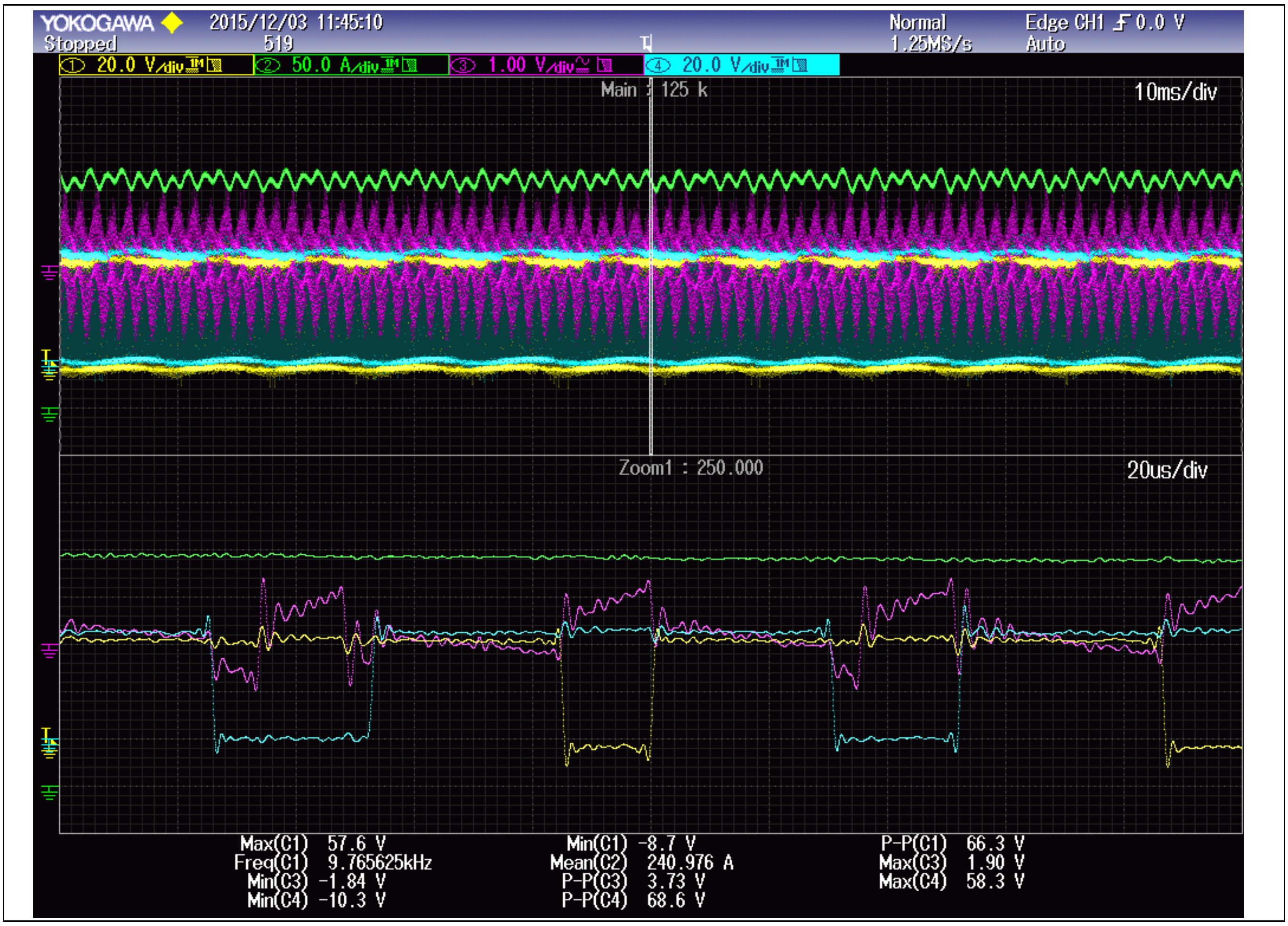


Figure 43 Voltage ripple waveform @ motoring 40Nm

C1 and C2: V_{DS} waveform of certain phase. C3: Voltage ripple of DC bus.

Figure 44 Voltage ripple waveform @ Generating 16.5Nm

C1 and C2: V_{DS} waveform of certain phase. C3: Voltage ripple of DC bus.

Figure 45 Voltage ripple waveform @ Generating 40Nm

C1 and C2: V_{DS} waveform of certain phase. C3: Voltage ripple of DC bus.

6 Summary

Electrical machines and inverters were used as Belt-driven Starter Generator (BSG) system in the Mild Hybrid vehicle to enhance the output torque of the engine. A 48V 12kW inverter of BSG was designed with paralleled TO-Leadless MOSFETs. The phase current was up to 500Arms while the V_{DS} voltage spike was under 70V. The maximum temperature rise of MOSFET was 30°C, and the current of MOSFET was balanced well. This design fulfilled the power requirement with 105°C liquid cooling system. It's scalable with optional numbers and different R_{DSon} of MOSFET in the same package and flexible for 3~6 phases inverter.

7 Reference

[1] Infineon AN2013-05 TO-Leadless: A new Package for High Current High Reliability Applications.

[2] Infineon Application Note: MOSFET Power Losses Calculation Using the Datasheet Parameters.

[3] Solder joint reliability against thermo-mechanical stress: Leadless packages for automotive MOSFET

Revision History

Major changes since the last revision

2018-08-2, V2.2 Add TOLG information.

Page or Reference	**Description of change**
Chapter 3.2.3	Add introduction of TOLG MOSFET
Chapter 3.2.3	Add available automotive TOLG MOSFET in the table
Chapter 4.2.5	TOLG MOSFET for Al based IMS board

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