swissbit®

Product Data Sheet

Industrial SDXC Memory Card

S-55 High reliability series

UHS-I Interface, 3D TLC

Extended and Industrial Temperature Grade

Date: March 25, 2022
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Made in Germany

Contents

S-55 High reliability series
Industrial SDXC Memory Card – 64 GBytes up to 512 GBytes

1. Product Summary

- **Capacities:** 64 GBytes, 128 GBytes, 256 GBytes, 512 GBytes
- **Form Factor:** Standard SD Memory card form factor - 32.0mm x 24.0mm x 2.1mm, Write Protect slider
- **Compliance[1]:** Fully compliant with SD Memory Card specification 6.10
  - SDXC high speed mode, UHS-I
  - Speed class 10/U3/V30/A1/A2 according SD6.10 specification
  - SD2.0 backward compliant
  - exFAT preformatted
- **Environmental:** RoHS / REACH Compliant
- **Compatibility:** Support SD SPI mode
- **Performance (max. capacity):**
  - Read performance: sequential read up to 97 MBytes/s
  - Write performance: sequential write up to 60 MBytes/s
  - SDR12, SDR25, SDR50, SDR104, DDR50 mode
- **Operating Temperature Range:**
  - Extended: -25 °C to 85 °C
  - Industrial: -40 °C to 85 °C
- **Storage Temperature Range:** -40 °C to 85 °C
- **Operating Voltage:** 2.7...3.6V
- **Data Retention:** 10 years @ life begin; 1 year @ life end
- **Error Correction:** Advanced ECC (Error Correction Code)
  - Mean Time Between Failure (MTBF): > 3,000,000 hours
  - Number of insertions: up to 20,000

2. Product Features

- High performance 6.10 specification
  - SD burst up to 104MB/s
  - SD Normal speed 0...25MHz clock rate
  - SD High speed 25...50MHz clock rate
  - SD UHS-I speed 0...50MHz (DDR) and 0...208MHz (SDR)
- Power Supply: (Low-power CMOS technology)
  - 2.7...3.6V normal operating voltage
- Optimized FW algorithms especially for read/write access, highest random write performance and best endurance with long data retention.
  - Designed for usage in applications with highest requirements regarding reliability like data logging, POS/POI, Medical and other demanding use-cases.
  - Especially suitable for intensive read/write operations
  - Advanced power-off reliability technology
  - Wear Leveling technology
    Equal wear leveling of static and dynamic data. The wear leveling assures that dynamic data as well as static data is balanced evenly across the memory. With that the maximum write endurance of the device is guaranteed
  - The S-55 high reliability series is optimized for high read/write traffic for demanding industrial applications.

[1] The verification of host system and storage device compatibility is in customer's responsibility. Swissbit can provide guidance and support on request.

  - Read Disturb Management
    The read commands are monitored and the content is refreshed when critical levels have occurred
  - Data Care Management
    The interruptible background process maintain the user data for Read Disturb effects or Retention degradation due to high temperature effects
  - Near miss ECC technology
    Minimize the risk of uncorrectable bit failure over the product life time. Each read command analyzes the ECC margin level and refresh data if necessary
  - Diagnostic features with Life Time Monitoring tool support
- High reliability
  - The product is optimized for long life cycle that requires superior data retention because of high temperature mission profile
  - FW is designed to ensure highest reliability at lowest possible DPPM rates
  - Number of card insertions/removals up to 20,000
  - Industrial Temperature range -40° up to 85°C
  - SIP (System In Package) process for extreme dust, water and ESD proof
- Controlled "Locked" BOM & PCN process
- Customized options like CID registers, CPRM keys, firmware incl. settings and marking on request
- Manufactured in a TS 16949 certified factory
- In-field firmware update[2]
- Swissbit Life Time Monitoring (SBLTM) Tool and SDK for SBLTM (on request)

[2] The support of In-Field FW update capabilities on host systems is recommended.

3. Ordering Information

Table 1: Standard Product List

Capacity	Temperature	
	Extended	Industrial
	Part Number	Part Number
64 GBytes	SFSD064GLgAM1MT-E-xx-2y1-STD	SFSD064GLgAM1MT-I-xx-2y1-STD
128 GBytes	SFSD128GLgAM1MT-E-xx-2y1-STD	SFSD128GLgAM1MT-I-xx-2y1-STD
256 GBytes	SFSD256GLgAM1MT-E-xx-2y1-STD	SFSD256GLgAM1MT-I-xx-2y1-STD
512 GBytes	SFSD512GLgAM1MT-E-xx-2y1-STD	SFSD512GLgAM1MT-I-xx-2y1-STD

g = product generation, xx = flash configuration, y = firmware revision

Table 2: Available Part Numbers

Capacity	Temperature	
	Extended	Industrial
	Part Number	Part Number
64 GBytes	SFSD064GL1AM1MT-E-5E-211-STD	SFSD064GL1AM1MT-I-5E-211-STD
128 GBytes	SFSD128GL1AM1MT-E-6F-211-STD	SFSD128GL1AM1MT-I-6F-211-STD
256 GBytes	SFSD256GL1AM1MT-E-7G-211-STD	SFSD256GL1AM1MT-I-7G-211-STD
512 GBytes	SFSD512GL1AM1MT-E-8H-211-STD	SFSD512GL1AM1MT-I-8H-211-STD

4. Product Description

The SD Memory Card is a small form factor non-volatile memory card that provides high capacity data storage. Its aim is to capture, retain and transport data, audio and images, facilitating the transfer of all types of digital information between a large variety of digital systems.
The card operates in two basic modes:

- SDXC and UHS-I card modes
- SPI mode

The SD Memory Card also supports SD Default and High Speed mode with up to 50MHz clock frequency as well as UHS-I modes DDR50, SDR12/25/50/104 with up to 208MHz clock frequency.

- SD Memory card Specification Part 1, Physical layer Specification V6.10
- SD Memory card Specification Part 2, File System Specification V3.00
- Standard Size SD Card Mechanical Addendum Ver6.10

Simplified specifications are available at https://www.sdcard.org/

The Card has an internal intelligent controller that manages interface protocols, data storage and retrieval as well as hardware LDPC Error Correction Code (ECC), defect handling, diagnostics and clock control.
The advanced wear leveling mechanism assures an equal usage of the Flash memory cells to extend the lifetime.
The hardware LDPC-code ECC allows to detect and correct up to 120 defect bits per 1kByte.

The card has a power-loss management feature to prevent data corruption after power-down.

The cards are RoHS compliant and lead-free.

4.1 Performance Specifications

The S-55 read/write sequential and random CDM performance benchmarks are detailed in Table 3.

Table 3: Read/Write Performance

System Performance	typ[3]				Unit
	64GB	128GB	256GB	512GB	
Sequential Read	97	97	97	97	MB/s
Sequential Write	31	58	60	60	
Random Read 4k	1970	1970	1970	1970	IOPS
Random Write 4k	760	760	760	840	

4.2 Environmental Specifications

4.2.1 Recommended operating conditions

Table 4: SD Memory Card recommended operating conditions

Parameter	min	typ	max	unit
Extended Operating Temperature	-25	25	85	°C
Industrial Operating Temperature	-40	25	85	°C

[3] Card Speed measured with USB-SD Memory Card reader with Crystal Disk Mark 5.1.2 test tool 5x 1GB.

4.2.2 Recommended storage conditions

Table 5: SD Memory Card recommended storage conditions[4]

Parameter	min	typ	max[5]	unit
Extended Storage Temperature	-25	25	100	°C
Industrial Storage Temperature	-40	25	100	°C

4.2.3 Humidity & EMC

Table 6: Humidity & EMC

Parameter	Condition
Humidity (non-condensing)	85% RH @85°C 1000h
ESD	up to ±4 kV (contact discharge), according to IEC61000-4-2 and SDA, Human Body Model 150pF/ 330Ohm, on each contact pad, non-operating up to ±15 kV, (air discharge), according to IEC61000-4-2 and SDA, Human Body Model 150pF/ 330Ohm, isolated contact pad area, non-operating

4.2.4 Environmental conditions

Table 7: Environmental conditions

Parameter	Condition
UV light exposure	UV: 254nm, 15Ws/cm² according to ISO7816-1
X-Ray	0.1 Gy 70keV to 140KeV (ISO7816-1) according SDA
Durability	20,000 mating cycles
Drop Test	1.5m free fall
Bending / Torque	10N / 0.15Nm ±2.5° max
Mechanical Shock	1500G, 0.5ms, half sine wave ±xyz-axis, 4 pulses each non-operating, JESD22B110/B104 Condition B
Vibration	Non-operating, JESD22B110/B104 Condition B

4.3 Regulatory Compliance

The S-55 devices comply with the regulations / standards listed in Table 8.

Table 8: Environmental conditions

Abbreviation	Regulation/ Standard
EMC	CE – 2014/30/EU FCC – 47 CFR Part 15 UKCA – S.I. 2016 No. 1091 and S.I. 2012 No. 3032
RoHS	2011/65/EU with 2015/863/EU and 2017/2102/EU
REACh	1907/2006/EU and 207/2011/EU
WEEE	2012/19/EU

[4] The data retention time at temperature above 40°C is reduced. Swissbit can provide more data and support on request.
[5] High Temperature storage without operation reduces the data retention, in operation the data will be refreshed, if data error issues were detected

4.4 Physical dimensions

Table 9: Physical dimensions

Outer Physical dimensions	Value	Unit
Length	32.00±0.1	mm
Width	24.00±0.1	
Thickness	2.10±0.15	
Weight (typ.)	2	g

4.5 Reliability

Data reliability with data retention at the beginning and end of life is provided in the table below.

Table 10: Reliability[6]

Parameter	Value[7]
Data Retention at beginning @ 40°C	10 years
Data Retention at life end @ 40°C	1 year

4.6 Endurance

Endurance represented as TeraBytes Written (TBW) is provided in the following Table 11:

Table 11: Endurance[8, 9]

Drive Capacity	TeraBytes Written (TBW) @ Seq. Write 1MB Operation	TeraBytes Written (TBW) @ Random Write 128kB Operation	TeraBytes Written (TBW) @ Random Write 4kB Operation
64 GBytes	140	3.5	0.8
128 GBytes	270	7.5	1.0
256 GBytes	475	20	2.6
512 GBytes	940	40	4.5

5. User density specification

Table 12: SD Memory Card capacity specification

Capacity	Sectors	Total addressable Bytes
64 GBytes	121,634,816	62,277,025,792
128 GBytes	244,809,728	125,342,580,736
256 GBytes	492,077,056	251,943,452,672
512 GBytes	984,154,112	503,886,905,344

[6] NAND Flash data retention and endurance characteristics are defined according to JEDEC JESD47 and JESD22. The endurance limits of the storage shall be monitored by the life time information and simulated before field usage by the customer.

[7] After every power on the card reads the whole flash and performs a data refresh if necessary. Therefore, the data retention can be much longer in most use cases.

[8] The specified TBW is valid, if the amount of data is spread evenly over at least 24 months. Higher daily data volume or frequent writing below 0°C reduces the specified TBW. The drive endurance limit, also called EOL or 0% remaining life, is defined as TBW or DWPD over the product's limited lifetime warranty period. TBW calculations refer to the JEDEC JESD218A and JESD219A standard for SSD device life and endurance measurement techniques if not otherwise specified.

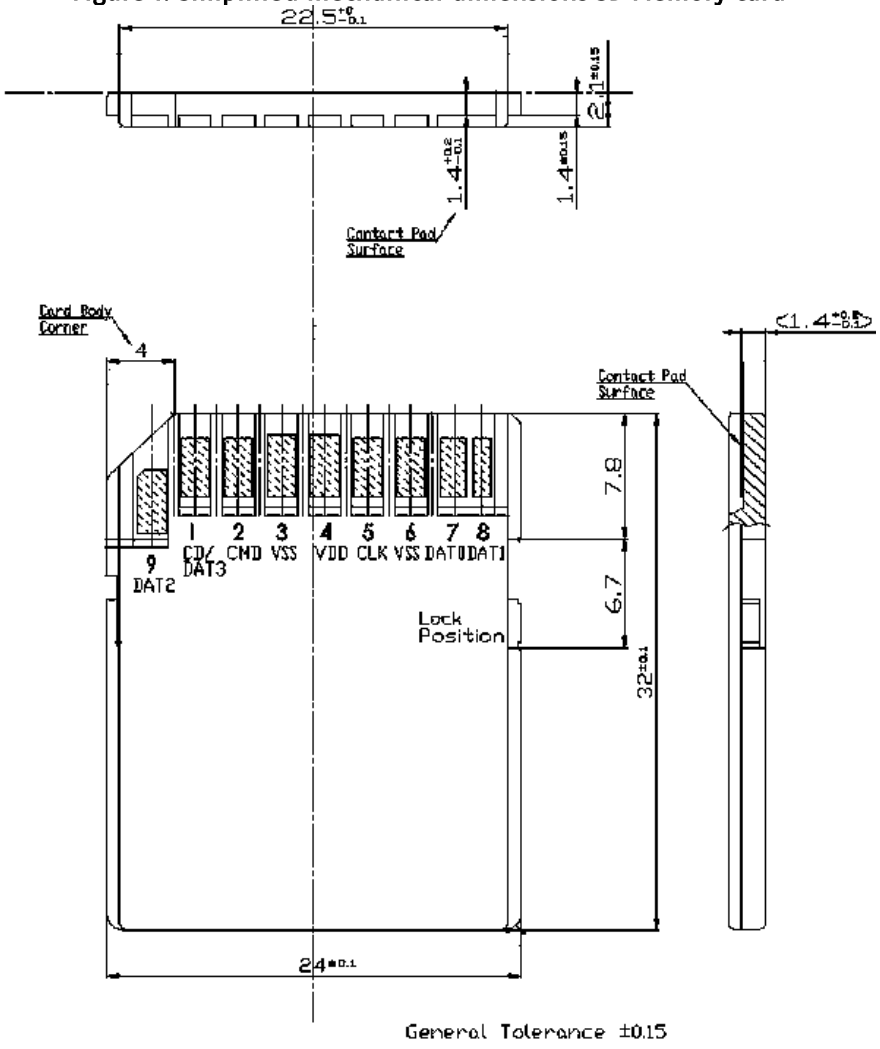
[9] Sequential write 1MB simulates a continuous stream recording on a drive which has been preconditioned with a sequential write of the complete drive, Random Write 128KB or 4KB represent data logging applications with large or small block sizes.

6. Card physical

6.1 Physical description

The SD Memory Card contains a single chip controller and Flash memory module(s). The controller interfaces with a host system allowing data to be written to and read from the Flash memory module(s).

Figure 1: Simplified mechanical dimensions SD Memory Card



7. Electrical interface

7.1 Electrical description

Figure 2: SD Memory Card shape and Interface (bottom view)

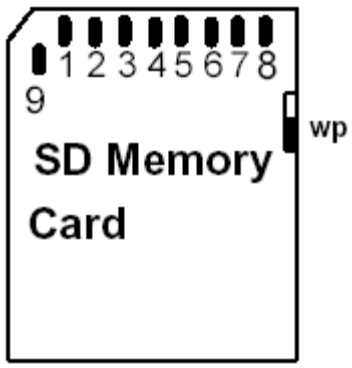


Table 13: Pad Assignment – SD Mode

Pin	SD Mode		
	Name	Type[10]	Description
1	CD/DAT3[11]	I/O/PP[12]	Card Detect/Data Line [Bit 3]
2	CMD	PP	Command/Response
3	VSS1	S	Supply voltage ground
4	VDD	S	Supply voltage
5	CLK	I	Clock
6	VSS2	S	Supply voltage ground
7	DAT0	I/O/PP	Data Line [Bit 0]
8	DAT1[13]	I/O/PP	Data Line [Bit 1]
9	DAT2[14]	I/O/PP	Data Line [Bit 2]

[10] S: power supply; I: input; O: output using push-pull drivers; PP: I/O using push-pull drivers
[11] The extended DAT lines (DAT1-DAT3) are input on power up. They start to operate as DAT lines after SET_BUS_WIDTH command. The Host shall keep its own DAT1-DAT3 lines in input mode, as well, while they are not used.
[12] At power up this line has a 50k0hm pull up enabled in the card. This resistor serves two functions Card detection and Mode Selection. For Mode Selection, the host can drive the line high or let it be pulled high to select SD mode. If the host wants to select SPI mode it should drive the line low. For Card detection, the host detects that the line is pulled high. This pull-up should be disconnected by the user, during regular data transfer, with SET_CLR_CARD_DETECT (ACMD42) command
[13] DAT1 line may be used as Interrupt Output (from the Card) in SDIO mode during all the times that it is not in use for data transfer operations (refer to "SDIO Card Specification" for further details).
[14] DAT2 line may be used as Read Wait signal in SDIO mode (refer to "SDIO Card Specification" for further details).

Table 14: Pad Assignment – SPI Mode

Pin	SPI Mode		
	Name	Type[10]	Description
1	CS	I[12]	Chip Select (neg true)
2	DI	I	Data In
3	VSS	S	Supply voltage ground
4	VDD	S	Supply voltage
5	SCLK	I	Clock
6	VSS2	S	Supply voltage ground
7	DO	O/PP	Data Out
8	RSV		
9	RSV		

7.2 Power up / Power down behavior and reset

7.2.1 Power up

The host can start with communication 1ms after 2.7V is reached according the SDA specification. That should perform 74 clock cycles and start with the sequence CMD0, CMD8, ACMD41 until card is ready as described in the SD specification 6.10.

7.2.2 Power down

When the power falls below 2.6V the controller stops the communication to the flash, but enables the flash to finish a started flash program operation (if voltage drop is not fast).

7.2.3 Power drop

If the voltage drops below 2.6V and rises again, the card performs a reset. The card must be initialized like after a power on.

7.3 DC characteristics

Measurements are not recommended operation conditions unless otherwise specified.

Table 15: DC characteristics

Symbol	Parameter	Density	Min	Typ	Max	Unit	Notes
I_{DD}	Operating Current Read (UHS-I / HS)	64GB		110 / 50	140	mA	@ 25°C
		128/256/512GB		110 / 50	140	mA	@ 25°C
I_{DD}	Operating Current Write (UHS-I / HS)	64GB		115 / 55	140	mA	@ 25°C
		128/256/512GB		130 / 65	170	mA	@ 25°C
I_{DD}	Standby Current			0.3	4	mA	@ 25°C
I_{DD}	Autoread Current (UHS-I / HS) during standby			90 / 45	110	mA	@ 25°C
I_{L3V3}	Leakage Current (3.3V signaling)		-10		10	µA	without pull up R
I_{L1V8}	Leakage Current (1.8V signaling)		-2		2	µA	without pull up R

Table 16: SD Memory Card recommended operation conditions

Symbol	Parameter		Min	Typ	Max	Unit
V_{DD}	Supply voltage	Normal operating status	2.7	3.3	3.6	V
-	Power Up Time (from 0V to VDD min)				250	ms

7.4 Signal loading

According to SD specification

7.5 AC characteristics

7.5.1 Default speed mode (0-25MHz)

According to SD specification

7.5.2 High speed mode (0-50MHz)

According to SD specification

7.5.3 UHS modes

UHS modes were driven with a signal level of 1.8V.
The cards support following UHS-I modes:

Table 17: Supported UHS-I modes

Mode	Max. Burst MB/s	Max. Clock frequency MHz
SDR12	12.5	25
SDR25	25	50
SDR50	50	100
SDR104	104	208
DDR50	50	50 (rising and falling edge)

According to the SD specification

8. Host access specification

The following chapters summarize how the host accesses the card:

- Chapter 8.1 summarizes the SD and SPI buses.
- Chapter 8.2 summarizes the registers.

8.1 SD and SPI Bus Modes

The card supports SD and the SPI Bus modes. Application can chose either one of the modes. Mode selection is transparent to the host. The card automatically detects the mode of the reset command and will expect all further communication to be in the same communication mode. The SD mode uses a 4-bit high performance data transfer, and the SPI mode provides compatible interface to MMC host systems with little redesign, but with a lower performance.

8.1.1 SD Bus Mode Protocol

The SD Bus mode has a single master (host) and multiple slaves (cards) synchronous topology. Clock, power, and ground signals are common to all cards. After power up, the SD Bus mode uses DAT0 only; after initialization, the host can change the cards' bus width from 1 bit (DAT0) to 4 bits (DAT0-DAT3). In high speed mode, only one card can be connected to the bus.
Communication over the SD bus is based on command and data bit streams which are initiated by a start bit and terminated by a stop bit.

- Command: a command is a token which starts an operation. A command is sent from the host either to a single card (addressed command) or to all connected cards (broadcast command). A command is transferred serially on the CMD line.
- Response: a response is a token which is sent from an addressed card, or (synchronously) from all connected cards, to the host as an answer to a previously received command. A response is transferred serially on the CMD line.
- Data: data can be transferred from the card to the host or vice versa. Data is transferred via the data lines.

8.1.2 SPI Bus Mode Protocol

The Serial Peripheral Interface (SPI) Bus is a general purpose synchronous serial interface. The SPI mode consists of a secondary communication protocol. The interface is selected during the first reset command after power up (CMD0) and it cannot be changed once the card is powered on.
While the SD channel is based on command and data bit streams which are initiated by a start bit and terminated by a stop bit, the SPI channel is byte oriented. Every command or data block is built of 8-bit bytes and is byte aligned to the CS signal.
The card identification and addressing methods are replaced by a hardware Chip Select (CS) signal. There are no broadcast commands. For every command, a card (slave) is selected by asserting (active low) the CS signal. The CS signal must be continuously active for the duration of the SPI transaction (command, response and data). The only exception occurs during card programming, when the host can de-assert the CS signal without affecting the programming process.
The bidirectional CMD and DAT lines are replaced by unidirectional dataIn and dataOut signals.

Table 18: SPI Bus signals

Signal	Description
/CS	Host to card chip select
CLK	Host to card clock signal
Data In	Host to card data signal
Data Out	Card to host data signal
Vdd, Vss	Power and ground

8.1.3 Mode Selection

The SD Memory Card wakes up in the SD mode. It will enter SPI mode if the CS signal is asserted (negative) during the reception of the reset command (CMD0) and the card is in idle_state. If the card recognizes that the SD mode is required it will not respond to the command and remain in the SD mode.
If SPI mode is required the card will switch to SPI and respond with the SPI mode R1 response.

The only way to return to the SD mode is by entering the power cycle. In SPI mode the SD Memory Card protocol state machine is not observed. All the SD Memory Card commands supported in SPI mode are always available. During the initialization sequence, if the host gets Illegal Command indication for ACMD41 sent to the card, it may assume that the card is Multimedia Card. In that case it should restart the card as Multimedia Card using CMD0 and CMD1.

8.2 Card Registers

The SD Memory Card has the following registers.

Table 19: SD Memory Card registers

Register name	Bit width	Description	Function
CID	128	Card Identification information	This register contains the card identification information used during the Card Identification phase.
OCR	32	Operation Conditions Registers	This register describes the operating voltage range and contains the status bit in the power supply.
CSD	128	Card specific information	This register provides information on how to access the card content. Some fields of this register are writeable by PROGRAM_CSD (CMD27).
SCR	64	SD Memory Card's Special features	This register provides information on special features.
RCA[15]	16	Relative Card Address	This register carries the card address is SD Card mode.
SSR	512	SD Status	information about the card proprietary features and vendor specific life time information

Table 20: CID register

Register name	Bit width	Description	Function
MID	8	Manufacture ID	0x5d
OID	16	OEM/Application ID	0x5342
PNM	40	Product Name	e.g."AEL10"
PRV	8	Product Revision	0xgg
PSN	32	Product Serial Number	xxxxxxxx
–	4	Reserved	0x0
MDT	12	Manufacture Date	0xyym
CRC	7	Check sum of CID contents	chksum
–	1	Not used; always=1	1

[15] RCA register is not available in SPI mode

Table 21: OCR register

OCR bit positon	VDD voltage windows	Typ. value	OCR bit position	VDD voltage window	Typ. value
0-3	Reserved	0	15	2.7-2.8	1
4	1.6-1.7	0	16	2.8-2.9	1
5	1.7-1.8	0	17	2.9-3.0	1
6	1.8-1.9	0	18	3.0-3.1	1
7	1.9-2.0	0	19	3.1-3.2	1
8	2.0-2.1	0	20	3.2-3.3	1
9	2.1-2.2	0	21	3.3-3.4	1
10	2.2-2.3	0	22	3.4-3.5	1
11	2.3-2.4	0	23	3.5-3.6	1
12	2.4-2.5	0	24	Switching to 1.8V accepted	1
13	2.5-2.6	0	25-29	Reserved	
14	2.6-2.7	0	30	Card Capacity Status (CCS)	*[16]
			31	0=busy; 1=ready	*[17]

Table 22: CSD register

Register name	Bits	Bit width	Description	Typ. value
CSD_STRUCTURE	127:126	2	CSD structure	01
–	125:120	6	Reserved	00000
TAAC	119:112	8	Data read access time 1	00001110
NSAC	111:104	8	Data read access time 2 (CLK cycle)	00000000
TRAN_SPEED	103:96	8	Data transfer rate	00110010 Default speed 00101011 SDR 104 or other values
CCC	95:84	12	Card command classes	010110110101
READ_BL_LEN	83:80	4	Read data block length	1001
READ_BL_PARTIAL	79	1	Partial blocks for read allowed	0
WRITE_BLK_MISALIGN	78	1	Write block misalignment	0
READ_BLK_MISALIGN	77	1	Read block misalignment	0
DSR_IMP	76	1	DSR implemented	0
–	75:70	6	Reserved	000000
C_SIZE	69:48	22	Device size	xxx[18]
–	47	1	Reserved	0
ERASE_BLK_EN	46	1	Erase single block enable	1
SECTOR_SIZE	45:39	7	Erase sector size	1111111
WP_GRP_SIZE	38:32	7	Write protect group size	0000000
WP_GRP_ENABLE	31	1	Write protect group enable	0
–	30:29	2	Reserved	00

[16] This bit is valid only when the card power up status bit is set
[17] This bit is set to LOW if the card has not finished the power up routine
[18] Drive size and block sizes vary with card capacity

R2W_FACTOR	28:26	3	Write speed factor	010
WRITE_BL_LEN	25:22	4	Write data block length	1001^{18}
WRITE_BL_PARTIAL	21	1	Partial blocks for write allowed	0
–	20:16	5	Reserved	00000
FILE_FORMAT_GRP	15	1	File format group	0 W(1)
COPY	14	1	Copy flag	0 W(1)
PERM_WRITE_PROTECT	13	1	Permanent write protection	0 W(1)
TMP_WRITE_PROTECT	12	1	Temporary write protection	0 W
FILE_FORMAT	11:10	2	File format	00 W(1)
–	9:8	2	Reserved	00 W
CRC	7:1	7	Checksum of CSD contents	xxxxxxx
–	0	1	Always=1	1

Memory capacity = (C_SIZE+1) * 512kByte

W value can be changed with CMD27 (PROGRAM_CSD)
W(1) value can be changed ONCE with CMD27 (PROGRAM_CSD)

Table 23: SCR register

Field	Bits	Bit width	Typ. value	Remark
SCR_STRUCTURE	63:60	4	0000	SCR 1.0
SD_SPEC	59:56	4	0010	SD 2.0 or higher
DATA_STAT_AFTER_ERASE	55	1	0	data are 0xFF after erase
SD_SECURITY	54:52	3	000	No security
SD_BUS_WIDTHS	51:48	4	0101	1 or 4 bit
SD_SPEC3	47	1	1	yes
EX_SECURITY	46:43	4	0000	no extended security
SD_SPEC4	42:42	1	1	yes
SD_SPECX	41:38	4	2	Version 6.xx
Reserved	37:36	9	0	
CMD_SUPPORT	35:32	2	11	CMD23 and CMD20 supported
Reserved	31:0	32	0	

Table 24: RCA register

Field	Bits	Bit width
RCA	16	0x0000 / 59b4[19]

[19] After initialization the card can change the RCA register

Table 25: SSR register

Field	Bits	Bit width	Typ. value	Remark
Data bus width	511:510	2	0x2[20]	4 bit width
Secured mode	509:509	1	0x0	not secured
Reserved for security	508:502	7	0x00	-
Reserved	501:496	6	0x00	-
SD card type	495:480	16	0x0000	Regular SD
Size protected area	479:448	32	0x0xxxxxxx	
Speed class	447:440	8	0x04	Class 10
Move performance	439:432	8	0x00	Sequential write
Allocation unit size	431:428	4	0x9	4 MiB
Reserved	427:424	4	0x0	
Erase unit size	423:408	16	0x8	8 AU
Erase unit timeout	407:402	6	0x04	4 seconds
Erase unit offset	401:400	2	0x1	1 second
UHS mode Speed Grade	399:396	4	0x1 / 0x3	UHS Grade 1 / 3
Allocation unit size in UHS mode	395:392	4	0x9	4MB/s
Video Speed Class	391:384	8	0x1e	Video Speed Class 30
Reserved	383:378	6	0x0	
AU size for Video Speed Class	377:368	10	0x8	8 MiB
Suspension Address	367:346	22	0x0	
Reserved	345:340	6	0x0	
Application Performance Class	339:336	4	1 / 2	Class A1 / A2
Performance Enhancement	335:328	8	0x00 / 0xfc	
Reserved	327:314	14	0x0	
Discard support	313:313	1	0x0	Not supported
Full User Area Logical Erase Support	312:312	1	0x0	Not supported

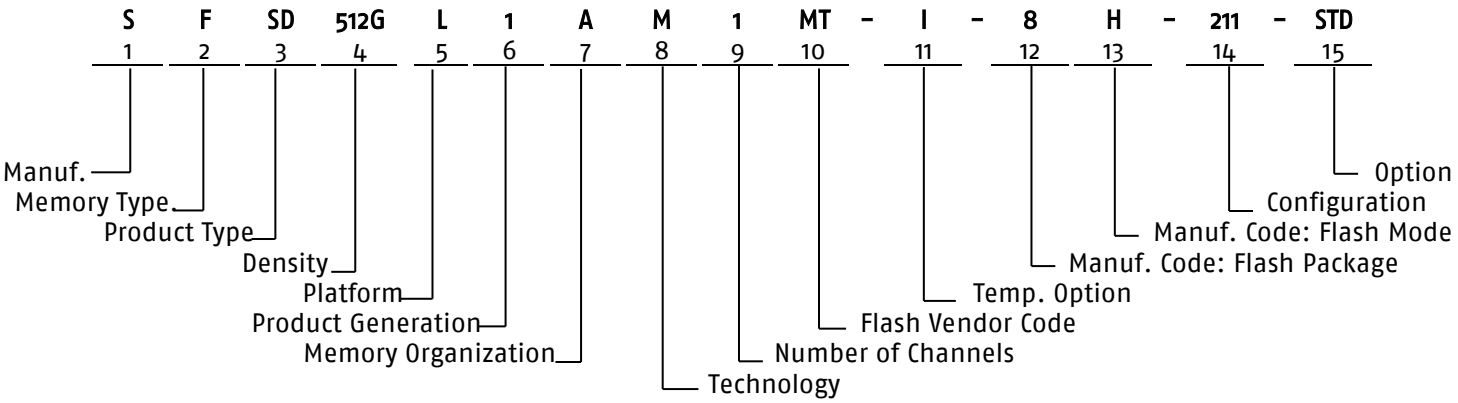
[20] Value change in operation

9. Life Time Monitoring

The products support life time monitoring with a vendor specific SD command CMD56 with argument 0x53420001 (read transfer). CMD56 follows the SD protocol specification and returns 512 bytes of data.
All multi-byte values are in big endian order (most significant byte first).

Field	Bytes	Byte width	Remark
Unique ID	0:7	8	53 77 69 73 73 62 69 74 «Swissbit» in ASCII
Reserved	8:15	8	All 0x00
SD CID Register	16:31	16	See chapter 8.2
Firmware Revision	32:47	16	ASCII Null-Terminated
User Area Rated Cycles	48:51	4	
User Area Max. Cycle Count	52:55	4	
User Area Total Cycle Count	56:59	4	
User Area Average Cycle Count	60:63	4	
Reserved	64:67	4	All 0x00
System Area Max. Cycle Count	68:71	4	
System Area Total Cycle Count	72:75	4	
System Area Average Cycle Count	76:79	4	
Remaining Card Lifetime Percent (user area)	80:80	1	
Reserved	81:85	5	All 0x00
Current SD Card Speed Mode	86:86	1	0x00: Default Speed 0x01: High Speed 0x10: SDR12 0x11: SDR25 0x12: SDR50 0x14: DDR50 0x18: SDR104
Current SD Card Bus Width	87:87	1	0x00: 1 bit width 0x10: 4 bit width
Current Spare Blocks User Area	88:91	4	
Current Spare Blocks System Area	92:95	4	
Runtime Bad Blocks User Area	96:99	4	
Runtime Bad Blocks System Area	100:103	4	
Refresh Count User Area	104:107	4	
Refresh Count System Area	108:111	4	
Host Interface CRC count	112:115	4	
Power Cycle Counter	116:119	4	
Reserved	120:511	392	

10. Part Number Decoder



10.1 Manufacturer

Swissbit code	S

10.2 Memory Type

Flash	F

10.3 Product Type

SD Memory Card	SD

10.4 Density

64 GBytes	064G
128 GBytes	128G
256 GBytes	256G
512 GBytes	512G

10.5 Platform

SD Memory Card	L

10.6 Product Generation

10.7 Memory Organization

x8	A

10.8 Technology

SD Memory Card controller	S-5x Platform	M

10.9 Channels

1 Flash channel	1

10.10 Flash Code

Micron	MT

10.11 Temperature Option

Extended Temp. Range: -25°C to 85°C	E
Industrial Temperature Range: -40 °C to 85 °C	I

10.12 Die Classification

3D TLC MONO (single die package)	5
3D TLC DDP (dual die package)	6
3D TLC QDP (quad die package)	7
3D TLC ODP (oct die package)	8

10.13 Pin Mode

Single nCE & R/nB	E
Dual nCE & R/nB	F
Quad nCE & R/nB	G
Octo nCE & R/nB	H

10.14 Drive configuration XYZ

X = Configuration

Configuration	**X**
UHS-I	2

Y = Firmware Revision

FW Revision	**Y**
High reliability series firmware	1

Z = Feature

Feature	**Z**
Standard	1

10.15 Option

Swissbit / Standard	STD

11. Marking Specification

11.1 Top View

Figure 3: S-55 top view

11.2 Back side marking

Figure 4: S-55 bottom view

Swissbit
Part number

Manufacturing date / Lot code
Made in Germany

CE / WEEE logo

12. Revision History

Table 26: Document Revision History

Date	Revision	Description	Revision Details
22-FEB-2022	1.00	Initial release version	Doc. req. no. 5250
25-MAR-2022	1.01	Updated MTBF value	Doc. req. no. 5322