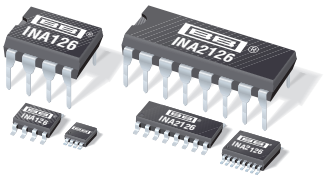


INA126
INA2126

SBOS062A – JANUARY 1996 – REVISED AUGUST 2005

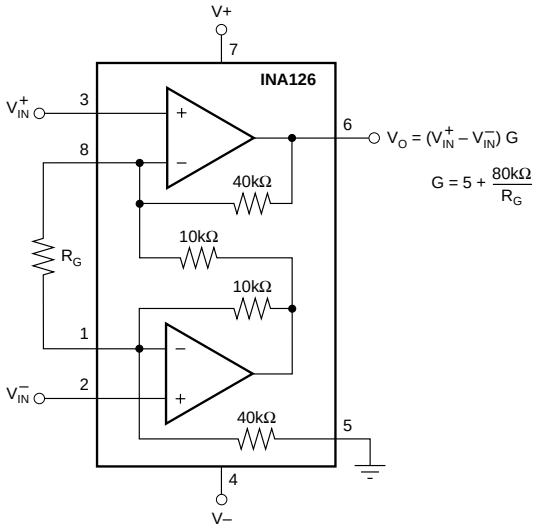
*Micro*POWER INSTRUMENTATION AMPLIFIER
Single and Dual Versions

FEATURES

- **LOW QUIESCENT CURRENT: 175μA/chan.**
- **WIDE SUPPLY RANGE: ±1.35V to ±18V**
- **LOW OFFSET VOLTAGE: 250μV max**
- **LOW OFFSET DRIFT: 3μV/°C max**
- **LOW NOISE: 35nV/√Hz**
- **LOW INPUT BIAS CURRENT: 25nA max**
- **8-PIN DIP, SO-8, MSOP-8 SURFACE- MOUNT DUAL: 16-Pin DIP, SO-16, SSOP-16**

APPLICATIONS

- **INDUSTRIAL SENSOR AMPLIFIER: Bridge, RTD, Thermocouple**
- **PHYSIOLOGICAL AMPLIFIER: ECG, EEG, EMG**
- **MULTI-CHANNEL DATA ACQUISITION**
- **PORTABLE, BATTERY OPERATED SYSTEMS**

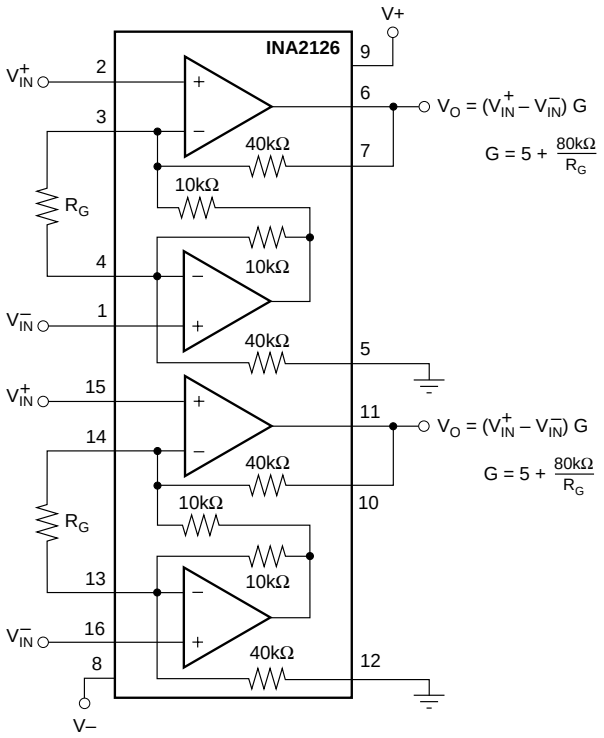


DESCRIPTION

The INA126 and INA2126 are precision instrumentation amplifiers for accurate, low noise differential signal acquisition. Their two-op-amp design provides excellent performance with very low quiescent current (175μA/channel). This, combined with a wide operating voltage range of ±1.35V to ±18V, makes them ideal for portable instrumentation and data acquisition systems.

Gain can be set from 5V/V to 10000V/V with a single external resistor. Laser trimmed input circuitry provides low offset voltage (250μV max), low offset voltage drift (3μV/°C max) and excellent common-mode rejection.

Single version package options include 8-pin plastic DIP, SO-8 surface mount, and fine-pitch MSOP-8 surface-mount. Dual version is available in the space-saving SSOP-16 fine-pitch surface mount, SO-16, and 16-pin DIP. All are specified for the –40°C to +85°C industrial temperature range.



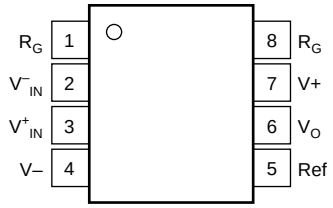
ABSOLUTE MAXIMUM RATINGS[1]

Power Supply Voltage, V+ to V–	36V
Input Signal Voltage[2]	(V–)–0.7 to (V+)+0.7V
Input Signal Current[2]	10mA
Output Short Circuit	Continuous
Operating Temperature	–55°C to +125°C
Storage Temperature	–55°C to +125°C
Lead Temperature (soldering, 10s)	+300°C

NOTES: (1) Stresses above these ratings may cause permanent damage. (2) Input signal voltage is limited by internal diodes connected to power supplies. See text.

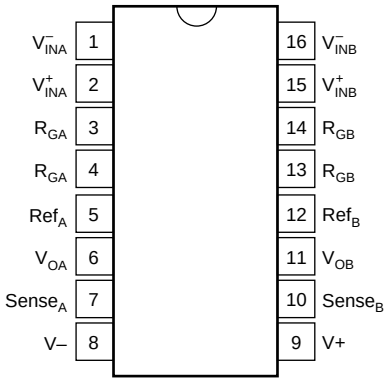
PIN CONFIGURATION (Single)

Top View **8-Pin DIP, SO-8, MSOP-8**



PIN CONFIGURATION (Dual)

Top View **16-Pin DIP, SO-16, SSOP-16**



ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION

PRODUCT	PACKAGE-LEAD	PACKAGE MARKING
Single		
INA126PA INA126P	DIP-8 DIP-8	INA126PA INA126P
INA126UA INA126U	SO-8 SO-8	INA126UA INA126U
INA126EA[2] " INA126E[2] "	MSOP-8 " MSOP-8 "	A26[3] " A26[3] "
Dual		
INA2126PA INA2126P	DIP-16 DIP-16	INA2126PA INA2126P
INA2126UA INA2126U	SO-16 SO-16	INA2126UA INA2126U
INA2126EA[2] " INA2126E[2] "	SSOP-16 " SSOP-16 "	INA2126EA " INA2126E "

NOTES: (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com. (2) MSOP-8 and SSOP-16 packages are available only on 250 or 2500 piece reels. (3) Grade designation is marked on reel.

ELECTRICAL CHARACTERISTICS

At T_A = +25°C, V_S = ±15V, R_L = 25kΩ, unless otherwise noted.

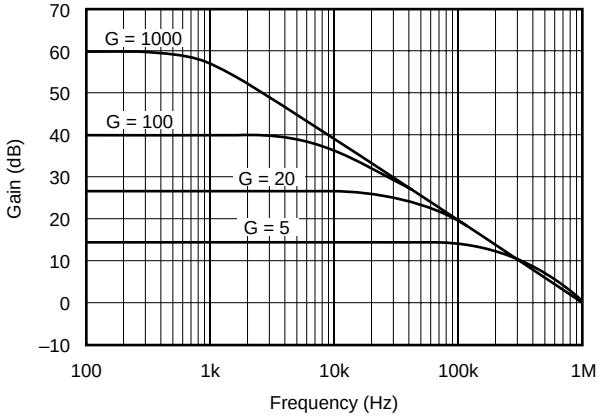
PARAMETER	CONDITIONS	INA126P, U, E INA2126P, U, E MIN	TYP	MAX	INA126PA, UA, EA INA2126PA, UA, EA MIN	TYP	MAX	UNITS
INPUT								
Offset Voltage, RTI			±100	±250		±150	±500	µV
vs Temperature			±0.5	±3		*	±5	µV/°C
vs Power Supply (PSRR)	V_S = ±1.35V to ±18V		5	15		*	50	µV/V
Input Impedance			10^9 || 4			*		Ω || pF
Safe Input Voltage	R_S = 0	(V–)–0.5		(V+)+0.5	*		*	V
	R_S = 1kΩ	(V–)–10		(V+)+10	*		*	V
Common-Mode Voltage Range	V_O = 0V	±11.25	±11.5		*	*		V
Channel Separation (dual)	G = 5, dc		130					dB
Common-Mode Rejection	R_S = 0, V_{CM} = ±11.25V	83	94		74	90		dB
INA2126U (dual SO-16)		80	94					dB
INPUT BIAS CURRENT			–10	–25		*	–50	nA
vs Temperature			±30			*		pA/°C
Offset Current			±0.5	±2		*	±5	nA
vs Temperature			±10			*		pA/°C
GAIN			G = 5 to 10k			*		V/V
Gain Equation			$G = 5 + 80k\Omega/R_G$			*		V/V
Gain Error	V_O = ±14V, G = 5		±0.02	±0.1		*	±0.18	%
vs Temperature	G = 5		±2	±10		*	*	ppm/°C
Gain Error	V_O = ±12V, G = 100		±0.2	±0.5		*	±1	%
vs Temperature	G = 100		±25	±100		*	*	ppm/°C
Nonlinearity	G = 100, V_O = ±14V		±0.002	±0.012		*	*	%
NOISE								
Voltage Noise, f = 1kHz			35			*		$nV/\sqrt{Hz}$
f = 100Hz			35			*		$nV/\sqrt{Hz}$
f = 10Hz			45			*		$nV/\sqrt{Hz}$
f_B = 0.1Hz to 10Hz			0.7			*		μV_{PP}
Current Noise, f = 1kHz			60			*		$fA/\sqrt{Hz}$
f_B = 0.1Hz to 10Hz			2			*		pA_{PP}
OUTPUT								
Voltage, Positive	R_L = 25kΩ	(V+)–0.9	(V+)–0.75		*	*		V
Negative	R_L = 25kΩ	(V–)+0.95	(V–)+0.8		*	*		V
Short-Circuit Current	Short-Circuit to Ground		+10/–5			*		mA
Capacitive Load Drive			1000			*		pF
FREQUENCY RESPONSE								
Bandwidth, –3dB	G = 5		200			*		kHz
	G = 100		9			*		kHz
	G = 500		1.8			*		kHz
Slew Rate	V_O = ±10V, G = 5		0.4			*		V/µs
Settling Time, 0.01%	10V Step, G = 5		30			*		µs
	10V Step, G = 100		160			*		µs
	10V Step, G = 500		1500			*		µs
Overload Recovery	50% Input Overload		4			*		µs
POWER SUPPLY								
Voltage Range		±1.35	±15	±18	*	*	*	V
Current (per channel)	I_O = 0		±175	±200		*	*	µA
TEMPERATURE RANGE								
Specification Range		–40		+85	*		*	°C
Operation Range		–55		+125	*		*	°C
Storage Range		–55		+125	*		*	°C
Thermal Resistance, θ_{JA}								
8-Pin DIP			100			*		°C/W
SO-8 Surface-Mount			150			*		°C/W
MSOP-8 Surface-Mount			200			*		°C/W
16-Pin DIP (dual)			80			*		°C/W
SO-16 (dual)			100			*		°C/W
SSOP-16 (dual)			100			*		°C/W

* Specification same as INA126P, INA126U, INA126E; INA2126P, INA2126U, INA2126E.

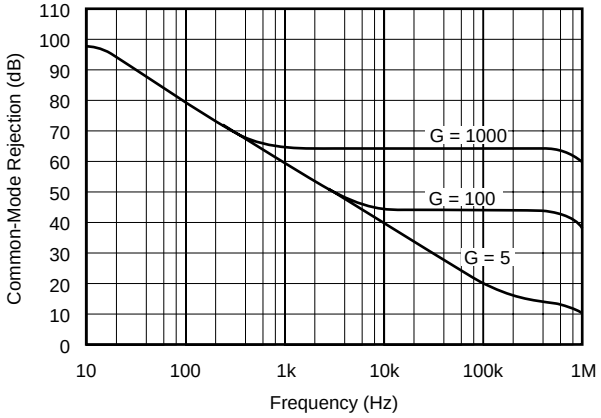
TYPICAL CHARACTERISTICS

At T_A = +25°C and V_S = ±15V, unless otherwise noted.

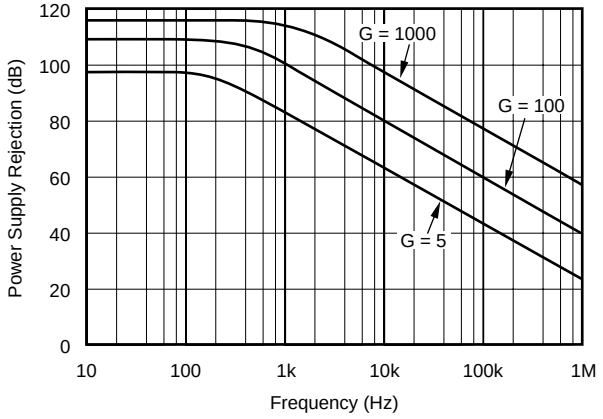
GAIN vs FREQUENCY



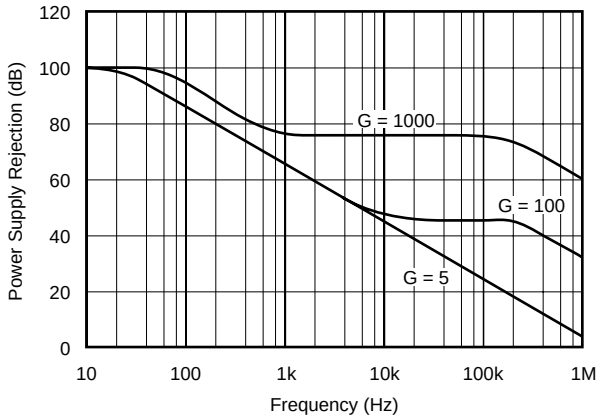
COMMON-MODE REJECTION vs FREQUENCY



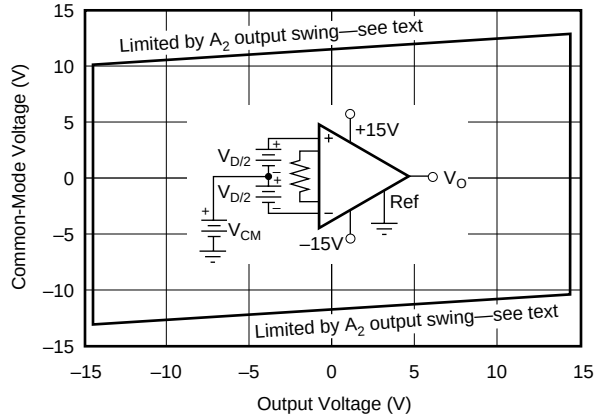
POSITIVE POWER SUPPLY REJECTION vs FREQUENCY



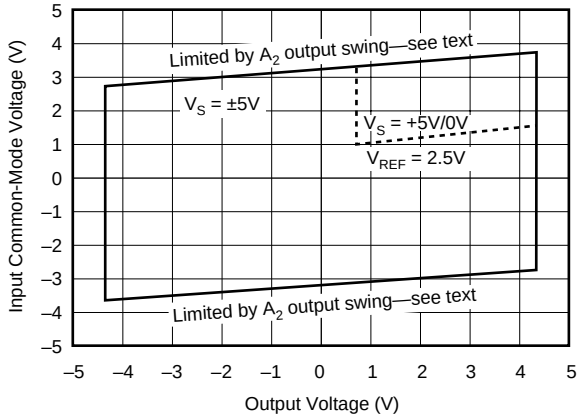
NEGATIVE POWER SUPPLY REJECTION vs FREQUENCY



INPUT COMMON-MODE RANGE vs OUTPUT VOLTAGE, V_S = ±15V



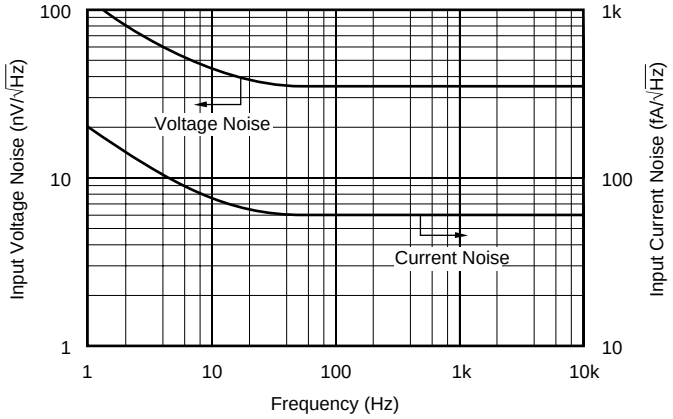
INPUT COMMON-MODE VOLTAGE RANGE vs OUTPUT VOLTAGE, V_S = ±5V



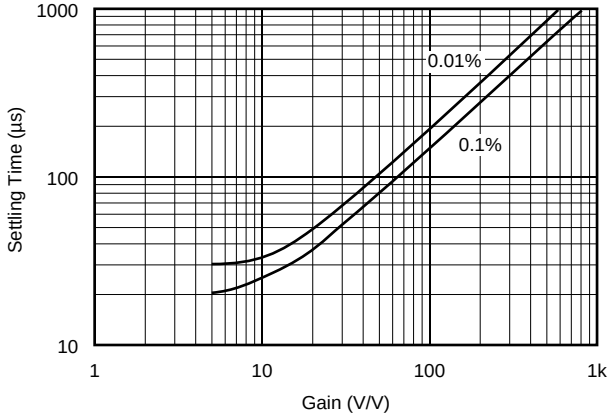
TYPICAL CHARACTERISTICS (Cont.)

At T_A = +25°C and V_S = ±15V, unless otherwise noted.

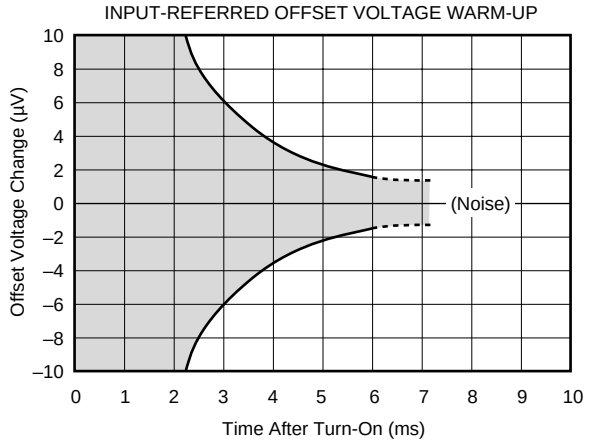
INPUT-REFERRED NOISE vs FREQUENCY



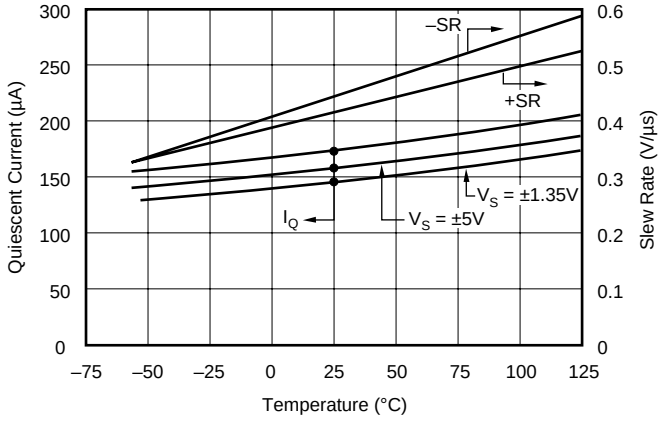
SETTLING TIME vs GAIN



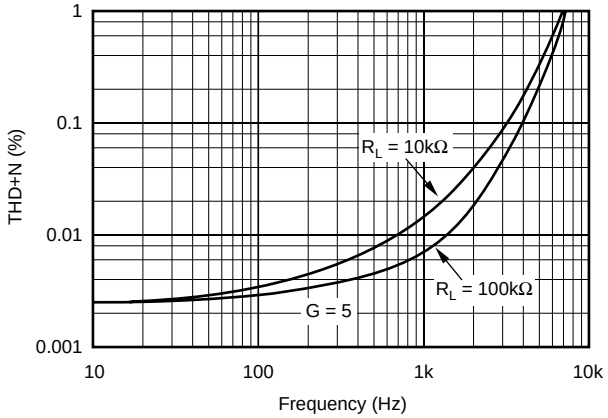
INPUT-REFERRED OFFSET VOLTAGE WARM-UP



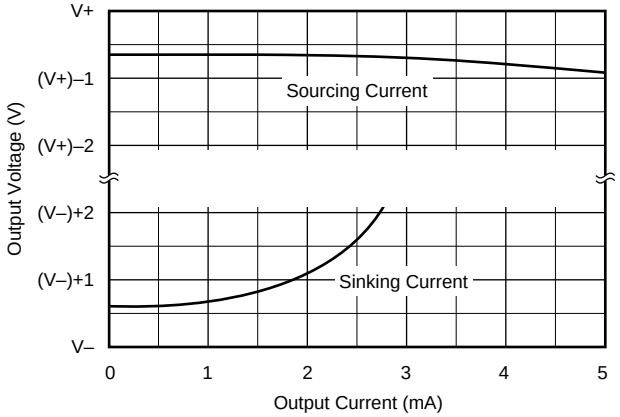
QUIESCENT CURRENT AND SLEW RATE vs TEMPERATURE



TOTAL HARMONIC DISTORTION+NOISE vs FREQUENCY



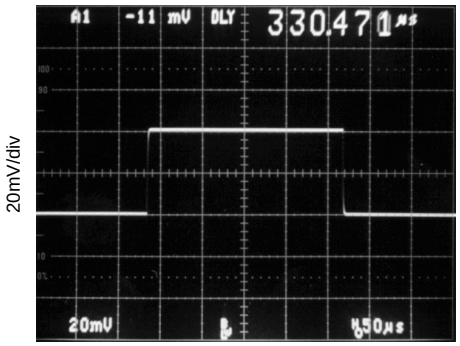
OUTPUT VOLTAGE SWING vs OUTPUT CURRENT



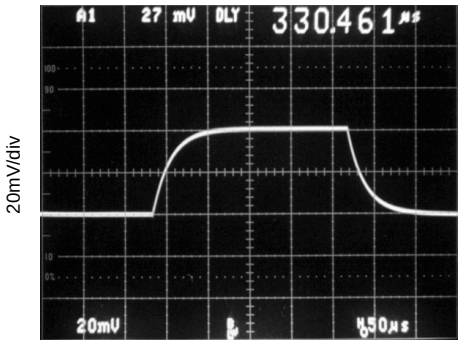
TYPICAL CHARACTERISTICS (Cont.)

At T_A = +25°C and V_S = ±15V, unless otherwise noted.

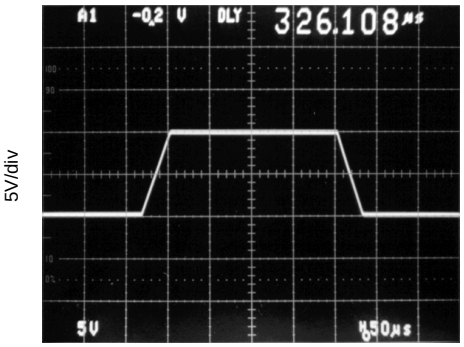
SMALL-SIGNAL RESPONSE, G = 5



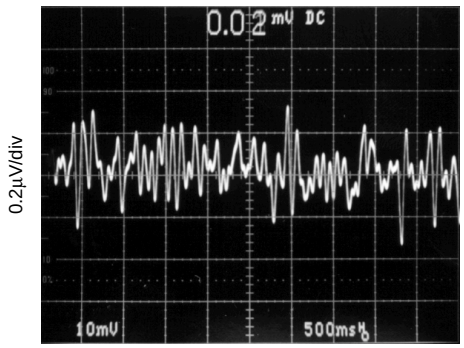
SMALL-SIGNAL RESPONSE, G = 100



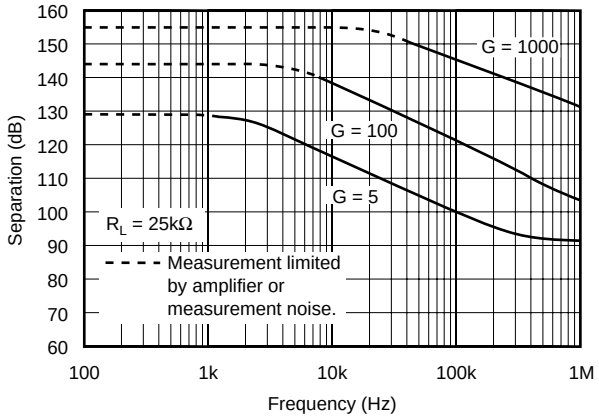
LARGE-SIGNAL RESPONSE, G = 5



VOLTAGE NOISE, 0.1Hz to 10Hz



CHANNEL SEPARATION vs FREQUENCY, RTI
(Dual Version)



APPLICATION INFORMATION

Figure 1 shows the basic connections required for operation of the INA126. Applications with noisy or high impedance power supplies may require decoupling capacitors close to the device pins as shown.

The output is referred to the output reference (Ref) terminal which is normally grounded. This must be a low-impedance connection to ensure good common-mode rejection. A resistance of 8Ω in series with the Ref pin will cause a typical device to degrade to approximately 80dB CMR.

Dual versions (INA2126) have feedback sense connections, $Sense_A$ and $Sense_B$. These must be connected to their respective output terminals for proper operation. The sense connection can be used to sense the output voltage directly at the load for best accuracy.

SETTING THE GAIN

Gain is set by connecting an external resistor, R_G, as shown:

$$G = 5 + \frac{80k\Omega}{R_G} \quad (1)$$

Commonly used gains and R_G resistor values are shown in Figure 1.

The 80kΩ term in equation 1 comes from the internal metal film resistors which are laser trimmed to accurate absolute values. The accuracy and temperature coefficient of these resistors are included in the gain accuracy and drift specifications.

The stability and temperature drift of the external gain setting resistor, R_G, also affects gain. R_G's contribution to gain accuracy and drift can be directly inferred from the gain equation (1). Low resistor values required for high gain can make wiring resistance important. Sockets add to the wiring resistance, which will contribute additional gain error in gains of approximately 100 or greater.

OFFSET TRIMMING

The INA126 and INA2126 are laser trimmed for low offset voltage and offset voltage drift. Most applications require no external offset adjustment. Figure 2 shows an optional circuit for trimming the output offset voltage. The voltage applied to the Ref terminal is added to the output signal. An op amp buffer is used to provide low impedance at the Ref terminal to preserve good common-mode rejection.

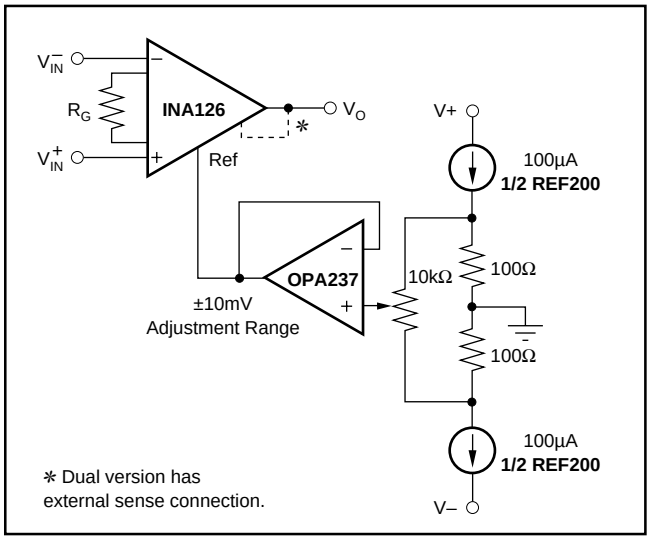
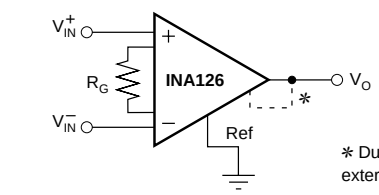
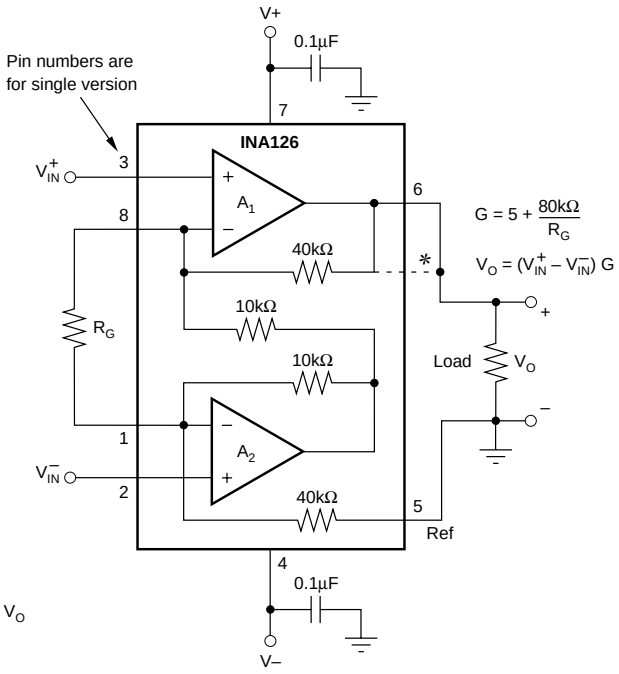


FIGURE 2. Optional Trimming of Output Offset Voltage.

DESIRED GAIN (V/V)	R_G (Ω)	NEAREST 1% R_G VALUE
5	NC	NC
10	16k	15.8k
20	5333	5360
50	1779	1780
100	842	845
200	410	412
500	162	162
1000	80.4	80.6
2000	40.1	40.2
5000	16.0	15.8
10000	8.0	7.87

NC: No Connection.





* Dual version has external sense connection.

FIGURE 1. Basic Connections.

INPUT BIAS CURRENT RETURN

The input impedance of the INA126/2126 is extremely high—approximately $10^9\Omega$. However, a path must be provided for the input bias current of both inputs. This input bias current is typically –10nA (current flows out of the input terminals). High input impedance means that this input bias current changes very little with varying input voltage.

Input circuitry must provide a path for this input bias current for proper operation. Figure 3 shows various provisions for an input bias current path. Without a bias current path, the inputs will float to a potential which exceeds the common-mode range and the input amplifiers will saturate.

If the differential source resistance is low, the bias current return path can be connected to one input (see the thermocouple example in Figure 3). With higher source impedance, using two equal resistors provides a balanced input with advantages of lower input offset voltage due to bias current and better high-frequency common-mode rejection.

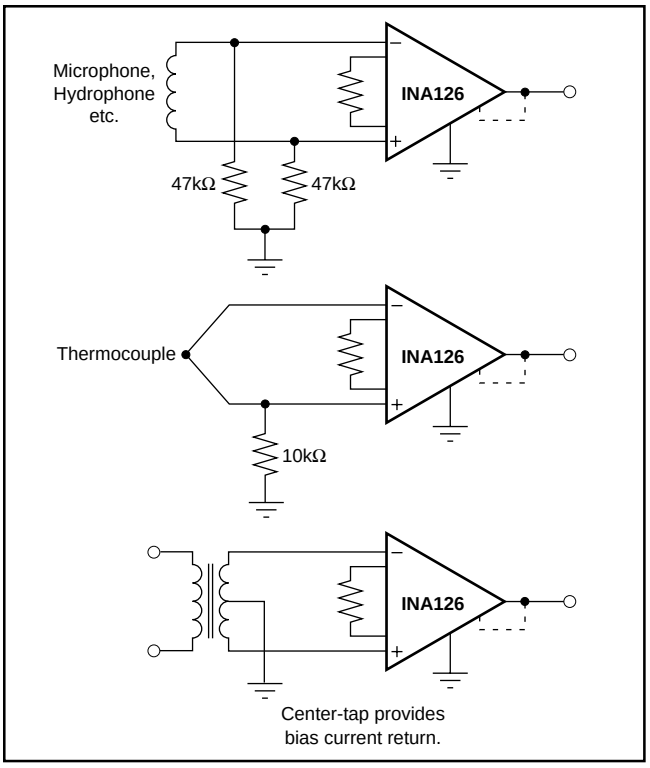


FIGURE 3. Providing an Input Common-Mode Current Path.

INPUT COMMON-MODE RANGE

The input common-mode range of the INA126/2126 is shown in the typical characteristic curves. The common-mode range is limited on the negative side by the output voltage swing of A_2, an internal circuit node that cannot be measured on an external pin. The output voltage of A_2 can be expressed as:

$$V_{O2} = 1.25\ V_{IN}^- - (V_{IN}^+ - V_{IN}^-)\ (10k\Omega/R_G) \qquad (2)$$

(Voltages referred to Ref terminal, pin 5)

The internal op amp A_2 is identical to A_1 and its output swing is limited to typically 0.7V from the supply rails. When the input common-mode range is exceeded (A_2's output is saturated), A_1 can still be in linear operation and respond to changes in the non-inverting input voltage. The output voltage, however, will be invalid.

LOW VOLTAGE OPERATION

The INA126/2126 can be operated on power supplies as low as ±1.35V. Performance remains excellent with power supplies ranging from ±1.35V to ±18V. Most parameters vary only slightly throughout this supply voltage range—see typical characteristic curves. Operation at very low supply voltage requires careful attention to ensure that the common-mode voltage remains within its linear range. See "Input Common-Mode Voltage Range."

The INA126/2126 can be operated from a single power supply with careful attention to input common-mode range, output voltage swing of both op amps and the voltage applied to the Ref terminal. Figure 4 shows a bridge amplifier circuit operated from a single +5V power supply. The bridge provides an input common-mode voltage near 2.5V, with a relatively small differential voltage.

INPUT PROTECTION

The inputs are protected with internal diodes connected to the power supply rails. These diodes will clamp the applied signal to prevent it from exceeding the power supplies by more than approximately 0.7V. If the signal source voltage can exceed the power supplies, the source current should be limited to less than 10mA. This can generally be done with a series resistor. Some signal sources are inherently current-limited and do not require limiting resistors.

CHANNEL CROSSTALK—DUAL VERSION

The two channels of the INA2126 are completely independent, including all bias circuitry. At DC and low frequency there is virtually no signal coupling between channels. Crosstalk increases with frequency and is dependent on circuit gain, source impedance and signal characteristics.

As source impedance increases, careful circuit layout will help achieve lowest channel crosstalk. Most crosstalk is produced by capacitive coupling of signals from one channel to the input section of the other channel. To minimize coupling, separate the input traces as far as practical from any signals associated with the opposite channel. A grounded guard trace surrounding the inputs helps reduce stray coupling between channels. Carefully balance the stray capacitance of each input to ground, and run the differential inputs of each channel parallel to each other, or directly adjacent on top and bottom side of a circuit board. Stray coupling then tends to produce a common-mode signal that is rejected by the IA's input.

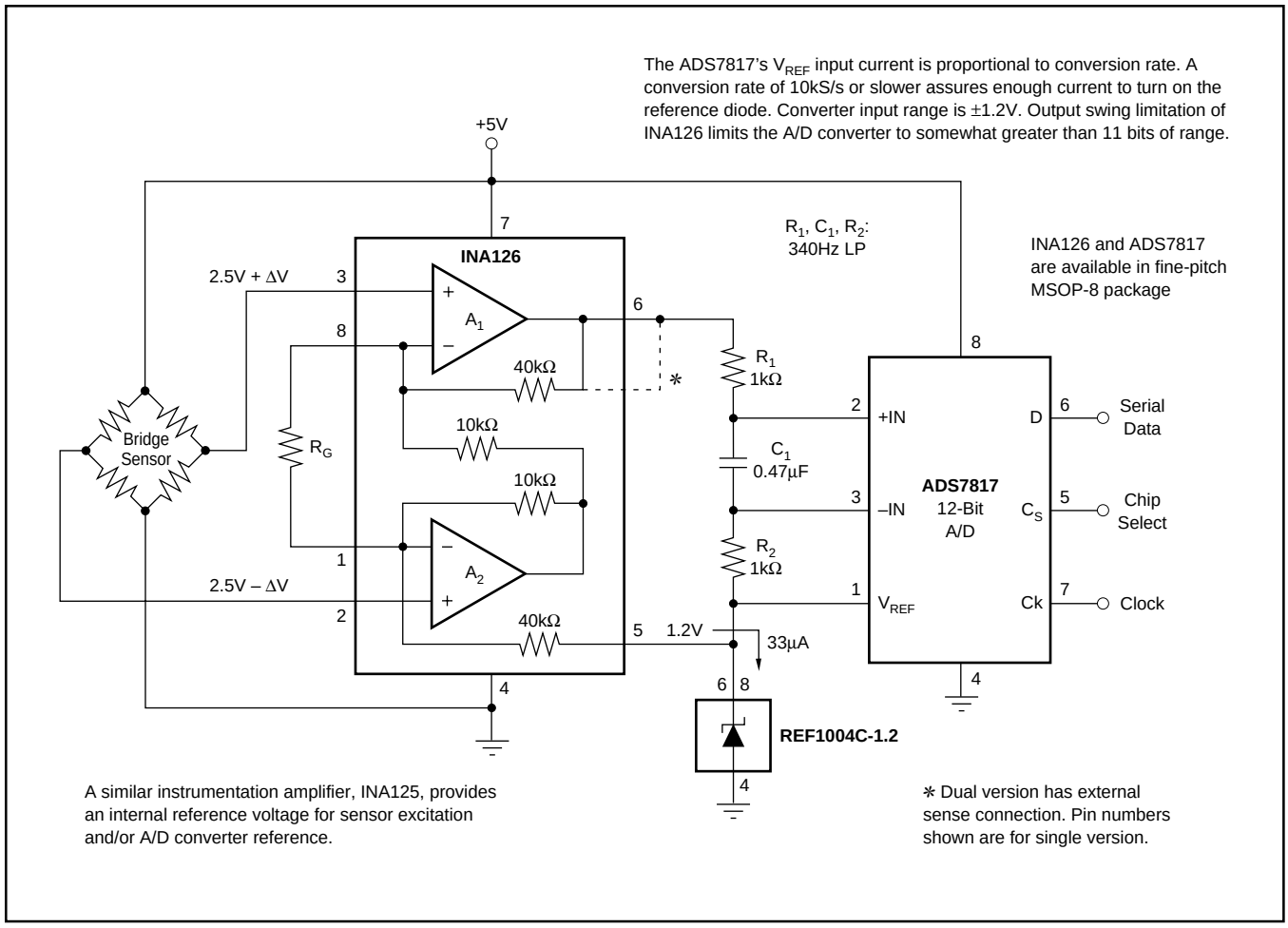
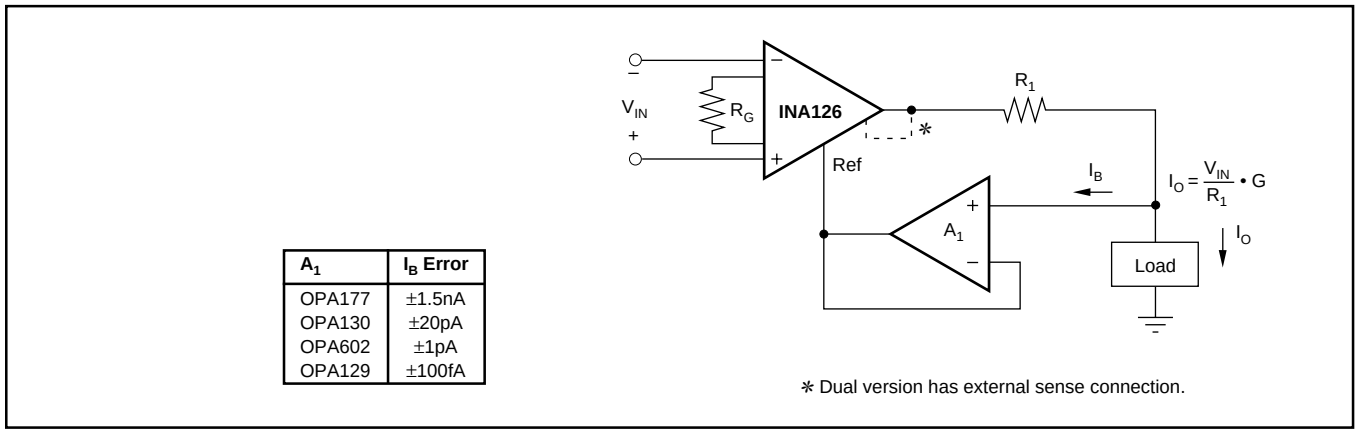


FIGURE 4. Bridge Signal Acquisition—Single 5V Supply.



A_1	I_B Error
OPA177	±1.5nA
OPA130	±20pA
OPA602	±1pA
OPA129	±100fA

FIGURE 5. Differential Voltage-to-Current Converter.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
INA126E/250	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU | CU NIPDAUAG	Level-2-260C-1 YEAR		A26	Samples
INA126E/250G4	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR		A26	Samples
INA126E/2K5	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU | CU NIPDAUAG	Level-2-260C-1 YEAR		A26	Samples
INA126E/2K5G4	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR		A26	Samples
INA126EA/250	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU | CU NIPDAUAG	Level-2-260C-1 YEAR		A26	Samples
INA126EA/250G4	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR		A26	Samples
INA126EA/2K5	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU | CU NIPDAUAG	Level-2-260C-1 YEAR		A26	Samples
INA126EA/2K5G4	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR		A26	Samples
INA126P	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type		INA126P	Samples
INA126PA	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type		INA126P A	Samples
INA126PAG4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type		INA126P A	Samples
INA126PG4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type		INA126P	Samples
INA126U	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR		INA 126U	Samples
INA126U/2K5	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR		INA 126U	Samples
INA126U/2K5G4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR		INA 126U	Samples
INA126UA	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR		INA 126U A	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
INA126UA/2K5	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR		INA 126U A	Samples
INA126UAG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR		INA 126U A	Samples
INA126UG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR		INA 126U	Samples
INA2126E/250	ACTIVE	SSOP	DBQ	16	250	Green (RoHS & no Sb/Br)	Call TI	Level-3-260C-168 HR		INA 2126E A	Samples
INA2126E/250G4	ACTIVE	SSOP	DBQ	16	250	Green (RoHS & no Sb/Br)	Call TI	Level-3-260C-168 HR		INA 2126E A	Samples
INA2126E/2K5	ACTIVE	SSOP	DBQ	16	2500	Green (RoHS & no Sb/Br)	Call TI	Level-3-260C-168 HR		INA 2126E A	Samples
INA2126E/2K5G4	ACTIVE	SSOP	DBQ	16	2500	Green (RoHS & no Sb/Br)	Call TI	Level-3-260C-168 HR		INA 2126E A	Samples
INA2126EA/250	ACTIVE	SSOP	DBQ	16	250	Green (RoHS & no Sb/Br)	Call TI	Level-3-260C-168 HR		INA 2126E A	Samples
INA2126EA/250G4	ACTIVE	SSOP	DBQ	16	250	Green (RoHS & no Sb/Br)	Call TI	Level-3-260C-168 HR		INA 2126E A	Samples
INA2126EA/2K5	ACTIVE	SSOP	DBQ	16	2500	Green (RoHS & no Sb/Br)	Call TI	Level-3-260C-168 HR		INA 2126E A	Samples
INA2126P	ACTIVE	PDIP	N	16	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type		INA2126P	Samples
INA2126PA	ACTIVE	PDIP	N	16	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type		INA2126P A	Samples
INA2126PAG4	ACTIVE	PDIP	N	16	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type		INA2126P A	Samples
INA2126PG4	ACTIVE	PDIP	N	16	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type		INA2126P	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
INA2126U	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR		INA2126U	Samples
INA2126UA	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	INA2126U A	Samples
INA2126UA/2K5	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	INA2126U A	Samples
INA2126UAE4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	INA2126U A	Samples
INA2126UAG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	INA2126U A	Samples
INA2126UE4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR		INA2126U	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

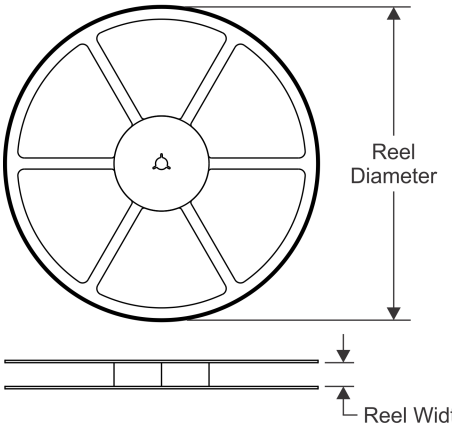
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

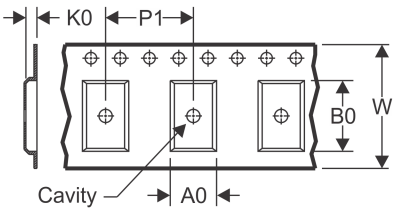
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

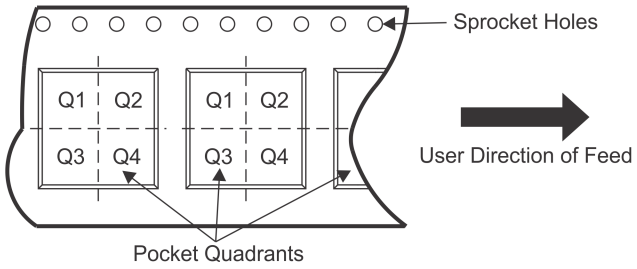


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

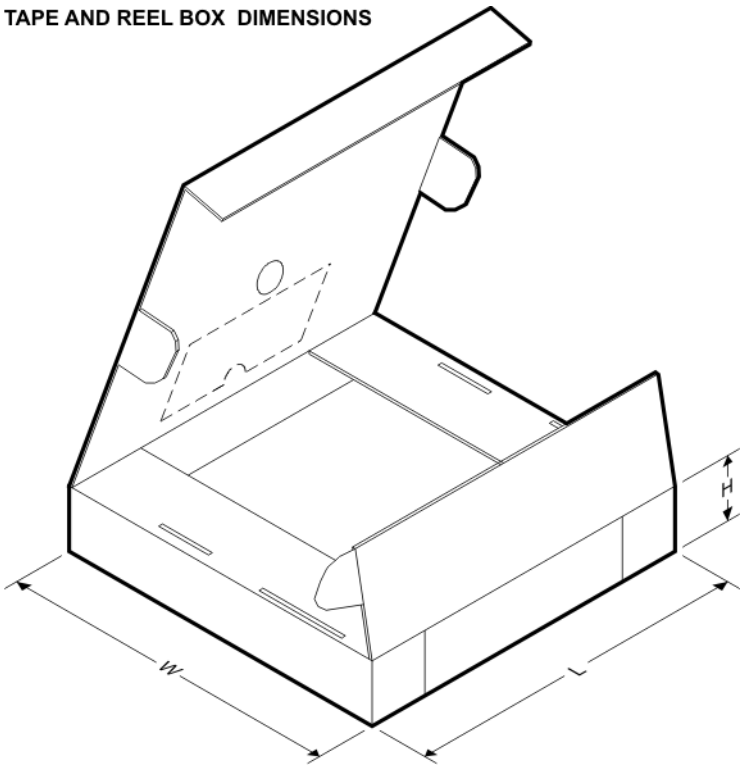
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
INA126E/250	VSSOP	DGK	8	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
INA126E/2K5	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
INA126EA/250	VSSOP	DGK	8	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
INA126EA/2K5	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
INA126U/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
INA126UA/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
INA2126UA/2K5	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1

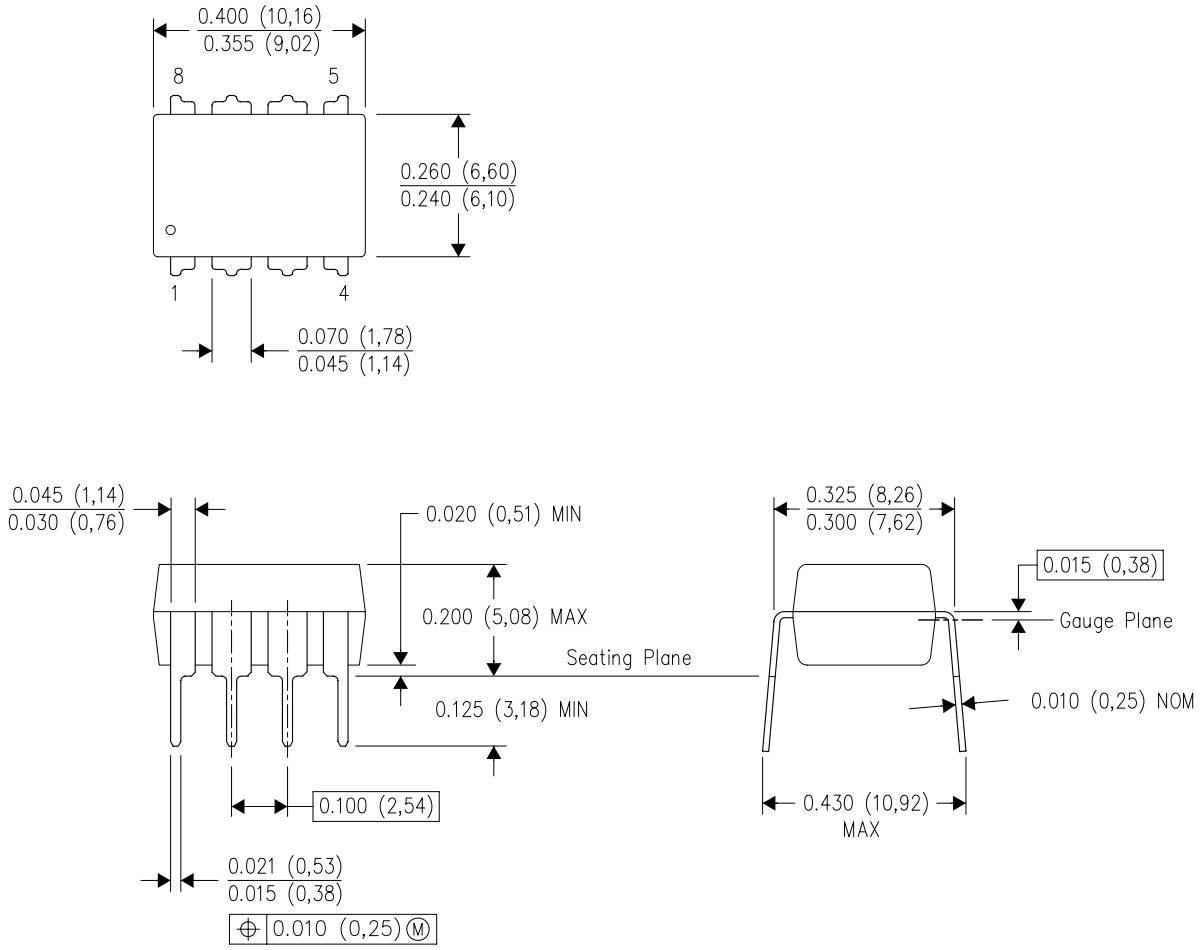
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

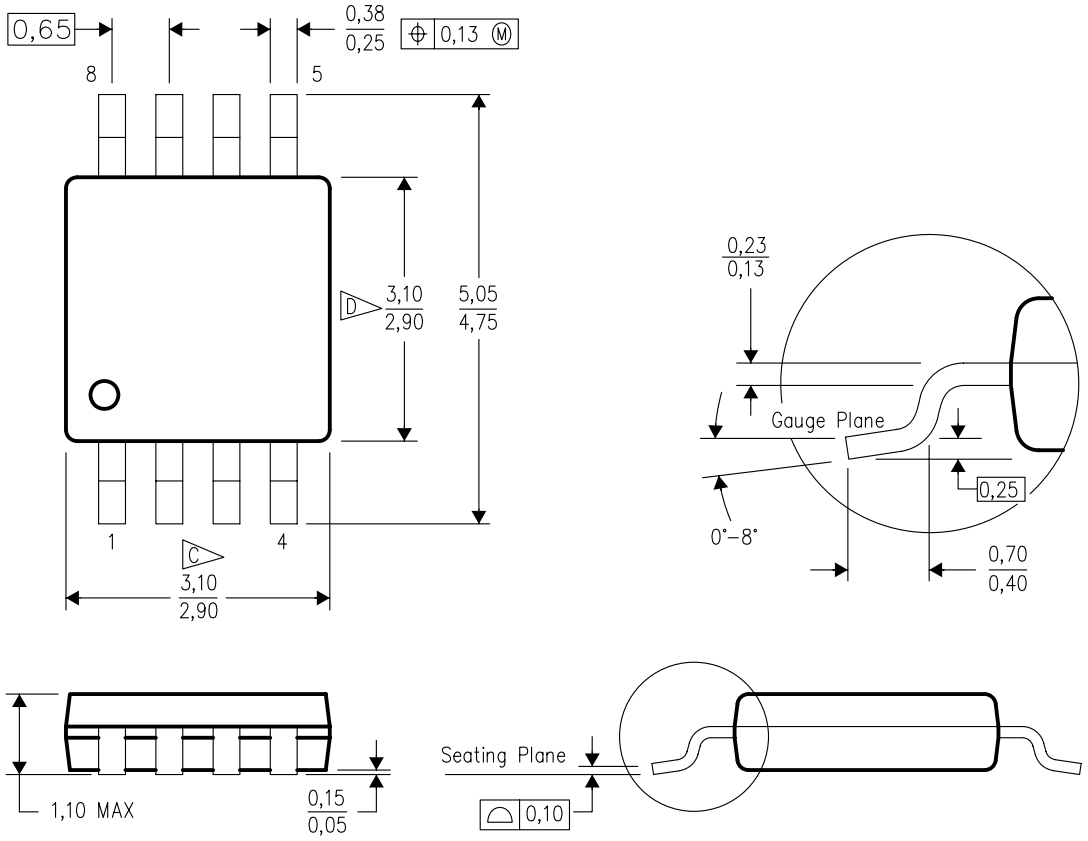
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
INA126E/250	VSSOP	DGK	8	250	210.0	185.0	35.0
INA126E/2K5	VSSOP	DGK	8	2500	367.0	367.0	35.0
INA126EA/250	VSSOP	DGK	8	250	210.0	185.0	35.0
INA126EA/2K5	VSSOP	DGK	8	2500	367.0	367.0	35.0
INA126U/2K5	SOIC	D	8	2500	367.0	367.0	35.0
INA126UA/2K5	SOIC	D	8	2500	367.0	367.0	35.0
INA2126UA/2K5	SOIC	D	16	2500	367.0	367.0	38.0

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



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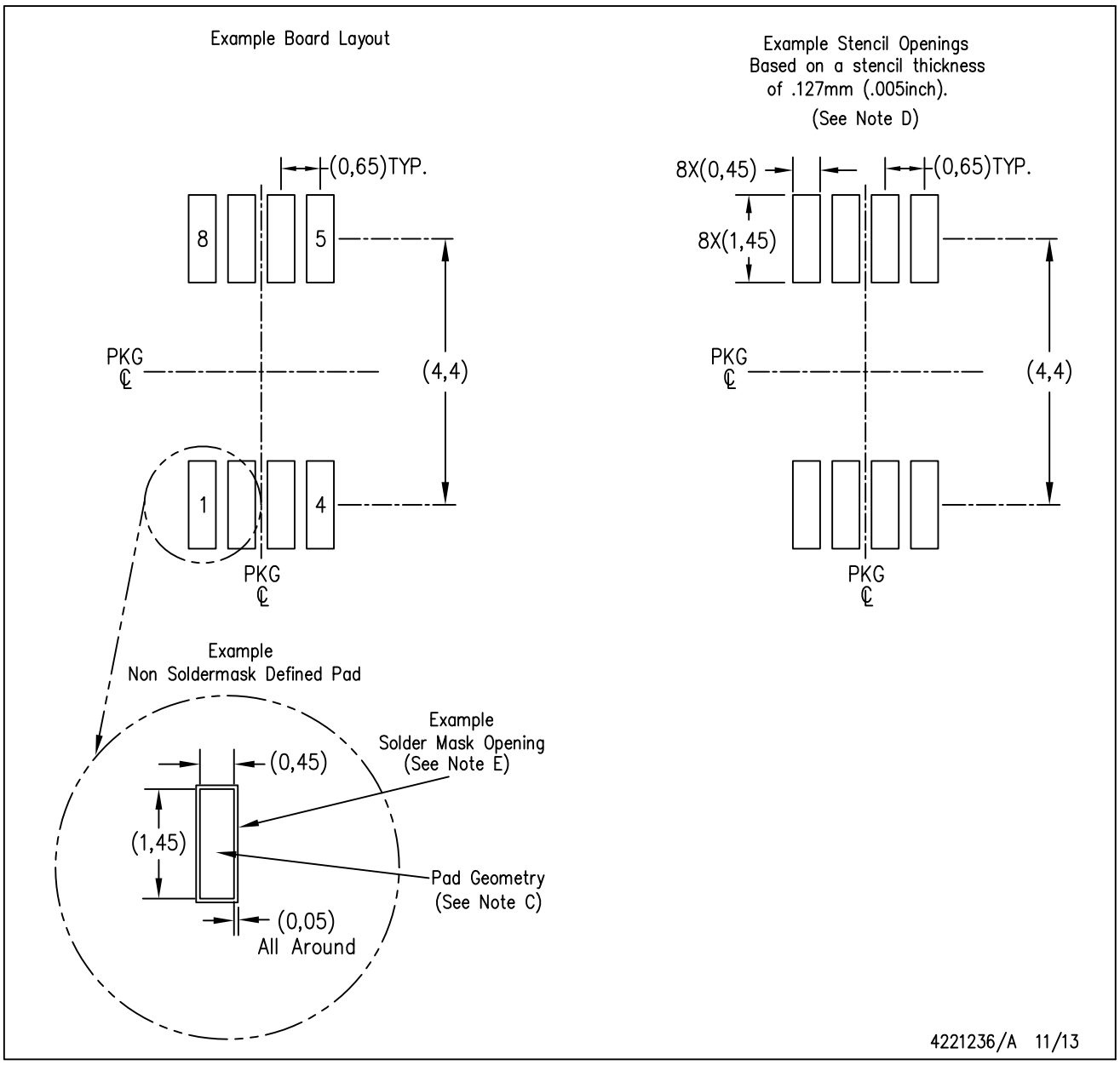
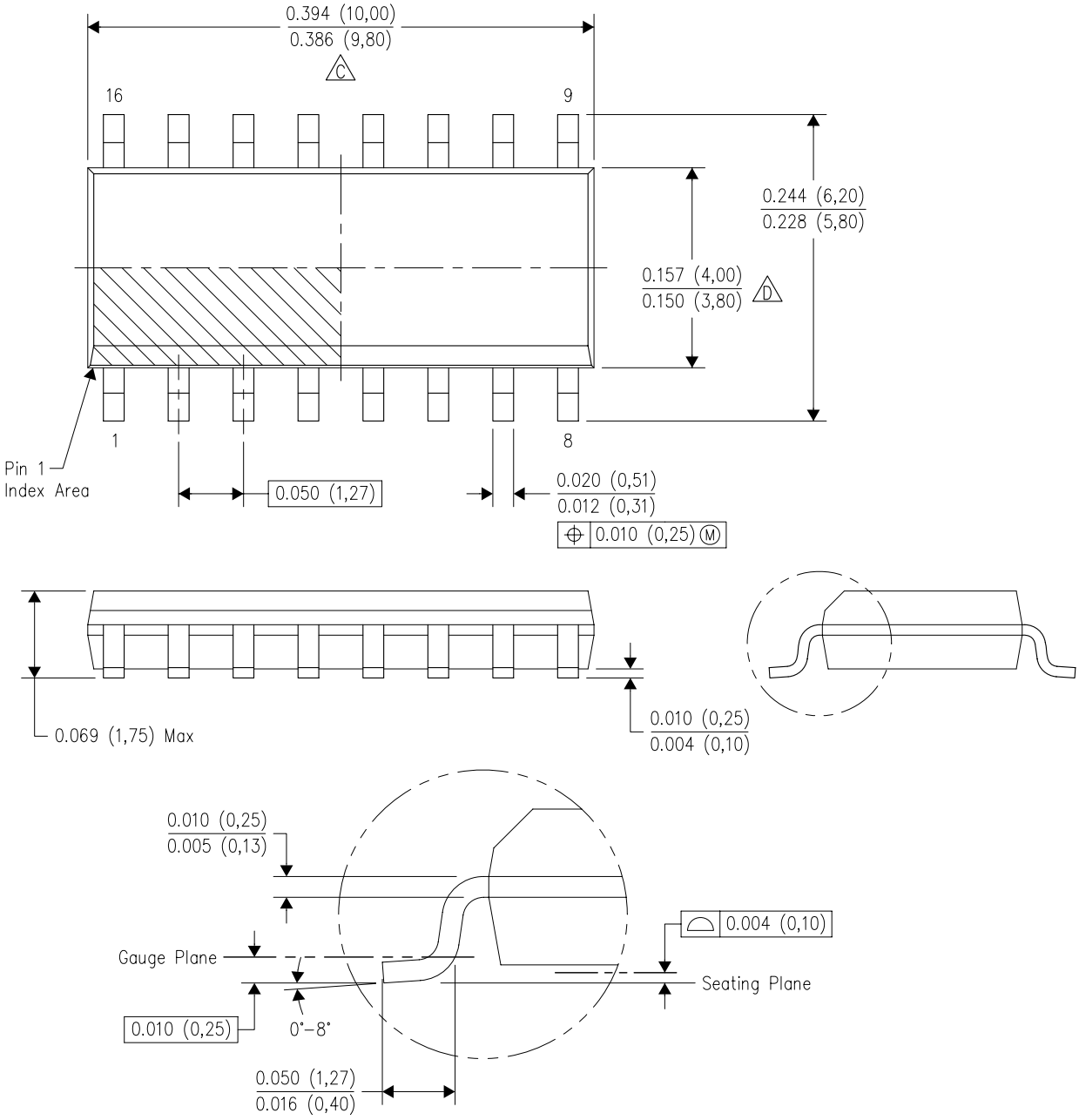
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

DGK (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE



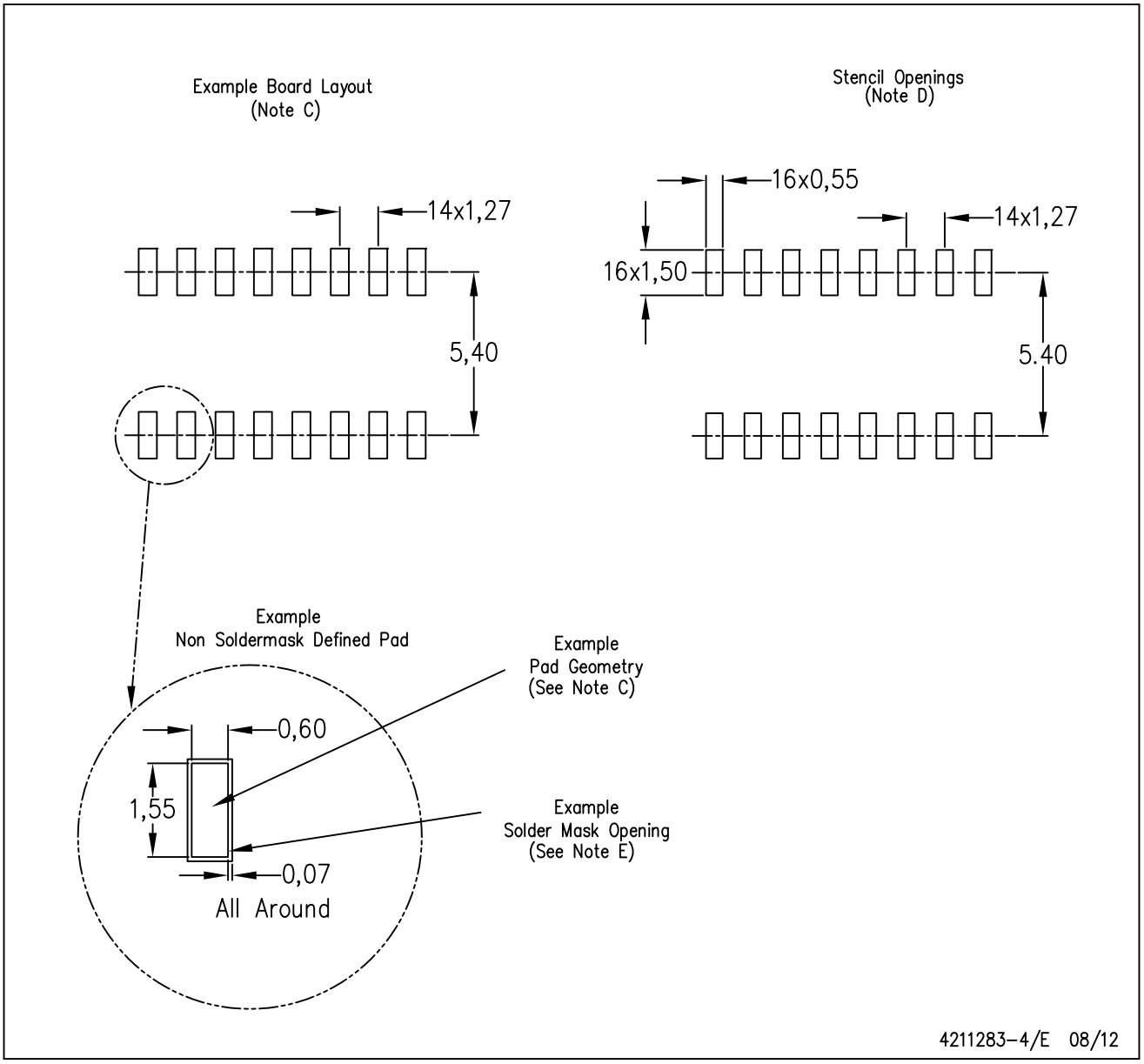
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



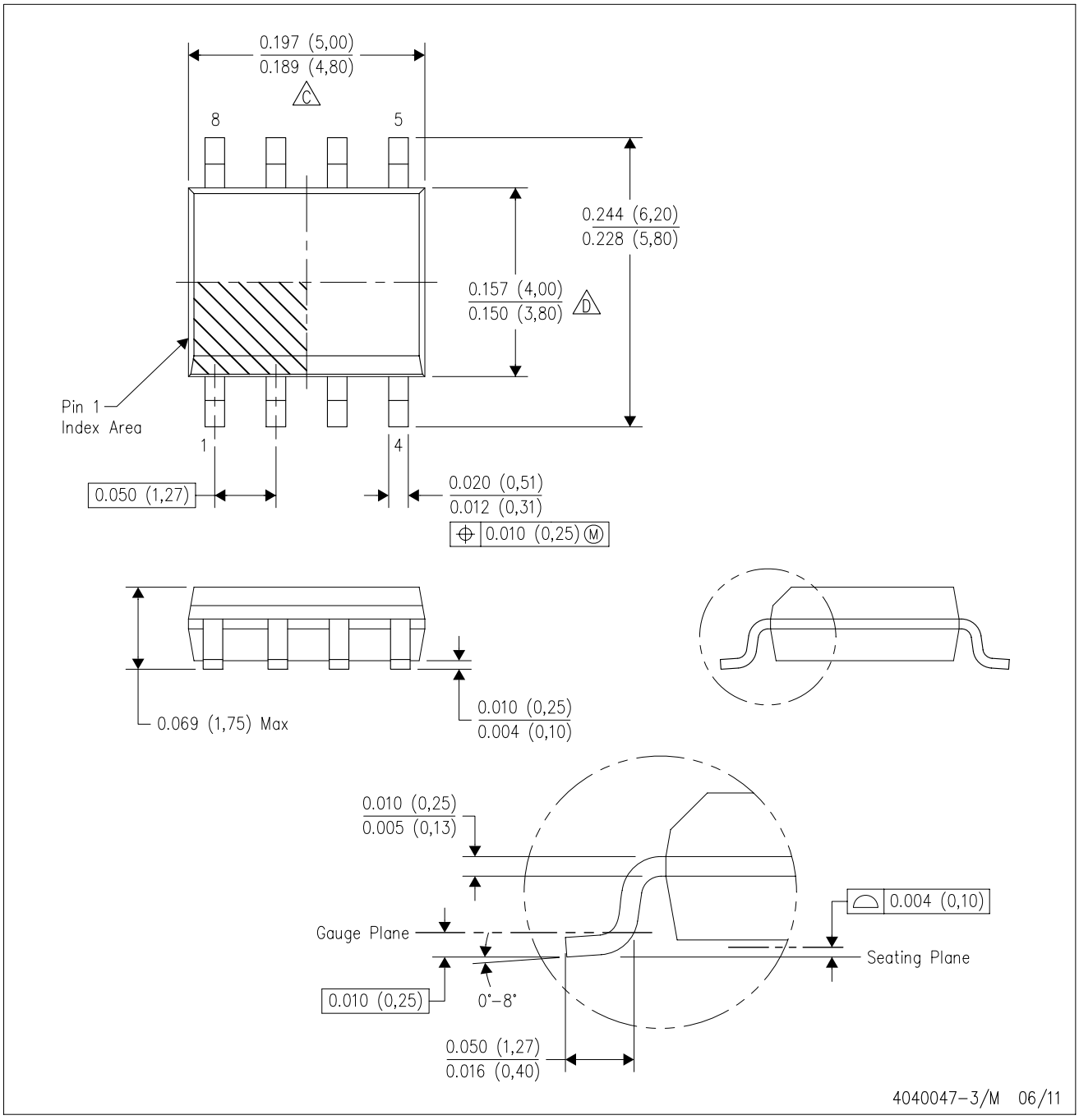
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



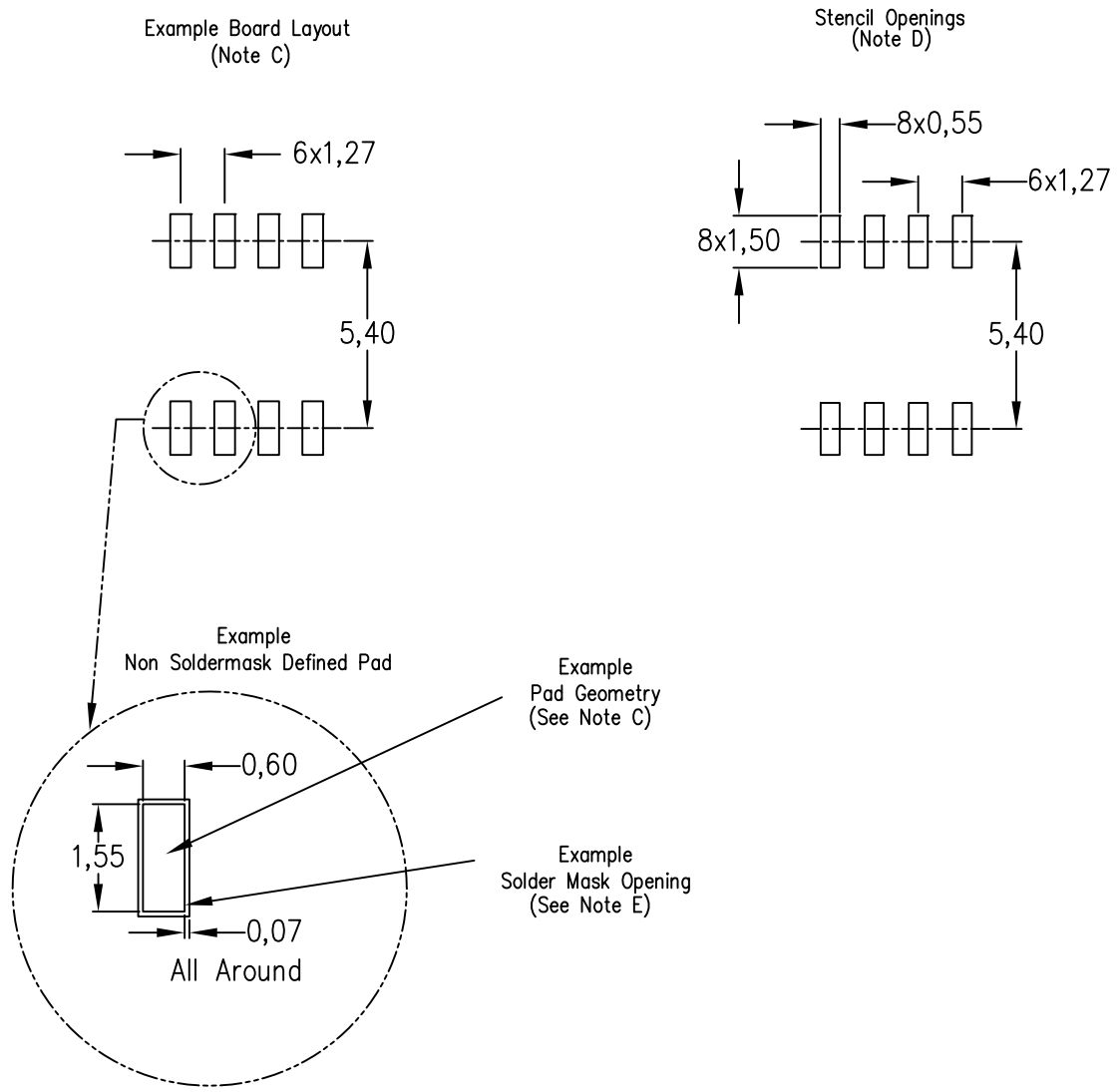
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



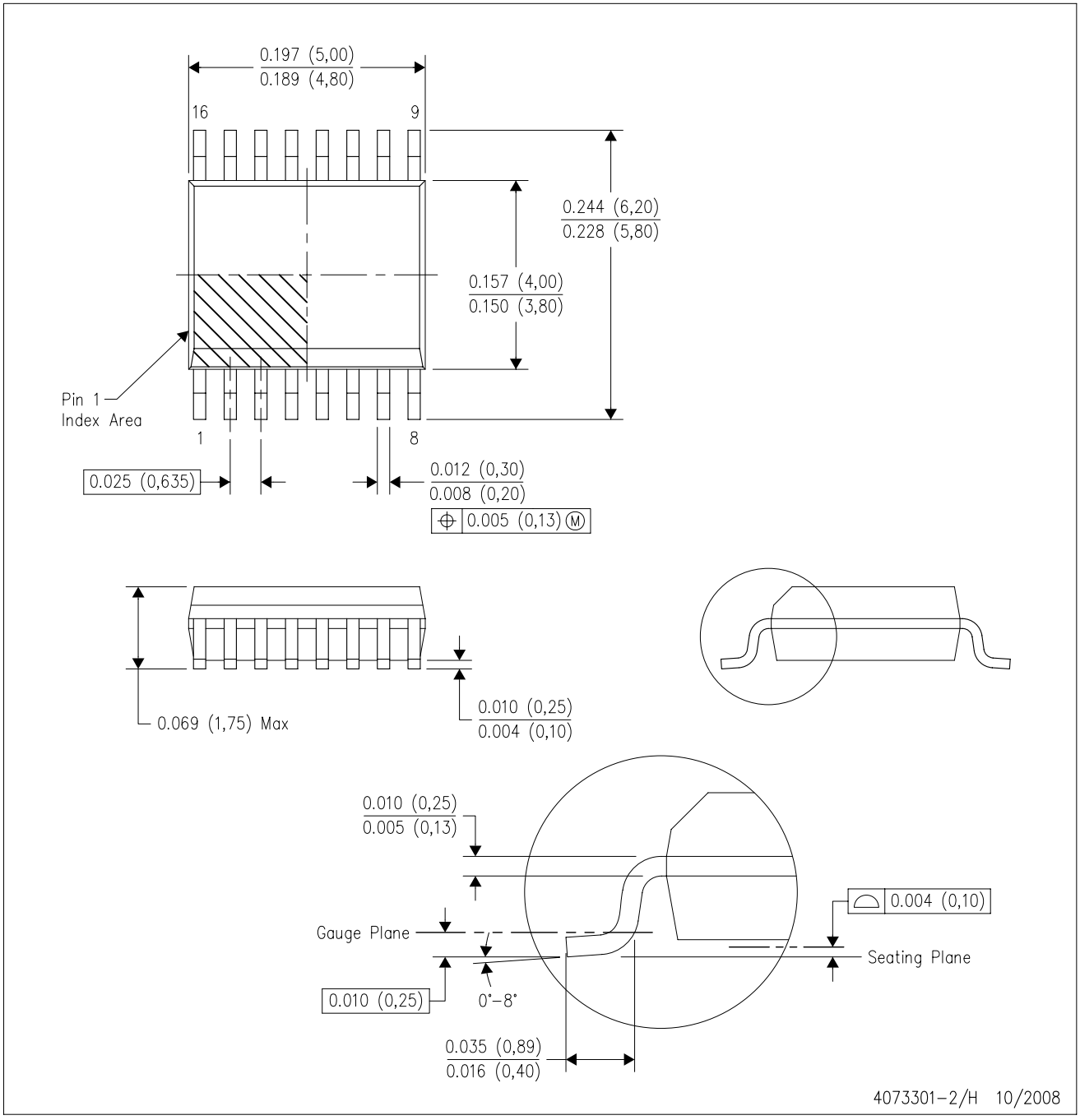
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

DBQ (R–PDSO–G16) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15) per side.
D. Falls within JEDEC MO–137 variation AB.

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