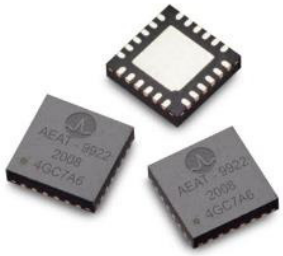
BROADCOM®

Data Sheet

AEAT-9922

10-Bit to 18-Bit Programmable Angular Magnetic Encoder IC for On- and Off-Axis Applications



Description

The Broadcom® AEAT-9922 is an angular magnetic rotary sensor that provides accurate angular measurement over a full 360 degrees of rotation.

It is a sophisticated system that uses integrated Hall sensor elements with complex analog and digital signal processing within a single device.

A simple two-pole magnet generates the necessary magnetic field by rotating it in perpendicular. Wide magnetic field sensor configurations allow On-Axis (end of shaft) or Off-Axis (side of shaft) modes in application.

The Broadcom AEAT-9922 is a versatile solution capable of supporting a broad range of applications with its robust architecture to measure and deliver both absolute and incremental signals.

The absolute angle measurement provides an instant indication of the magnet's angular position with a selectable and reprogrammable resolution from 10 bits to 18 bits.

When selected, its positioning data is then represented in its digital form to be assessed through a standard SSI (parity) and SPI (with CRC and Parity option) communication protocol. Where desired, users may also choose to receive its absolute angle position in PWM-encoded output signals with initialization and error bits option.

The incremental positions are indicated on ABI and UVW signals with wide user configurable resolution from 1CPR and up to 10,000 CPR of ABI signals and pole pairs from 1 to 32 pole pairs (2 to 64 poles) for UVW commutation signals.

Features

- 5V and 3.3V operation
- Programmable 10 bits to 18 bits of absolute resolution
- Flexible Incremental ABI resolution ranging from 1 to 10,000 CPR
- Commutation angle output UVW 1 to 32 pole-pair
- PWM output modes with initialization and error bits option
- User-programmable zero position, direction, index width and index position
- Programmable hysteresis
- Absolute output over 2-wire SSI, 3-wire SSI, and 4-wire SPI. Each available in different mode.
- Compact QFN-24 leads (4 mm × 4 mm) package
- RoHS compliant
- INL angle correction for high accuracy
- Wide operating temperature –40°C to 125°C

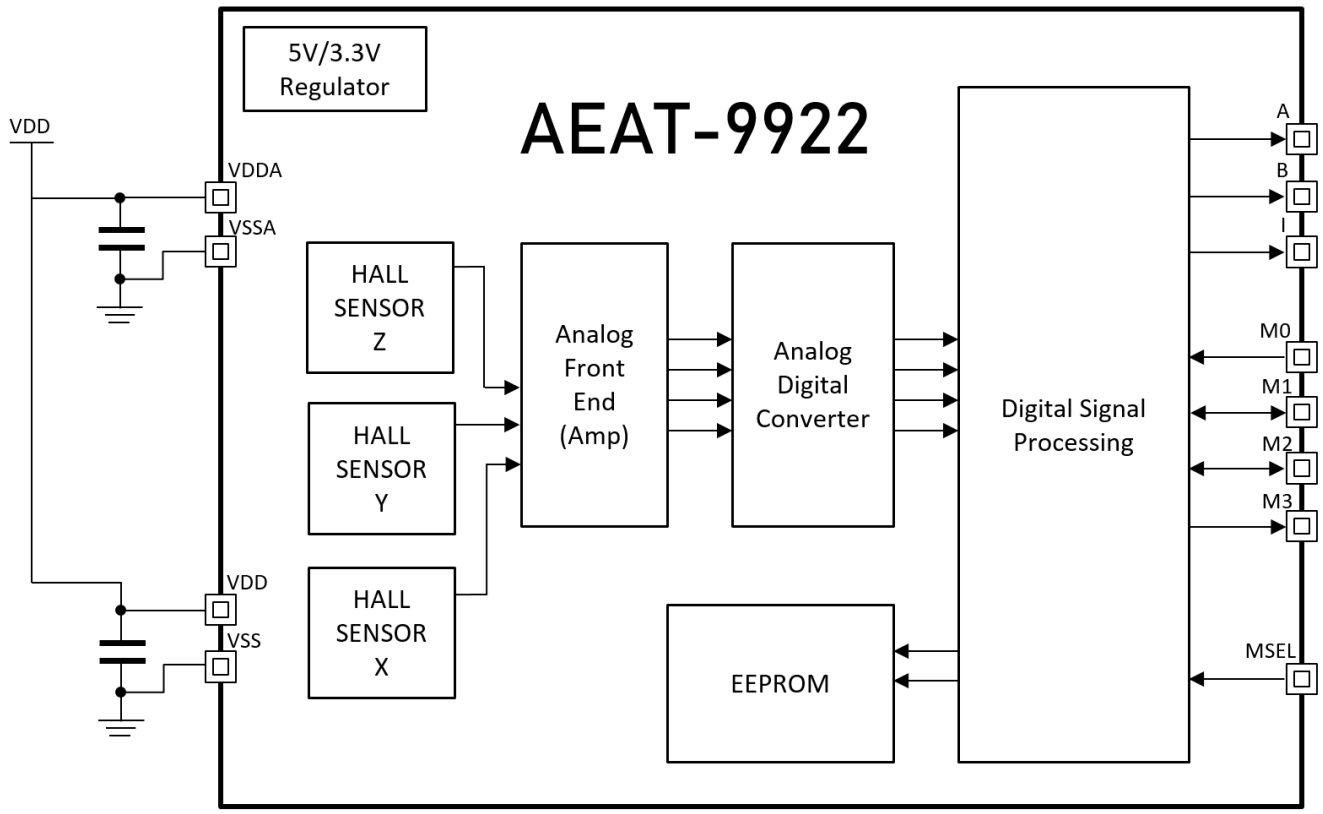
Applications

- Brushless DC motor and stepper motor
- Resolver and potentiometer replacement
- Industrial automation and robotics
- Industrial sewing machine and textiles equipment

NOTE: This product is not specifically designed or manufactured for use in any specific device. Customers are solely responsible for determining the suitability of this product for its intended application and solely liable for all loss, damage, expense, or liability in connection with such use.

Functional Description

Figure 1: AEAT-9922 Block Diagram



The AEAT-9922 is manufactured with a CMOS standard process. It is capable of accurately measuring a magnet's rotational angle when it is placed in alignment and in perpendicular to the device by using its integrated Hall sensors to detect its magnetic field. The detected magnetic signals are then taken as input signals to be properly conditioned to negate its non-idealities before inputting them into the analog amplifiers for strength amplification and filtering. After which, the amplified analog signals are then fed into the internal analog-to-digital converter (ADC) to be converted into digital signals for the final stage of digital processing. The digital processing provides a digitized output of the absolute and incremental signals.

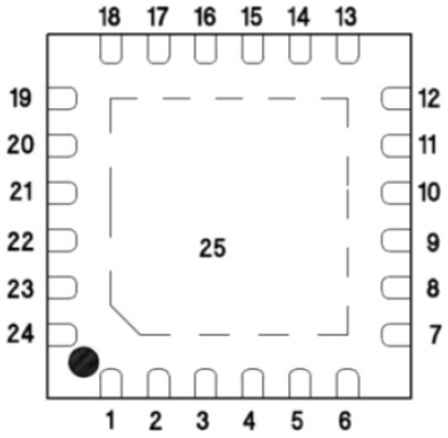
The used magnet should have sufficient magnetic field strength mT to generate the magnetic field for the signal generation (see Recommended Magnetic Input Specifications). The device provides digital information of magnetic field strength high MHi and magnetic field strength low MLo from output protocols to indicate whether the magnets are too close or too far away from our device's surface.

Users can access the device's digitized absolute data using standard Synchronous Serial Interface (SSI) or Serial Peripheral Interface (SPI) protocols. In addition, an absolute angular representation also can be selected using a pulse width modulated (PWM) signal.

The incremental outputs are available from digital outputs of their dedicated A, B, and I pins. The U, V, and W commutation outputs are switchable on the general I/O pins.

Pin Assignment

Figure 2: Pin Configurations



Pinout Description

Pin QFN24	Pin Name	I/O	Type	Functional Description
1 to 6	NC	—	—	No Connection
7	VDDA	—	Power	3.3V/5V Supply Input (Analog)
8	VSSA	—	Power	Supply Ground (Analog)
9	M0	I/O	Digital	SPI3 and SSI Selection/SPI Chip Select/ERR Output
10	M1	I/O	Digital	SPI Data Input/SSI NSL Pin/U Commutation Output (UVW)
11	M2	I/O	Digital	SPI/SSI Clock Input/V Commutation Output (UVW)
12	M3	O	Digital	SPI/SSI Data Out/W Commutation Output (UVW)/PWM Output
13 to 18	NC	—	—	No Connection
19	MSEL	I	Digital	Mode Selection
20	I	O	Digital	Incremental Index Output (ABI)
21	VDD	—	Power	3.3V/5V Supply Input (Digital)
22	VSS	—	Power	Supply Ground (Digital)
23	B	O	Digital	Incremental B Output (ABI)
24	A	O	Digital	Incremental A Output (ABI)
25	VSS	—	Power	Supply Ground

Electrical Characteristics

Absolute Maximum Ratings

Table 1: Maximum Rating

Parameter	Symbol	Min.	Max.	Units	Notes
Storage Temperature	T_S	–40	125	°C	
DC Supply Voltage VDDA Pin	 VDD	 –0.3	 6	 V	
Input Voltage Range	V_{in}	–0.3	6	V	
Electrostatic Discharge (HBM)		–4.0	+4.0	kV	
Moisture Sensitivity Level		—	1		

CAUTION!

- Subjecting the product to stresses beyond those listed in this section may cause permanent damage to the devices.
- These are stress ratings only and do not imply that the devices will function beyond these ratings. Exposure to the extremes of these conditions for extended periods may affect product reliability.

Recommended Operating Conditions

Table 2: Recommended Operating Conditions for the Encoder IC

Parameter	Symbol	Min.	Typ.	Max.	Units	Notes
Operating Ambient Temperature	T_A	–40	—	125	°C	
DC Supply Voltage to VDD Pin 5V Operation 3.3V Operation	VDD	 4.5 3.0	 5.0 3.3	 5.5 3.6	V	
Incremental Output Frequency	f_{MAX}	—	—	1.0	MHz	Frequency = Velocity(rpm) × CPR/60
Load Capacitance	C_L	—	—	15	pF	

Systems Parameters

Table 3: Systems Parameters

Parameter	Symbol	Min.	Typ.	Max.	Units	Notes
Current Consumption						
Supply Current Normal Operation Mode	I_{DD}	—	25	—	mA	5V
	I_{DD}	—	24	—	mA	3.3V
Digital Outputs (DOs)						
High Level Output Voltage	V_{OH}	VDD – 0.5	—	—	V	Normal operation
Low Level Output Voltage	V_{OL}	—	—	GND + 0.4	V	
Power-Up Time Absolute Output Incremental Output PWM Output	t_{PwrUp}	—	10	—	ms	
Digital Inputs (DIs)						
Input High Level	V_{IH}	0.7 × VDD	—	—	V	
Input Low Level	V_{IL}	—	—	0.3 × VDD	V	
Pull-Up Low Level Input Current	I_{IL}	—	—	120	µA	
Pull-Down High Level Input Current	I_{IH}	—	—	120	µA	

NOTE: Electrical characteristics over the recommended operating conditions. Typical values specified at VDD = 5.0V and 25°C, at optimum placement of magnet.

Encoding Characteristics

Table 4: Encoding Output Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Units	Notes
Absolute Output						
Resolution	RES	10	—	18	Bit	Programmable 10 to 18 bits
Integral Non-Linearity On-Axis	INL_{nom}	—	± 0.1	—	Degree	Best fit line, centered magnet. T_A = 25°C, Voltage = 5V, INL angle correction
Integral Non-Linearity Off-Axis		—	± 0.15	—		
Integral Non-Linearity On-Axis	INL_{dis}	—	± 0.2	—	Degree	Best fit line, over displacement of magnet. T_A = 25°C, Voltage = 5V
Integral Non-Linearity Off-Axis		—	± 0.3	—		
Integral Non-Linearity On-Axis	INL_{temp}	—	± 0.5	—	Degree	Best fit line, over displacement of the magnet and temperature variation. T_A = –40°C to +125°C, Voltage = 5V
Integral Non-Linearity Off-Axis		—	± 0.7	—		
Code Monotony		—	1	—	LSB	14-bits absolute (Static)
Output Sampling Rate	f_S	—	10	—	MHz	Based on SSI3 protocol
Latency		—	80	—	ns	
Incremental Output (Channel ABI)						
Resolution	R_{INC}	1	—	10000	CPR	Programmable
Index Pulse Width	P_O	90	—	360	°e	Programmable options: 90, 180, 270, or 360 °e. See Figure 25.
Index State		90	—	360	°e	Programmable options: 90, 180, 270, or 360 °e. See Figure 25.
Relative Angular Accuracy	%	—	10	—	%	Reference to an output period at output A and B, at 512 CPR, 5V, and 3000 RPM
PWM Output						
PWM Frequency	f_{PWM}	122	—	976	Hz	Adjustable based on PWM settings
Minimum Pulse Width	PW_{MIN}	—	1	—	µs	
Maximum Pulse Width	PW_{MAX}	—	16,384		µs	

NOTE: Encoding characteristics over recommended operating range unless otherwise specified.

Encoding Timing Characteristics

Table 5: Encoder Timing Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Units	Notes
Incremental Output (ABI and UVW)						
System Reaction Time	t_{delay}	—	10	—	ms	First ABI pulse detection upon power up.

Mechanical and Magnetic Specifications

Recommended Magnetic Input Specifications

Table 6: Magnet Specifications

Parameter	Symbol	Min.	Typ.	Max.	Units	Notes
Diameter	d					Recommended magnet: Cylindrical magnet or ring magnet diametrically magnetized and 1-pole pair.
Disc Magnet		4	6	—	mm	
Ring Magnet ID /OD		—	ID,15 OD,25	—	mm mm	
Thickness	t					
Disc Magnet		—	2.5	—	mm	
Ring Magnet		2	6	—	mm	
Magnetic Input Field Magnitude	Bpk					Required vertical/horizontal component of the magnetic field strength on the die's surface, measured along concentric circle.
On-Axis (Disc Magnet)		45	—	100	mT	
Off-Axis (Ring Magnet)		30	—	150	mT	
Magnet Displacement Radius	R_m	—	—	0.25	mm	Displacement between magnet axis to the device center.
Recommended Magnet Material and Temperature Drift		—	–0.12	—	%/K	NdFeB (Neodymium Iron Boron), grade N35SH.

Figure 3: Direction Definition When the Magnet Rotates

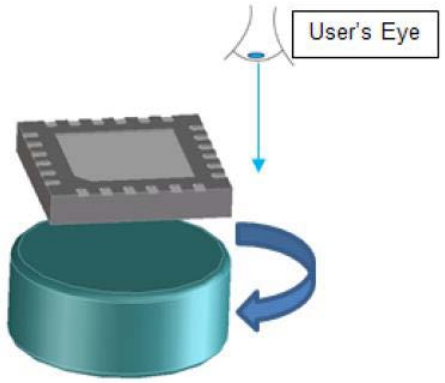
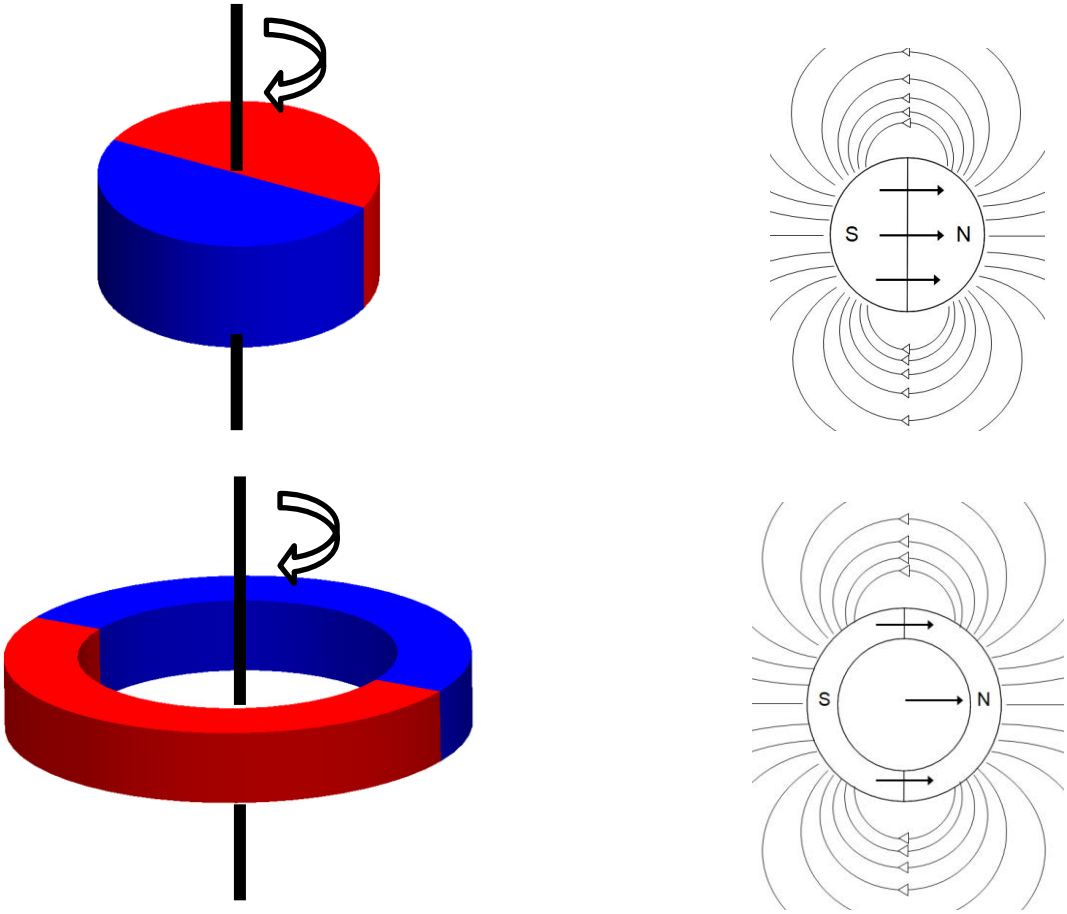


Figure 4: Diametrically Magnetized Magnet



Communication Protocol

AEAT-9922 has a total of 10 interfaces; one is dedicated for incremental ABI and remaining are multiplexed to I/O pin M0, M1, M2, and M3. Each output is configurable using the M0 pin, the MSEL pin, and the PSEL registers as shown in the following table.

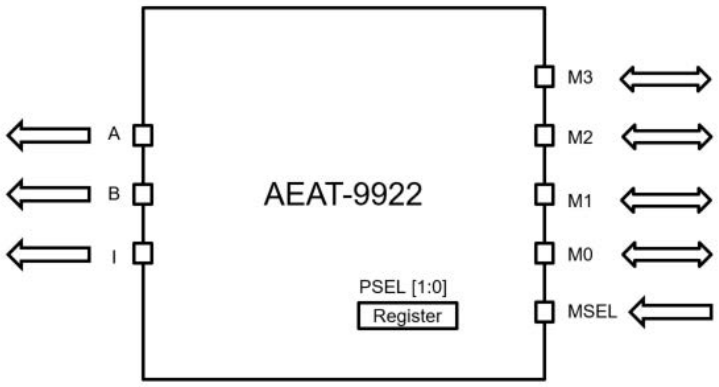
Table 7: Configurable interface IO and selection

Pin	Mode									
	SPI-3	**SSI-3(A)**	**SSI-3(B)**	**SSI-2(A)**	**SSI-2(B)**	**SPI-4(A)**	**SPI-4(B)**	**UVW**	**PWM**	**Remarks**
MSEL	0	0	0	0	0	1	1	1	1	I/O Pin
PSEL[1]	x	x	x	x	x	0	0	1	1	Memory
PSEL[0]	x	0	1	0	1	0	1	0	1	Memory
M0	0	1	1	1	1	NCS	NCS	ERR	ERR	I/O Pin
M1	DIN	NSL	NSL	0	0	MOSI	MOSI	U	N/A	I/O Pin
M2	SCK	SCL	SCL	SCL	SCL	SCK	SCK	V	N/A	I/O Pin
M3	DO	DO	DO	DO	DO	MISO	MISO	W	PWM	I/O Pin

NOTE:

1. PSEL[1] and PSEL[0] are configurable through memory.
2. MSEL, M0, M1, M2, and M3 are configurable through I/O pads.

Figure 5: Interface Selection and IO Pins



SPI4 Protocol

SPI4 protocol uses four pins from AEAT-9922. These four pins are shared between the UVW, SSI, and SPI protocols. MSEL (input pin) selects one of these protocols at a time. Assert 1 on the MSEL pin to select the SPI4 protocol.

SPI4 protocols allow user to access memory read or write and position data. They use CPOL=0, CPHA=1 for triggering.

- M0 → SPI_Chip Select (NCS) signal for SPI protocol, input to AEAT-9922
- M1 → SPI_Data Input (MOSI) signal for SPI protocol, input to AEAT-9922
- M2 → SPI_Clock Input (SCK) signal for SPI protocol, input to AEAT-9922
- M3 → SPI_Data Output (MISO) signal for SPI protocol, output from AEAT-9922

Figure 6: SPI4 Timing Diagram

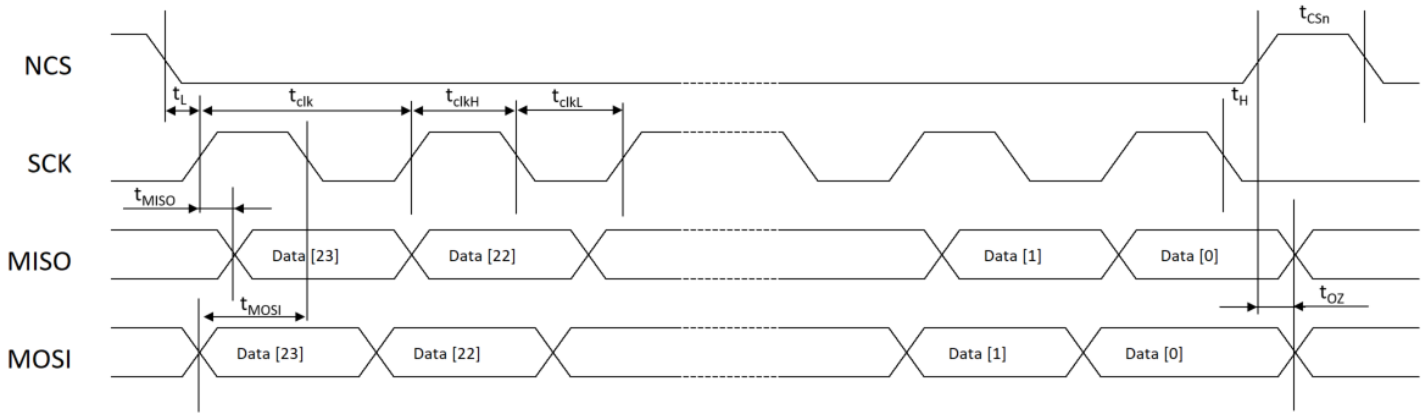


Table 8: SPI4 Timing Characteristics

Symbol	Description	Min.	Typ.	Max.	Units
t_L	Time between NCS falling edge and CLK rising edge	350	—	—	ns
t_{clk}	Serial clock period	100	—	—	ns
t_{clkL}	Low period of serial clock	50	—	—	ns
t_{clkH}	High period of serial clock	50	—	—	ns
t_H	Time between last falling edge of SCK and rising edge of NCS	t_{clk} /2	—	—	ns
t^{CSn}	High time of NCS between two transmission	350	—	—	ns
t_{MOSI}	Data input valid to clock edge	20	—	—	ns
t_{MISO}	SCK edge to data output valid	—	51	—	ns
t_{OZ}	Time between NCS rising edge and MISO	—	10	—	ns

NOTE: The user should read back data to confirm data is written successfully.

SPI4 Command and Data Frame

Figure 7: SPI4 Read Sequence

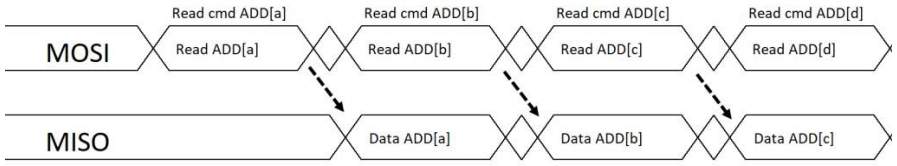


Figure 8: SPI4 Write Sequence

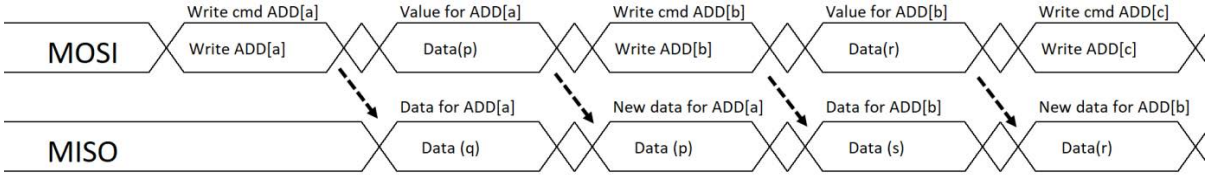


Figure 9: SPI-4(A) 16-bit (Parity)

By default, the chip is configured to SPI4 16-bit selection, **PSEL [1] = 0**, **PSEL [0] = 0** in the register setting.

	Data Format																			
	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Master to Slave					P	RW	0	0	0	0	0	0	Addr/Data[7:0]							
Slave to Master (memory)					P	EF	0	0	0	0	0	0	Data[7:0]							
Slave to Master (pos 10b)					P	EF	Pos[9:0]										0	0	0	0
Slave to Master (pos 11b)					P	EF	Pos[10:0]											0	0	0
Slave to Master (pos 12b)					P	EF	Pos[11:0]												0	0
Slave to Master (pos 13b)					P	EF	Pos[12:0]													0
Slave to Master (pos 14b)					P	EF	Pos[13:0]													
Slave to Master (pos 15b)				P	EF	Pos[14:0]														
Slave to Master (pos 16b)			P	EF	Pos[15:0]															
Slave to Master (pos 17b)		P	EF	Pos[16:0]																
Slave to Master (pos 18b)	P	EF	Pos[17:0]																	

NOTE: P: Parity; EF: Error Flag; RW: Read = 1, Write = 0

Figure 10: SPI4-(B) 24-bit (CRC)

To configure the chip to SPI4 24-bit selection, set **PSEL [1] = 0**, **PSEL [0] = 1** in the register setting.

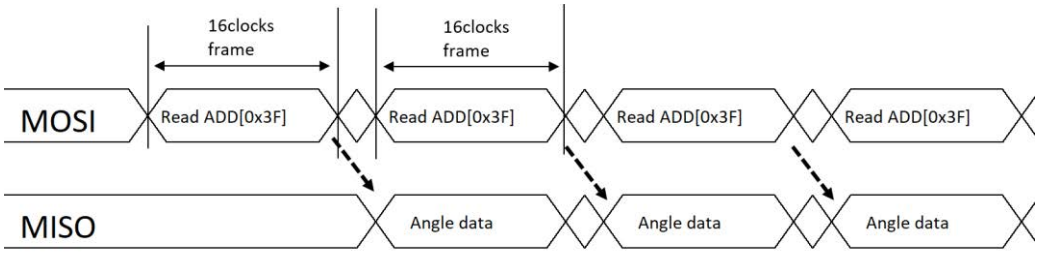
	Data Format																											
	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Master to Slave					0	RW	0	0	0	0	0	0	Addr/Data[7:0]								CRC[7:0]							
Slave to Master (memory)					W	E	0	0	0	0	0	0	Data[7:0]								CRC[7:0]							
Slave to Master (pos 10b)					W	E	Pos[9:0]										0	0	0	0	CRC[7:0]							
Slave to Master (pos 11b)					W	E	Pos[10:0]											0	0	0	CRC[7:0]							
Slave to Master (pos 12b)					W	E	Pos[11:0]												0	0	CRC[7:0]							
Slave to Master (pos 13b)					W	E	Pos[12:0]													0	CRC[7:0]							
Slave to Master (pos 14b)					W	E	Pos[13:0]														CRC[7:0]							
Slave to Master (pos 15b)				W	E	Pos[14:0]															CRC[7:0]							
Slave to Master (pos 16b)			W	E	Pos[15:0]																CRC[7:0]							
Slave to Master (pos 17b)		W	E	Pos[16:0]																	CRC[7:0]							
Slave to Master (pos 18b)	W	E	Pos[17:0]																		CRC[7:0]							

NOTE: W: Warning; E: Error; RW: Read = 1, Write = 0

Position Read

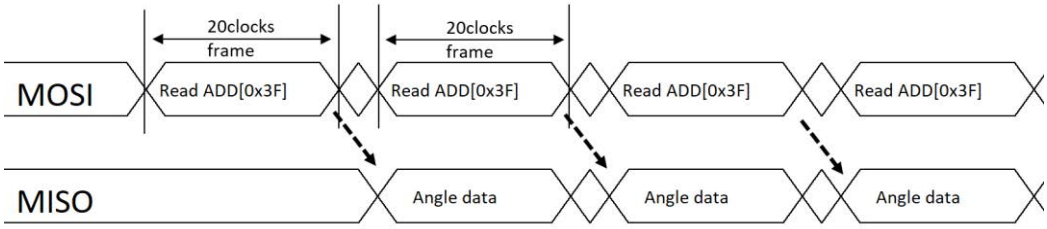
Absolute position data can be obtained by sending a read command to address **0x3F**.

Figure 11: Read Command



In the event of higher single turn resolution (15-bit and above), the command and data frame size is adjusted accordingly.

Figure 12: Command and Data Frame Example for 18-bit (Position) + 2-bit (Parity and Error)



Warning and Error Bit

Error bit is triggered if either Magnet High (MHI), Magnet Low (MLO), Memory Error (MEM_Err) or communication error.

Details of error bits are available in the register address that follows.

Table 9: Error Bits Register

Address	Bit								
[decimal]	[hex]	7	6	5	4	3	2	1	0
33	0x21	RDY	MHI	MLO	MEM_Err				

- **Magnet High (MHI) Error**: This indicates that the magnet strength detected by the chip is too strong. When this is flagged high consistently, change to a weaker magnet or increase the distance between the chip and the magnet. The value for this alarm is represented as 1.
- **Magnet Low (MLO) Error**: This indicates that the magnet strength detected by the chip is too weak. When this is flagged high consistently, change to a stronger magnet or decrease the distance between the chip and the magnet. The value for this alarm is represented as 1.
- **Ready (RDY)**: The chip is ready, and the ready value is 1.
- **Memory Error (MEM_Err)**: The chip memory content is corrupted (per CRC check)

SPI3 Protocol

SPI3 protocols only allow access to memory read write. Assert 0 on the **MSEL** and **M0** pins to configure it.

- M1 → SPI_Data Input (DIN) signal for SPI protocol, input to AEAT-9922
- M2 → SPI_Clock Input (SCK) signal for SPI protocol, input to AEAT-9922
- M3 → SPI_Data Output (DO) signal for SPI protocol, output from AEAT-9922

Figure 13: SPI3 Timing Diagram

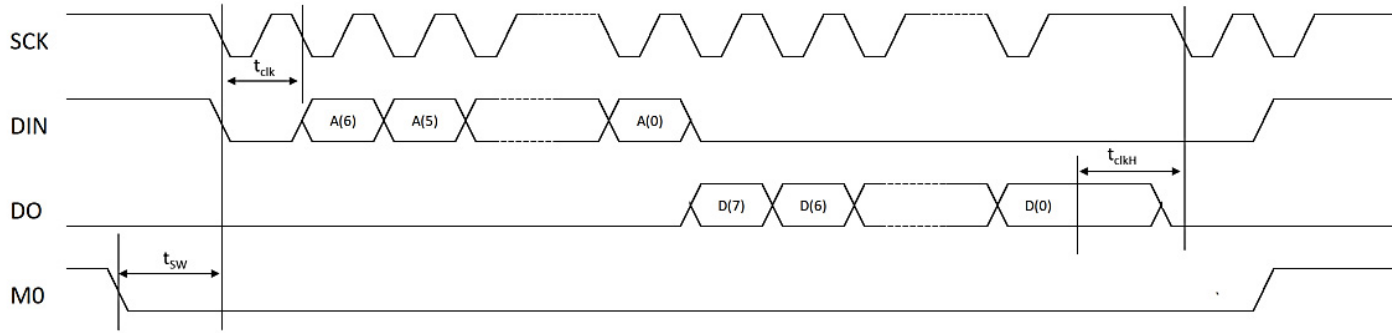


Table 10: SPI3 Timing Characteristics

Symbol	Description	Min.	Typ.	Max.	Units
t_{SW}	Time between M0 falling edge and SCK falling edge	1	—	—	µs
t_{clk}	Serial clock period	—	—	100	ns
t_{clkH}	SCK clock high time after end of last clock period	300	—	—	ns

NOTE: The user should read back data to confirm data is written successfully.

Figure 14: SPI3 Read

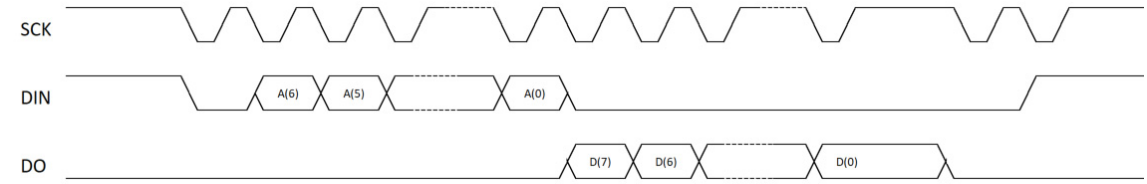
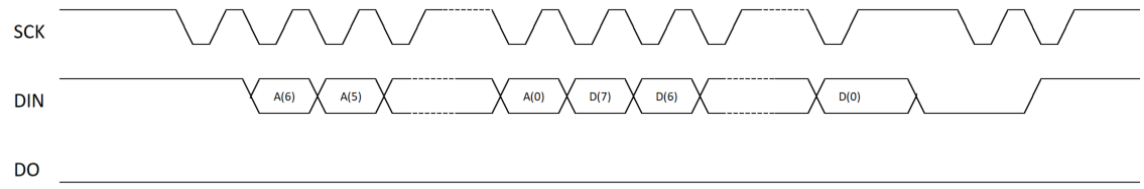


Figure 15: SPI3 Write

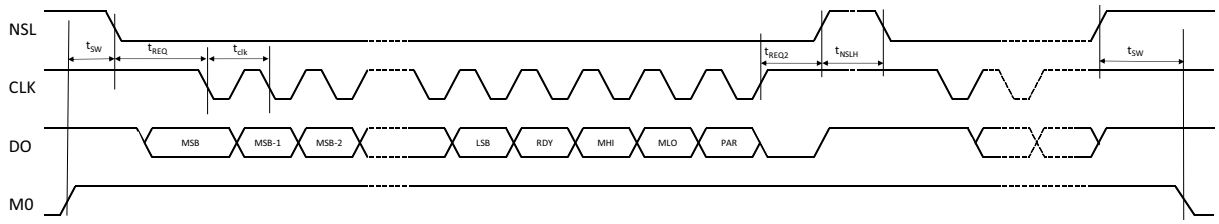


Serial Synchronous Interface 3-wire (SSI3)

SSI3 protocol uses three pins from AEAT-9922. These three pins are shared between the UVW, SSI, and SPI protocols. MSEL (input pin) selects one protocol at a time. Assert 0 on the **MSEL** pin and 1 on the **M0** pin to select the SSI protocol.

- M1 → SSI_NSL Input (NSL) signal for SSI protocol, input to from AEAT-9922
- M2 → SSI_Clock Input (CLK) signal for SSI protocol, input to AEAT-9922
- M3 → SSI_Data Output (DO) signal for SSI protocol, output from AEAT-9922

Figure 16: SSI-3A Protocol Timing Diagram



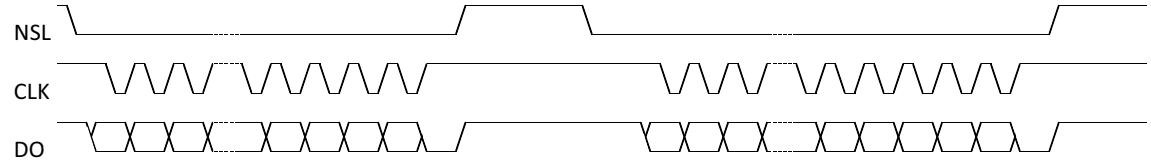
Default: Data Output with 3-wire SSI to 10-MHz clock rates.

Table 11: SSI3 Protocol Timing

Symbol	Description	Min.	Typ.	Max.	Units
t_{sw}	Time between M0 and NSL switching edges	1	—	—	µs
t_{clk}	Serial clock period	100	—	—	ns
t_{REQ}	CLK high time between NSL falling edge and first CLK falling edge	300	—	—	ns
t_{REQ2}	NSL low time after rising edge of last clock period for an SSI read	200	—	—	ns
t_{NSLH}	NSL high time between two successive SSI reads	200	—	—	ns

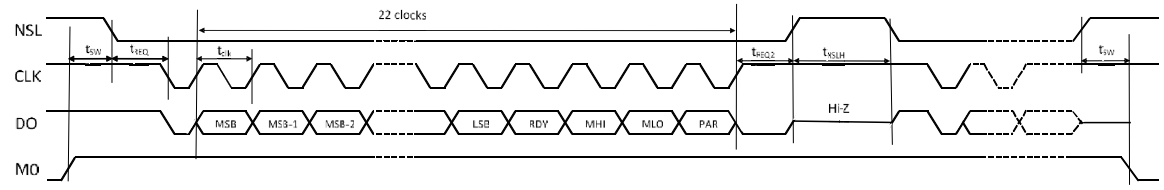
SSI3 is available in two options per the PSEL register setting,

Figure 17: SSI-3(A)



The DO pin is held at high state when the NSL pin is high.

Figure 18: SSI-3(B)



The DO pin is at tristate (high impedance) when the NSL pin is high.

Serial Synchronous Interface 2-Wire (SSI2)

SSI2 protocol uses two pins from AEAT-9922. These two pins are shared among the UVW, SSI, and SPI protocols. MSEL (input pin) selects one protocol at a time. Assert 0 on the **MSEL** pin and the **M1** pin and 1 on the **M0** pin upon power-up.

- M2 → SSI_Clock Input (CLK) signal for SSI protocol, input to AEAT-9922
- M3 → SSI_Data Output (DO) signal for SSI protocol, output from AEAT-9922

Figure 19: SSI 2-Wire Timing Diagram

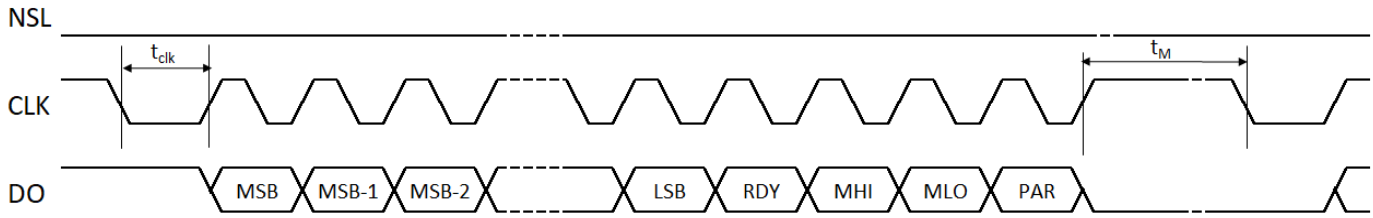
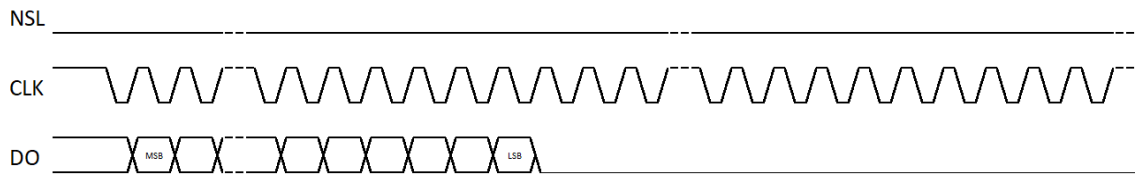


Table 12: SSI 2-Wire Timing Characteristics

Symbol	Description	Min.	Typ.	Max.	Units
t_{clk}	CLK low time after the first falling edge for an SSI read	250	—	t_M / 2	ns
t_M	CLK high time between 2 successive SSI reads	—	16.5	18.0	µs

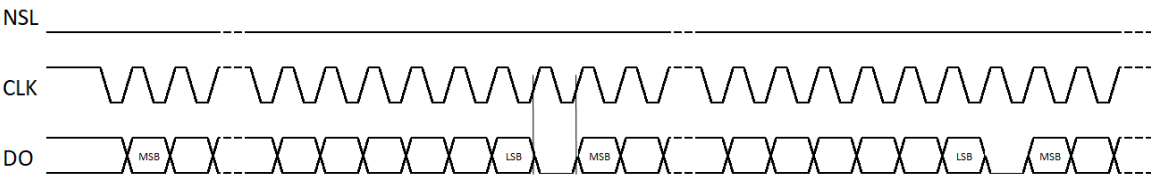
SSI2 is available in two options per the PSEL register setting:

Figure 20: SSI-2(A)



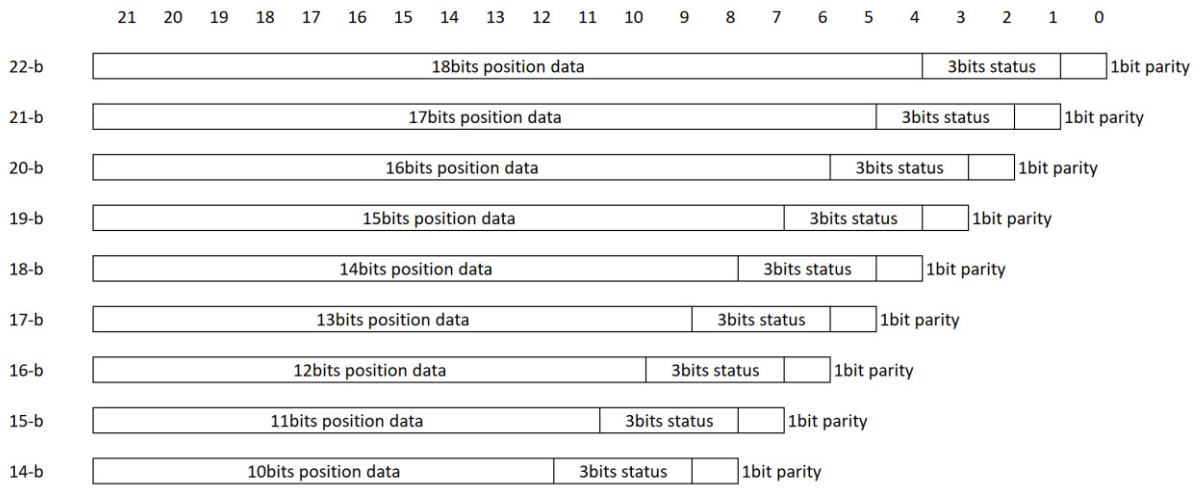
Output single data position and remains low after LSB until the next monoflop (t_M) expires.

Figure 21: SSI-2(B)



The same position data can be continuously output by sending clock train and data is separated by a single low pulse. Data will be refreshed on the next monoflop (t_M) expires.

Figure 22: SSI2 Read Data Format



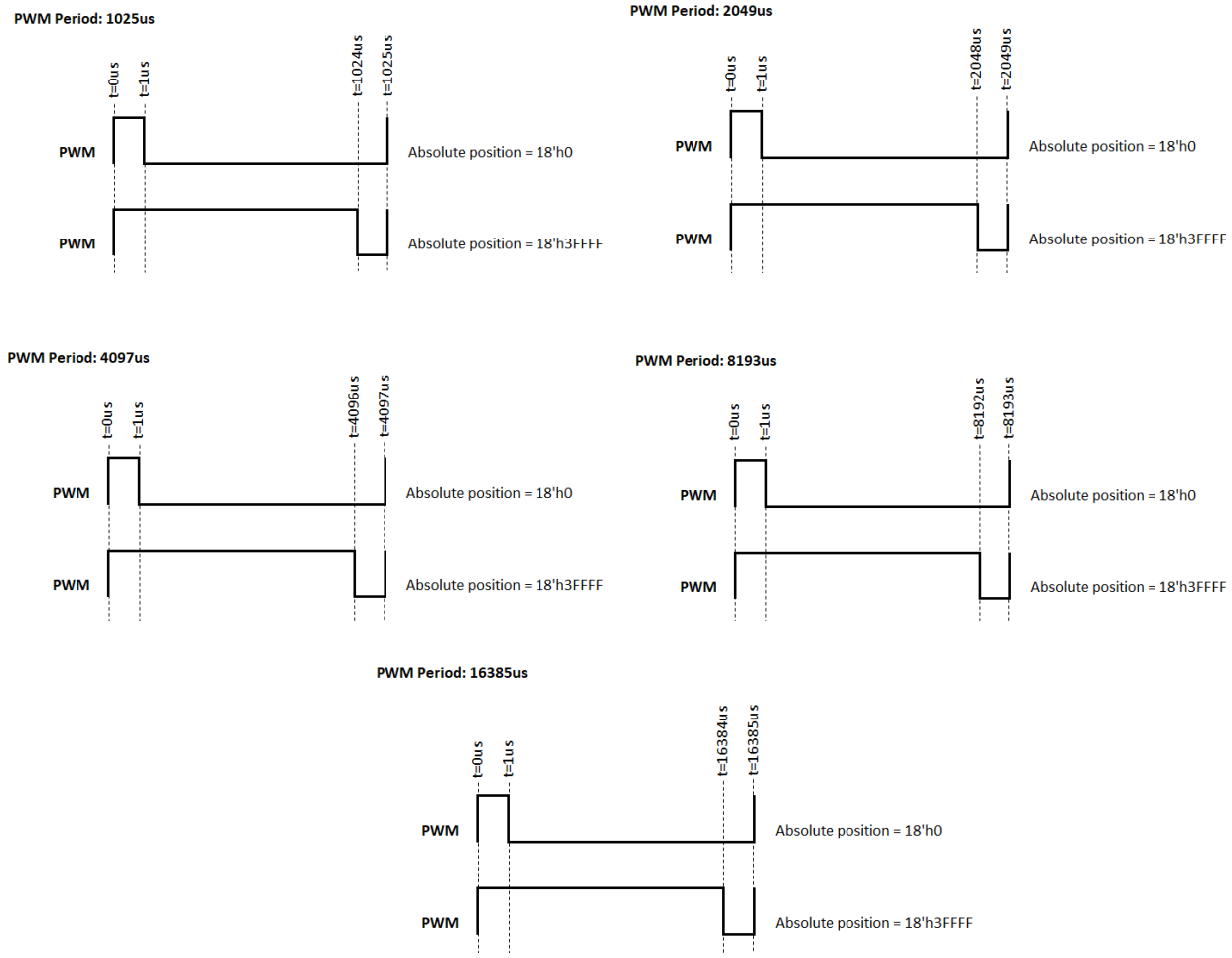
NOTE: 3-b status: {Ready, MHI, MLO}.

- **Magnet High (MHI) Error:** This indicates that the magnet strength detected by the chip is too strong. When this is flagged high consistently, change the weaker magnet or increase the distance between the chip and the magnet. The value for this alarm is represented as 1.
- **Magnet Low (MLO) Error**: This indicates that the magnet strength detected by the chip is too weak. When this is flagged high consistently, change the stronger magnet or decrease the distance between the chip and the magnet. The value for this alarm is represented as 1.
- **Ready**: The chip is ready, and the ready value is 1.
- **Parity**: 1-b parity is even parity.

PWM

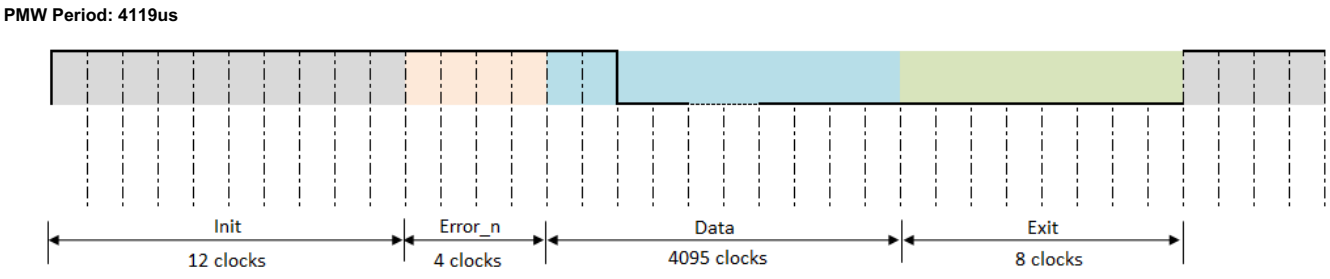
PWM protocol uses one output pin (W_PWM) from AEAT-9922. Note that W_PWM pin is shared between UVW and PWM protocols. The PWM signals are configurable to have period of 1025, 2049, 4097, 8193 or 16385 µs. During power-up, the PWM signal is 0 before chip ready.

Figure 23: PWM Signals (Period = 1025/2049/4097/8193/16385 µs)



PWM protocols are also available with Init, Error_n, and Exit along with Data information.

Figure 24: PWM Signals (Period = 1047/2071/4119/8215/16407 µs)



Incremental Output Format

The AEAT-9922 provides ABI and UVW signals to indicate incremental position of the motor.

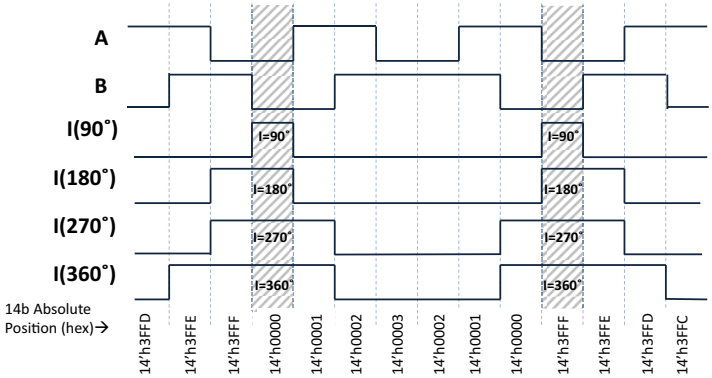
ABI

The ABI incremental interface is available to provide position data and direction data from the three output pins (A, B, and I).

The index signal marks the absolute angular position and typically occurs once per revolution The ABI signal is configurable using the memory map registers. It supports the following configurations:

- Programmable CPR: 1 to 10,000 CPR
- Programmable I-width 90, 180, 270, or 360 electrical degrees (°e)
- Programmable I-State: 90, 180, 270, or 360 electrical degrees (°e)

Figure 25: ABI Signal (4096 CPR, with Different I-Width Settings)

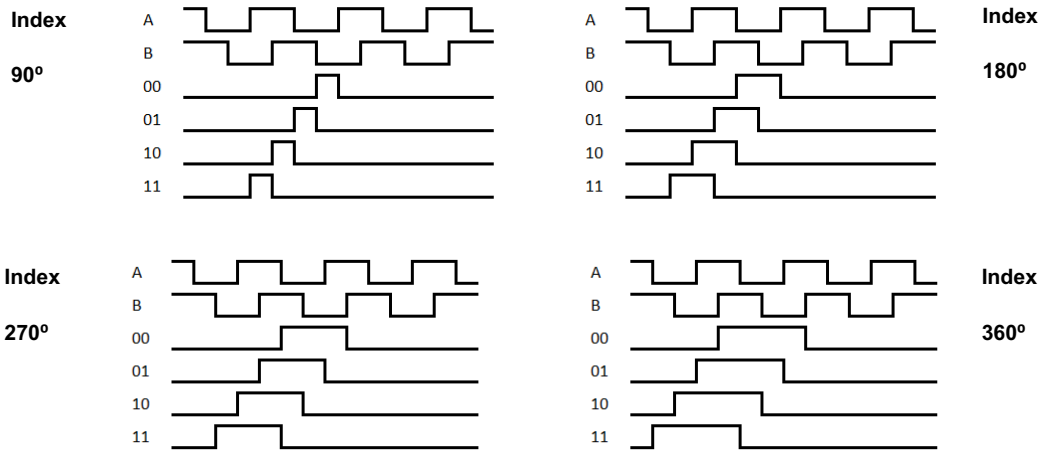


NOTE: Assuming the user sets the hysteresis at 0.02 mechanical degrees.

The Index position is configurable among the incremental state.

Index signal rises high once per revolution at the absolute zero position.

Figure 26: Index Signal Configuration

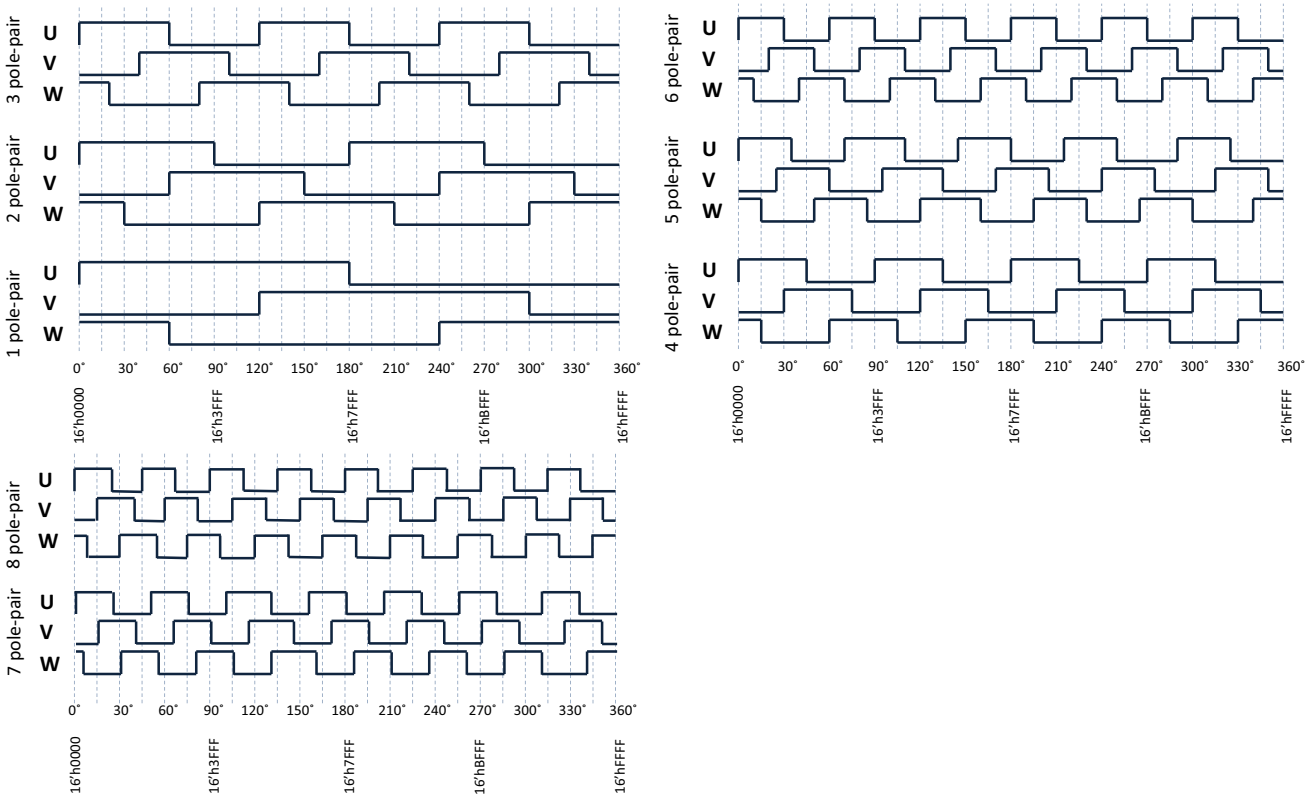


UVW

Three-channel integrated commutation output (U, V, W) emulates Hall sensor feedback and is available using three output pins. AEAT-9922 can configure from 1 to 32 pole pairs, equivalents to 2 to 64 poles.

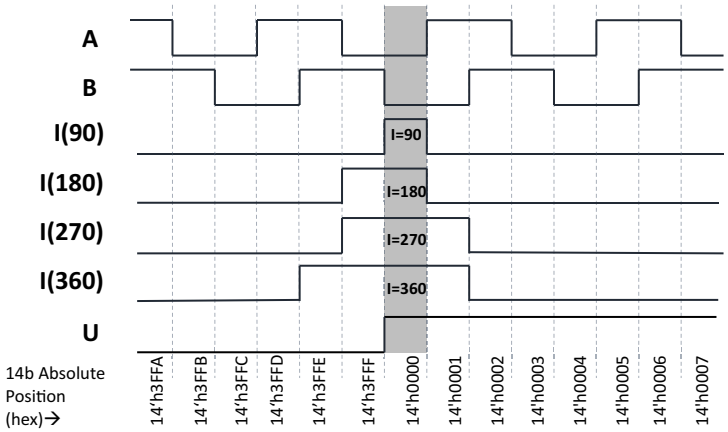
Note that W_PWM pin is shared between the UVW and PWM protocols.

Figure 27: Commutation Output



Note that signal U from UVW protocol is tagged to signal I from the ABI protocol as shown in the following figure.

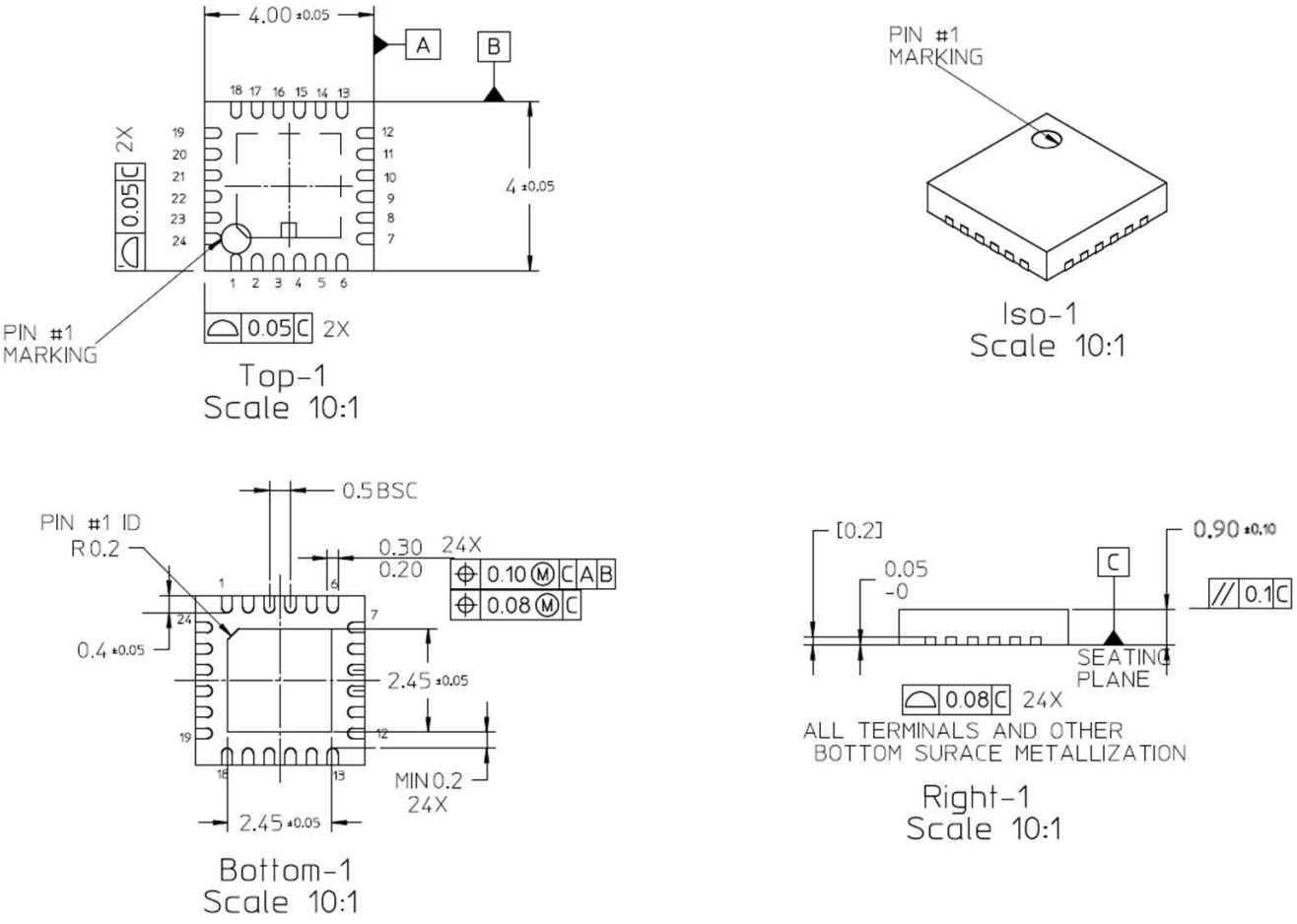
Figure 28: U-to-I Tagging



Package Drawings

Dimensions are in mm unless otherwise specified.

Figure 29: AEAT-9922, 24 QFN Dimensions



Recommended PCB Land Pattern and Soldering Profile

Figure 30: Land Pattern Dimensions in mm

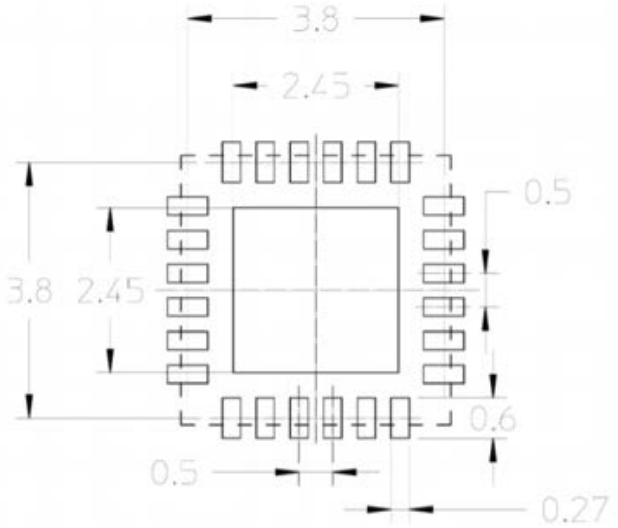
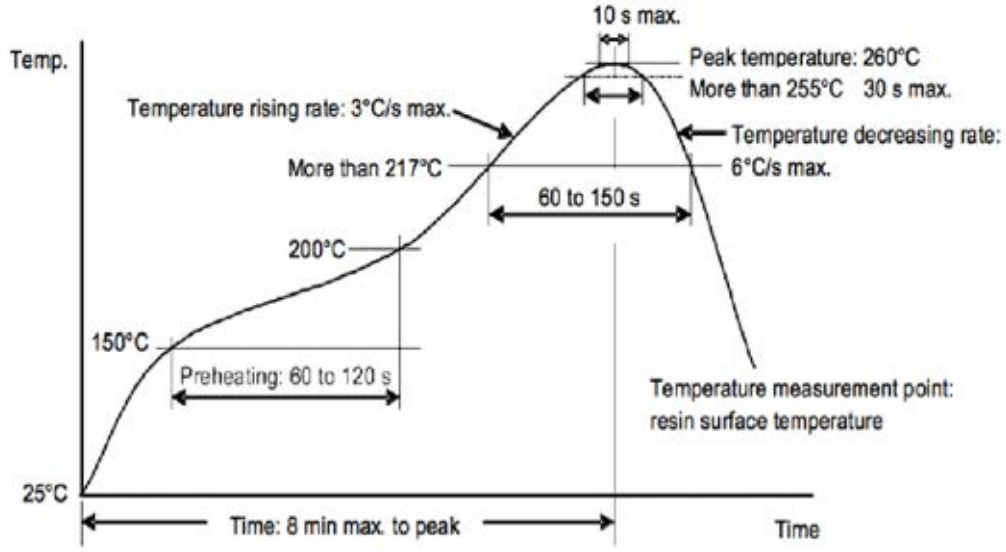


Figure 31: Recommended Lead-Free Solder Reflow Soldering Temperature Profile



Product Ordering Information

Ordering Part Number	Product Description	Package	Delivery Form
AEAT-9922-100	18 Bits Magnetic Encoder On-Off Axis Tape and Reel, 1000 pieces	QFN 24 leads, 4 mm × 4 mm	Tape and Reel
AEAT-9922-102	18 Bits Magnetic Encoder On-Off Axis Tape and Reel, 100 pieces	QFN 24 leads, 4 mm × 4 mm	Tape and Reel
AEAT-9922-Q24	18 Bits Magnetic Encoder On-Off Axis Tube, 73 pieces	QFN 24 leads, 4 mm × 4 mm	Tube

Accessories Ordering Information

Ordering Part Number	Product Description	Remarks
HEDS-9922PRGEVB	AEAT-9922 Programming Kit, Evaluation Board and Magnet Evaluation Set	1 unit of SPI programming kit, 2 units of sensor board, 2 pieces of on-axis magnets, USB cable for PC interface and the associated software
HEDS-9922EVB	AEAT-9922 Evaluation Board	1 unit of sensor board

Packaging Information

Figure 32: Reel Dimensions

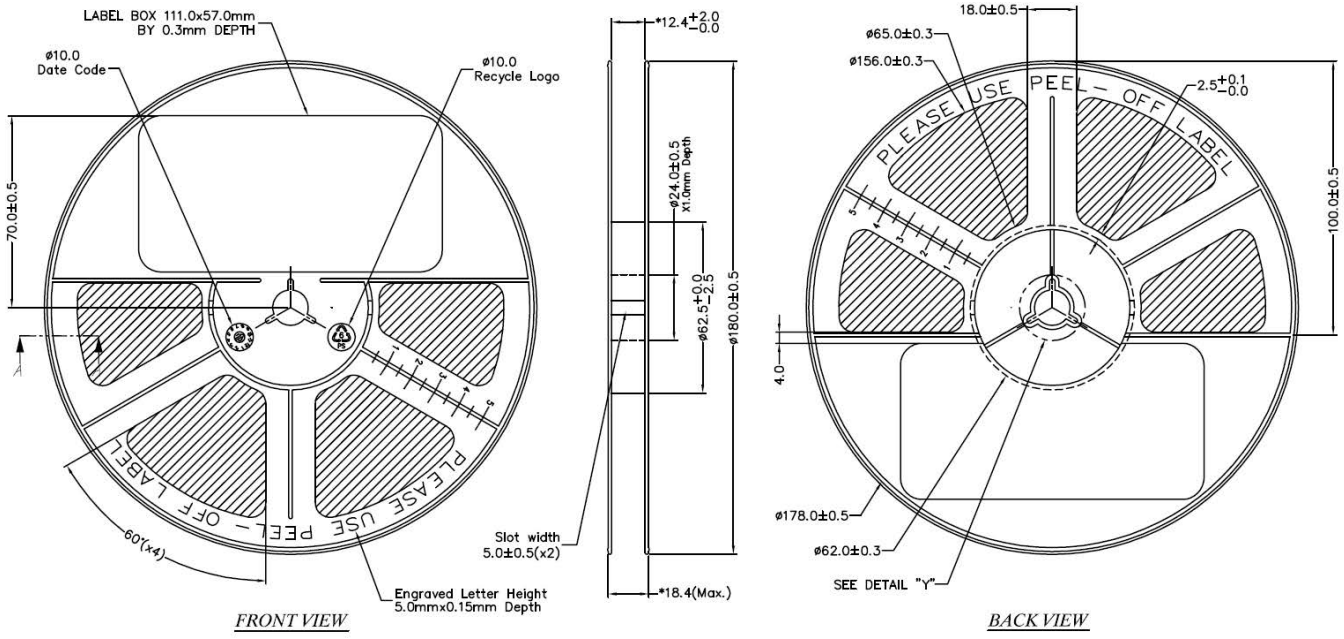


Figure 33: User Feed Direction

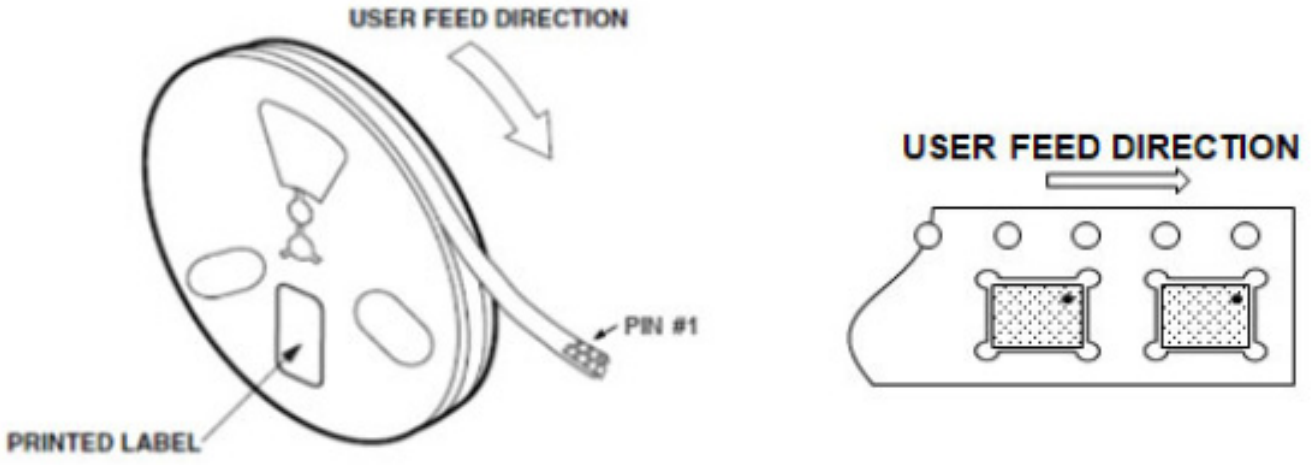


Figure 34: Top Cavity Dimensions

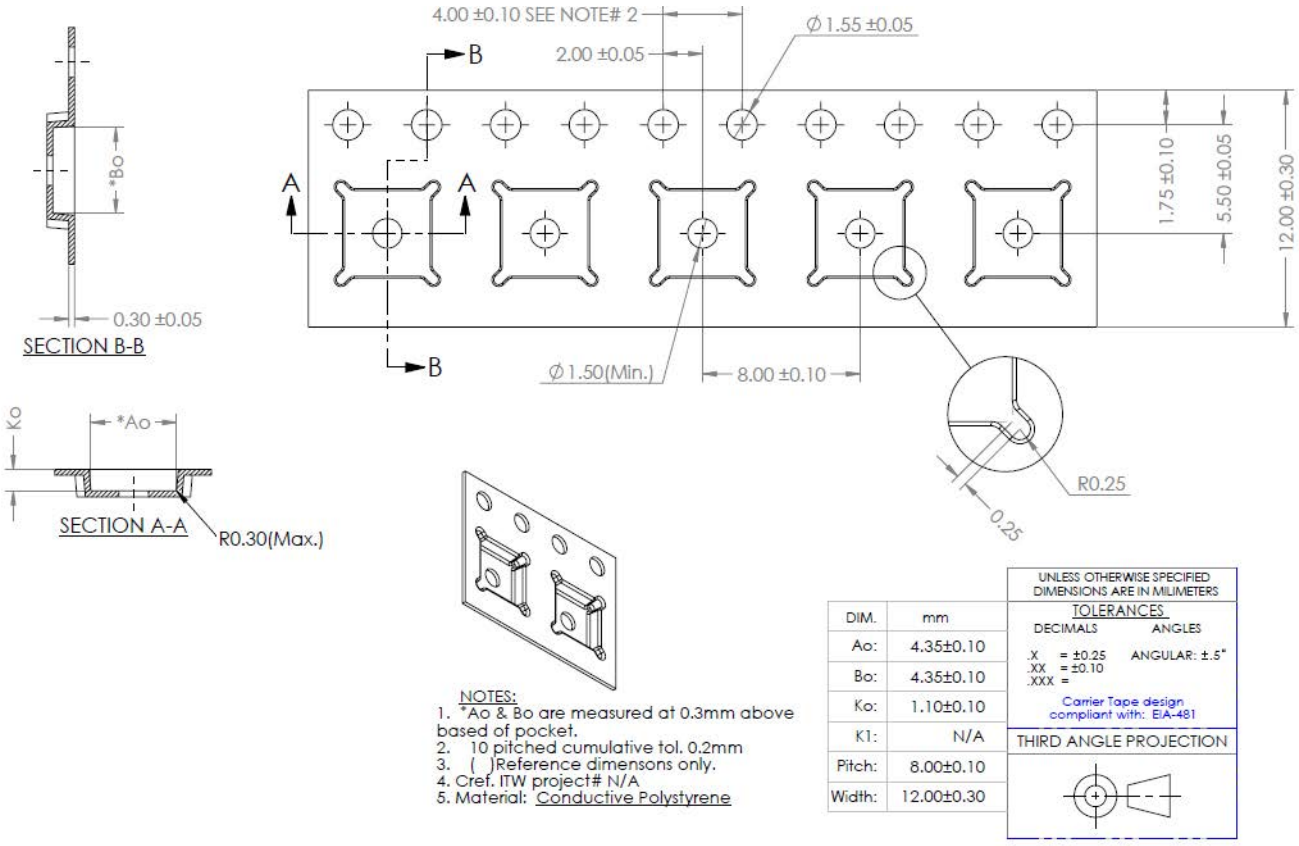


Figure 35: AEAT-9922 Series Package Marking

Table 13: AEAT-9922 Series Package Marking

Row	Length	Description
1	9 digits	Product part number
2	4 digits	Manufacturing date code, “YY” is year, “WW” is work week
3	6 digits	Wafer batch number

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