NTS0304E

4-bit dual supply translating transceiver; open drain; auto direction sensing

Rev. 1 — 01 February 2019 Product data sheet

1. General description

The NTS0304E is a 4-bit, dual supply translating transceiver family with auto direction sensing, that enables bidirectional voltage level translation. It features eight 1-bit input-output ports (A and B), one output enable input (OE) and two supply pins ($V_{CC(A)}$ and $V_{CC(B)}$). $V_{CC(A)}$ can be supplied at any voltage between 0.95 V and 3.6 V. $V_{CC(B)}$ can be supplied at any voltage between 1.65 V and 5.5 V. This flexibility makes the device suitable for translating between any of the voltage nodes (0.95 V, 1.2 V, 1.8 V, 2.5 V, 3.3 V and 5.0 V). Pins A and OE are referenced to $V_{CC(A)}$ and pin B is referenced to $V_{CC(B)}$. A LOW level at pin OE causes the outputs to assume a high-impedance OFF-state.

2. Features and benefits

- Wide supply voltage range:
  - $V_{CC(A)}$: 0.95 V to 3.6 V and $V_{CC(B)}$: 1.65 V to 5.5 V
- No power-sequencing required
- Maximum data rate
  - Open-drain: 2 Mbps
  - Push-pull: 20 Mbps
- Longer one-shot pulse for driving larger capacitive loads with much reduced ringing and overshoot
- A-side and OE inputs accept voltages up to 3.6 V and are 3.6 V tolerant
- B-side inputs accept voltages up to 5.5 V and are 5.5 V tolerant
- ESD protection:
  - IEC 61000-4-2 Class 4, 8 kV contact for B-side port
  - HBM JESD22-A114E Class 2 exceeds 2000 V for both ports
  - CDM JESD22-C101E exceeds 1000 V for both ports
- Latch-up performance exceeds 100 mA per JESD 78B Class II
- Package options: TSSOP14 and WLCSP12
- Specified from –40 °C to +125 °C

3. Applications

- I^2C/SMBus, UART
- GPIO

4. Ordering information

Table 1. Ordering information

Type number	Topside marking	Package		
		Name	Description	Version
NTS0304EUK	S4	WLCSP12	wafer level chip scale package; 12 balls with 0.4 mm pitch; 1.42 x 1.97 x 0.525 mm	SOT1390-10
NTS0304EPW	NTS0304	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1

4.1 Ordering options

Table 2. Ordering options

Type number	Orderable part number	Package	Packing method	Minimum order quantity	Temperature
NTS0304EUK	NTS0304EUKZ	WLCSP12	reel 7" q1/t1 *special mark chips dp	4000	T_{amb} = –40 °C to +125 °C
NTS0304EPW	NTS0304EPWJ	TSSOP14	reel 13" q1/t1 *standard mark smd	2500	T_{amb} = –40 °C to +125 °C

5. Functional diagram

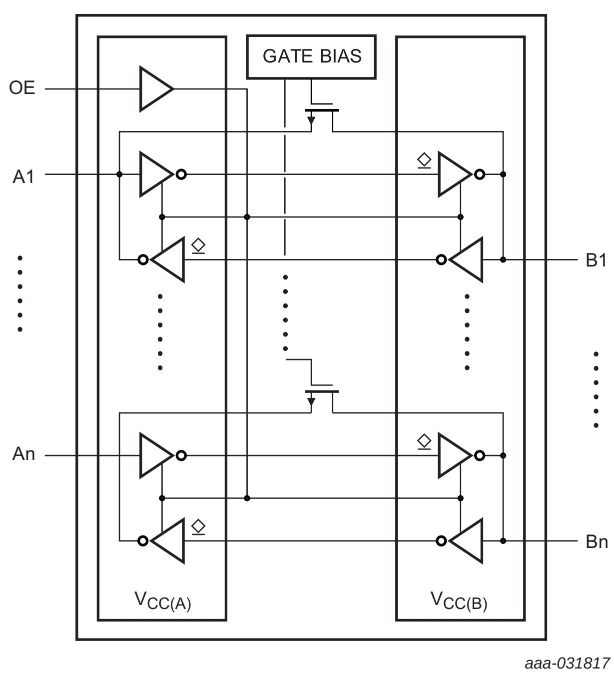


Fig 1. Logic symbol

6. Pinning information

6.1 Pinning

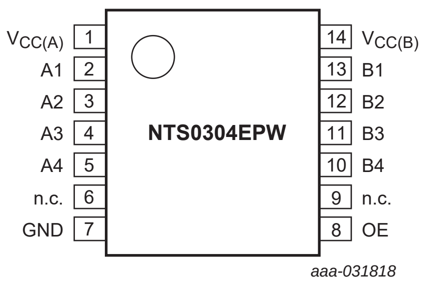


Fig 2. NTS0304EPW Pin configuration

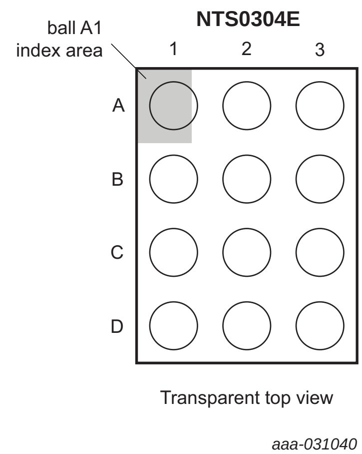


Fig 3. NTS0304EUK Pin configuration WLCSP12

6.2 Pin description

Table 3. NTS0304E Pin description

Symbol	Pin	Ball	Description
	SOT402-1	WLCSP12	
$V_{CC(A)}$	1	B2	supply voltage A
A1, A2, A3, A4	2, 3, 4, 5	A3, B3, C3, D3	data input or output (referenced to $V_{CC(A)}$)
n.c.	6, 9	-	not connected
GND	7	D2	ground (0 V)
OE	8	C2	output enable input (active HIGH; referenced to $V_{CC(A)}$)
B4, B3, B2, B1	10, 11, 12, 13	D1, C1, B1, A1	data input or output (referenced to $V_{CC(B)}$)
$V_{CC(B)}$	14	A2	supply voltage B

7. Functional description

Table 4. Function table[1]

Supply voltage		Input	Input/output	
$V_{CC(A)}$	$V_{CC(B)}$	OE	A	B
0.95 V to $V_{CC(B)}$	1.65 V to 5.5 V	L	Z	Z
0.95 V to $V_{CC(B)}$	1.65 V to 5.5 V	H	input or output	output or input
GND[2]	GND[2]	X	Z	Z

[1] H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state.

[2] When either $V_{CC(A)}$ or $V_{CC(B)}$ is at GND level, the device goes into power-down mode.

8. Limiting values

Table 5. Limiting values
In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC(A)}$	supply voltage A		–0.5	+4.6	V
$V_{CC(B)}$	supply voltage B		–0.5	+6.5	V
V_I	input voltage	A port and OE input [1][2]	–0.5	+6.5	V
		B port [1][2]	–0.5	+6.5	V
V_O	output voltage	Active mode [1][2]			
		A or B port	–0.5	V_{CCO} + 0.5	V
		Power-down or 3-state mode [1]			
		A port	–0.5	+4.6	V
		B port	–0.5	+6.5	V
I_{IK}	input clamping current	V_I < 0 V	–50	-	mA
I_{OK}	output clamping current	V_O < 0 V	–50	-	mA
I_O	output current	V_O = 0 V to V_{CCO} [2]	-	±50	mA
I_{CC}	supply current	$I_{CC(A)}$ or $I_{CC(B)}$	-	100	mA
I_{GND}	ground current		–100	-	mA
T_{stg}	storage temperature		–65	+150	°C

[1] The minimum input and minimum output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] V_{CCO} is the supply voltage associated with the output.

9. Recommended operating conditions

Table 6. Recommended operating conditions[1][2]

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC(A)}$	supply voltage A	[2]	0.95	3.6	V
$V_{CC(B)}$	supply voltage B		1.65	5.5	V
V_{I_EN}	EN input voltage		-0.3	$V_{CC(A)}$+0.3	V
T_{amb}	ambient temperature		–40	+125	°C
T_J	junction temperature	[3]	–40	+85	°C
$\Delta t/\Delta V$	input transition rise and fall rate	A or B port; push-pull driving			
		$V_{CC(A)}$ = 0.95 V to 3.6 V; $V_{CC(B)}$ = 1.65 V to 5.5 V [2]	-	10	ns/V
		OE input			
		$V_{CC(A)}$ = 0.95 V to 3.6 V; $V_{CC(B)}$ = 1.65 V to 5.5 V	-	10	ns/V

[1] The A and B sides of an unused I/O pair must be held in the same state, both at V_{CCI} or both at GND.

[2] $V_{CC(A)}$ must be less than or equal to $V_{CC(B)}$.

[3] The T_J limits shall be supported by proper thermal PCB design taking the power consumption and the thermal resistance as listed in Table 7 into account.

10. Thermal characteristics

Table 7. Thermal resistance information

Symbol	Rating	NTS0304EPW (TSSOP14)	NTS0304EUK (WLCSP12)
$R_{\theta JA}$	Junction to ambient	114.9	57.8
ψ_{JT}	Junction to top characterization	1.6	0.2

11. Static characteristics

Table 8. Typical static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V); T_{amb} = 25 °C.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
I_I	input leakage current	OE input; V_I = 0 V to 3.6 V; $V_{CC(A)}$ = 0.95 V to 3.6 V; $V_{CC(B)}$ = 1.65 V to 5.5 V		-	-	±1	μA
I_{OZ}	OFF-state output current	A or B port; V_O = 0 V or V_{CCO}; $V_{CC(A)}$ = 0.95 V to 3.6 V; $V_{CC(B)}$ = 1.65 V to 5.5 V	[1]	-	-	±1	μA
C_I	input capacitance	OE input; $V_{CC(A)}$ = 3.3 V; $V_{CC(B)}$ = 3.3 V		-	1	-	pF
$C_{I/O}$	input/output capacitance	A port		-	4	-	pF
		B port		-	7.5	-	pF
		A or B port; $V_{CC(A)}$ = 3.3 V; $V_{CC(B)}$ = 3.3 V		-	11	-	pF

[1] V_{CCO} is the supply voltage associated with the output.

Table 9. Typical supply current

At recommended operating conditions; voltages are referenced to GND (ground = 0 V); T_{amb} = 25 °C.

$V_{CC(A)}$	$V_{CC(B)}$								Unit
	1.65 V		2.5 V		3.3 V		5.0 V		
	$I_{CC(A)}$	$I_{CC(B)}$	$I_{CC(A)}$	$I_{CC(B)}$	$I_{CC(A)}$	$I_{CC(B)}$	$I_{CC(A)}$	$I_{CC(B)}$	
0.95 V	0.1	0.1	0.1	0.5	0.1	0.5	0.1	3	μA
1.2 V	0.1	0.1	0.1	0.5	0.1	0.5	0.1	3	μA
1.8 V	-	-	0.1	0.5	0.1	0.5	0.1	3	μA
2.5 V	-	-	0.2	0.5	0.1	0.5	0.1	3	μA
3.3 V	-	-	-	-	0.1	0.1	0.1	2	μA

Table 10. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		–40 °C to +85 °C		–40 °C to +125 °C		Unit
				Min	Max	Min	Max	
V_{IH}	HIGH-level input voltage	A port						
		$V_{CC(A)}$ = 0.95 V to 1.65 V; $V_{CC(B)}$ = 1.65 V to 5.5 V	[1]	V_{CCI} – 0.2	-	V_{CCI} – 0.2	-	V
		$V_{CC(A)}$ = 1.65 V to 3.6 V; $V_{CC(B)}$ = 2.3 V to 5.5 V	[1]	V_{CCI} – 0.4	-	V_{CCI} – 0.4	-	V
		B port						
		$V_{CC(A)}$ = 0.95 V to 3.6 V; $V_{CC(B)}$ = 1.65 V to 5.5 V	[1]	V_{CCI} – 0.4	-	V_{CCI} – 0.4	-	V
		OE input						
		$V_{CC(A)}$ = 0.95 V to 3.6 V; $V_{CC(B)}$ = 1.65 V to 5.5 V		$0.65V_{CC(A)}$	-	$0.65V_{CC(A)}$	-	V
V_{IL}	LOW-level input voltage	A or B port						
		$V_{CC(A)}$ = 0.95 V to 1.65 V; $V_{CC(B)}$ = 1.65 V to 5.5 V		-	0.13	-	0.13	V
		$V_{CC(A)}$ = 1.65 V to 3.6 V; $V_{CC(B)}$ = 2.3 V to 5.5 V		-	0.15	-	0.15	V
		OE input						
		$V_{CC(A)}$ = 0.95 V to 3.6 V; $V_{CC(B)}$ = 1.65 V to 5.5 V		-	$0.35V_{CC(A)}$	-	$0.35V_{CC(A)}$	V
V_{OHA}	HIGH-level output voltage	I_O = –20 μA						
		$V_{CC(B)}$ = 1.65 V to 5.5 V; V_{CCI} = $V_{CC(B)}$ - 0.4 V	[2]					
		$V_{CC(A)}$ = 1.65 V to 3.6 V	[2]	$0.8V_{CC(A)}$	-	$0.75V_{CC(A)}$	-	V
		$V_{CC(A)}$ = 0.95 V to 1.65 V	[2]	$0.65V_{CC(A)}$	-	$0.62V_{CC(A)}$	-	V
V_{OHB}	HIGH-level output voltage	I_O = –20 μA						
		$V_{CC(A)}$ = 0.95 V to 3.6 V; $V_{CC(B)}$ = 1.65 V to 5.5 V; V_{CCI} = $V_{CC(A)}$ - 0.2 V	[2]	$0.8V_{CC(B)}$	-	$0.75V_{CC(B)}$	-	V
V_{OL}	LOW-level output voltage	A or B port; I_O = 1 mA	[2]					
		$V_I \leq 0.15$ V; $V_{CC(A)}$ = 0.95 V to 3.6 V; $V_{CC(B)}$ = 1.65 V to 5.5 V		-	0.30	-	0.30	V
I_I	input leakage current	OE input; V_I = 0 V to 3.6 V; $V_{CC(A)}$ = 0.95 V to 3.6 V; $V_{CC(B)}$ = 1.65 V to 5.5 V		-	±2	-	±12	μA
I_{OZ}	OFF-state output current	A or B port; V_O = 0 V or V_{CCO}; $V_{CC(A)}$ = 0.95 V to 3.6 V; $V_{CC(B)}$ = 1.65 V to 5.5 V	[2]	-	±2	-	±12	μA

Table 10. Static characteristics *...continued*
At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		–40 °C to +85 °C		–40 °C to +125 °C		Unit
				Min	Max	Min	Max	
I_{CC}	supply current	V_I = 0 V or V_{CCI}; I_O = 0 A	[1]					
		$I_{CC(A)}$						
		$V_{CC(A)}$ = 0.95 V to 3.6 V; $V_{CC(B)}$ = 1.65 V to 5.5 V		-	2.4	-	15	μA
		$V_{CC(A)}$ = 3.6 V; $V_{CC(B)}$ = 0 V		-	2.2	-	15	μA
		$V_{CC(A)}$ = 0 V; $V_{CC(B)}$ = 5.5 V		-	–1	-	–8	μA
		$I_{CC(B)}$						
		$V_{CC(A)}$ = 0.95 V to 3.6 V; $V_{CC(B)}$ = 1.65 V to 5.5 V		-	18	-	51	μA
		$V_{CC(A)}$ = 3.6 V; $V_{CC(B)}$ = 0 V		-	–1	-	–5	μA
		$V_{CC(A)}$ = 0 V; $V_{CC(B)}$ = 5.5 V		-	18	-	46	μA
		$I_{CC(A)} + I_{CC(B)}$						
		$V_{CC(A)}$ = 0.95 V to 3.6 V; $V_{CC(B)}$ = 1.65 V to 5.5 V		-	14.4	-	59	μA

[1] V_{CCI} is the supply voltage associated with the input.

[2] V_{CCO} is the supply voltage associated with the output.

12. Dynamic characteristics

Table 11. Dynamic characteristics for temperature range −40 °C to +125 °C[1]

Voltages are referenced to GND (ground = 0 V); for test circuit, see Figure 6; for wave forms, see Figure 4 and Figure 5.

Symbol	Parameter	Conditions		$V_{CC(B)}$						Unit
				1.8 V		3.3 V		5.0 V		
				Min	Max	Min	Max	Min	Max	
$V_{CC(A)}$ = 0.95V										
t_{PHL}	HIGH to LOW propagation delay	A to B		-	20	-	11.1	-	12.3	ns
t_{PLH}	LOW to HIGH propagation delay	A to B		-	14.8	-	12.5	-	12.2	ns
t_{PHL}	HIGH to LOW propagation delay	B to A		-	9.2	-	5.2	-	5.2	ns
t_{PLH}	LOW to HIGH propagation delay	B to A		-	8.8	-	2.9	-	1.4	ns
t_{en}	enable time	OE to A; B		-	200	-	200	-	200	ns
t_{dis}	disable time	OE to A; no external load	[2]	-	100	-	100	-	100	ns
		OE to B; no external load	[2]	-	100	-	100	-	100	ns
		OE to A		-	250	-	250	-	250	ns
		OE to B		-	220	-	220	-	220	ns
t_{TLH}	LOW to HIGH output transition time	A port		6.0	15.3	2.2	15.1	1.8	11.1	ns
		B port		6.0	17.0	4.0	14.0	4.0	20.0	ns
t_{THL}	HIGH to LOW output transition time	A port		0.9	18.0	0.7	9.0	0.6	9.0	ns
		B port		1.6	22.0	2.8	10.7	3.2	14.2	ns
t_W	pulse width	data inputs		49	-	49	-	49	-	ns
f_{data}	data rate		[3]	-	20	-	20	-	20	Mbps

[1] t_{en} is the same as t_{PZL} and t_{PZH}.
t_{dis} is the same as t_{PLZ} and t_{PHZ}.

[2] Delay between OE going LOW and when the outputs are disabled.

[3] Assuming a maximum one-shot accelerator pulse length of 50ns and equal time for 1 and 0 bit information

Table 12. Dynamic characteristics for temperature range −40 °C to +125 °C[1]
Voltages are referenced to GND (ground = 0 V); for test circuit, see Figure 6; for wave forms, see Figure 4 and Figure 5.

Symbol	Parameter	Conditions		$V_{CC(B)}$						Unit
				2.5 V		3.3 V		5.0 V		
				Min	Max	Min	Max	Min	Max	
$V_{CC(A)}$ = 1.8 V										
t_{PHL}	HIGH to LOW propagation delay	A to B		-	5.8	-	5.9	-	7.3	ns
t_{PLH}	LOW to HIGH propagation delay	A to B		-	8.5	-	8.5	-	8.8	ns
t_{PHL}	HIGH to LOW propagation delay	B to A		-	5.5	-	5.7	-	5.9	ns
t_{PLH}	LOW to HIGH propagation delay	B to A		-	6.7	-	5.7	-	1.4	ns
t_{en}	enable time	OE to A; B		-	200	-	200	-	200	ns
t_{dis}	disable time	OE to A; no external load	[2]	-	100	-	100	-	100	ns
		OE to B; no external load	[2]	-	100	-	100	-	100	ns
		OE to A		-	250	-	250	-	250	ns
		OE to B		-	220	-	220	-	220	ns
t_{TLH}	LOW to HIGH output transition time	A port		3.2	11.9	1.2	11.7	1.1	9.5	ns
		B port		3.3	13.5	2.7	14.5	2.7	13.5	ns
t_{THL}	HIGH to LOW output transition time	A port		1.2	7.4	1.0	7.5	1.0	16.7	ns
		B port		2.6	9.5	2.2	9.4	2.8	12.5	ns
t_W	pulse width	data inputs		49	-	49	-	49	-	ns
f_{data}	data rate		[3]	-	20	-	20	-	20	Mbps
$V_{CC(A)}$ = 2.5 V										
t_{PHL}	HIGH to LOW propagation delay	A to B		-	4.0	-	4.2	-	4.3	ns
t_{PLH}	LOW to HIGH propagation delay	A to B		-	4.4	-	5.2	-	5.5	ns
t_{PHL}	HIGH to LOW propagation delay	B to A		-	3.8	-	4.5	-	5.4	ns
t_{PLH}	LOW to HIGH propagation delay	B to A		-	3.2	-	2.0	-	1.5	ns
t_{en}	enable time	OE to A; B		-	200	-	200	-	200	ns
t_{dis}	disable time	OE to A; no external load	[2]	-	100	-	100	-	100	ns
		OE to B; no external load	[2]	-	100	-	100	-	100	ns
		OE to A		-	220	-	220	-	220	ns
		OE to B		-	220	-	220	-	220	ns
t_{TLH}	LOW to HIGH output transition time	A port		2.8	10	1.4	8.3	1.2	7.8	ns
		B port		3.2	10.4	2.9	15.5	2.4	16.9	ns
t_{THL}	HIGH to LOW output transition time	A port		1.0	7.2	1.0	6.9	1.0	6.7	ns
		B port		2.2	9.8	2.4	8.4	2.6	8.3	ns

Table 12. Dynamic characteristics for temperature range –40 °C to +125 °C[1] *…continued*

Voltages are referenced to GND (ground = 0 V); for test circuit, see Figure 6; for wave forms, see Figure 4 and Figure 5.

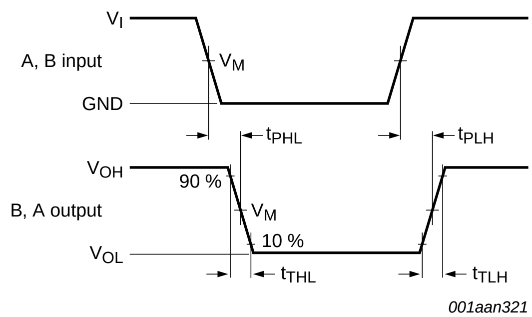
Symbol	Parameter	Conditions		$V_{CC(B)}$						Unit
				2.5 V		3.3 V		5.0 V		
				Min	Max	Min	Max	Min	Max	
t_W	pulse width	data inputs		49	-	49	-	49	-	ns
f_{data}	data rate		[3]	-	20	-	20	-	20	Mbps
$V_{CC(A)}$ = 3.3 V										
t_{PHL}	HIGH to LOW propagation delay	A to B		-	-	-	3.0	-	3.9	ns
t_{PLH}	LOW to HIGH propagation delay	A to B		-	-	-	5.3	-	5.5	ns
t_{PHL}	HIGH to LOW propagation delay	B to A		-	-	-	3.2	-	4.2	ns
t_{PLH}	LOW to HIGH propagation delay	B to A		-	-	-	3.2	-	3.3	ns
t_{en}	enable time	OE to A; B		-	-	-	200	-	200	ns
t_{dis}	disable time	OE to A; no external load	[2]	-	-	-	100	-	100	ns
		OE to B; no external load	[2]	-	-	-	100	-	100	ns
		OE to A		-	-	-	280	-	280	ns
		OE to B		-	-	-	220	-	220	ns
t_{TLH}	LOW to HIGH output transition time	A port		-	-	1.2	13.1	1.1	7.4	ns
		B port		-	-	2.5	14.2	2.1	16.0	ns
t_{THL}	HIGH to LOW output transition time	A port		-	-	1.0	6.8	1.0	6.3	ns
		B port		-	-	2.3	9.3	2.4	9.5	ns
t_W	pulse width	data inputs		-	-	49	-	49	-	ns
f_{data}	data rate		[3]	-	-	-	20	-	20	Mbps

[1] t_{en} is the same as t_{PZL} and t_{PZH}.
t_{dis} is the same as t_{PLZ} and t_{PHZ}.

[2] Delay between OE going LOW and when the outputs are disabled.

[3] Assuming a maximum one-shot accelerator pulse length of 50ns and equal time for 1 and 0 bit information

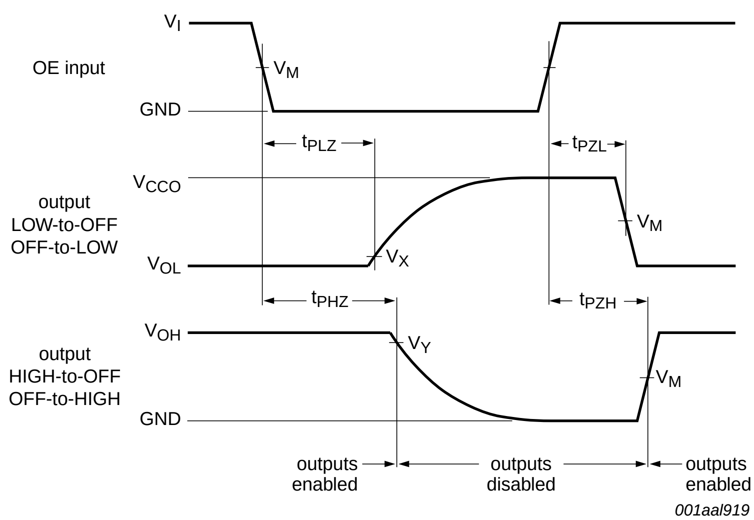
13. Waveforms



Measurement points are given in Table 13.

V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig 4. The data input (A, B) to data output (B, A) propagation delay times



Measurement points are given in Table 13.

V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

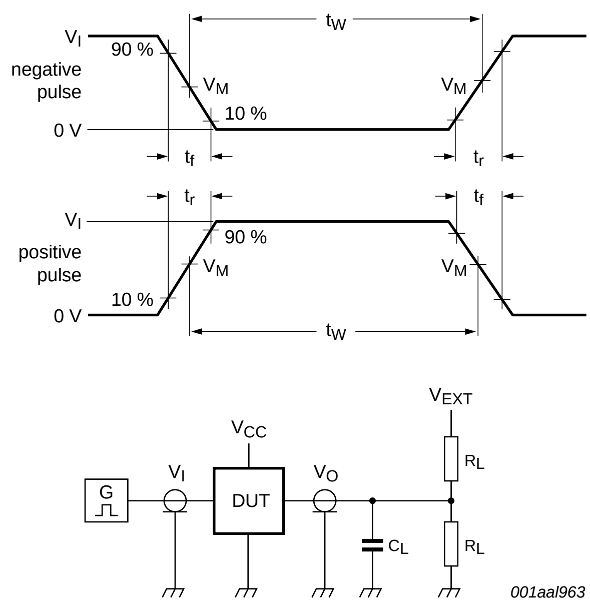
Fig 5. Enable and disable times

Table 13. Measurement points[1][2]

Supply voltage	Input	Output		
V_{CCO}	V_M	V_M	V_X	V_Y
0.95 V	$0.5V_{CCI}$	$0.5V_{CCO}$	V_{OL} + 0.1 V	V_{OH} − 0.1 V
1.8 V ± 0.15 V	$0.5V_{CCI}$	$0.5V_{CCO}$	V_{OL} + 0.15 V	V_{OH} − 0.15 V
2.5 V ± 0.2 V	$0.5V_{CCI}$	$0.5V_{CCO}$	V_{OL} + 0.15 V	V_{OH} − 0.15 V
3.3 V ± 0.3 V	$0.5V_{CCI}$	$0.5V_{CCO}$	V_{OL} + 0.3 V	V_{OH} − 0.3 V
5.0 V ± 0.5 V	$0.5V_{CCI}$	$0.5V_{CCO}$	V_{OL} + 0.3 V	V_{OH} − 0.3 V

[1] V_{CCI} is the supply voltage associated with the input.

[2] V_{CCO} is the supply voltage associated with the output.



Test data is given in Table 14.

All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz; Z_O = 50 Ω; dV/dt ≥ 1.0 V/ns.

R_L = Load resistance.

C_L = Load capacitance including jig and probe capacitance.

V_{EXT} = External voltage for measuring switching times.

Fig 6. Test circuit for measuring switching times

Table 14. Test data

Supply voltage		Input		Load		V_{EXT}		
$V_{CC(A)}$	$V_{CC(B)}$	V_I[1]	Δt/ΔV	C_L	R_L[2]	t_{PLH}, t_{PHL}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}[3]
0.95 V to 3.6 V	1.65 V to 5.5 V	V_{CCI}	≤ 1.0 ns/V	15 pF	50 kΩ, 1 MΩ	open	open	$2V_{CCO}$

[1] V_{CCI} is the supply voltage associated with the input.

[2] For measuring data rate, pulse width, propagation delay and output rise and fall measurements, R_L = 1 MΩ. For measuring enable and disable times, R_L = 50 KΩ.

[3] V_{CCO} is the supply voltage associated with the output.

14. Application information

14.1 Applications

Voltage level-translation applications. The NTS0304E can be used in point-to-point applications to interface between devices or systems operating at different supply voltages. The device is primarily targeted at I^2C or 4-wire which use open-drain drivers. It may also be used in applications where push-pull drivers are connected to the ports, however the NTB010x or the newer lower voltage NTB030x series of devices are more suitable.

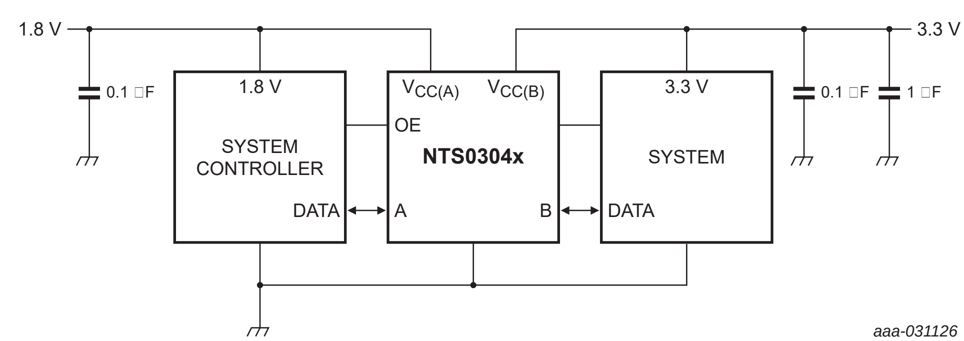


Fig 7. Typical operating circuit

14.2 Architecture

The architecture of the NTS0304E is shown in Figure 8. The device does not require an extra input signal to control the direction of data flow from A to B or B to A.

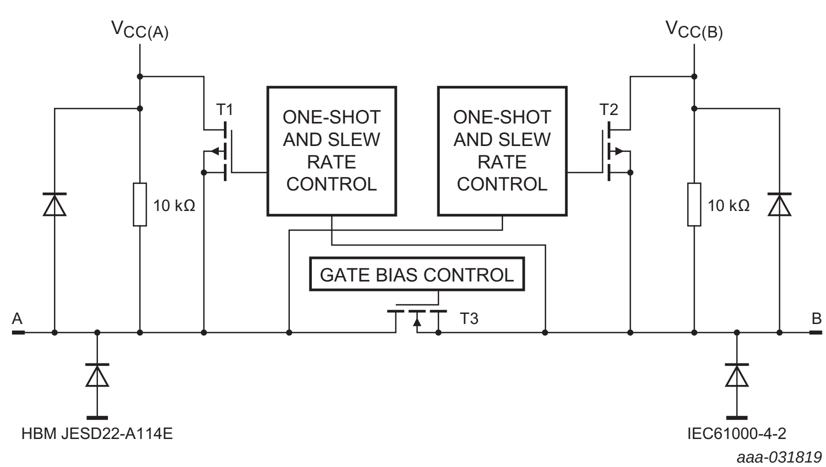


Fig 8. Architecture of NTS0304E I/O cell

The NTS0304E is a “switch” type voltage translator, it employs two key circuits to enable voltage translation:

1. A pass-gate transistor (N-channel) that ties the ports together.

2. An output edge-rate accelerator that detects and accelerates rising edges on the I/O pins.

The gate bias voltage of the pass gate transistor (T3) is set at approximately one threshold voltage above the V_{CC} level of the low-voltage side. During a LOW-to-HIGH transition, the output one-shot accelerates the output transition by switching on the PMOS transistors (T1, T2). It bypasses the 10 kΩ pull-up resistors and increases the current drive capability. The one-shot is activated once the input transition reaches approximately $V_{CCI}/2$; it is deactivated approximately 50 ns after the output reaches $V_{CCO}/2$. During the acceleration time, the driver output resistance is between approximately 50 Ω and 70 Ω. To avoid signal contention and minimize dynamic I_{CC}, the user should wait for the one-shot circuit to turn-off before applying a signal in the opposite direction. Pull-up resistors are included in the device for DC current sourcing capability.

14.3 Input driver requirements

As the NTS0304E is a switch type translator, properties of the input driver directly effect the output signal. The external open-drain or push-pull driver applied to an I/O determines the static current sinking capability of the system. The max data rate, HIGH-to-LOW output transition time (t_{THL}), and propagation delay (t_{PHL}), are dependent upon the output impedance and edge-rate of the external driver. The limits provided for these parameters in the data sheet assume a driver with output impedance below 50 Ω is used.

14.4 Output load considerations

The maximum lumped capacitive load that can be driven is dependent upon the one-shot pulse duration. In cases with very heavy capacitive loading, there is a risk that the output does not reach the positive rail within the one-shot pulse duration. The NTS0304E has a longer one-shot pulse for driving larger capacitive loads.

To avoid excessive capacitive loading and to ensure correct triggering of the one-shot, use short trace lengths and low capacitance connectors on NTS0304E PCB layouts. The length of the PCB trace should be such that the round-trip delay of any reflection is within the one-shot pulse duration (approximately 50 ns). It ensures low impedance termination and avoids output signal oscillations and one-shot retriggering.

14.5 Output single shot slew rate control

Integrated slew-rate control and timed increase of the one-shot driver output current reduce EMI. An additional comparator circuit on the V_{OUT} side starts to reduce the one-shot driver current when $V_{OUT} > 0.65V_{OUT}$ with a slight delay, so it can safely drive the output voltage to a safe high-level while at the same time reducing the driver strength early enough to reduce overshoots and ringing.

14.6 Power-up

During operation, $V_{CC(A)}$ must never be higher than $V_{CC(B)}$. However, during power-up, $V_{CC(A)} \geq V_{CC(B)}$ does not damage the device, so either power supply can be ramped up first. There is no special power-up sequencing required. The NTS0304E includes circuitry that disables all output ports when either $V_{CC(A)}$ or $V_{CC(B)}$ is switched off.

14.7 Enable and disable

An output enable input (OE) is used to disable the device. Setting OE = LOW causes all I/Os to assume the high-impedance OFF-state. The disable time (t_{dis} with no external load) indicates the delay between when OE goes LOW and when outputs actually become disabled. The enable time (t_{en}) indicates the amount of time the user must allow for one one-shot circuitry to become operational after OE is taken HIGH. To ensure the high-impedance OFF-state during power-up or power-down, pin OE should be tied to GND through a pull-down resistor. The current-sourcing capability of the driver determines the minimum value of the resistor.

14.8 Pull-up or pull-down resistors on I/Os lines

The A port I/O has an internal 10 kΩ pull-up resistor to $V_{CC(A)}$. The B port I/O has an internal 10 kΩ pull-up resistor to $V_{CC(B)}$. If a smaller value of pull-up resistor is required, add an external resistor in parallel to the internal 10 kΩ. This pull-up resistor effects the V_{OL} level. When OE goes LOW, the internal pull-ups of the NTS0304E are disabled.

14.9 ESD protection on I/Os lines

The NTS0304E contains rail to rail ESD protection structures connecting the A and B I/O to their respective supply. As a consequence, if a supply pin is pulled low, the related I/Os are pulled low too through the upper ESD protection diode and the 10 kΩ pull-up resistor. Additionally, besides the normal HBM and CDM ESD protection features on both A and B Port I/O the B Port I/O features integrated ESD protection to IEC 61000-4-2 Class 4 system ESD level of 8kV contact for when users plug cameras, games, and other items into their USB or video ports in real-world ESD stress applications.

15. Package outline

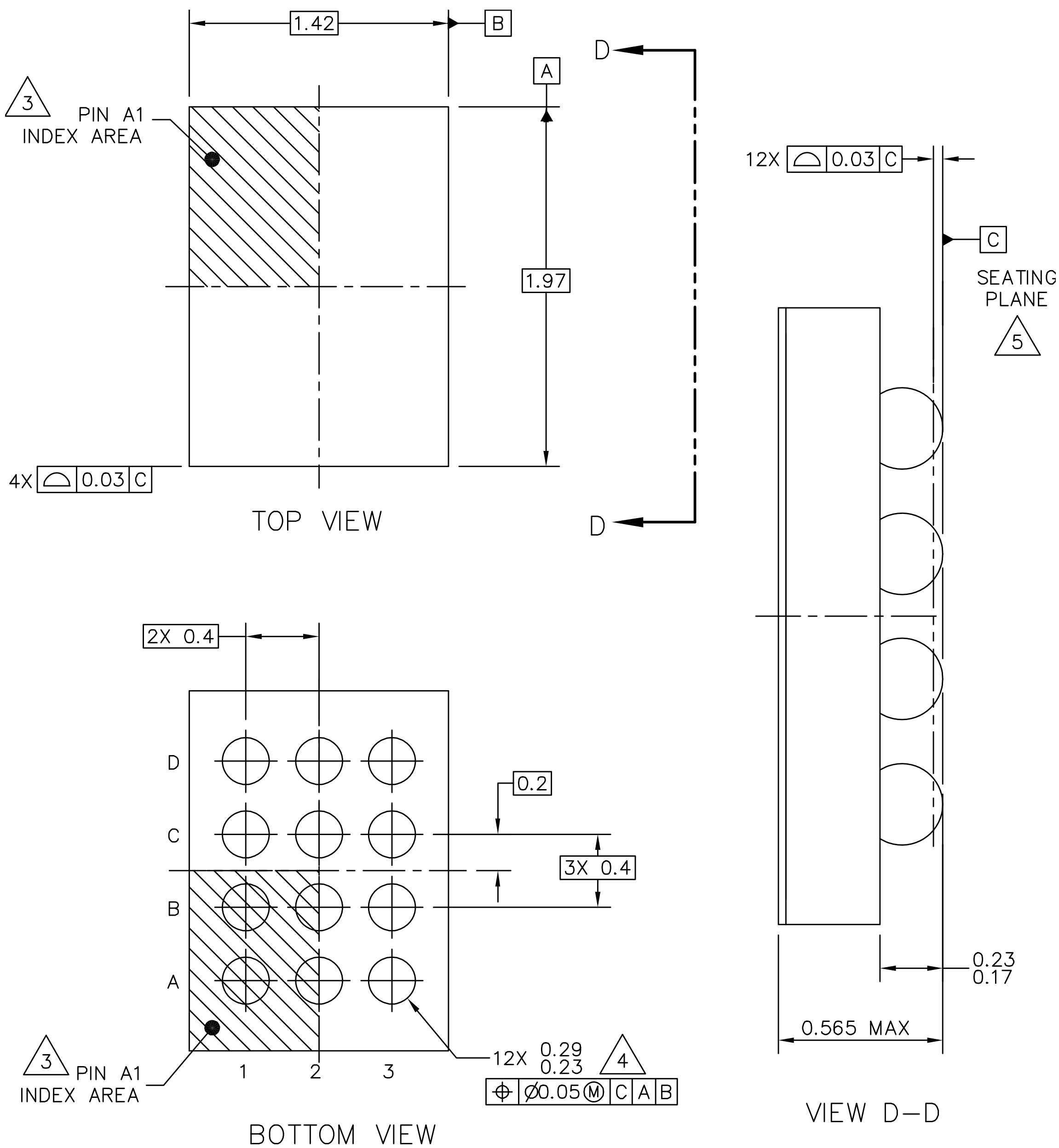


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Fig 9. Package outline SOT1390-10 (WLCSP12) 1 of 2

NOTES:

1. ALL DIMENSIONS IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M—1994.
3. PIN A1 FEATURE SHAPE, SIZE AND LOCATION MAY VARY.
4. MAXIMUM SOLDER BALL DIAMETER MEASURED PARALLEL TO DATUM C.
5. DATUM C, THE SEATING PLANE, IS DETERMINED BY THE SPHERICAL CROWNS OF THE SOLDER BALL
6. THIS PACKAGE HAS A BACK SIDE COATING THICKNESS OF 0.025.

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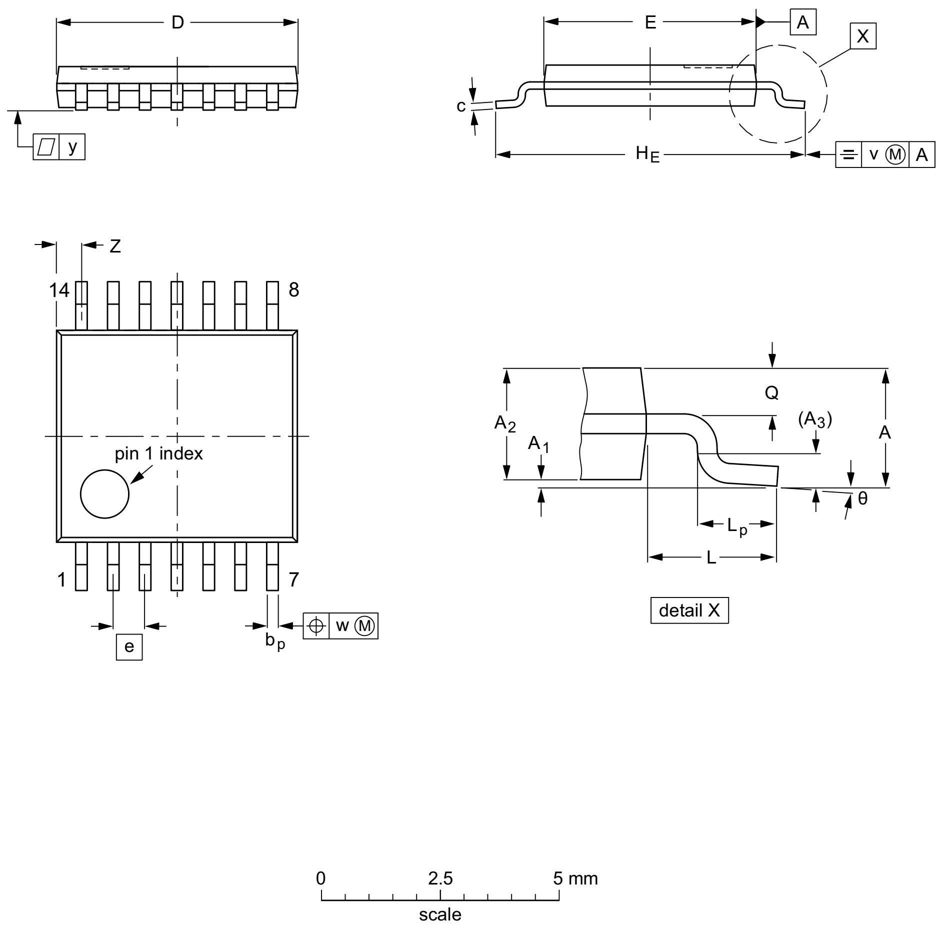
Fig 10. Package outline SOT1390-10 (WLCSP12) 2 of 2

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm **SOT402-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.72 0.38	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT402-1		MO-153				~~99-12-27~~ 03-02-18

Fig 11. NTS0304E Package outline SOT402-1 (TSSOP14)

16. Soldering

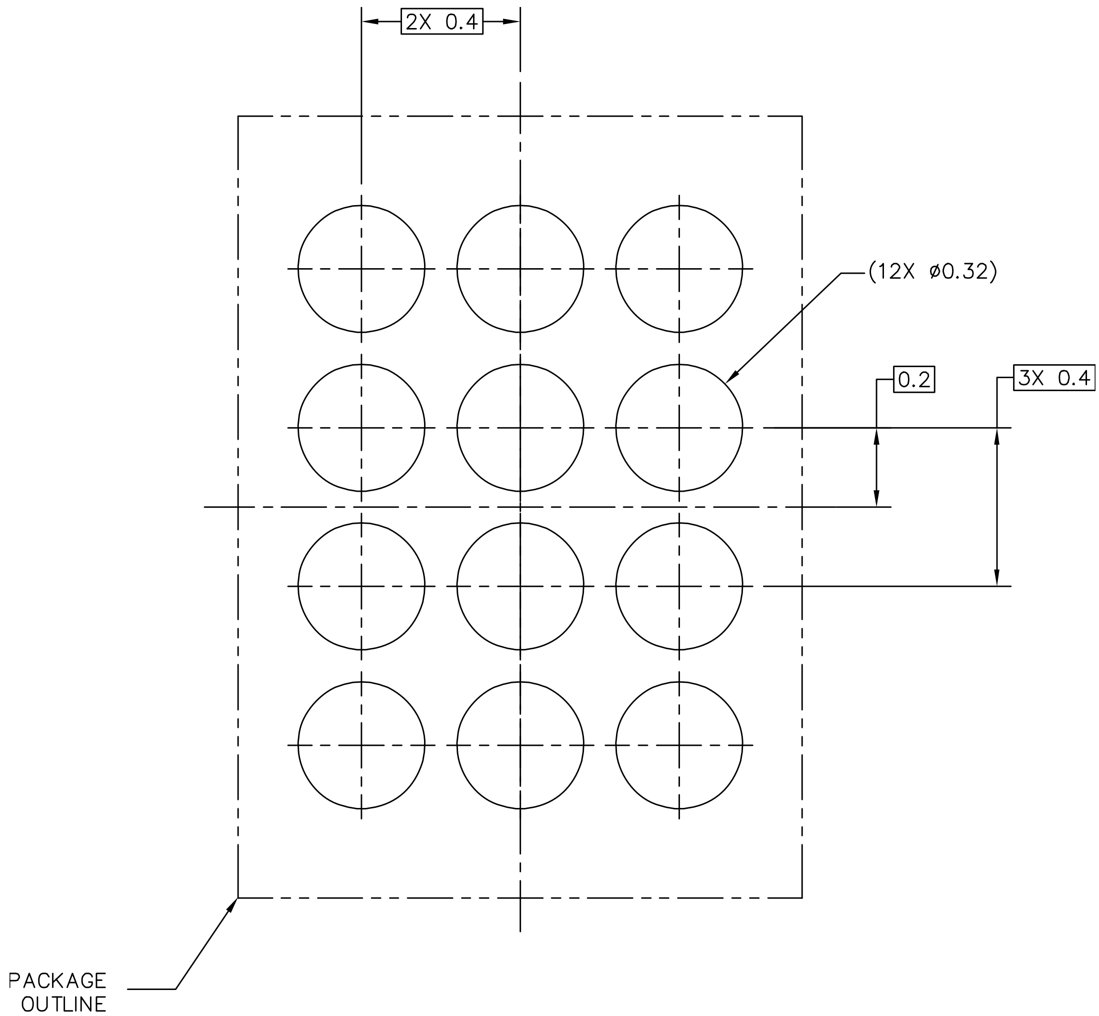


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Fig 12. Soldering footprint for SOT1390-10 (WLCSP12) 1 of 3

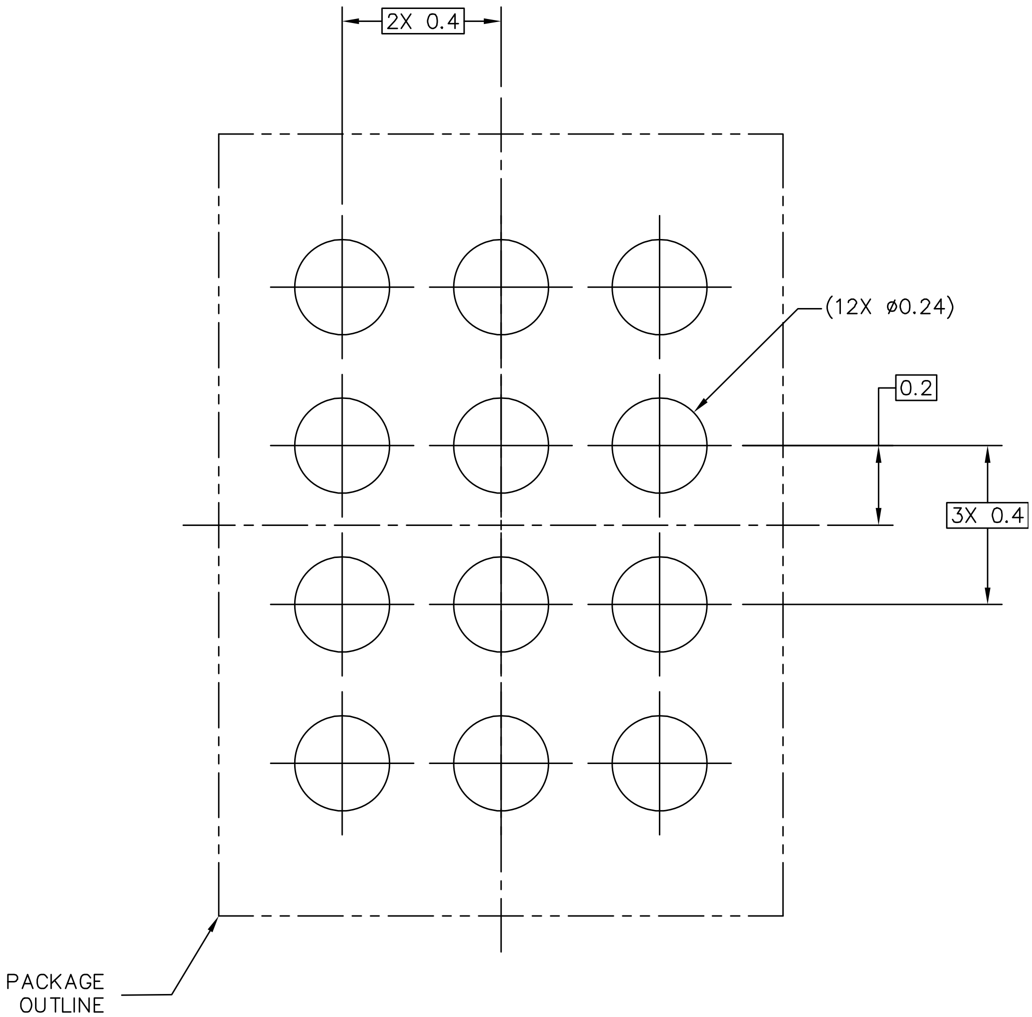

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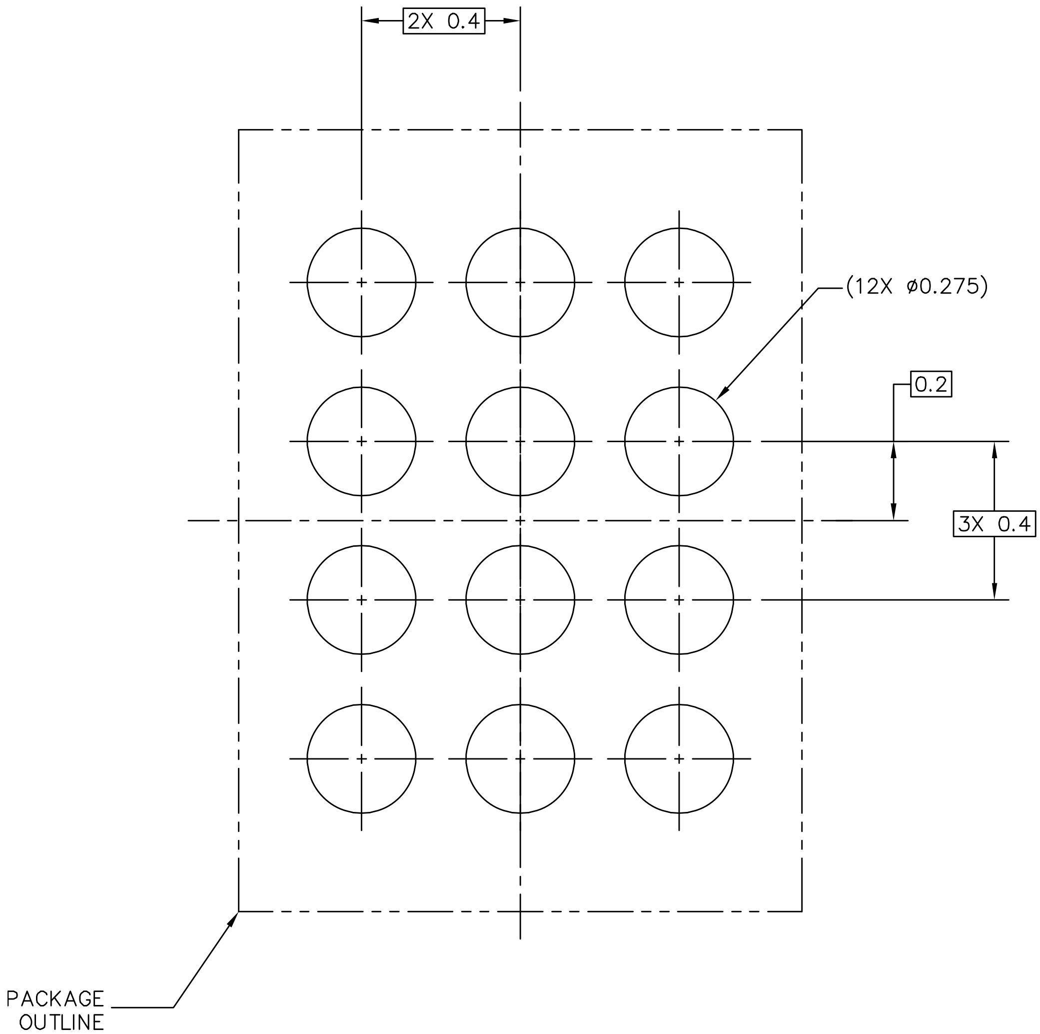
Fig 13. Soldering footprint for SOT1390-10 (WLCSP12) 2 of 3



RECOMMENDED STENCIL THICKNESS 0.1

PCB DESIGN GUIDELINES – SOLDER PASTE STENCIL

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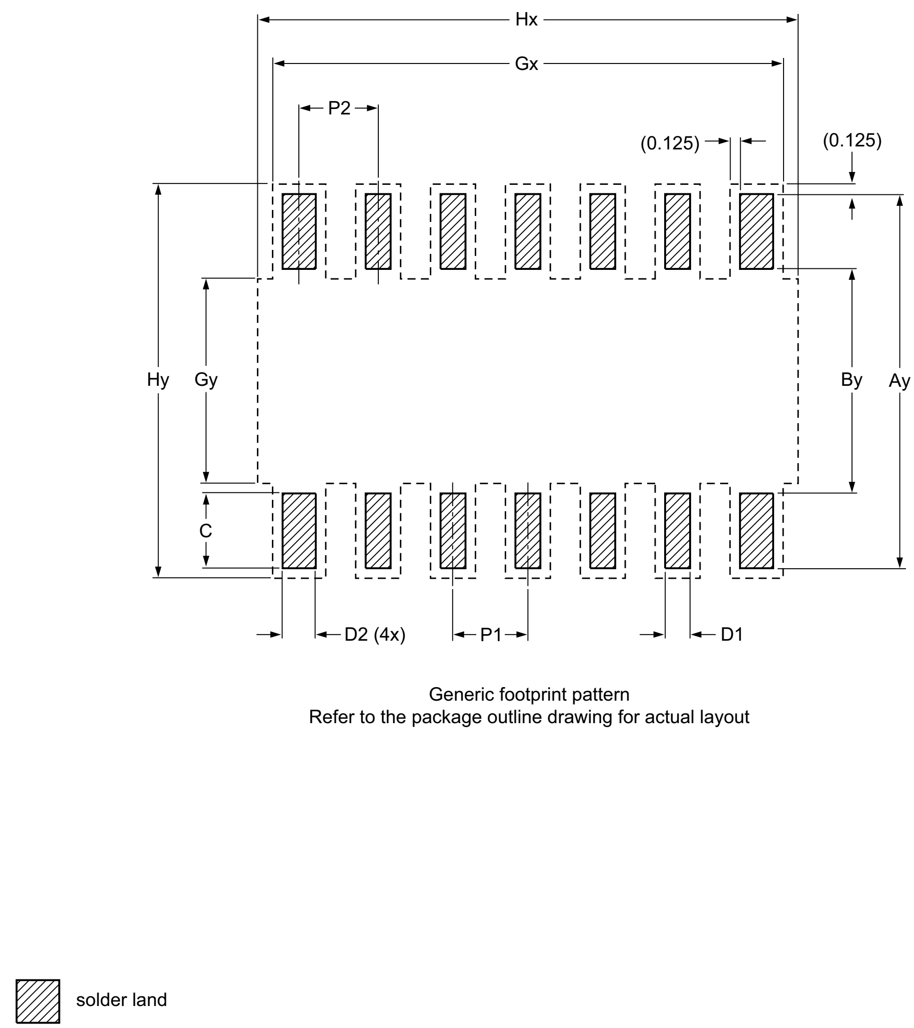
DATE:19 JUNE 2018

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: 98ASA01259D	REVISION: O	PAGE:

Fig 14. Soldering footprint for SOT1390-10 (WLCSP12) 3 of 3

Footprint information for reflow soldering of TSSOP14 package **SOT402-1**



DIMENSIONS in mm

P1	P2	Ay	By	C	D1	D2	Gx	Gy	Hx	Hy
0.650	0.750	7.200	4.500	1.350	0.400	0.600	4.950	5.300	5.800	7.450

sot402-1_fr

Fig 15. Soldering footprint for SOT402-1 (TSSOP14)

17. Abbreviations

Table 15. Abbreviations

Acronym	Description
CDM	Charged Device Model
DUT	Device Under Test
ESD	ElectroStatic Discharge
GPIO	General Purpose Input Output
HBM	Human Body Model
I^2C	Inter-Integrated Circuit
IEC	International Electrotechnical Commission
MM	Machine Model
PCB	Printed-Circuit Board
PMOS	Positive Metal Oxide Semiconductor
SMBus	System Management Bus
UART	Universal Asynchronous Receiver Transmitter

18. Revision history

Table 16. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
NTS0304E v.1.0	20190201	Product data sheet	-	-

19. Legal information

19.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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21. Contents

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