iCE40 LP/HX Family

Data Sheet

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Contents

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Figures

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Tables

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Acronyms in This Document

A list of acronyms used in this document.

Acronym	Definition
DFF	D-style Flip-Flop
DSP	Digital Signal Processor
EBR	Embedded Block RAM
HFOSC	High Frequency Oscillator
I^2C	Inter-Integrated Circuit
LFOSC	Low Frequency Oscillator
LUT	Look Up Table
LVCMOS	Low-Voltage Complementary Metal Oxide Semiconductor
NVCM	Non Volatile Configuration Memory
PFU	Programmable Functional Unit
PLB	Programmable Logic Blocks
PLL	Phase Locked Loops
SPI	Serial Peripheral Interface
WLCSP	Wafer Level Chip Scale Packaging

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1. General Description

The iCE40™ LP/HX family of ultra-low power, non-volatile FPGAs has five devices with densities ranging from 384 to 7,680 Look-Up Tables (LUTs). In addition to LUT-based, low-cost programmable logic, these devices feature Embedded Block RAM (EBR), Non-volatile Configuration Memory (NVCM) and Phase Locked Loops (PLLs). These features allow the devices to be used in low-cost, high-volume consumer and system applications. Select packages offer High-Current drivers that are ideal to drive three white LEDs, or one RGB LED.

The iCE40 LP/HX devices are fabricated on a 40 nm CMOS low power process. The device architecture has several features such as programmable low-swing differential I/O and the ability to turn off on-chip PLLs dynamically. These features help manage static and dynamic power consumption, resulting in low static power for all members of the family. The iCE40 LP/HX devices are available in two versions – ultra low power (LP) and high performance (HX) devices.

The iCE40 LP/HX FPGAs are available in a broad range of advanced halogen-free packages ranging from the space saving 1.40 x 1.48 mm WLCSP to the PCB-friendly 20 x 20 mm TQFP. Table 2.1 shows the LUT densities, package and I/O options, along with other key parameters.

The iCE40 LP/HX devices offer enhanced I/O features such as pull-up resistors. Pull-up features are controllable on a per-pin basis.

The iCE40 LP/HX devices also provide flexible, reliable and secure configuration from on-chip NVCM. These devices can also configure themselves from external SPI Flash or be configured by an external master such as a CPU.

Lattice provides a variety of design tools that allow complex designs to be efficiently implemented using the iCE40 LP/HX family of devices. Popular logic synthesis tools provide synthesis library support for iCE40 LP/HX. Lattice design tools use the synthesis tool output along with the user-specified preferences and constraints to place and route the design in the iCE40 LP/HX device. These tools extract the timing from the routing and back-annotate it into the design for timing verification.

Lattice provides many pre-engineered IP (Intellectual Property) modules, including a number of reference designs, licensed free of charge, optimized for the iCE40 LP/HX FPGA family. By using these configurable soft core IP cores as standardized blocks, users are free to concentrate on the unique aspects of their design, increasing their productivity.

1.1. Features

- Flexible Logic Architecture
  - Five devices with 384 to 7,680 LUT4s and 10 to 206 I/O
- Ultra-low Power Devices
  - Advanced 40 nm low power process
  - As low as 21 µA standby power
  - Programmable low swing differential I/O
- Embedded and Distributed Memory
  - Up to 128 kb sysMEM™ Embedded Block RAM
- Pre-Engineered Source Synchronous I/O
  - DDR registers in I/O cells
- High Current LED Drivers
  - Three High Current Drivers used for three different LEDs or one RGB LED
- High Performance, Flexible I/O Buffer
  - Programmable sysI/O™ buffer supports wide range of interfaces:
  - LVCMOS 3.3/2.5/1.8
  - LVDS25E, subLVDS
  - Schmitt trigger inputs, to 200 mV typical hysteresis
- Programmable pull-up mode
- Flexible On-Chip Clocking
  - Eight low skew global signal resources
  - Up to two analog PLLs per device
- Flexible Device Configuration
  - SRAM is configured through:
  - Standard SPI Interface
  - Internal Nonvolatile Configuration Memory (NVCM)
- Broad Range of Package Options
  - WLCSP, QFN, VQFP, TQFP, ucBGA, caBGA, and csBGA package options
  - Small footprint package options
  - As small as 1.40 x 1.48 mm
  - Advanced halogen-free packaging

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2. Product Family

Table 2.1 lists device information and packages of the iCE40 LP/HX family.

Table 2.1. iCE40 LP/HX Family Selection Guide

Part Number		LP384	LP640	LP1K	LP4K	LP8K	HX1K	HX4K	HX8K
Logic Cells (LUT + Flip-Flop)		**384**	**640**	**1,280**	**3,520**	**7,680**	**1,280**	**3,520**	**7,680**
RAM4K Memory Blocks		0	8	16	20	32	16	20	32
RAM4K RAM bits		0	32K	64K	80K	128K	64K	80K	128K
Phase-Locked Loops (PLLs)		0	0	1[1]	2[2]	2[2]	1[1]	2	2
Maximum Programmable I/O Pins		63	25	95	167	178	95	95	206
Maximum Differential Input Pairs		8	3	12	20	23	11	12	26
High Current LED Drivers		0	3	3	0	0	0	0	0
Package	**Code**	**Programmable I/O: Max Input (LVDS25)**							
16 WLCSP (1.40 x 1.48 mm, 0.35 mm)	SWG16		10(0)[1]	10(0)	—	—	—	—	—
32 QFN (5 x 5 mm, 0.5 mm)	SG32	21(3)	—	—	—	—	—	—	—
36 ucBGA (2.5 x 2.5 mm, 0.4 mm)	CM36	25(3)	—	25(3)	—	—	—	—	—
49 ucBGA (3 x 3 mm, 0.4 mm)	CM49	37(6)	—	35(5)	—	—	—	—	—
81 ucBGA (4 x 4 mm, 0.4 mm)	CM81	—	—	63(8)	63(9)[2]	63(9)[2]	—	—	—
81 csBGA (5 x 5 mm, 0.5 mm)	CB81	—	—	62(9)	—	—	—	—	—
84 QFN (7 x 7 mm, 0.5 mm)	QN84	—	—	67(7)	—	—	—	—	—
100 VQFP (14 x 14 mm, 0.5 mm)	VQ100	—	—	—	—	—	72(9)[1]	—	—
121 ucBGA (5 x 5 mm, 0.4 mm)	CM121	—	—	95(12)	93(13)	93(13)	—	—	—
121 csBGA (6 x 6 mm, 0.5 mm)	CB121	—	—	92(12)	—	—	—	—	—
121 caBGA (9 x 9 mm, 0.8 mm)	BG121	—	—	—	—	—	—	93(13)	93(13)
132 csBGA (8 x 8 mm, 0.5 mm)	CB132	—	—	—	—	—	95(11)	95(12)	95(12)
144 TQFP (20 x 20 mm, 0.5 mm)	TQ144	—	—	—	—	—	96(12)	107(14)	—
225 ucBGA (7 x 7 mm, 0.4 mm)	CM225	—	—	—	178(23)	178(23)	—	—	178(23)
256-ball caBGA (14 x 14 mm, 0.8 mm)	CT256	—	—	—	—	—	—	—	206(26)

Notes:

1. No PLL available on the 16 WLCSP, 36 ucBGA, 81 csBGA, 84 QFN, and 100 VQFP packages.
2. Only one PLL available on the 81 ucBGA package.
3. High Current I/O only available on the 16 WLCSP package.

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3. Architecture

3.1. Architecture Overview

The iCE40 LP/HX family architecture contains an array of Programmable Logic Blocks (PLB), sysCLOCK™ PLLs, Nonvolatile Programmable Configuration Memory (NVCM) and blocks of sysMEM Embedded Block RAM (EBR) surrounded by Programmable I/O (PIO). Figure 3.1 shows the block diagram of the iCE40LP/HX1K device.

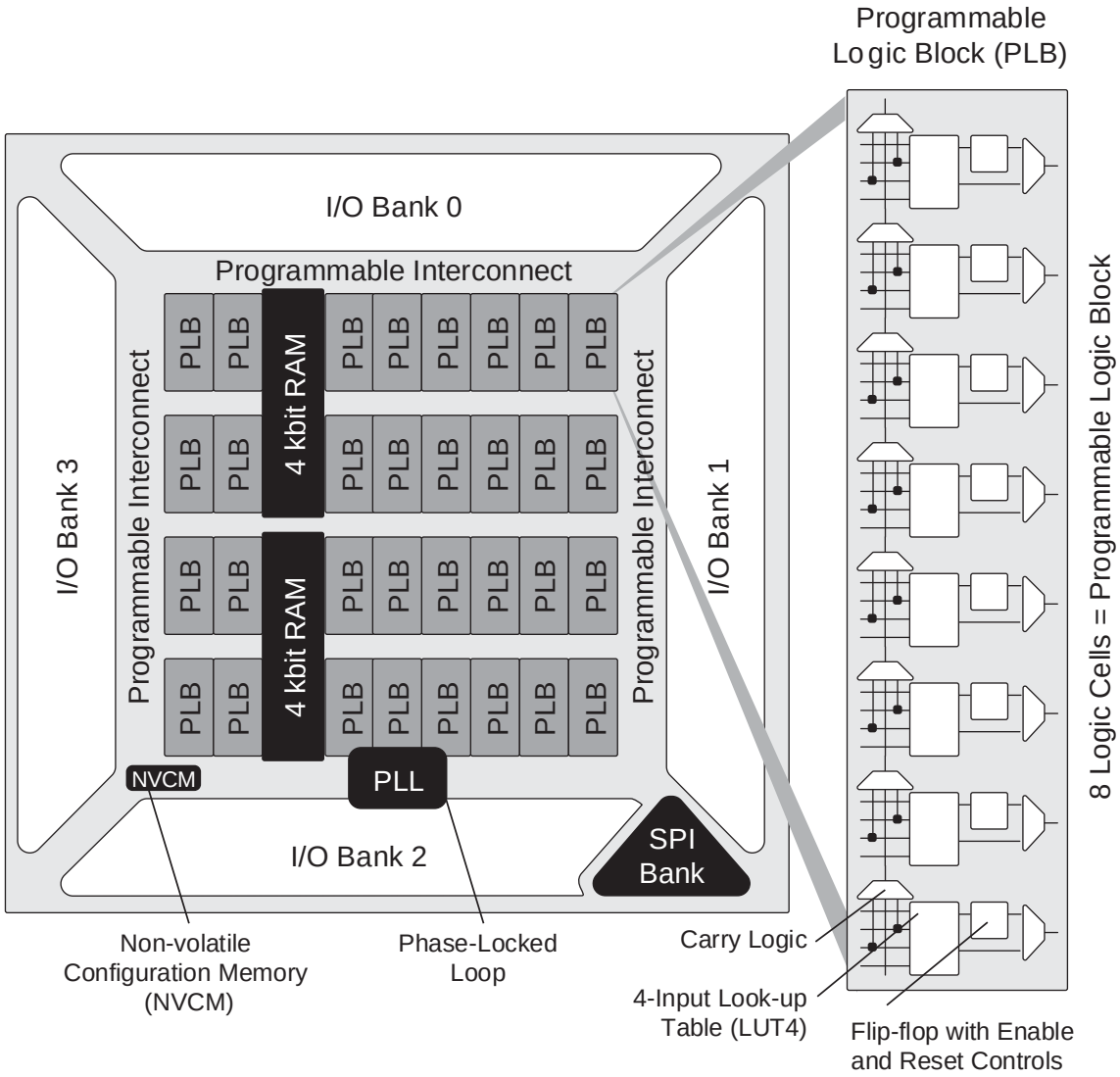

Figure 3.1. iCE40LP/HX1K Device, Top View

The logic blocks, Programmable Logic Blocks (PLB) and sysMEM EBR blocks, are arranged in a two-dimensional grid with rows and columns. Each column has either logic blocks or EBR blocks. The PIO cells are located at the periphery of the device, arranged in banks. The PLB contains the building blocks for logic, arithmetic, and register functions. The PIOs utilize a flexible I/O buffer referred to as a sysI/O buffer that supports operation with a variety of interface standards. The blocks are connected with many vertical and horizontal routing channel resources. The place and route software tool automatically allocates these routing resources.

In the iCE40 LP/HX family, there are up to four independent sysI/O banks. Note on some packages V_{CCIO} banks are tied together. There are different types of I/O buffers on the different banks. Refer to the details in later sections of this

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document. The sysMEM EBRs are large 4 kbit, dedicated fast memory blocks. These blocks can be configured as RAM, ROM or FIFO.

The iCE40 LP/HX architecture also provides up to two sysCLOCK Phase Locked Loop (PLL) blocks. The PLLs have multiply, divide, and phase shifting capabilities that are used to manage the frequency and phase relationships of the clocks.

Every device in the family has a SPI port that supports programming and configuration of the device. The iCE40 LP/HX includes on-chip, Nonvolatile Configuration Memory (NVCM).

3.1.1. PLB Blocks

The core of the iCE40 LP/HX device consists of Programmable Logic Blocks (PLB) which can be programmed to perform logic and arithmetic functions. Each PLB consists of eight interconnected Logic Cells (LC) as shown in Figure 3.2. Each LC contains one LUT and one register.

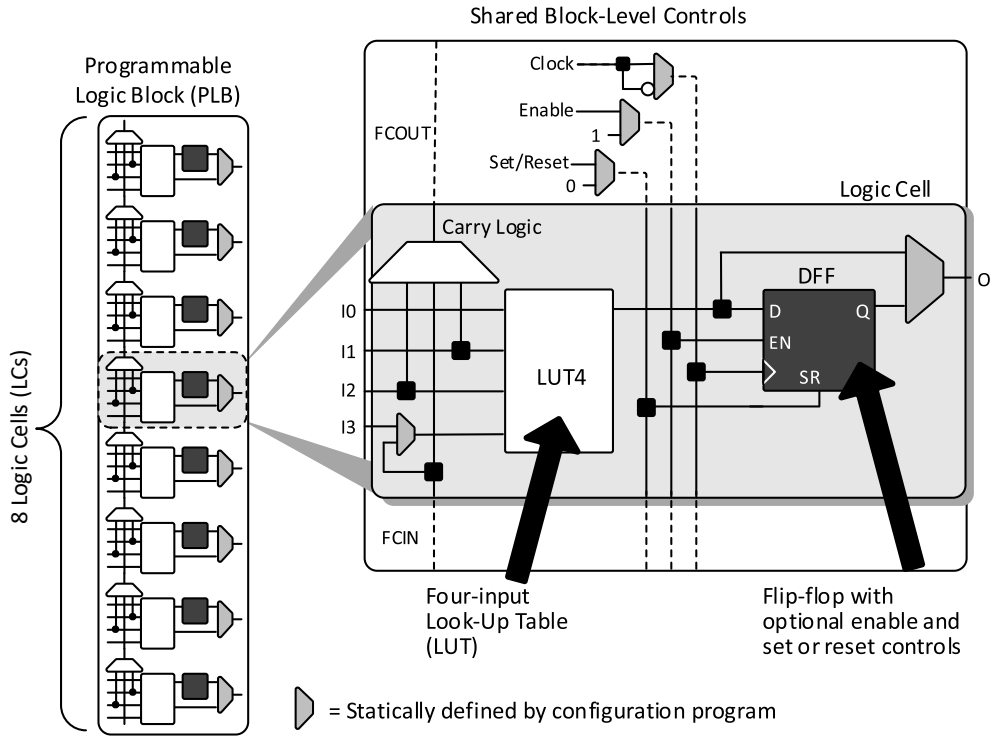

Figure 3.2. PLB Block Diagram

Logic Cells

Each Logic Cell includes three primary logic elements shown in Figure 3.2.

- A four-input Look-Up Table (LUT) builds any combinational logic function, of any complexity, requiring up to four inputs. Similarly, the LUT4 element behaves as a 16 x 1 Read-Only Memory (ROM). Combine and cascade multiple LUT4s to create wider logic functions.
- A D-style Flip-Flop (DFF), with an optional clock-enable and reset control input, builds sequential logic functions. Each DFF also connects to a global reset signal that is automatically asserted immediately following device configuration.
- Carry Logic boosts the logic efficiency and performance of arithmetic functions, including adders, subtracters, comparators, binary counters and some wide, cascaded logic functions.

Table 3.1 lists the logic cell signals.

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Table 3.1. Logic Cell Signal Descriptions

Function	Type	Signal Name	Description
Input	Data signal	I0, I1, I2, I3	Inputs to LUT4
Input	Control signal	Enable	Clock enable shared by all LCs in the PLB
Input	Control signal	Set/Reset[1]	Asynchronous or synchronous local set/reset shared by all LCs in the PLB.
Input	Control signal	Clock	Clock one of the eight Global Buffers, or from the general-purpose interconnects fabric shared by all LCs in the PLB.
Input	Inter-PLB signal	FCIN	Fast carry in
Output	Data signals	O	LUT4 or registered output
Output	Inter-PFU signal	FCOUT	Fast carry out

Note:

1. If Set/Reset is not used, then the flip-flop is never set/reset, except when cleared immediately after configuration.

3.1.2. Routing

There are many resources provided in the iCE40 LP/HX devices to route signals individually with related control signals. The routing resources consist of switching circuitry, buffers, and metal interconnect (routing) segments.

The inter-PLB connections are made with three different types of routing resources: Adjacent (spans two PLBs), x4 (spans five PLBs) and x12 (spans thirteen PLBs). The Adjacent, x4, and x12 connections provide fast and efficient connections in the diagonal, horizontal and vertical directions.

The design tool takes the output of the synthesis tool and places and routes the design.

3.1.3. Clock/Control Distribution Network

Each iCE40 LP/HX device has eight global inputs, two pins on each side of the device. Note that not all GBINs are available in all packages.

These global inputs can be used as high fanout nets, clock, reset or enable signals. The dedicated global pins are identified as GBIN[7:0] and the global buffers are identified as-GBUF[7:0]. These eight inputs may be used as general purpose I/O if they are not used to drive the clock nets. Global buffer GBUF7 in I/O Bank 3 also provides an optional direct LVDS25 or subLVDS differential clock input.

Table 3.2 lists the connections between a specific global buffer and the inputs on a PLB. All global buffers optionally connect to the PLB CLK input. Any four of the eight global buffers can drive logic inputs to a PLB. Even-numbered global buffers optionally drive the Set/Reset input to a PLB. Similarly, odd-numbered buffers optionally drive the PLB clock-enable input.

Table 3.2. Global Buffer (GBUF) Connections to Programmable Logic Blocks

Global Buffer	LUT Inputs	Clock	Reset	Clock Enable
GBUF0	Yes, any 4 of 8 GBUF Inputs	Yes	Yes	—
GBUF1		Yes	—	Yes
GBUF2		Yes	Yes	—
GBUF3		Yes	—	Yes
GBUF4		Yes	Yes	—
GBUF5		Yes	—	Yes
GBUF6		Yes	Yes	—
GBUF7		Yes	—	Yes

The maximum frequency for the global buffers are listed in the External Switching Characteristics tables in this document.

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3.1.3.1. Global Hi-Z Control

The global high-impedance control signal, GHIZ, connects to all I/O pins on the iCE40 LP/HX device. This GHIZ signal is automatically asserted throughout the configuration process, forcing all user I/O pins into their high-impedance state.

3.1.3.2. Global Reset Control

The global reset control signal connects to all PLB and PIO flip-flops on the iCE40 LP/HX device. The global reset signal is automatically asserted throughout the configuration process, forcing all flip-flops to their defined wake-up state. For PLB flip-flops, the wake-up state is always reset, regardless of the PLB flip-flop primitive used in the application.

3.1.4. sysCLOCK Phase Locked Loops (PLLs)

The sysCLOCK PLLs provide the ability to synthesize clock frequencies. The iCE40 LP/HX devices have one sysCLOCK PLL. REFERENCECLK is the reference frequency input to the PLL and its source can come from an external I/O pin, the internal Oscillator Generators from internal routing. EXTFEEDBACK is the feedback signal to the PLL which can come from internal routing or an external I/O pin. The feedback divider is used to multiply the reference frequency and thus synthesize a higher frequency clock output.

The PLLOUT output has an output divider, thus allowing the PLL to generate different frequencies fo r each output. The output divider can have a value from 1 to 64 (in increments of 2X). The PLLOUT outputs can all be used to drive the iCE40 LP/HX global clock network directly or general purpose routing resources can be used.

The LOCK signal is asserted when the PLL determines it has achieved lock and de-asserted if a loss of lock is detected. A block diagram of the PLL is shown in Figure 3.3.

The timing of the device registers can be optimized by programming a phase shift into the PLLOUT output clock which will advance or delay the output clock with reference to the REFERENCECLK clock. This phase shift can be either programmed during configuration or can be adjusted dynamically. In dynamic mode, the PLL may lose lock after a phase adjustment on the output used as the feedback source and not relock until the tLOCK parameter has been satisfied.

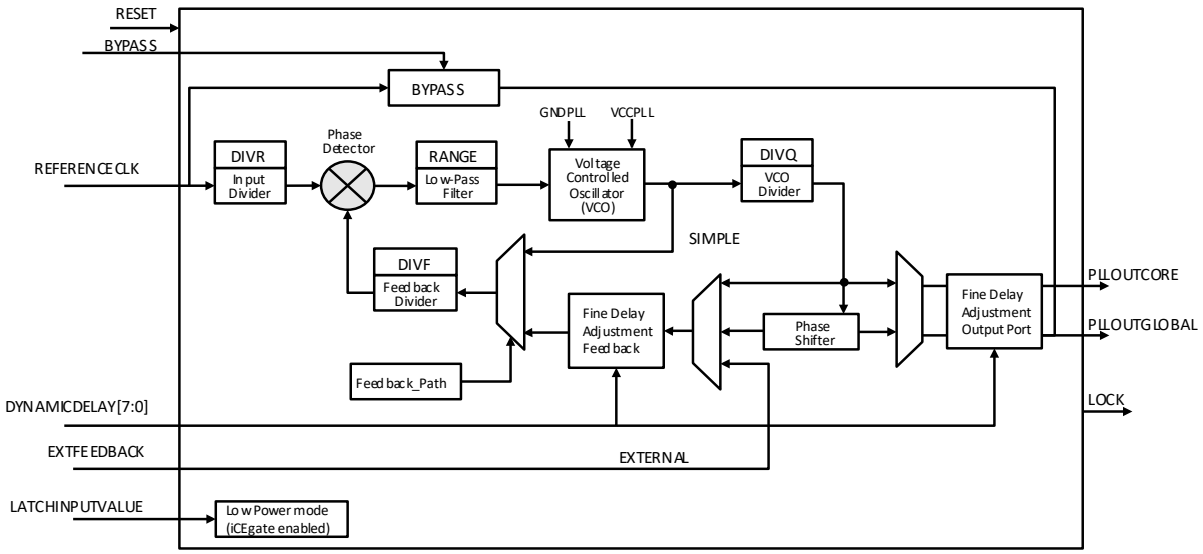

Figure 3.3. PLL Diagram

Table 3.3 provides signal descriptions of the PLL block.

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Table 3.3. PLL Signal Descriptions

Signal Name	Direction	Description
REFERENCECLK	Input	Input reference clock
BYPASS	Input	The BYPASS control selects which clock signal connects to the PLLOUT output. 0 – PLL generated signal 1 – REFERENCECLK
EXTFEEDBACK	Input	External feedback input to PLL. Enabled when the FEEDBACK_PATH attribute is set to EXTERNAL.
DYNAMICDELAY[7:0]	Input	Fine delay adjustment control inputs. Enabled when DELAY_ADJUSTMENT_MODE is set to DYNAMIC.
LATCHINPUTVALUE	Input	When enabled, puts the PLL into low-power mode; PLL output is held static at the last input clock value. Set ENABLE ICEGATE_PORTA and PORTB to 1 to enable.
PLLOUTGLOBAL	Output	Output from the Phase-Locked Loop (PLL). Drives a global clock network on the FPGA. The port has optimal connections to global clock buffers GBUF4 and GBUF5.
PLLOUTCORE	Output	Output clock generated by the PLL, drives regular FPGA routing. The frequency generated on this output is the same as the frequency of the clock signal generated on the PLLOUTLGOBAL port.
LOCK	Output	When High, indicates that the PLL output is phase aligned or locked to the input reference clock.
RESET	Input	Active low reset.
SCLK	Input	Input, Serial Clock used for re-programming PLL settings.
SDI	Input	Input, Serial Data used for re-programming PLL settings.

3.1.5. sysMEM Embedded Block RAM Memory

Larger iCE40 LP/HX device includes multiple high-speed synchronous sysMEM Embedded Block RAMs (EBRs), each 4 kbit in size. This memory can be used for a wide variety of purposes including data buffering and FIFO.

3.1.5.1. sysMEM Memory Block

The sysMEM block can implement single port, pseudo dual port, or FIFO memories with programmable logic resources. Each block can be used in a variety of depths and widths as listed in Table 3.4.

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Table 3.4. sysMEM Block Configurations[1]

Block RAM Configuration	Block RAM Configuration and Size	WADDR Port Size (Bits)	WDATA Port Size (Bits)	RADDR Port Size (Bits)	RDATA Port Size (Bits)	MASK Port Size (Bits)
SB_RAM256x16 SB_RAM256x16NR SB_RAM256x16NW SB_RAM256x16NRNW	256 x 16 (4 k)	8 [7:0]	16 [15:0]	8 [7:0]	16 [15:0]	16 [15:0]
SB_RAM512x8 SB_RAM512x8NR SB_RAM512x8NW SB_RAM512x8NRNW	512 x 8 (4 k)	9 [8:0]	8 [7:0]	9 [8:0]	8 [7:0]	No Mask Port
SB_RAM1024x4 SB_RAM1024x4NR SB_RAM1024x4NW SB_RAM1024x4NRNW	1024 x 4 (4 k)	10 [9:0]	4 [3:0]	10 [9:0]	4 [3:0]	No Mask Port
SB_RAM2048x2 SB_RAM2048x2NR SB_RAM2048x2NW SB_RAM2048x2NRNW	2048 x 2 (4 k)	11 [10:0]	2 [1:0]	11 [10:0]	2 [1:0]	No Mask Port

Note:

1. For iCE40 LP/HX EBR primitives with a negative-edged Read or Write clock, the base primitive name is appended with a 'N' and a 'R' or W depending on the clock that is affected.

3.1.5.2. RAM Initialization and ROM Operation

If desired, the contents of the RAM can be pre-loaded during device configuration.

By preloading the RAM block during the chip configuration cycle and disabling the write controls, the sysMEM block can also be utilized as a ROM.

Note that the sysMEM Embedded Block RAM Memory address 0 cannot be initialized.

3.1.5.3. Memory Cascading

Larger and deeper blocks of RAM can be created using multiple EBR sysMEM Blocks.

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3.1.5.4. RAM4k Block

Figure 3.4 shows the 256 x 16 memory configurations and their input/output names. In all the sysMEM RAM modes, the input data and addresses for the ports are registered at the input of the memory array.

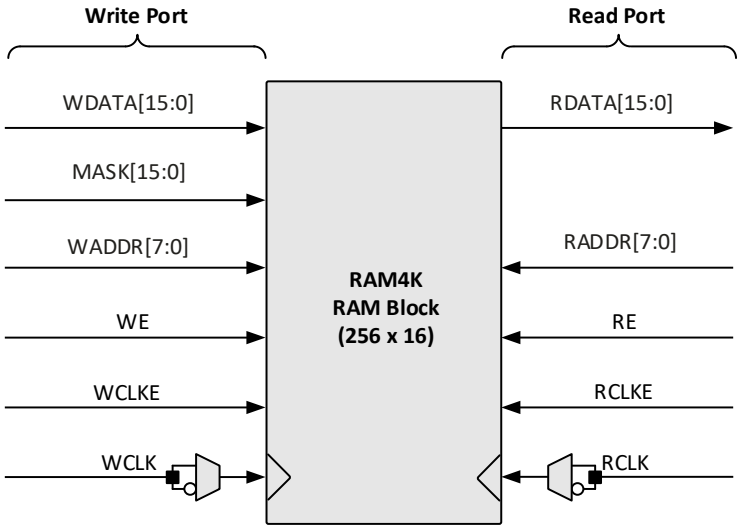

Figure 3.4. sysMEM Memory Primitives

Table 3.5 lists the EBR signals.

Table 3.5. EBR Signal Descriptions

Signal Name	Direction	Description
WDATA[15:0]	Input	Write Data input.
MASK[15:0]	Input	Masks write operations for individual data bit-lines. 0 – Write bit 1 – Do not write bit
WADDR[7:0]	Input	Write Address input. Selects one of 256 possible RAM locations.
WE	Input	Write Enable input.
WCLKE	Input	Write Clock Enable input.
WCLK	Input	Write Clock input. Default rising-edge, but with falling-edge option.
RDATA[15:0]	Output	Read Data output.
RADDR[7:0]	Input	Read Address input. Selects one of 256 possible RAM locations.
RE	Input	Read Enable input.
RCLKE	Input	Read Clock Enable input.
RCLK	Input	Read Clock input. Default rising-edge, but with falling-edge option.

For further information on the sysMEM EBR block, refer to Memory Usage Guide for iCE40 Devices (FPGA-TN-02002).

3.1.6. sysI/O

Buffer Banks

iCE40 LP/HX devices have up to four I/O banks with independent V_{CCIO} rails with an additional configuration bank V_{CC_SPI} for the SPI I/O.

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Programmable I/O (PIO)

The programmable logic associated with an I/O is called a PIO. The individual PIOs are connected to their respective sysI/O buffers and pads. The PIOs are placed on the top and bottom of the devices.

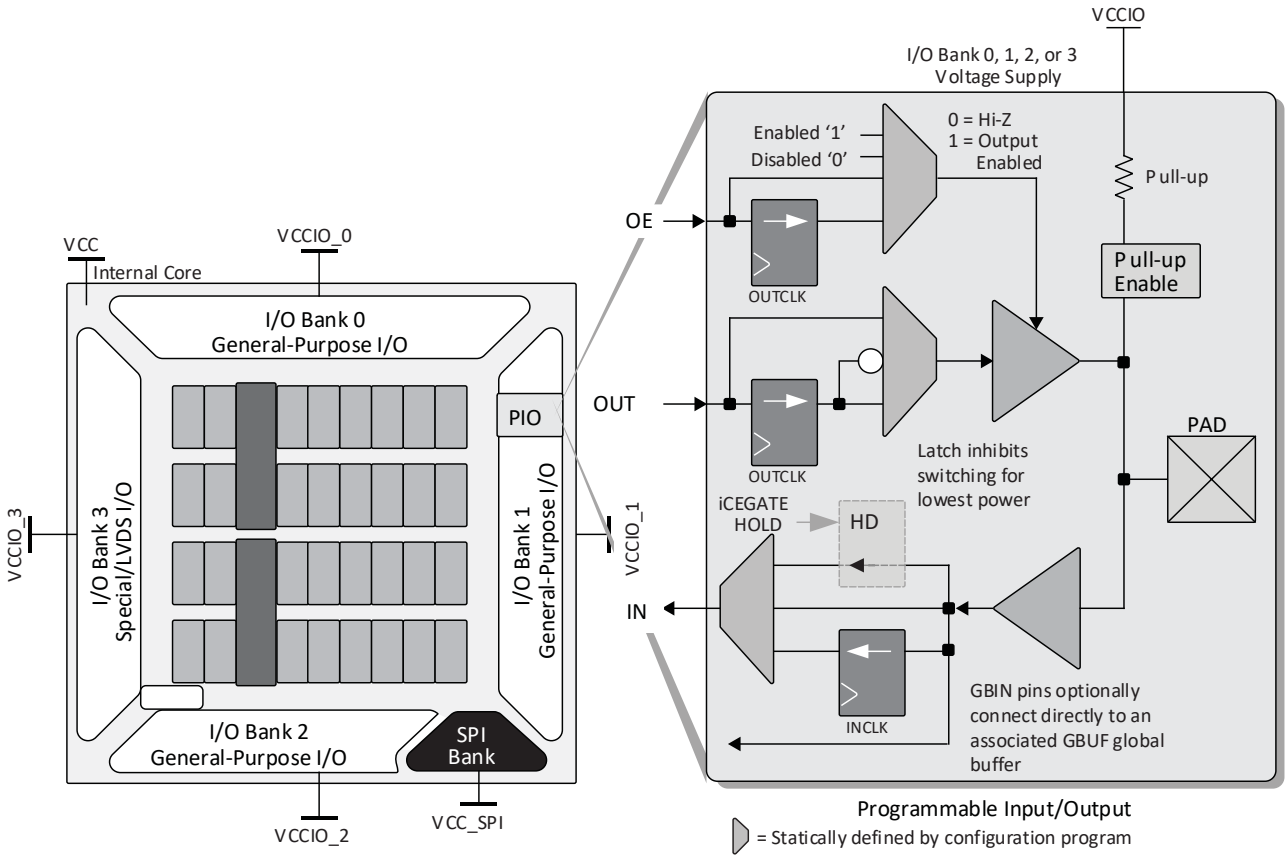

Figure 3.5. I/O Bank and Programmable I/O Cell

The PIO contains three blocks: an input register block, output register block iCEgate™ and tri-state register block. To save power, the optional iCEgate latch can selectively freeze the state of individual, non-registered inputs within an I/O bank. Note that the freeze signal is common to the bank. These blocks can operate in a variety of modes along with the necessary clock and selection logic.

Input Register Block

The input register blocks for the PIOs on all edges contain registers that can be used to condition high-speed interface signals before they are passed to the device core. In Generic DDR mode, two registers are used to sample the data on the positive and negative edges of the system clock signal, creating two data streams.

Output Register Block

The output register block can optionally register signals from the core of the device before they are passed to the sysI/O buffers. In Generic DDR mode, two registers are used to capture the data on the positive and negative edge of the system clock and then muxed creating one data stream.

Figure 3.6 shows the input/output register block for the PIOs.

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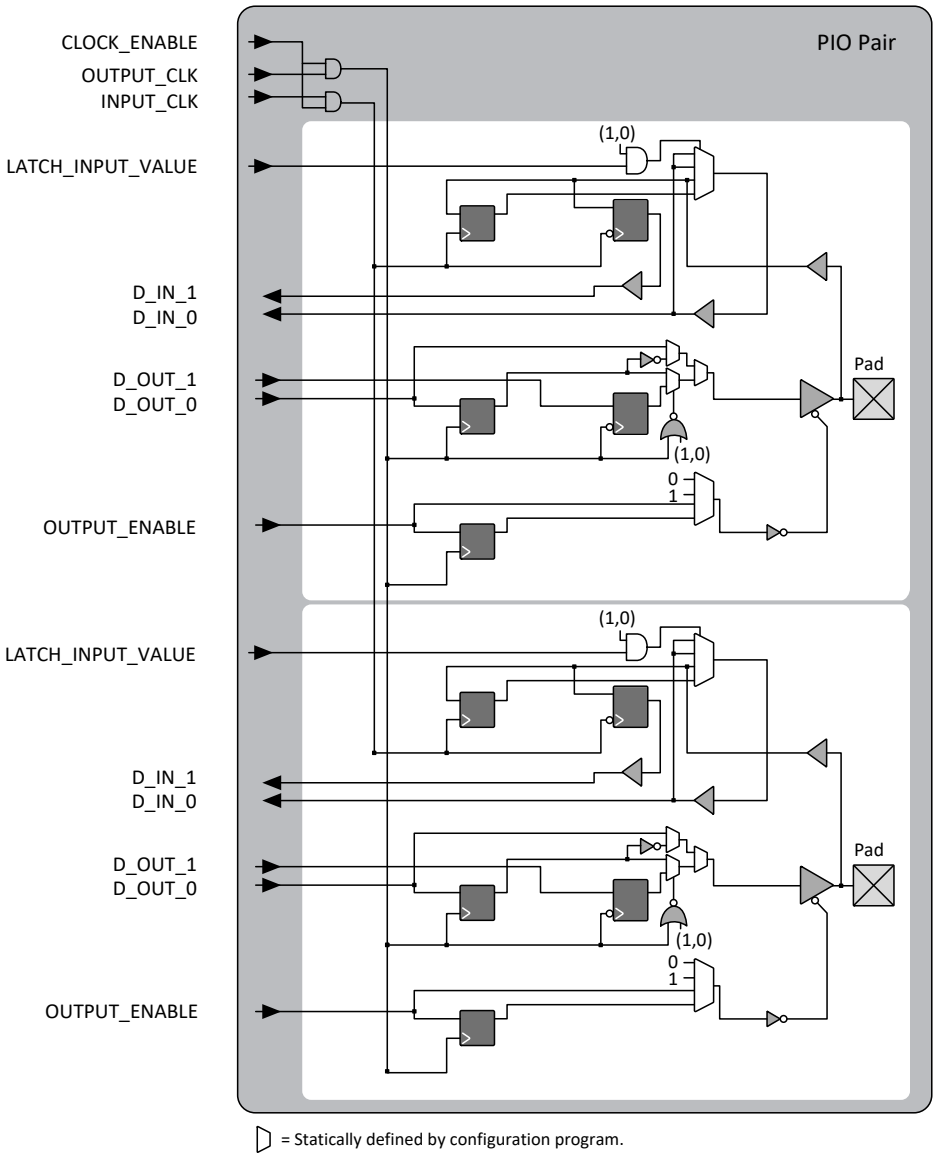

Figure 3.6. iCE I/O Register Block Diagram

Table 3.6. PIO Signal List

Pin Name	I/O Type	Description
OUTPUT_CLK	Input	Output register clock
CLOCK_ENABLE	Input	Clock enable
INPUT_CLK	Input	Input register clock
OUTPUT_ENABLE	Input	Output enable
D_OUT_0/1	Input	Data from the core
D_IN_0/1	Output	Data to the core
LATCH_INPUT_VALUE	Input	Latches/holds the Input Value

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3.1.7. sysI/O Buffer

Each I/O is associated with a flexible buffer referred to as a sysI/O buffer. These buffers are arranged around the periphery of the device in groups referred to as banks. The sysI/O buffers allow users to implement a wide variety of standards that are found in today's systems including LVCMOS and LVDS25.

High Current LED Drivers combine three sysI/O buffers together. This allows for programmable drive strength. This also allows for high current drivers that are ideal to drive three white LEDs, or one RGB LED. Each bank is capable of supporting multiple I/O standards including single-ended LVCMOS buffers and differential LVDS25E output buffers. Bank 3 additionally supports differential LVDS25 input buffers. Each sysI/O bank has its own dedicated power supply.

Typical I/O Behavior During Power-up

The internal power-on-reset (POR) signal is deactivated when V_{CC}, V_{CCIO_2}, V_{PP_2V5}, and V_{CC_SPI} have reached the level defined in Table 4.4. After the POR signal is deactivated, the FPGA core logic becomes active. It is your responsibility to ensure that all V_{CCIO} banks are active with valid input logic levels to properly control the output logic states of all the I/O banks that are critical to the application. The default configuration of the I/O pins in a device prior to configuration is tri-stated with a weak pull-up to V_{CCIO}. The I/O pins will maintain the pre-configuration state until V_{CC} and V_{CCIO} (for I/O banks containing configuration I/O) have reached levels, at which time the I/O will take on the software user-configured settings only after a proper download/configuration. Unused I/O are automatically blocked and the pull-up termination is disabled.

Supported Standards

The iCE40 LP/HX sysI/O buffer supports both single-ended input/output standards, and used as differential comparators. The buffer supports the LVCMOS 1.8 V, 2.5 V, and 3.3 V standards. The buffer has individually configurable options for bus maintenance (weak pull-up or none).

Table 3.7 and Table 3.8 show the I/O standards (together with their supply and reference voltages) supported by the iCE40 LP/HX devices.

Table 3.7. Supported Input Standards

I/O Standard	V_{CCIO} (Typical)		
	3.3 V	2.5 V	1.8 V
Single-Ended Interfaces			
LVCMOS33	Yes	—	—
LVCMOS25	—	Yes	—
LVCMOS18	—	—	Yes
Differential Interfaces			
LVDS25[1]	—	Yes	—
SubLVDS[1]	—	—	Yes

Note:

1. Bank 3 only.

Table 3.8. Supported Output Standards

I/O Standard	V_{CCIO} (Typical)
Single-Ended Interfaces	
LVCMOS33	3.3 V
LVCMOS25	2.5 V
LVCMOS18	1.8 V
Differential Interfaces	
LVDS25[1]	—
SubLVDS[1]	—

Note:

1. These interfaces can be emulated with external resistors in all devices.

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3.1.8. Non-Volatile Configuration Memory

All iCE40 LP/HX devices provide a Non-Volatile Configuration Memory (NVCM) block which can be used to configure the device.

For more information on the NVCM, refer to iCE40 Programming and Configuration (FPGA-TN-02001).

3.1.9. Power On Reset

iCE40 LP/HX devices have power-on reset circuitry to monitor V_{CC}, V_{CCIO_2}, V_{PP_2V5}, and V_{CC_SPI} voltage levels during power-up and operation. At power-up, the POR circuitry monitors V_{CC}, V_{CCIO_2}, V_{PP_2V5}, and V_{CC_SPI} (controls configuration) voltage levels. It then triggers download from the on-chip NVCM or external Flash memory after reaching the power-up levels specified in the Power-On-Reset Voltage table in the DC and Switching Characteristics section of this data sheet. Before and during configuration, the I/O are held in tri-state. I/O are released to user functionality once the device has finished configuration.

3.2. Programming and Configuration

This section describes the programming and configuration of the iCE40 LP/HX family.

Device Programming

The NVCM memory can be programmed through the SPI port.

Device Configuration

There are various ways to configure the Configuration RAM (CRAM) including:
Internal NVCM Download

- From an SPI Flash (Master SPI mode)
- System microprocessor to drive a Serial Slave SPI port (SSPI mode)

The image to configure the CRAM can be selected by the user on power up (Cold Boot) or once powered up (Warm Boot).

For more details on configuring the iCE40 LP/HX device, refer to iCE40 Programming and Configuration (FPGA-TN-02001).

3.2.1. Power Saving Options

iCE40 LP/HX devices are available in two options for maximum flexibility: LP and HX devices. The LP devices have ultra low static and dynamic power consumption. HX devices are designed to provide high performance. Both the LP and the HX devices operate at 1.2 V V_{CC}.

iCE40 LP/HX devices feature iCEGate and PLL low power mode to allow users to meet the static and dynamic power requirements of their applications. While these features are available in both device types, these features are mainly intended for use with iCE40 LP devices to manage power consumption.

Table 3.9. Power Saving Features Description

Device Subsystem	Feature Description
PLL	When LATCHINPUTVALUE is enabled, puts the PLL into low-power mode; PLL output held static at last input clock value.
iCEGate	To save power, the optional iCEGate latch can selectively freeze the state of individual, non-registered inputs within an I/O bank. Registered inputs are effectively frozen by their associated clock or clock-enable control.

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4. DC and Switching Characteristics

4.1. Absolute Maximum Ratings

Table 4.1. Absolute Maximum Ratings

Parameter	Min	Max	Unit
Supply Voltage V_{CC}	–0.5	1.42	V
Output Supply Voltage V_{CCIO}	–0.5	3.60	V
NVCM Supply Voltage V_{PP_2V5}	–0.5	3.60	V
PLL Supply Voltage V_{CCPLL}	–0.5	1.42	V
I/O Tri-state Voltage Applied	–0.5	3.60	V
Dedicated Input Voltage Applied	–0.5	3.60	V
Storage Temperature (Ambient)	–65	150	°C
Junction Temperature (T_J)	–55	125	°C

Notes:

- Stress above those listed under the “Absolute Maximum Ratings” may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.
- Compliance with the Thermal Management document is required.
- All voltages referenced to GND.
- I/O can support a 200 mV Overshoot above the Recommended Operating Conditions VCCIO (Max) and -200 mV Undershoot below VIL (Min). Overshoot and Undershoot is permitted for 25% duty cycle but must not exceed 1.6 ns.

4.2. Recommended Operating Conditions

Table 4.2. Recommended Operating Conditions

Symbol	Parameter		Min	Max	Unit
V_{CC}[1]	Core Supply Voltage		1.14	1.26	V
V_{PP_2V5}	V_{PP_2V5} NVCM Programming and Operating Supply Voltage	Slave SPI Configuration	1.71	3.46	V
		Master SPI Configuration	2.30	3.46	V
		Configuration from NVCM	2.30	3.46	V
		NVCM Programming	2.30	3.00	V
V_{PP_FAST}[4]	Optional fast NVCM programming supply. Leave unconnected.		N/A	N/A	V
V_{CCPLL}[5,6]	PLL Supply Voltage		1.14	1.26	V
V_{CCIO}[1,2,3]	I/O Driver Supply Voltage	VCCIO0-3	1.71	3.46	V
		V_{CC_SPI}	1.71	3.46	V
t_{JIND}	Junction Temperature, Industrial Operation		–40	100	°C
t_{PROG}	Junction Temperature NVCM Programming		10.00	30.00	°C

Notes:

1. Like power supplies must be tied together. For example, if V_{CCIO} and V_{CC_SPI} are both the same voltage, they must also be the same supply.
2. See recommended voltages by I/O standard in subsequent table.
3. V_{CCIO} pins of unused I/O banks should be connected to the VCC power supply on boards.
4. V_{PP_FAST}, used only for fast production programming, must be left floating or unconnected in applications, except CM36 and CM49 packages MUST have the V_{PP_FAST} ball connected to $V_{CCIO\_0\_1}$ ball externally.
5. No PLL available on the iCE40LP384 and iCE40LP640 device.
6. V_{CCPLL} is tied to VCC internally in packages without PLL pins.

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4.3. Power Supply Ramp Rates

Table 4.3. Power Supply Ramp Rates[1,2]

Symbol	Parameter		Min	Max	Unit
t_{RAMP}	Power supply ramp rates for all power supplies	All configuration modes. No power supply sequencing.	0.40	10	V/ms
		Configuring from Slave SPI. No power supply sequencing,	0.01	10	V/ms
		Configuring from NVCM. V_{CC} and V_{PP_2V5} to be powered 0.25 ms before V_{CC_SPI}.	0.01	10	V/ms
		Configuring from MSPI. V_{CC} and V_{PP_SPI} to be powered 0.25 ms before V_{PP_2V5}.	0.01	10	V/ms

Notes:

1. Assumes monotonic ramp rates.
2. iCE40LP384 requires VCC to be greater than 0.7 V when V_{CCIO} and V_{CC_SPI} are above GND.

4.4. Power-On-Reset Voltage Levels

Table 4.4. Power-On-Reset Voltage Levels[1]

Symbol	Device	Parameter		Min	Max	Unit
V_{PORUP}	iCE40LP384	Power-On-Reset ramp-up trip point (band gap based circuit monitoring V_{CC}, V_{CCIO_2}, V_{CC_SPI} and V_{PP_2V5})	V_{CC}	0.67	0.99	V
			V_{CCIO_2}	0.70	1.59	V
			V_{CC_SPI}	0.70	1.59	V
			V_{PP_2V5}	0.70	1.59	V
	iCE40LP640, iCE40LP/HX1K, iCE40LP/HX4K, iCE40LP/HX8K	Power-On-Reset ramp-up trip point (band gap based circuit monitoring V_{CC}, V_{CCIO_2}, V_{CC_SPI} and V_{PP_2V5})	V_{CC}	0.55	0.75	V
			V_{CCIO_2}	0.86	1.29	V
			V_{CC_SPI}	0.86	1.29	V
			V_{PP_2V5}	0.86	1.33	V
V_{PORDN}	iCE40LP384	Power-On-Reset ramp-down trip point (band gap based circuit monitoring V_{CC}, V_{CCIO_2}, V_{CC_SPI} and V_{PP_2V5})	V_{CC}	—	0.64	V
			V_{CCIO_2}	—	1.59	V
			V_{CC_SPI}	—	1.59	V
			V_{PP_2V5}	—	1.59	V
	iCE40LP640, iCE40LP/HX1K, iCE40LP/HX4K, iCE40LP/HX8K	Power-On-Reset ramp-down trip point (band gap based circuit monitoring V_{CC}, V_{CCIO_2}, V_{CC_SPI} and V_{PP_2V5})	V_{CC}	—	0.75	V
			V_{CCIO_2}	—	1.29	V
			V_{CC_SPI}	—	1.29	V
			V_{PP_2V5}	—	1.33	V

Note:

1. These POR trip points are only provided for guidance. Device operation is only characterized for power supply voltages specified under recommended operating conditions.

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4.5. Power-up Supply Sequence

It is recommended to bring up the power supplies in the order below.

Note: There is no specified timing delay between the power supplies. There is, however, a requirement for each supply to reach a level of 0.5 V, or higher, before any subsequent power supplies in the sequence are applied.

1. VCC and V_{CCPLL} should be the first two supplies to be applied. Note that these two supplies can be tied together subject to the recommendation to include a RC-based noise filter on the V_{CCPLL}. Refer to iCE40 Hardware Checklist (FPGA-TN-02006).
2. SPI_V_{CCIO1} should be the next supply, and can be applied any time after the previous supplies (VCC and V_{CCPLL}) have reached as level of 0.5 V or higher.
3. VPP_2V5 should be the next supply, and can be applied any time after previous supplies (VCC, V_{CCPLL} and SPI_V_{CCIO1}) have reached a level of 0.5 V or higher.
4. Other Supplies (V_{CCIO0} and V_{CCIO2}) do not affect device power-up functionality, and they can be applied any time after the initial power supplies (VCC and V_{CCPLL}) have reached a level of 0.5 V or greater. There is no power down sequence required. However, when partial power supplies are powered down, it is required the above sequence to be followed when these supplies are re-powered up again.

4.6. ESD Performance

Please refer to the iCE40 Product Family Qualification Summary for complete qualification data, including ESD performance.

4.7. DC Electrical Characteristics

Over recommended operating conditions.

Table 4.5. DC Electrical Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I_{IL}, I_{IH}[1, 3, 4, 5, 6, 7]	Input or I/O Leakage	0 V < V_{IN} < V_{CCIO} + 0.2 V	—	—	±10	µA
C_1[6, 7]	I/O Capacitance[2]	V_{CCIO} = 3.3 V, 2.5 V, 1.8 V V_{CC} = Typ, V_{IO} = 0 to V_{CCIO} + 0.2 V	—	6	—	pf
C_2[6, 7]	Global Input Buffer Capacitance[2]	V_{CCIO} = 3.3 V, 2.5 V, 1.8 V V_{CC} = Typ, V_{IO} = 0 to V_{CCIO} + 0.2 V	—	6	—	pf
V_{HYST}	Input Hysteresis	V_{CCIO} = 1.8 V, 2.5 V, 3.3 V	—	200	—	mV
I_{PU}[6, 7]	Internal PIO Pull-up	V_{CCIO} = 1.8 V, 0 ≤ V_{IN} ≤ 0.65 * V_{CCIO}	−3	—	−31	µA
		V_{CCIO} = 2.5 V, 0 ≤ V_{IN} ≤ 0.65 * V_{CCIO}	−8	—	−72	µA
		V_{CCIO} = 3.3 V, 0 ≤ V_{IN} ≤ 0.65 * V_{CCIO}	−11	—	−128	µA

Notes:

1. Input or I/O leakage current is measured with the pin configured as an input or as an I/O with the output driver tri-stated. It is not measured with the output driver active. Internal pull-up resistors are disabled.
2. T_J 25 °C, f = 1.0 MHz.
3. Refer to V_{IL} and V_{IH} in the sysI/O Single-Ended DC Electrical Characteristics table.
4. Only applies to I/O in the SPI bank following configuration.
5. Some products are clamped to a diode when V_{IN} is larger than V_{CCIO}.
6. High current I/O has three sysI/O buffers connected together.
7. The iCE40LP640 and iCE40LP1K SWG16 package has CDONE and a sysI/O buffer are connected together.

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4.8. Static Supply Current – LP Devices

Table 4.6. Supply Current– LP Devices[1, 2, 3, 4]

Symbol	Parameter	Device	Typ V_{CC}[4]	Unit
I_{CC}	Core Power Supply	iCE40LP384	21	µA
		iCE40LP640	100	µA
		iCE40LP1K	100	µA
		iCE40LP4K	250	µA
		iCE40LP8K	250	µA
I_{CCPLL}[5, 6]	PLL Power Supply	All devices	0.5	µA
I_{PP_2V5}	NVCM Power Supply	All devices	1.0	µA
I_{CCIO}, I_{CC_SPI}	Bank Power Supply[4] V_{CCIO} = 2.5 V	All devices	3.5	µA

Notes:

1. Assumes blank pattern with the following characteristics: all outputs are tri-stated, all inputs are configured as LVCMOS and held at V_{CCIO} or GND, on-chip PLL is off. For more detail with your specific design, use the Power Calculator tool. Power specified with master SPI configuration mode. Other modes may be up to 25% higher.
2. Frequency = 0 MHz.
3. T_J = 25 °C, power supplies at nominal voltage.
4. Does not include pull-up.
5. No PLL available on the iCE40LP384 and iCE40LP640 device.
6. V_{CCPLL} is tied to V_{CC} internally in packages without PLL pins.

4.9. Static Supply Current – HX Devices

Table 4.7. Supply Current– HX Devices[1, 2, 3, 4]

Symbol	Parameter	Device	Typ V_{CC}[4]	Unit
I_{CC}	Core Power Supply	iCE40HX1K	296	µA
		iCE40HX4K	1140	µA
		iCE40HX8K	1140	µA
I_{CCPLL}[5]	PLL Power Supply	All devices	0.5	µA
I_{PP_2V5}	NVCM Power Supply	All devices	1.0	µA
I_{CCIO}, I_{CC_SPI}	Bank Power Supply[4] V_{CCIO} = 2.5 V	All devices	3.5	µA

Notes:

1. Assumes blank pattern with the following characteristics: all outputs are tri-stated, all inputs are configured as LVCMOS and held at V_{CCIO} or GND, on-chip PLL is off. For more detail with your specific design, use the Power Calculator tool. Power specified with master SPI configuration mode. Other modes may be up to 25% higher.
2. Frequency = 0 MHz.
3. T_J = 25 °C, power supplies at nominal voltage.
4. Does not include pull-up.
5. V_{CCPLL} is tied to V_{CC} internally in packages without PLL pins.

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4.10. Programming NVCM Supply Current – LP Devices

Table 4.8. Programming NVCM Supply Current – LP Devices[1,2,3,4]

Symbol	Parameter	Device	Typ V_{CC}[5]	Unit
I_{CC}	Core Power Supply	iCE40LP384	60	µA
		iCE40LP640	120	µA
		iCE40LP1K	120	µA
		iCE40LP4K	350	µA
		iCE40LP8K	350	µA
		All devices	0.5	µA
I_{CCPLL}[6, 7]	PLL Power Supply	All devices	2.5	mA
I_{PP_2V5}	NVCM Power Supply	All devices	3.5	mA
I_{CCIO}[8], I_{CC_SPI}	Bank Power Supply[4]	iCE40LP384	60	µA

Notes:

1. Assumes all inputs are held at V_{CCIO} or GND and all outputs are tri-stated.
2. Typical user pattern.
3. SPI programming is at 8 MHz.
4. T_J = 25 °C, power supplies at nominal voltage.
5. Per bank. V_{CCIO} = 2.5 V. Does not include pull-up.
6. No PLL available on the iCE40LP384 and iCE40LP640 devices.
7. V_{CCPLL} is tied to V_{CC} internally in packages without PLLs pins.
8. V_{PP_FAST}, used only for fast production programming, must be left floating or unconnected in applications, except the CM36 and CM49 packages which MUST have the V_{PP_FAST} ball connected to $V_{CCIO\_0\_1}$ ball externally.

4.11. Programming NVCM Supply Current – HX Devices

Table 4.9. Programming NVCM Supply Current – HX Devices[1, 2, 3, 4]

Symbol	Parameter	Device	Typ. VCC[5]	Units
ICC	Core Power Supply	iCE40HX1K	278	µA
		iCE40HX4K	1174	µA
		iCE40HX8K	1174	µA
ICCPLL[6, 7]	PLL Power Supply	All devices	0.5	µA
IPP_2V5	NVCM Power Supply	All devices	2.5	mA
ICCIO[7], ICC_SPI	Bank Power Supply5	All devices	3.5	mA

Notes:

1. Assumes all inputs are held at V_{CCIO} or GND and all outputs are tri-stated.
2. Typical user pattern.
3. SPI programming is at 8 MHz.
4. T_J = 25 °C, power supplies at nominal voltage.
5. Per bank. V_{CCIO} = 2.5 V. Does not include pull-up.
6. V_{CCPLL} is tied to V_{CC} internally in packages without PLL pins.
7. V_{PP_FAST}, used only for fast production programming, must be left floating or unconnected in applications.

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4.12. Peak Startup Supply Current – LP Devices

Table 4.10. Peak Startup Supply Current – LP Devices

Symbol	Parameter	Device	Max	Units
I_{CCPEAK}	Core Power Supply	iCE40LP384	7.7	mA
		iCE40LP640	6.4	mA
		iCE40LP1K	6.4	mA
		iCE40LP4K	15.7	mA
		iCE40LP8K	15.7	mA
$I_{CCPLLPEAK}$[1, 2, 4]	PLL Power Supply	iCE40LP1K	1.5	mA
		iCE40LP640	1.5	mA
		iCE40LP4K	8.0	mA
		iCE40LP8K	8.0	mA
$I_{PP\_2V5PEAK}$	NVCM Power Supply	iCE40LP384	3.0	mA
		iCE40LP640	7.7	mA
		iCE40LP1K	7.7	mA
		iCE40LP4K	4.2	mA
		iCE40LP8K	4.2	mA
$I_{PP\_FASTPEAK}$[3]	NVCM Programming Supply	iCE40LP384	5.7	mA
		iCE40LP640	8.1	mA
		iCE40LP1K	8.1	mA
$I_{CCIOPEAK}$[5], $I_{CC\_SPIPEAK}$	Bank Power Supply	iCE40LP384	8.4	mA
		iCE40LP640	3.3	mA
		iCE40LP1K	3.3	mA
		iCE40LP4K	8.2	mA
		iCE40LP8K	8.2	mA

Notes:

1. No PLL available on the iCE40LP384 and iCE40LP640 device.
2. V_{CCPLL} is tied to V_{CC} internally in packages without PLLs pins.
3. V_{PP_FAST}, used only for fast production programming, must be left floating or unconnected in applications, except the CM36 and CM49 packages which MUST have the V_{PP_FAST} ball connected to $V_{CCIO\_0\_1}$ ball externally.
4. While no PLL is available in the iCE40LP640 the $I_{CCPLLPEAK}$ is additive to I_{CCPEAK}.
5. iCE40LP384 requires V_{CC} to be greater than 0.7 V when V_{CCIO} and V_{CC_SPI} are above GND.

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4.13. Peak Startup Supply Current – HX Devices

Table 4.11. Peak Startup Supply Current – HX Devices

Symbol	Parameter	Device	Max	Units
I_{CCPEAK}	Core Power Supply	iCE40HX1K	6.9	mA
		iCE40HX4K	22.3	mA
		iCE40HX8K	22.3	mA
$I_{CCPLLPEAK}$[1]	PLL Power Supply	iCE40HX1K	1.8	mA
		iCE40HX4K	6.4	mA
		iCE40HX8K	6.4	mA
$I_{PP\_2V5PEAK}$	NVCM Power Supply	iCE40HX1K	2.8	mA
		iCE40HX4K	4.1	mA
		iCE40HX8K	4.1	mA
$I_{CCIOPEAK}$, $I_{CC\_SPIPEAK}$	Bank Power Supply	iCE40HX1K	6.8	mA
		iCE40HX4K	6.8	mA
		iCE40HX8K	6.8	mA

Note:

1. V_{CCPLL} is tied to V_{CC} internally in packages without PLLs pins.

4.14. sysI/O Recommended Operating Conditions

Table 4.12. sysI/O Recommended Operating Conditions

Input/Output Standard	V_{CCIO} (V)		
	Min.	Typ.	Max.
LVCMOS 3.3	3.14	3.3	3.46
LVCMOS 2.5	2.37	2.5	2.62
LVCMOS 1.8	1.71	1.8	1.89
LVDS25E[1, 2]	2.37	2.5	2.62
subLVDSE[1, 2]	1.71	1.8	1.89

Notes:

1. Inputs on-chip. Outputs are implemented with the addition of external resistors.
2. Does not apply to Configuration Bank V_{CC_SPI}.

4.15. sysI/O Single-Ended DC Electrical Characteristics

Table 4.13. sysI/O Single-Ended DC Electrical Characteristics

Input/Output Standard	V_{IL}		V_{IH}[1]		V_{OL} Max. (V)	V_{OH} Min. (V)	I_{OL} Max. (mA)	I_{OH} Max. (mA)
	Min. (V)	Max. (V)	Min. (V)	Max. (V)				
LVCMOS 3.3	–0.3	0.8	2.0	V_{CCIO} + 0.2 V	0.4	V_{CCIO} – 0.4	8, 16[2], 24[2]	–8, –16[2], –24[2]
					0.2	V_{CCIO} – 0.2	0.1	–0.1
LVCMOS 2.5	–0.3	0.7	1.7	V_{CCIO} + 0.2 V	0.4	V_{CCIO} – 0.4	6, 12[2], 18[2]	–6, –12[2], –18[2]
					0.2	V_{CCIO} – 0.2	0.1	–0.1
LVCMOS 1.8	–0.3	$0.35V_{CCIO}$	$0.65V_{CCIO}$	V_{CCIO} + 0.2 V	0.4	V_{CCIO} – 0.4	4, 8[2], 12[2]	–4, –8[2], –12[2]
					0.2	V_{CCIO} – 0.2	0.1	–0.1

Notes:

1. Some products are clamped to a diode when V_{IN} is larger than V_{CCIO}.
2. Only for High Drive LED outputs.

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4.16. sysI/O Differential Electrical Characteristics

The LVDS25E/subLVDSE differential output buffers are available on all banks but the LVDS/subLVDS input buffers are only available on Bank 3 of iCE40 LP/HX devices.

4.16.1. LVDS25

Over recommended operating conditions.

Table 4.14. LVDS25

Parameter Symbol	Parameter Description	Test Conditions	Min.	Typ.	Max.	Units
V_{INP}, V_{INM}	Input Voltage	V_{CCIO}[1] = 2.5	0	—	2.5	V
V_{THD}	Differential Input Threshold	—	250	350	450	mV
V_{CM}	Input Common Mode Voltage	V_{CCIO}[1] = 2.5	(V_{CCIO}/2) - 0.3	V_{CCIO}/2	(V_{CCIO}/2) + 0.3	V
I_{IN}	Input Current	Power on	—	—	±10	µA

Note:

1. Typical

4.16.2. subLVDS

Over recommended operating conditions.

Table 4.15. subLVDS

Parameter Symbol	Parameter Description	Test Conditions	Min.	Typ.	Max.	Units
V_{INP}, V_{INM}	Input Voltage	V_{CCIO}[1] = 1.8	0	—	1.8	V
V_{THD}	Differential Input Threshold	—	100	150	200	mV
V_{CM}	Input Common Mode Voltage	V_{CCIO}[1] = 1.8	(V_{CCIO}/2) - 0.25	V_{CCIO}/2	(V_{CCIO}/2) + 0.25	V
I_{IN}	Input Current	Power on	—	—	±10	µA

Note:

1. Typical

4.17. LVDS25E Emulation

iCE40 LP/HX devices can support LVDSE outputs via emulation on all banks. The output is emulated using complementary LVCMOS outputs in conjunction with resistors across the driver outputs on all devices. The scheme shown in Figure 4.1. LVDS25E Using External Resistors is one possible solution for LVDS25E standard implementation. Resistor values in Figure 4.1. LVDS25E Using External Resistors are industry standard values for 1% resistors.

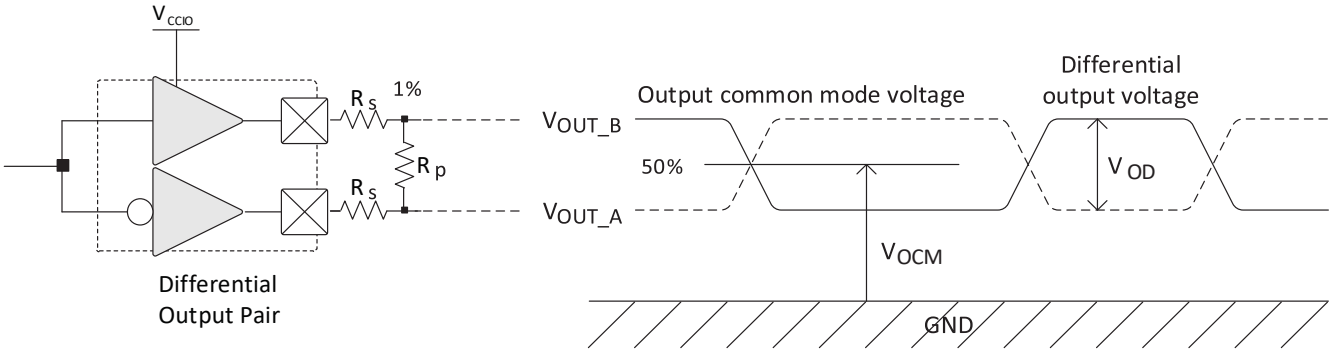

Figure 4.1. LVDS25E Using External Resistors

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Over recommended operating conditions.

Table 4.16. LVDS25E DC Conditions

Parameter	Description	Typ.	Units
Z_{OUT}	Output impedance	20	Ω
R_S	Driver series resistor	150	Ω
R_P	Driver parallel resistor	140	Ω
R_T	Receiver termination	100	Ω
V_{OH}	Output high voltage	1.43	V
V_{OL}	Output low voltage	1.07	V
V_{OD}	Output differential voltage	0.30	V
V_{CM}	Output common mode voltage	1.25	V
Z_{BACK}	Back impedance	100.5	Ω
I_{DC}	DC output current	6.03	mA

4.18. SubLVDS Emulation

The iCE40 LP/HX family supports the differential subLVDS standard. The output standard is emulated using complementary LVCMOS outputs in conjunction with resistors across the driver outputs on all banks of the devices. The subLVDS input standard is supported by the LVDS25 differential input buffer. The scheme shown in Figure 4.2 is one possible solution for subLVDSE output standard implementation. Use LVDS25E mode with suggested resistors for subLVDSE operation. Resistor values in Figure 4.2 are industry standard values for 1% resistors.

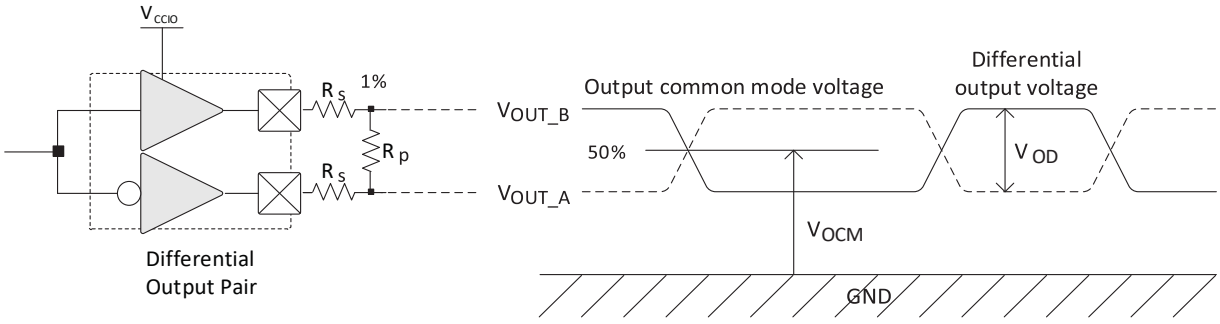

Figure 4.2. subLVDSE DC Conditions

Over recommended operating conditions.

Table 4.17. subLVDSE DC Conditions

Parameter	Description	Typ.	Units
Z_{OUT}	Output impedance	20	Ω
R_S	Driver series resistor	270	Ω
R_P	Driver parallel resistor	120	Ω
R_T	Receiver termination	100	Ω
V_{OH}	Output high voltage	1.43	V
V_{OL}	Output low voltage	1.07	V
V_{OD}	Output differential voltage	0.35	V
V_{CM}	Output common mode voltage	0.9	V
Z_{BACK}	Back impedance	100.5	Ω
I_{DC}	DC output current	2.8	mA

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4.19. Typical Building Block Function Performance – LP Devices[1,2]

4.19.1. Pin-to-Pin Performance (LVCMOS25) – LP Devices

Table 4.18. Pin-to-Pin Performance (LVCMOS25) – LP Devices

Function	Timing	Units
Basic Functions		
16-bit decoder	11.0	ns
4:1 MUX	12.0	ns
16:1 MUX	13.0	ns

4.19.2. Register-to-Register Performance – LP Devices

Table 4.19. Register-to-Register Performance – LP Devices

Function	Timing	Units
Basic Functions		
16:1 MUX	190	MHz
16-bit adder	160	MHz
16-bit counter	175	MHz
Embedded Memory Functions		
256 x 16 Pseudo-Dual Port RAM	240	MHz

Notes:

1. The above timing numbers are generated using the iCECube2 design tool. Exact performance may vary with device and tool version. The tool uses internal parameters that have been characterized but are not tested on every device.
2. Using a VCC of 1.14 V at Junction Temp 85 °C.

4.20. Typical Building Block Function Performance – HX Devices[1,2]

4.20.1. Pin-to-Pin Performance (LVCMOS25) – HX Devices

Table 4.20. Pin-to-Pin Performance (LVCMOS25) – HX Devices

Function	Timing	Units
Basic Functions		
16-bit decoder	10.0	ns
4:1 MUX	9.0	ns
16:1 MUX	9.5	ns

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4.20.2. Register-to-Register Performance – HX Devices

Table 4.21. Register-to-Register Performance – HX Devices

Function	Timing	Units
Basic Functions		
16:1 MUX	305	MHz
16-bit adder	220	MHz
16-bit counter	255	MHz
64-bit counter	105	MHz
Embedded Memory Functions		
256 x 16 Pseudo-Dual Port RAM	403	MHz

Notes:

1. The above timing numbers are generated using the iCECube2 design tool. Exact performance may vary with device and tool version. The tool uses internal parameters that have been characterized but are not tested on every device.
2. Using a VCC of 1.14 V at Junction Temp 85 °C.

4.21. Derating Logic Timing

Logic timing provided in the following sections of the data sheet and the Lattice design tools are worst case numbers in the operating range. Actual delays may be much faster. Lattice design tools can provide logic timing numbers at a particular temperature and voltage.

4.22. Maximum sysI/O Buffer Performance

Table 4.22. Register-to-Register Performance[1]

I/O Standard	Max. Speed	Units
Inputs		
LVDS25[2]	400	MHz
subLVDS18[2]	400	MHz
LVCMOS33	250	MHz
LVCMOS25	250	MHz
LVCMOS18	250	MHz
Outputs		
LVDS25E	250	MHz
subLVDS18E	155	MHz
LVCMOS33	250	MHz
LVCMOS25	250	MHz
LVCMOS18	155	MHz

Notes:

1. Measured with a toggling pattern.
2. Supported in Bank 3 only.

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4.23. Timing Adders

Over recommended operating conditions.

Table 4.23. Timing Adders – LP Devices[1,2,3,4,5]

Input Adjusters			
LVDS25	LVDS, V_{CCIO} = 2.5 V	–0.18	ns
subLVDS	subLVDS, V_{CCIO} = 1.8 V	0.82	ns
LVCMOS33	LVCMOS, V_{CCIO} = 3.3 V	0.18	ns
LVCMOS25	LVCMOS, V_{CCIO} = 2.5 V	0.00	ns
LVCMOS18	LVCMOS, V_{CCIO} = 1.8 V	0.19	ns
Output Adjusters			
LVDS25E	LVDS, Emulated, V_{CCIO} = 2.5 V	0.00	ns
subLVDSE	subLVDS, Emulated, V_{CCIO} = 1.8 V	1.32	ns
LVCMOS33	LVCMOS, V_{CCIO} = 3.3 V	–0.12	ns
LVCMOS25	LVCMOS, V_{CCIO} = 2.5 V	0.00	ns
LVCMOS18	LVCMOS, V_{CCIO} = 1.8 V	1.32	ns

Notes:

1. Timing adders are relative to LVCMOS25 and characterized but not tested on every device.
2. LVCMOS timing measured with the load specified in the Switching Test Condition table.
3. All other standards tested according to the appropriate specifications.
4. Commercial timing numbers are shown.
5. Not all I/O standards are supported for all banks. See the Architecture section of this data sheet for details.

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Over recommended operating conditions.

Table 4.24. Timing Adders – HX Devices[1,2,3,4,5]

Input Adjusters			
LVDS25	LVDS, V_{CCIO} = 2.5 V	0.13	ns
subLVDS	subLVDS, V_{CCIO} = 1.8 V	1.03	ns
LVCMOS33	LVCMOS, V_{CCIO} = 3.3 V	0.16	ns
LVCMOS25	LVCMOS, V_{CCIO} = 2.5 V	0.00	ns
LVCMOS18	LVCMOS, V_{CCIO} = 1.8 V	0.23	ns
Output Adjusters			
LVDS25E	LVDS, Emulated, V_{CCIO} = 2.5 V	0.00	ns
subLVDSE	subLVDS, Emulated, V_{CCIO} = 1.8 V	1.76	ns
LVCMOS33	LVCMOS, V_{CCIO} = 3.3 V	0.17	ns
LVCMOS25	LVCMOS, V_{CCIO} = 2.5 V	0.00	ns
LVCMOS18	LVCMOS, V_{CCIO} = 1.8 V	1.76	ns

Notes:
1. Timing adders are relative to LVCMOS25 and characterized but not tested on every device.
2. LVCMOS timing measured with the load specified in the Switching Test Condition table.
3. All other standards tested according to the appropriate specifications.
4. Commercial timing numbers are shown.
5. Not all I/O standards are supported for all banks. See the Architecture section of this data sheet for details.

4.24. External Switching Characteristics – LP Devices

Over recommended operating conditions.

Table 4.25. External Switching Characteristics – LP Devices[1, 2]

Parameter	Description	Device	Min.	Max.	Units
Clock					
Global Clocks					
f_{MAX_GBUF}	Frequency for Global Buffer Clock network	All iCE40 LP devices	—	275	MHz
t_{W_GBUF}	Clock Pulse Width for Global Buffer	All iCE40 LP devices	0.92	—	ns
t_{SKEW_GBUF}	Global Buffer Clock Skew Within a Device	iCE40LP384	—	370	ps
		iCE40LP640	—	230	ps
		iCE40LP1K	—	230	ps
		iCE40LP4K	—	340	ps
		iCE40LP8K	—	340	ps
Pin-LUT-Pin Propagation Delay					
t_{PD}	Best case propagation delay through one LUT-4	All iCE40 LP devices	—	9.36	ns
General I/O Pin Parameters (Using Global Buffer Clock without PLL)[3]					
t_{SKEW_IO}	Data bus skew across a bank of IOs	iCE40LP384	—	300	ps
		iCE40LP640	—	200	ps
		iCE40LP1K	—	200	ps
		iCE40LP4K	—	280	ps
		iCE40LP8K	—	280	ps
t_{CO}	Clock to Output - PIO Output Register	iCE40LP384	—	6.33	ns
		iCE40LP640	—	5.91	ns
		iCE40LP1K	—	5.91	ns
		iCE40LP4K	—	6.58	ns
		iCE40LP8K	—	6.58	ns

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Parameter	Description	Device	Min.	Max.	Units
t_{SU}	Clock to Data Setup - PIO Input Register	iCE40LP384	–0.08	—	ns
		iCE40LP640	–0.33	—	ns
		iCE40LP1K	–0.33	—	ns
		iCE40LP4K	–0.63	—	ns
		iCE40LP8K	–0.63	—	ns
t_{H}	Clock to Data Hold - PIO Input Register	iCE40LP384	1.99	—	ns
		iCE40LP640	2.81	—	ns
		iCE40LP1K	2.81	—	ns
		iCE40LP4K	3.48	—	ns
		iCE40LP8K	3.48	—	ns
General I/O Pin Parameters (Using Global Buffer Clock with PLL)[3]					
t_{COPLL}	Clock to Output - PIO Output Register	iCE40LP1K	—	2.20	ns
		iCE40LP4K	—	2.30	ns
		iCE40LP8K	—	2.30	ns
t_{SUPLL}	Clock to Data Setup - PIO Input Register	iCE40LP1K	5.23	—	ns
		iCE40LP4K	6.13	—	ns
		iCE40LP8K	6.13	—	ns
t_{HPLL}	Clock to Data Hold - PIO Input Register	iCE40LP1K	–0.90	—	ns
		iCE40LP4K	–0.80	—	ns
		iCE40LP8K	–0.80	—	ns

Notes:

1. Exact performance may vary with device and design implementation. Commercial timing numbers are shown at 85°C and 1.14 V. Other operating conditions can be extracted from the iCECube2 software.
2. General I/O timing numbers based on LVCMOS 2.5, 0 pf load.
3. Supported on devices with a PLL.

4.25. External Switching Characteristics – HX Devices

Over recommended operating conditions.

Table 4.26. External Switching Characteristics – HX Devices[1, 2]

Parameter	Description	Device	Min.	Max.	Units
Clock					
Global Clocks					
f_{MAX_GBUF}	Frequency for Global Buffer Clock network	All iCE40 HX devices	—	275	MHz
t_{W_GBUF}	Clock Pulse Width for Global Buffer	All iCE40 HX devices	0.88	—	ns
t_{SKEW_GBUF}	Global Buffer Clock Skew Within a Device	iCE40HX1K	—	727	ps
		iCE40HX4K	—	300	ps
		iCE40HX8K	—	300	ps
Pin-LUT-Pin Propagation Delay					
t_{PD}	Best case propagation delay through one LUT-4	All iCE40 HX devices	—	7.30	ns
General I/O Pin Parameters (Using Global Buffer Clock without PLL)					
t_{SKEW_IO}	Data bus skew across a bank of IOs	iCE40HX1K	—	696	ps
		iCE40HX4K	—	290	ps
		iCE40HX8K	—	290	ps
t_{CO}	Clock to Output - PIO Output Register	iCE40HX1K	—	5.00	ns
		iCE40HX4K	—	5.41	ns
		iCE40HX8K	—	5.41	ns

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Parameter	Description	Device	Min.	Max.	Units
t_{SU}	Clock to Data Setup - PIO Input Register	iCE40HX1K	–0.23	—	ns
		iCE40HX4K	–0.43	—	ns
		iCE40HX8K	–0.43	—	ns
t_{H}	Clock to Data Hold - PIO Input Register	iCE40HX1K	1.92	—	ns
		iCE40HX4K	2.38	—	ns
		iCE40HX8K	2.38	—	ns
General I/O Pin Parameters (Using Global Buffer Clock with PLL)[3]					
t_{COPLL}	Clock to Output - PIO Output Register	iCE40HX1K	—	2.96	ns
		iCE40HX4K	—	2.51	ns
		iCE40HX8K	—	2.51	ns
t_{SUPLL}	Clock to Data Setup - PIO Input Register	iCE40HX1K	3.10	—	ns
		iCE40HX4K	4.16	—	ns
		iCE40HX8K	4.16	—	ns
t_{HPLL}	Clock to Data Hold - PIO Input Register	iCE40HX1K	–0.60	—	ns
		iCE40HX4K	–0.53	—	ns
		iCE40HX8K	–0.53	—	ns

Notes:

1. Exact performance may vary with device and design implementation. Commercial timing numbers are shown at 85 °C and 1.14 V. Other operating conditions, including industrial, can be extracted from the iCECube2 software.
2. General I/O timing numbers based on LVCMOS 2.5, 0pf load.
3. Supported on devices with a PLL.

4.26. sysClock PLL Timing

Over recommended operating conditions.

Table 4.27. sysClock PLL Timing

Parameter	Descriptions	Conditions	Min.	Max.	Units
f_{IN}	Input Clock Frequency (REFERENCECLK, EXTFEEDBACK)	—	10	133	MHz
f_{OUT}	Output Clock Frequency (PLLOUT)	—	16	275	MHz
f_{VCO}	PLL VCO Frequency	—	533	1066	MHz
AC Characteristics					
t_{DT}	Output Clock Duty Cycle	f_{OUT} < 175 MHz	40	50	%
		175 MHz < f_{OUT} < 275 MHz	35	65	"%
t_{PH}	Output Phase Accuracy	—	—	+/–12	deg
t_{OPJIT}[1, 5]	Output Clock Period Jitter	f_{OUT} <= 100 MHz	—	450	ps p-p
		f_{OUT} > 100 MHz	—	0.05	UIPP
	Output Clock Cycle-to-cycle Jitter	f_{OUT} <= 100 MHz	—	750	ps p-p
		f_{OUT} > 100 MHz	—	0.10	UIPP
	Output Clock Phase Jitter	f_{PFD} <= 25 MHz	—	275	ps p-p
		f_{PFD} > 25 MHz	—	0.05	UIPP
t_{W}	Output Clock Pulse Width	At 90% or 10%	1.3	—	ns
t_{LOCK}[2, 3]	PLL Lock-in Time	—	—	50	us
t_{UNLOCK}	PLL Unlock Time	—	—	50	ns
t_{IPJIT}[4]	Input Clock Period Jitter	$f_{PFD} \geq$ 20 MHz	—	1000	ps p-p
		f_{PFD} < 20 MHz	—	0.02	UIPP

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Parameter	Descriptions	Conditions	Min.	Max.	Units
t_{FDTAP}	Fine Delay adjustment, per Tap	—	147	195	ps
t_{STABLE}[3]	LATCHINPUTVALUE LOW to PLL Stable	—	—	500	ns
t_{STABLE_PW}[3]	LATCHINPUTVALUE Pulse Width	—	—	100	ns
t_{RST}	RESET Pulse Width	—	10	—	ns
t_{RSTREC}	RESET Recovery Time	—	10	—	us
$t_{DYNAMIC\_WD}$	DYNAMICDELAY Pulse Width	—	100	—	VCO Cycles
$t_{PDBYPASS}$	Propagation delay with the PLL in bypass mode	iCE40 LP	1.18	4.68	ns
		iCE40 HX	1.73	4.07	ns

Notes:

1. Period jitter sample is taken over 10,000 samples of the primary PLL output with a clean reference clock. Cycle-to-cycle jitter is taken over 1000 cycles. Phase jitter is taken over 2000 cycles. All values per JESD65B.
2. Output clock is valid after t_{LOCK} for PLL reset and dynamic delay adjustment.
3. At minimum f_{PFD}. As the f_{PFD} increases the time will decrease to approximately 60% the value listed.
4. Maximum limit to prevent PLL unlock from occurring. Does not imply the PLL will operate within the output specifications listed in this table.
5. The jitter values will increase with loading of the PLD fabric and in the presence of SSO noise.

4.27. SPI Master or NVCM Configuration Time

Table 4.28. SPI Master or NVCM Configuration Time[1, 2]

Symbol	Parameter	Condition	Typ.	Units
t_{CONFIG}	POR/CRESET_B to Device I/O Active	iCE40LP384 - Low Frequency (Default)	25	ms
		iCE40LP384 - Medium Frequency	15	ms
		iCE40LP384 - High Frequency	11	ms
		iCE40LP640 - Low Frequency (Default)	53	ms
		iCE40LP640 - Medium Frequency	25	ms
		iCE40LP640 - High Frequency	13	ms
		iCE40LP/HX1K - Low Frequency (Default)	53	ms
		iCE40LP/HX1K - Medium Frequency	25	ms
		iCE40LP/HX1K - High Frequency	13	ms
		iCE40LP/HX4K - Low Frequency (Default)	230	ms
		iCE40LP/HX4K - Medium Frequency	110	ms
		iCE40LP/HX4K - High Frequency	70	ms
		iCE40LP/HX8K - Low Frequency (Default)	230	ms
		iCE40LP/HX8K - Medium Frequency	110	ms
		iCE40LP/HX8K - High Frequency	70	ms

Notes:

1. Assumes sysMEM Block is initialized to an all zero pattern if they are used.
2. The NVCM download time is measured with a fast ramp rate starting from the maximum voltage of POR trip point.

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4.28. sysCONFIG Port Timing Specifications

Table 4.29. sysCONFIG Port Timing Specifications[1]

Symbol	Parameter		Min	Typ	Max	Unit
All Configuration Modes						
t_{CRESET_B}	Minimum CRESET_B Low pulse width required to restart configuration, from falling edge to rising edge	—	200	—	—	ns
t_{DONE_IO}	Number of configuration clock cycles after CDONE goes High before the PIO pins are activated	—	49	—	—	Clock Cycles
Slave SPI						
t_{CR_SCK}	Minimum time from a rising edge on CRESET_B until the first SPI write operation, first SPI_SCK. During this time, the iCE40 device is clearing its internal configuration memory.	iCE40LP384	600	—	—	us
		iCE40LP640, iCE40LP/HX1K	800	—	—	us
		iCE40LP/HX4K	1200	—	—	us
		iCE40LP/HX8K	1200	—	—	us
f_{MAX}	CCLK clock frequency	Write	1	—	25	MHz
		Read iCE40LP384[2]	—	15	—	MHz
		Read iCE40LP640, iCE40LP/HX1K[2]	—	15	—	MHz
		Read iCE40LP/HX4K[2]	—	15	—	MHz
		Read iCE40LP/HX8K[2]	—	15	—	MHz
t_{CCLKH}	CCLK clock pulse width high	—	20	—	—	ns
t_{CCLKL}	CCLK clock pulse width low	—	20	—	—	ns
t_{STSU}	CCLK setup time	—	12		—	ns
t_{STH}	CCLK hold time	—	12	—	—	ns
t_{STCO}	CCLK falling edge to valid output	—	13	—	—	ns
Master SPI						
f_{MCLK}	MCLK clock frequency	Off	—	0	—	MHz
		Low Frequency (Default)	—	7.5	—	MHz
		Medium Frequency[3]	—	24	—	MHz
		High Frequency[3]	—	40	—	MHz
t_{MCLK}	CRESET_B high to first MCLK edge	iCE40LP384 - Low Frequency (Default)	600	—	—	us
		iCE40LP384 - Medium Frequency	600	—	—	us
		iCE40LP384 - High Frequency	600	—	—	us
		iCE40LP640, iCE40LP/HX1K - Low Frequency (Default)	800	—	—	us
		iCE40LP640, iCE40LP/HX1K - Medium Frequency	800	—	—	us
		iCE40LP640, iCE40LP/HX1K - High Frequency	800	—	—	us
		iCE40LP/HX1K -Low Frequency (Default)	800	—	—	us
		iCE40LP/HX1K - Medium Frequency	800	—	—	us
		iCE40LP/HX1K - High Frequency	800	—	—	us
		iCE40LP/HX4K - Low Frequency (Default)	1200	—	—	us
		iCE40LP/HX4K - Medium Frequency	1200	—	—	us

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Symbol	Parameter		Min	Typ	Max	Unit
		iCE40LP/HX4K - high frequency	1200	—	—	us
		iCE40LP/HX8K - Low Frequency (Default)	1200	—	—	us
		iCE40LP/HX8K - Medium Frequency	1200	—	—	us
		iCE40LP/HX8K - High Frequency	1200	—	—	us

Notes:
1. Does not apply for NVCM.
2. Supported only with 1.2 V V_{CC} and at 25 °C.
3. Extended range f_{MAX} Write operations support up to 53 MHz only with 1.2 V V_{CC} and at 25 °C.

4.29. Switching Test Conditions

Figure 4.3 shows the output test load that is used for AC testing. The specific values for resistance, capacitance, voltage, and other test conditions are listed in Table 4.30.

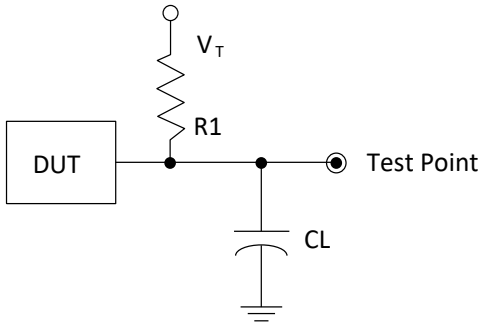

Figure 4.3. Output Test Load, LVCMOS Standards

Table 4.30. Test Fixture Required Components, Non-Terminated Interfaces[1]

Test Condition	R_1	C_L	Timing Reference	V_T
LVCMOS settings (L ≥ H, H ≥ L)	∞	0 pF	LVCMOS 3.3 = 1.5 V	—
			LVCMOS 2.5 = $V_{CCIO}/2$	—
			LVCMOS 1.8 = $V_{CCIO}/2$	—
LVCMOS 3.3 (Z ≥ H)	188	0 pF	1.5 V	V_{OL}
LVCMOS 3.3 (Z ≥ L)			1.5 V	V_{OH}
Other LVCMOS (Z ≥ H)			$V_{CCIO}/2$	V_{OL}
Other LVCMOS (Z ≥ L)			$V_{CCIO}/2$	V_{OH}
LVCMOS (H ≥ Z)			V_{OH} – 0.15 V	V_{OL}
LVCMOS (L ≥ Z)			V_{OL} – 0.15 V	V_{OH}

Note:
1. Output test conditions for all other interfaces are determined by the respective standards.

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5. Pinout Information

5.1. Signal Descriptions

5.1.1. General Purpose

Signal Name	I/O	Description
IO[Bank]_[Row/Column Number][A/B]	I/O	[Bank] indicates the bank of the device on which the pad is located. [Number] indicates I/O number on the device.
IO[Bank]_[Row/Column Number][A/B]	I/O	[Bank] indicates the bank of the device on which the pad is located. [Number] indicates I/O number on the device. [A/B] indicates the differential I/O. 'A' = negative input. 'B' = positive input.
HCIO[Bank]_[Number]	I/O	High Current I/O. [Bank] indicates the bank of the device on which the pad is located. [Number] indicates IO number.
NC	—	No connect
GND	—	GND – Ground. Dedicated pins. It is recommended that all GNDs are tied together.
VCC	—	VCC – The power supply pins for core logic. Dedicated pins. It is recommended that all VCCs are tied to the same supply.
V_{CCIO_x}	—	V_{CCIO} – The power supply pins for I/O Bank x. Dedicated pins. All VCCIOs located in the same bank are tied to the same supply.

5.1.2. PLL and Global Functions (Used as user-programmable I/O pins when not used for PLL or clock pins)

Signal Name	I/O	Description
V_{CCPLLx}	—	PLL VCC – Power. Dedicated pins. The PLL requires a separate power and ground that is quiet and stable to reduce the output clock jitter of the PLL.
GNDPLLx	—	PLL GND – Ground. Dedicated pins. The sysCLOCK PLL has the DC ground connection made on the FPGA, so the external PLL ground connection (GNDPLL) must NOT be connected to the board's ground.
GBINx	—	Global pads. Two per side.

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5.1.3. Programming and Configuration

Signal Name	I/O	Description
CBSEL[0:1]	I/O	Dual function pins. I/O when not used as CBSEL. Optional ColdBoot configuration Select input, if ColdBoot mode is enabled.
CRESET_B	I	Configuration Reset, active Low. Dedicated input. No internal pull-up resistor. Either actively drive externally or connect a 10 kΩ pull-up resistor to V_{CCIO_2}.
CDONE	I/O	Configuration Done. Includes a permanent weak pull-up resistor to V_{CCIO_2}. If driving external devices with CDONE output, an external pull-up resistor to V_{CCIO_2} may be required. Refer to the iCE40 Programming and Configuration (FPGA-TN-02001) for more details. Following device configuration the iCE40LP640 and iCE40LP1K in the SWG16 package CDONE pin can be used as a user output.
V_{CC_SPI}	—	SPI interface voltage supply input. Must have a valid voltage even if configuring from NVCM.
SPI_SCK	I/O	Input Configuration Clock for configuring an FPGA in Slave SPI mode. Output Configuration Clock for configuring an FPGA configuration modes.
SPI_SS	I/O	SPI Slave Select. Active Low. Includes an internal weak pull-up resistor to VCC_SPI during configuration. During configuration, the logic level sampled on this pin determines the configuration mode used by the iCE40 LP/HX device. An input when sampled at the start of configuration. An input when in SPI Peripheral configuration mode (SPI_SS = Low). An output when in Master SPI Flash configuration mode.
SPI_SI	I/O	Slave SPI serial data input and master SPI serial data output
SPI_SO	I/O	Slave SPI serial data output and master SPI serial data input
V_{PP_FAST}	—	Optional fast NVCM programming supply. V_{PP_FAST}, used only for fast production programming, must be left floating or unconnected in applications, except the CM36 and CM49 packages which MUST have the V_{PP_FAST} ball connected to $V_{CCIO\_0\_1}$ ball externally.
V_{PP_2V5}	—	V_{PP_2V5} NVCM programming and operating supply

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5.2. Pin Information Summary

	iCE40LP384			iCE40LP640	iCE40LP1K							
	SG32	CM36[2]	CM49[2]	SWG16	SWG16	CM36[1,]	CM49[1,]	CM81	CB81	QN84	CM121	CB121
General Purpose I/O per Bank												
Bank 0	6	4	10	3	3	4	10	17	17	17	24	24
Bank 1	5	7	7	0	0	7	7	15	16	17	25	21
Bank 2	0	4	4	1	1	4	4	11	8	11	18	19
Bank 3	6	6	12	2	2	6	10	16	17	18	24	24
Configuration	4	4	4	4	4	4	4	4	4	4	4	4
Total General Purpose Single	21	25	37	10	10	25	35	63	62	67	95	92
High Current Outputs per Bank												
Bank 0	0	0	0	3	3	0	0	0	0	0	0	0
Bank 1	0	0	0	0	0	0	0	0	0	0	0	0
Bank 2	0	0	0	0	0	0	0	0	0	0	0	0
Bank 3	0	0	0	0	0	0	0	0	0	0	0	0
Total Current	0	0	0	3	3	0	0	0	0	0	0	0
Differential Inputs per Bank												
Bank 0	0	0	0	0	0	0	0	0	0	0	0	0
Bank 1	0	0	0	0	0	0	0	0	0	0	0	0
Bank 2	0	0	0	0	0	0	0	0	0	0	0	0
Bank 3	3	3	6	1	1	3	5	8	9	7	12	12
Total Differential	3	3	6	1	1	3	5	8	9	7	12	12
Dedicated Inputs per Bank												
Bank 0	0	0	0	0	0	0	0	0	0	0	0	0
Bank 1	0	0	0	0	0	0	0	0	0	0	0	0
Bank 2	2	2	2	1	1	2	2	2	2	2	2	2
Bank 3	0	0	0	0	0	0	0	0	0	0	0	0
Configuration	0	0	0	0	0	0	0	0	0	0	0	0
Total Dedicated	2	2	2	1	1	2	2	2	2	2	2	2
V_{ccio} Pins												
Bank 0	1	1	1	1	1	1	1	1	1	1	2	1
Bank 1	1	1	1	0	0	0	0	1	1	1	2	1
Bank 2	1	1	1	1	1	1	1	1	1	1	2	1
Bank 3	1	0	0	0	0	0	0	1	1	1	2	2
V_{CC}	1	1	2	1	1	1	2	3	3	4	4	4
V_{CC_SPI}	1	1	1	0	0	1	1	1	1	1	1	1
V_{PP_2V}[5]	1	1	1	0	0	1	1	1	1	1	1	1
V_{PP_FAST}[3]	0	0	0	0	0	1	1	1	0	1	1	1
V_{CCPLL}	0	0	0	0	0	0	1	1	0	0	1	1
GND	2	3	3	2	2	3	4	5	8	4	8	11
NC	0	0	0	0	0	0	0	0	0	0	0	3
Total Count of Bonded Pins	32	36	49	16	16	36	49	81	81	84	121	121

Notes:

1. V_{CCIO0} and V_{CCIO1} are connected together.
2. V_{CCIO2} and V_{CCIO3} are connected together.
3. V_{PP_FAST}, used only for fast production programming, must be left floating or unconnected in applications, except the CM36 and CM49 packages which MUST have the V_{PP_FAST} ball connected to $V_{CCIO\_0\_1}$ ball externally.

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	iCE40LP4K			iCE40LP8K			iCE40HX1K		
	CM81	**CM121**	**CM225**	**CM81**	**CM121**	**CM225**	**VQ100**	**CB132**	**TQ144**
General Purpose I/O per Bank									
Bank 0	17	23	46	17	23	46	19	24	23
Bank 1	15	21	42	15	21	42	19	25	25
Bank 2	9	19	40	9	19	40	12	20	20
Bank 3	18	26	46	18	26	46	18	22	24
Configuration	4	4	4	4	4	4	4	4	4
Total General Purpose	63	93	178	63	93	178	72	95	96
High Current Outputs per Bank									
Bank 0	0	0	0	0	0	0	0	0	0
Bank 1	0	0	0	0	0	0	0	0	0
Bank 2	0	0	0	0	0	0	0	0	0
Bank 3	0	0	0	0	0	0	0	0	0
Total Differential	0	0	0	0	0	0	0	0	0
Differential Inputs per Bank									
Bank 0	0	0	0	0	0	0	0	0	0
Bank 1	0	0	0	0	0	0	0	0	0
Bank 2	0	0	0	0	0	0	0	0	0
Bank 3	9	13	23	9	13	23	9	11	12
Total Differential	9	13	23	9	13	23	9	11	12
Dedicated Inputs per Bank									
Bank 0	0	0	0	0	0	0	0	0	0
Bank 1	0	0	1	0	0	1	0	0	0
Bank 2	2	2	2	2	2	2	2	2	2
Bank 3	0	0	0	0	0	0	0	0	0
Configuration	0	0	0	0	0	0	0	0	0
Total Dedicated	2	2	3	2	2	3	2	2	2
V_{ccio} Pins									
Bank 0	1	1	3	1	1	3	2	2	2
Bank 1	1	1	3	1	1	3	2	2	2
Bank 2	1	1	3	1	1	3	2	2	2
Bank 3	1	2	4	1	2	4	3	3	2
V_{CC}	3	4	8	3	4	8	4	5	4
V_{CC_SPI}	1	1	1	1	1	1	1	1	1
V_{PP_2V5}	1	1	1	1	1	1	1	1	1
V_{PP_FAST}[1]	1	1	1	1	1	1	1	1	1
V_{CCPLL}	1	2	2	1	2	2	0	1	1
GND	5	12	18	5	12	18	10	14	10
NC	0	0	0	0	0	0	0	2	19
Total Count of Bonded Pins	81	121	225	81	121	225	100	132	144

Note:

1. V_{PP_FAST}, used only for fast production programming, must be left floating or unconnected in applications

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	iCE40HX4K			iCE40HX8K			
	BG121	CB132	TQ144	BG121	CB132	CM225	CT256
General Purpose I/O per Bank							
Bank 0	23	24	27	23	24	46	52
Bank 1	21	25	29	21	25	42	52
Bank 2	19	18	19	19	18	40	46
Bank 3	26	24	28	26	24	46	52
Configuration	4	4	4	4	4	4	4
Total General Purpose Single Ended I/O	93	95	107	93	95	178	206
High Current Outputs per Bank							
Bank 0	0	0	0	0	0	0	0
Bank 1	0	0	0	0	0	0	0
Bank 2	0	0	0	0	0	0	0
Bank 3	0	0	0	0	0	0	0
Total Differential Inputs	0	0	0	0	0	0	0
Differential Inputs per Bank							
Bank 0	0	0	0	0	0	0	0
Bank 1	0	0	0	0	0	0	0
Bank 2	0	0	0	0	0	0	0
Bank 3	13	12	14	13	12	23	26
Total Differential Inputs	13	12	14	13	12	23	26
Dedicated Inputs per Bank							
Bank 0	0	0	0	0	0	0	0
Bank 1	0	0	0	0	0	0	0
Bank 2	2	2	2	2	2	2	2
Bank 3	0	0	0	0	0	0	0
Configuration	0	0	0	0	0	0	0
Total Dedicated Inputs	2	2	2	2	2	2	2
V_{ccio} Pins							
Bank 0	1	2	2	1	2	3	4
Bank 1	1	2	2	1	2	3	4
Bank 2	1	2	2	1	2	3	4
Bank 3	2	3	2	2	3	4	4
V_{CC}	4	5	4	4	5	8	6
V_{CC_SPI}	1	1	1	1	1	1	1
V_{PP_2V5}	1	1	1	1	1	1	1
V_{PP_FAST}[1]	1	1	1	1	1	1	1
V_{CCPLL}	2	2	2	2	2	2	2
GND	12	15	11	12	15	18	20
NC	0	0	6	0	0	0	0
Total Count of Bonded Pins	121	132	144	121	132	225	256

Note:

1. V_{PP_FAST}, used only for fast production programming, must be left floating or unconnected in applications.

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5.3. iCE40 LP/HX Part Number Description

5.3.1. Ultra Low Power (LP) Devices

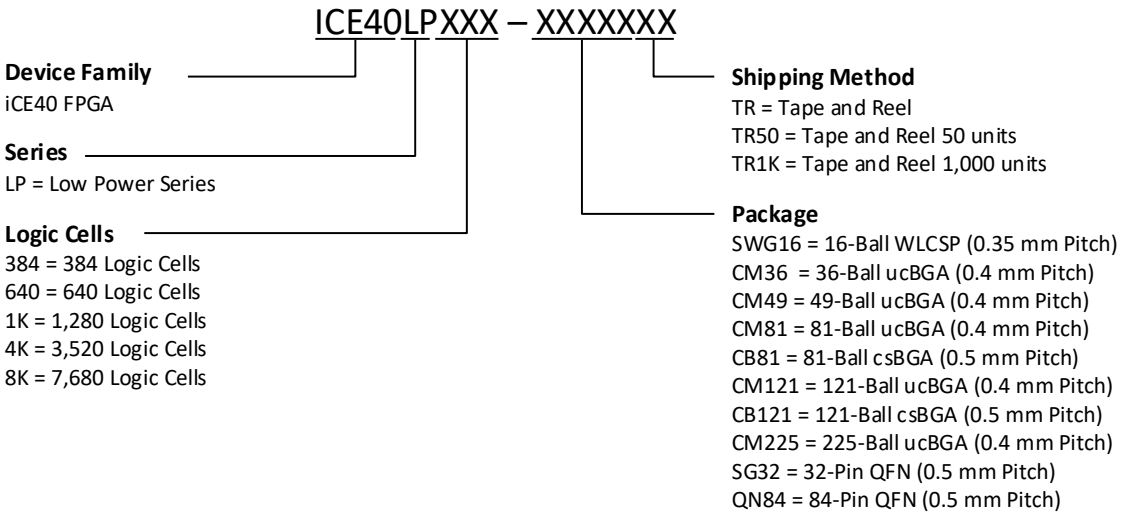

Figure 5.1. Low Power (LP) Devices

5.3.2. High Performance (HX) Devices

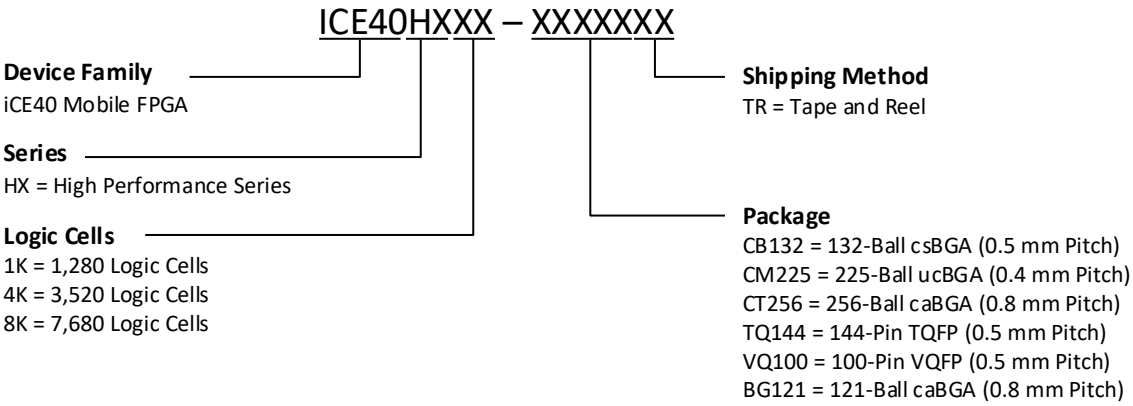

Figure 5.2. High Performance (HX) Devices

Note: All parts shipped in trays unless noted.

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5.4. Ordering Information

iCE40 LP/HX devices have top-side markings as shown below:

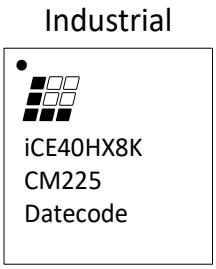

Figure 5.3. High Performance (HX) Devices

Note: Markings are abbreviated for small packages.

5.5. Ordering Part Numbers

5.5.1. Ultra Low Power Industrial Grade Devices, Halogen Free (RoHS) Packaging

Part Number	LUTs	Supply Voltage	Package	Leads	Temperature
ICE40LP384-CM36	384	1.2 V	Halogen-Free ucBGA	36	IND
ICE40LP384-CM36TR	384	1.2 V	Halogen-Free ucBGA	36	IND
ICE40LP384-CM36TR1K	384	1.2 V	Halogen-Free ucBGA	36	IND
ICE40LP384-CM49	384	1.2 V	Halogen-Free ucBGA	49	IND
ICE40LP384-CM49TR	384	1.2 V	Halogen-Free ucBGA	49	IND
ICE40LP384-CM49TR1K	384	1.2 V	Halogen-Free ucBGA	49	IND
ICE40LP384-SG32	384	1.2 V	Halogen-Free QFN	32	IND
ICE40LP384-SG32TR	384	1.2 V	Halogen-Free QFN	32	IND
ICE40LP384-SG32TR1K	384	1.2 V	Halogen-Free QFN	32	IND
ICE40LP640-SWG16TR	640	1.2 V	Halogen-Free WLCSP	16	IND
ICE40LP640-SWG16TR1K	640	1.2 V	Halogen-Free WLCSP	16	IND
ICE40LP640-CM36A	640	1.2 V	Halogen-Free ucBGA	36	IND
ICE40LP1K-SWG16TR	1280	1.2 V	Halogen-Free WLCSP	16	IND
ICE40LP1K-SWG16TR1K	1280	1.2 V	Halogen-Free WLCSP	16	IND
ICE40LP1K-CM36	1280	1.2 V	Halogen-Free ucBGA	36	IND
ICE40LP1K-CM36A	1280	1.2 V	Halogen-Free ucBGA	36	IND
ICE40LP1K-CM36TR	1280	1.2 V	Halogen-Free ucBGA	36	IND
ICE40LP1K-CM36TR1K	1280	1.2 V	Halogen-Free ucBGA	36	IND
ICE40LP1K-CM49	1280	1.2 V	Halogen-Free ucBGA	49	IND
ICE40LP1K-CM49TR	1280	1.2 V	Halogen-Free ucBGA	49	IND
ICE40LP1K-CM49TR1K	1280	1.2 V	Halogen-Free ucBGA	49	IND
ICE40LP1K-CM81	1280	1.2 V	Halogen-Free ucBGA	81	IND
ICE40LP1K-CM81TR	1280	1.2 V	Halogen-Free ucBGA	81	IND
ICE40LP1K-CM81TR1K	1280	1.2 V	Halogen-Free ucBGA	81	IND
ICE40LP1K-CB81	1280	1.2 V	Halogen-Free csBGA	81	IND
ICE40LP1K-CM121	1280	1.2 V	Halogen-Free ucBGA	121	IND
ICE40LP1K-CM121TR	1280	1.2 V	Halogen-Free ucBGA	121	IND
ICE40LP1K-CM121TR1K	1280	1.2 V	Halogen-Free ucBGA	121	IND

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Part Number	LUTs	Supply Voltage	Package	Leads	Temperature
ICE40LP1K-CB121	1280	1.2 V	Halogen-Free csBGA	121	IND
ICE40LP1K-QN84	1280	1.2 V	Halogen-Free QFN	84	IND
ICE40LP4K-CM81	3520	1.2 V	Halogen-Free ucBGA	81	IND
ICE40LP4K-CM81TR	3520	1.2 V	Halogen-Free ucBGA	81	IND
ICE40LP4K-CM81TR1K	3520	1.2 V	Halogen-Free ucBGA	81	IND
ICE40LP4K-CM121	3520	1.2 V	Halogen-Free ucBGA	121	IND
ICE40LP4K-CM121TR	3520	1.2 V	Halogen-Free ucBGA	121	IND
ICE40LP4K-CM121TR1K	3520	1.2 V	Halogen-Free ucBGA	121	IND
ICE40LP4K-CM225	3520	1.2 V	Halogen-Free ucBGA	225	IND
ICE40LP8K-CM81	7680	1.2 V	Halogen-Free ucBGA	81	IND
ICE40LP8K-CM81TR	7680	1.2 V	Halogen-Free ucBGA	81	IND
ICE40LP8K-CM81TR1K	7680	1.2 V	Halogen-Free ucBGA	81	IND
ICE40LP8K-CM121	7680	1.2 V	Halogen-Free ucBGA	121	IND
ICE40LP8K-CM121TR	7680	1.2 V	Halogen-Free ucBGA	121	IND
ICE40LP8K-CM121TR1K	7680	1.2 V	Halogen-Free ucBGA	121	IND
ICE40LP8K-CM225	7680	1.2 V	Halogen-Free ucBGA	225	IND

5.5.2. High-Performance Industrial Grade Devices, Halogen Free (RoHS) Packaging

Part Number	LUTs	Supply Voltage	Package	Leads	Temperature
ICE40HX1K-CB132	1280	1.2 V	Halogen-Free csBGA	132	IND
ICE40HX1K-VQ100	1280	1.2 V	Halogen-Free VQFP	100	IND
ICE40HX1K-TQ144	1280	1.2 V	Halogen-Free TQFP	144	IND
ICE40HX4K-BG121	3520	1.2 V	Halogen-Free caBGA	121	IND
ICE40HX4K-BG121TR	3520	1.2 V	Halogen-Free caBGA	121	IND
ICE40HX4K-CB132	3520	1.2 V	Halogen-Free csBGA	132	IND
ICE40HX4K-TQ144	3520	1.2 V	Halogen-Free TQFP	144	IND
ICE40HX8K-BG121	7680	1.2 V	Halogen-Free caBGA	121	IND
ICE40HX8K-BG121TR	7680	1.2 V	Halogen-Free caBGA	121	IND
ICE40HX8K-CB132	7680	1.2 V	Halogen-Free csBGA	132	IND
ICE40HX8K-CM225	7680	1.2 V	Halogen-Free ucBGA	225	IND
ICE40HX8K-CT256	7680	1.2 V	Halogen-Free caBGA	256	IND

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Supplemental Information

For Further Information

A variety of technical documents for the iCE40 LP/HX family are available on the Lattice web site.

- iCE40 Programming and Configuration (FPGA-TN-02001)
- Memory Usage Guide for iCE40 Devices (FPGA-TN-02002)
- iCE40 sysCLOCK PLL Design and Usage Guide (FPGA-TN-02009)
- iCE40 Hardware Checklist (FPGA-TN-02006)
- Using Differential I/O LVDS Sub-LVDS in iCE40 Devices (FPGA-TN-02213)
- PCB Layout Recommendations for BGA Packages (FPGA-TN-02010)
- iCE40 LED Driver Usage Guide (FPGA-TN-02021)
- iCE40 Pinout Files
- Thermal Management
- Lattice design tools
- IBIS
- Package Diagrams
- Schematic Symbols

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Revision History

Revision 3.9, July 2022

Section	Change Summary
Pinout Information	Updated ordering part numbers list for Ultra Low Power Industrial Grade Devices, Halogen Free (RoHS) Packaging: • Added part numbers ICE40LP640-CM36A and ICE40LP1K-CM36A • Deleted part numbers ICE40LP640-SWG16TR50, ICE40LP1K-SWG16TR50, ICE40LP1K-CB81TR, and ICE40LP1K-CB81TR1K

Revision 3.8, April 2022

Section	Change Summary
DC and Switching Characteristics	• Updated the definition of V_{PP_FAST}. • Updated footnote 4 in Table 4.2. Recommended Operating Conditions. • Updated footnote 8 in Table 4.8. Programming NVCM Supply Current – LP Devices. • Updated footnote 3 in Table 4.10. Peak Startup Supply Current – LP Devices.
Pinout Information	Updated footnote 3 in section Pin Information Summary.

Revision 3.7, October 2020

Section	Change Summary
DC and Switching Characteristics	Updated Table 4.29. sysCONFIG Port Timing Specifications1. Changed duplicated t_{CR_SCK} entry to f_{MAX} and corrected parameter.

Revision 3.6, October 2020

Section	Change Summary
Disclaimers	Added this section.
Product Family	Updated Table 2.1. iCE40 LP/HX Family Selection Guide.
Architecture	Updated Figure 3.3. PLL Diagram.
DC and Switching Characteristics	• Added Power-up Supply Sequence section. • Updated Test Conditions values in Table 4.15. subLVDS.

Revision 3.5, September 2018

Section	Change Summary
All	• Changed document number from DS1040 to FPGA-DS-02029. • Updated document template.
Pinout Information	Changed signal name from SPI_SS_B to SPI_SS in Signal Descriptions table.

Revision 3.4, October 2017

Section	Change Summary
Pin Information	Modified the dedicated inputs for Bank 1 of iCE40HX1K (CB132, TQ144), iCE40HX4K (CB132, TQ144) and iCE40HX8K (CB132, CM225, CT256).

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Revision 3.3, March 2017

Section	Change Summary
Introduction	Updated Features section. Added 121-ball caBGA package for ICE40 HX4K/8K to Table 2.1, iCE40 LP/HX Family Selection Guide.
Architecture	Updated PLB Blocks section. Changed “subtracters” to “subtractors” in the Carry Logic description.
	Updated Clock/Control Distribution Network section. Switched the Clock Enable and the Reset headings in Table 3.1, Global Buffer (GBUF) Connections to Programmable Logic Blocks.
Pinout Information	Updated Pin Information Summary section. Added BG121 information under iCE40HX4K and iCE40HX8K.
Ordering Information	Updated iCE40 LP/HX Part Number Description section. Added Shipping Method and BG121 package under High Performance (HX) Devices.
	Updated Ordering Information section. Added part numbers for BG121 under High-Performance Industrial Grade Devices, Halogen Free (RoHS) Packaging.
Supplemental Information	Corrected reference to “Package Diagrams Data Sheet”.

Revision 3.2, October 2015

Section	Change Summary
Introduction	Updated Features section. Added footnote to 16 WLCSP Programmable I/O: Max Inputs (LVDS25) in Table 2.1, iCE40 LP/HX Family Selection Guide.
DC and Switching Characteristics	Updated sysCLOCK PLL Timing section. Changed tDT conditions.
	Updated Programming NVCM Supply Current – LP Devices section. Changed IPP_2V5 and ICCIO, ICC_SPI units.

Revision 3.1, March 2015

Section	Change Summary
DC and Switching Characteristics	Updated sysI/O Single-Ended DC Electrical Characteristics section. Changed LVCMOS 3.3 and LVCMOS 2. 5 VOH Min. (V) from 0.5 to 0.4.

Revision 3.0, July 2014

Section	Change Summary
DC and Switching Characteristics	Revised and/or added Typ. V_{CC} data in the following sections. • Static Supply Current – LP Devices • Static Supply Current – HX Devices • Programming NVCM Supply Current – LP Devices • Programming NVCM Supply Current – HX Devices In each section table, the footnote indicating Advanced device status was removed.
Pinout Information	Updated Pin Information Summary section. Added footnote 1 to CM49 under iCE40LP1K.

Revision 2.9, April 2014

Section	Change Summary
Ordering Information	Changed “i” to “I” in part number description and ordering part numbers.
	Added part numbers to the Ultra Low Power Industrial Grade Devices, Halogen Free (RoHS) Packaging table.

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Revision 2.8, February 2014

Section	Change Summary
DC and Switching Characteristics	Updated Features section. • Corrected standby power units. • Included High Current LED Drivers.
	• Updated Table 2.1, iCE40 LP/HX Family Selection Guide. • Removed LP384 Programmable I/O for 81 ucBGA package.
Architecture	Updated Supported Standards section. Added information on High Current LED drivers.
DC and Switching Characteristics	Corrected typos.
	Added footnote to the Peak Startup Supply Current – LP Devices table.
Ordering Information	Updated part number description in the Ultra Low Power (LP) Devices section.
	Added part numbers to the Ultra Low Power Industrial Grade Devices, Halogen Free (RoHS) Packaging table.

Revision 2.7, October 2013

Section	Change Summary
Introduction	Updated Features list and iCE40 LP/HX Family Selection Guide table.
Architecture	Revised iCE40-1K device to iCE40LP/HX1K device.
DC and Switching Characteristics	Added iCE40LP640 device information.
Pinout Information	Added iCE40LP640 and iCE40LP1K information.
Ordering Information	Added iCE40LP640 and iCE40LP1K information.

Revision 2.6, September 2013

Section	Change Summary
DC and Switching Characteristics	Updated Absolute Maximum Ratings section.
	Updated sysCLOCK PLL Timing – Preliminary table.
Pinout Information	Updated Pin Information Summary table.

Revision 2.5, August 2013

Section	Change Summary
Introduction	Updated the iCE40 LP/HX Family Selection Guide table.
DC and Switching Characteristics	Updated the following tables: • Absolute Maximum Ratings • Power-On-Reset Voltage Levels • Static Supply Current – LP Devices • Static Supply Current – HX Devices • Programming NVCM Supply Current – LP Devices • Programming NVCM Supply Current – HX Devices • Peak Startup Supply Current – LP Devices • sysI/O Recommended Operating Conditions • Typical Building Block Function Performance – HX Devices • External Switching Characteristics – HX Devices • sysCLOCK PLL Timing – Preliminary • SPI Master or NVCM Configuration Time
Pinout Information	Updated the Pin Information Summary table.

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Revision 2.4, July 2013

Section	Change Summary
Introduction	Updated the iCE40 LP/HX Family Selection Guide table.
DC and Switching Characteristics	Updated the sysCONFIG Port Timing Specifications table.
	Updated footnote in DC Electrical Characteristics table.
	GDDR tables removed. Support to be provided in a technical note.
Pinout Information	Updated the Pin Information Summary table.
Ordering Information	Updated the top-side markings figure.
	Updated the Ultra Low Power Industrial Grade Devices, Halogen Free (RoHS) Packaging table.

Revision 2.3, May 2013

Section	Change Summary
DC and Switching Characteristics	Added new data from Characterization.

Revision 2.2, April 2013

Section	Change Summary
Introduction	Added the LP8K 81 ucBGA.
Architecture	Corrected typos.
DC and Switching Characteristics	Corrected typos.
Pinout Information	Added 7:1 LVDS waveforms.
Ordering Information	Corrected typos in signal descriptions.

Revision 2.1, March 2013

Section	Change Summary
DC and Switching Characteristics	Recommended operating conditions added requirement for Master SPI.
	Updated Recommended Operating Conditions for VPP_2V5.
	Updated Power-On-Reset Voltage Levels and sequence requirements.
	Updated Static Supply Current conditions.
	Changed unit for tSKEW_IO from ns to ps.
	Updated range of CCLK fMAX.
Ordering Information	Updated ordering information to include tape and reel part numbers.

Revision 2.0, September 2012

Section	Change Summary
All	Merged SiliconBlue iCE40 LP and HX data sheets and updated to Lattice format.

Revision 1.31, September 2012

Section	Change Summary
Introduction	Updated Table 3.1.

Revision 1.3, September 2012

Section	Change Summary
All	Production release.
Architecture	• Updated notes on Table 3.2: Recommended Operating Conditions. • Updated values in Table 3.3 and Table 3.4.
DC and Switching Characteristics	Updated values in Table 4.2, Table 4.3 and Table 4.7.

Revision 1.21, September 2012

Section	Change Summary
Architecture	Updated Figure 3.3 and Figure 3.4 to specify iCE40.

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Revision 1.2, August 2012

Section	Change Summary
All	Updated company name.

Revision 1.1, July 2011

Section	Change Summary
Product Family	Moved package specifications to iCE40 pinout Excel files.
	Updated Table 2.1 maximum I/O.

Revision 1.01, July 2011

Section	Change Summary
Product Family	Added 640, 1K and 4K to Table 4.3 configuration times. Updated Table 2.1 maximum I/O.

Revision 1.0, July 2011

Section	Change Summary
All	Initial release.

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