TEXAS INSTRUMENTS

OPA227, OPA2227, OPA4227
OPA228, OPA2228, OPA4228

SBOS110B – MAY 1998 – REVISED JUNE 2015

OPAx22x High Precision, Low Noise Operational Amplifiers

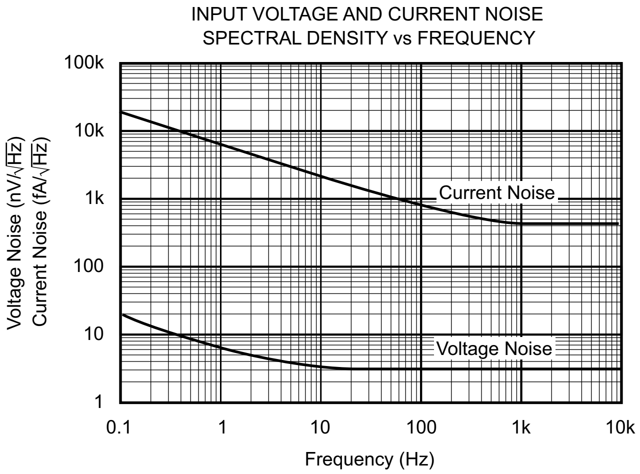
1 Features

- Low Noise: 3nV/√Hz
- Wide Bandwidth:
  - OPA227: 8 MHz, 2.3 V/µs
  - OPA228: 33 MHz, 10 V/µs
- Settling Time: 5 µs (Significant Improvement Over OP-27)
- High CMRR: 138 dB
- High Open-loop Gain: 160 dB
- Low Input Bias Current: 10 nA Maximum
- Low Offset Voltage: 75 µV Maximum
- Wide Supply Range: ±2.5 V to ±18 V
- OPA227 Replaces OP-27, LT1007, MAX427
- OPA228 Replaces OP-37, LT1037, MAX437
- Single, Dual, and Quad Versions

2 Applications

- Data Acquisition
- Telecom Equipment
- Geophysical Analysis
- Vibration Analysis
- Spectral Analysis
- Professional Audio Equipment
- Active Filters
- Power Supply Controls

Input Referred Noise



3 Description

The OPAx22x series operational amplifiers combine low noise and wide bandwidth with high precision to make them the ideal choice for applications requiring both AC and precision DC performance.

The OPAx227 is unity-gain stable and features high slew rate (2.3V/µs) and wide bandwidth (8MHz). The OPAx228 is optimized for closed-loop gains of 5 or greater, and offers higher speed with a slew rate of 10V/µs and a bandwidth of 33MHz.

The OPAx227 and OPAx228 series operational amplifiers are ideal for professional audio equipment. In addition, low quiescent current and low cost make them ideal for portable applications requiring high precision.

The OPAx227 and OPAx228 series operational amplifiers are pin-for-pin replacements for the industry standard OP-27 and OP-37 with substantial improvements across the board. The dual and quad versions are available for space savings and per channel cost reduction.

The OPAx227, OPAx228, are available in DIP-8 and SO-8 packages. The OPA4227 and OPA4228 are available in DIP-14 and SO-14 packages with standard pin configurations. Operation is specified from –40°C to 85°C.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
OPA227 OPA228	PDIP (8)	9.81 mm × 6.35 mm
	SOIC (8)	4.90 mm × 3.91 mm
OPA2227 OPA2228	PDIP (8)	9.81 mm × 6.35 mm
	SOIC (8)	4.90 mm × 3.91 mm
OPA4227 OPA4228	PDIP (14)	19.30 mm × 6.35 mm
	SOIC (14)	8.65 mm × 3.91 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Table of Contents

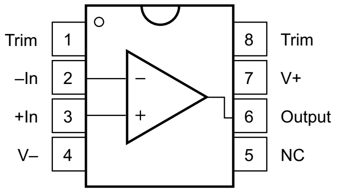
4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (January 2005) to Revision B	**Page**
• Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1

5 Pin Configuration and Functions

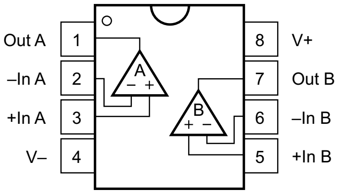
OPA227, OPA228: P or D Package
8-Pin PDIP or 8-Pin SOIC
Top View



DIP-8, SO-8

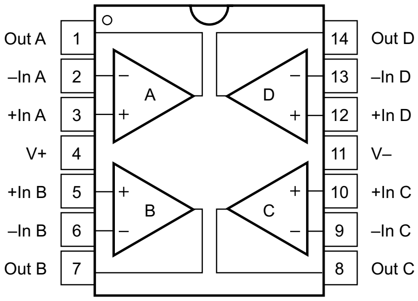
NC = Not Connected

OPA2227, OPA2228: P or D Package
8-Pin PDIP or 8-Pin SOIC
Top View



DIP-8, SO-8

OPA4227, OPA4228: N or D Package
14-Pin PDIP or 14-Pin-SOIC
Top View



DIP-14, SO-14

Pin Functions: OPA227 and OPA228

PIN		I/O	DESCRIPTION
NAME	PDIP, SOIC		
Offset Trim	1	I	Input offset voltage trim (leave floating if not used)
-In	2	I	Inverting input
+In	3	I	Noninverting input
V-	4	—	Negative (lowest) power supply
NC	5	—	No internal connection (can be left floating)
Output	6	O	Output
V+	7	—	Positive (highest) power supply
Offset Trim	8	—	Input offset voltage trim (leave floating if not used)

Pin Functions: OPA2227 and OPA2228

PIN		I/O	DESCRIPTION
NAME	PDIP, SOIC		
Out A	1	O	Output channel A
–In A	2	I	Inverting input channel A
+In A	3	I	Noninverting input channel A
V-	4	—	Negative (lowest) power supply
+In B	5	I	Noninverting input channel B
–In B	6	I	Inverting input channel B
Out B	7	O	Output channel B
V+	8	—	Positive (highest) power supply

Pin Functions: OPA4227 and OPA4228

PIN		I/O	DESCRIPTION
NAME	PDIP, SOIC		
Out A	1	O	Output channel A
-In A	2	I	Inverting input channel A
+In A	3	I	Noninverting input channel A
V+	4	—	Positive (highest) power supply
+In B	5	I	Noninverting input channel B
-In B	6	I	Inverting input channel B
Out B	7	O	Output channel B
Out C	8	O	Output channel C
-In C	9	I	Inverting input channel C
+In C	10	I	Noninverting input channel C
V-	11	—	Negative (lowest) power supply
+In D	12	I	Noninverting input channel D
-In D	13	I	Inverting input channel D
Out D	14	O	Output channel D

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

			MIN	MAX	UNIT
	Supply voltage, Vs = (V+) - (V-)			36	V
	Signal input terminals	Voltage	(V–) – 0.7	(V+) +0.7	V
		Current		20	mA
	Output short-circuit (2)		Continuous		
	Operating temperature		–55	125	°C
	Junction temperature			150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Short-circuit to ground, one amplifier per package

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
Supply voltage, Vs = (V+) - (V-)	±2.5	±15	±18	V
Specified temperature	–40		85	°C

6.4 Thermal Information: OPA227U/UA and OPA228U/UA

THERMAL METRIC (1)		OPA227U/UA OPA228U/UA	OPA2227U/UA OPA2228U/UA	OPA4227UA OPA4228UA	UNIT
		D (SOIC)	D (SOIC)	D (SOIC)	
		8 PINS	8 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	110.1	101.9	65	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	52.2	46.3	23.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	52.3	45.5	20.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	10.4	6.6	1.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	51.5	42.8	19.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Thermal Information: OPA227P/PA and OPA228P/PA

THERMAL METRIC[1]		OPA227P/PA OPA228P/PA			UNIT
		P (PDIP)	D (SOIC)	N (PDIP)	
		8 PINS	8 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	48.9	110.1	65.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	37.7	52.2	20	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	26.1	52.3	25.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	15.1	10.4	1.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	26	51.5	25.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.6 Electrical Characteristics: OPAx227 Series (V_S = ±5 V to ±15 V)

At T_A = 25°C, and R_L = 10 kΩ, unless otherwise noted.

PARAMETER			TEST CONDITIONS	OPA227P, U OPA2227P, U			OPA227PA, UA OPA2227PA, UA OPA4227PA, UA			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
OFFSET VOLTAGE										
V_{OS}	Input Offset Voltage				±5	±75		±10	±200	μV
			T_A = –40°C to 85°C			±100			±200	μV
dV_{OS}/dT	vs Temperature		T_A = –40°C to 85°C		±0.1	±0.6		±0.3	±2	μV/°C
PSRR	vs Power Supply		V_S = ±2.5 V to ±18 V		±0.5	±2		±0.5	±2	μV/V
			T_A = –40°C to 85°C			±2			±2	μV/V
	vs Time				0.2			0.2		μV/mo
	Channel Separation (dual, quad)		DC		0.2			0.2		μV/V
			f = 1 kHz, R_L = 5 kΩ		110			110		dB
INPUT BIAS CURRENT										
I_B	Input Bias Current				±2.5	±10		±2.5	±10	nA
			T_A = –40°C to 85°C			±10			±10	nA
I_{OS}	Input Offset Current				±2.5	±10		±2.5	±10	nA
			T_A = –40°C to 85°C			±10			±10	nA
NOISE										
	Input Voltage Noise, f = 0.1 Hz to 10 Hz				90			90		nVp-p
					15			15		nVrms
e_n	Input Voltage Noise Density	f = 10 Hz			3.5			3.5		nV/√Hz
		f = 100 Hz			3			3		nV/√Hz
		f = 1 kHz			3			3		nV/√Hz
i_n	Current Noise Density	f = 1 kHz			0.4			0.4		pA/√Hz
INPUT VOLTAGE RANGE										
V_{CM}	Common-Mode Voltage Range			(V–)+2		(V+)–2	(V–)+2		(V+)–2	V
CMRR	Common-Mode Rejection		V_{CM} = (V–)+2 V to (V+)–2 V	120	138		120	138		dB
			T_A = –40°C to 85°C	120			120			dB
INPUT IMPEDANCE										
	Differential				10^7 || 12			10^7 || 12		Ω || pF
	Common-Mode		V_{CM} = (V–)+2 V to (V+)–2 V		10^9 || 3			10^9 || 3		Ω || pF
OPEN-LOOP GAIN										
A_{OL}	Open-Loop Voltage Gain		V_O = (V–)+2 V to (V+)–2 V, R_L = 10 kΩ	132	160		132	160		dB
			T_A = –40°C to 85°C	132			132			dB
			V_O = (V–)+3.5V to (V+)–3.5 V, R_L = 600 Ω	132	160		132	160		dB
			T_A = –40°C to 85°C	132			132			dB
FREQUENCY RESPONSE										
GBW	Gain Bandwidth Product				8			8		MHz
SR	Slew Rate				2.3			2.3		V/μs
	Settling Time	0.1%	G = 1, 10 V Step, C_L = 100 pF		5			5		μs
		0.01%	G = 1, 10 V Step, C_L = 100 pF		5.6			5.6		μs
	Overload Recovery Time		V_{IN} × G = V_S		1.3			1.3		μs
THD+N	Total Harmonic Distortion + Noise		f = 1 kHz, G = 1, V_O = 3.5 Vrms		0.00005%			0.00005%		
OUTPUT										
	Voltage Output		R_L = 10 kΩ	(V–)+2		(V+)–2	(V–)+2		(V+)–2	V
			R_L = 10 kΩ T_A = –40°C to 85°C	(V–)+2		(V+)–2	(V–)+2		(V+)–2	V
			R_L = 600 Ω	(V–)+3.5		(V+)–3.5	(V–)+3.5		(V+)–3.5	V
			R_L = 600 Ω T_A = –40°C to 85°C	(V–)+3.5		(V+)–3.5	(V–)+3.5		(V+)–3.5	V
I_{SC}	Short-Circuit Current				±45			±45		mA
C_{LOAD}	Capacitive Load Drive				See *Typical Characteristics*			See *Typical Characteristics*		
Z_O	Open-loop output impedance		f = 1 MHz		27			27		Ω

Electrical Characteristics: OPAx227 Series (V_S = ±5 V to ±15 V) (continued)

At T_A = 25°C, and R_L = 10 kΩ, unless otherwise noted.

PARAMETER		TEST CONDITIONS	OPA227P, U OPA2227P, U			OPA227PA, UA OPA2227PA, UA OPA4227PA, UA			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
POWER SUPPLY									
V_S	Specified Voltage Range		±5		±15	±5		±15	V
	Operating Voltage Range		±2.5		±18	±2.5		±18	V
I_Q	Quiescent Current (per amplifier)	I_O = 0		±3.7	±3.8		±3.7	±3.8	mA
		I_O = 0 T_A = –40°C to 85°C			±4.2			±4.2	mA
TEMPERATURE RANGE									
	Specified Range		–40		85	–40		85	°C
	Operating Range		–55		125	–55		125	°C
	Storage Range		–65		150	–65		150	°C
θ_{JA}	Thermal Resistance								
	SO-8 Surface Mount			150			150		°C/W
	DIP-8			100			100		°C/W
	DIP-14			80			80		°C/W
	SO-14 Surface Mount			100			100		°C/W

6.7 Electrical Characteristics: OPAx228 Series (V_S = ±5 V to ±15 V)

At T_A = 25°C, and R_L = 10 kΩ, unless otherwise noted.

PARAMETER			TEST CONDITIONS	OPA228P, U OPA2228P, U			OPA228PA, UA OPA2228PA, UA OPA4228PA, UA			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
OFFSET VOLTAGE										
V_{OS}	Input Offset Voltage				±5	±75		±10	±200	μV
			T_A = –40°C to 85°C			±100			±200	μV
dV_{OS}/dT	vs Temperature		T_A = –40°C to 85°C		±0.1	±0.6		±0.3	±2	μV/°C
PSRR	vs Power Supply		V_S = ±2.5 V to ±18 V		±0.5	±2		±0.5	±2	μV/V
			T_A = –40°C to 85°C			±2			±2	μV/V
	vs Time				0.2			0.2		μV/mo
	Channel Separation (dual, quad)		DC		0.2			0.2		μV/V
			f = 1kHz, R_L = 5 kΩ		110			110		dB
INPUT BIAS CURRENT										
I_B	Input Bias Current				±2.5	±10		±2.5	±10	nA
			T_A = –40°C to 85°C			±10			±10	nA
I_{OS}	Input Offset Current				±2.5	±10		±2.5	±10	nA
			T_A = –40°C to 85°C			±10			±10	nA
NOISE										
	Input Voltage Noise, f = 0.1 Hz to 10 Hz				90			90		nVp-p
					15			15		nVrms
e_n	Input Voltage Noise Density	f = 10 Hz			3.5			3.5		nV/√Hz
		f = 100 Hz			3			3		nV/√Hz
		f = 1 kHz			3			3		nV/√Hz
i_n	Current Noise Density	f = 1 kHz			0.4			0.4		pA/√Hz
INPUT VOLTAGE RANGE										
V_{CM}	Common-Mode Voltage Range			(V–)+2		(V+)–2	(V–)+2		(V+)–2	V
CMRR	Common-Mode Rejection		V_{CM} = (V–)+2 V to (V+)–2 V	120	138		120	138		dB
			T_A = –40°C to 85°C	120			120			dB
INPUT IMPEDANCE										
	Differential				10^7 || 12			10^7 || 12		Ω || pF
	Common-Mode		V_{CM} = (V–)+2 V to (V+)–2 V		10^9 || 3			10^9 || 3		Ω || pF

Electrical Characteristics: OPAx228 Series (V_S = ±5 V to ±15 V) (continued)

At T_A = 25°C, and R_L = 10 kΩ, unless otherwise noted.

PARAMETER			TEST CONDITIONS	OPA228P, U OPA2228P, U			OPA228PA, UA OPA2228PA, UA OPA4228PA, UA			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
OPEN-LOOP GAIN										
A_{OL}	Open-Loop Voltage Gain		V_O = (V–)+2 V to (V+)–2 V, R_L = 10 kΩ	132	160		132	160		dB
			T_A = –40°C to 85°C	132			132			dB
			V_O = (V–)+3.5 V to (V+)–3.5 V, R_L = 600 Ω	132	160		132	160		dB
			T_A = –40°C to 85°C	132			132			dB
FREQUENCY RESPONSE										
	Minimum Closed-Loop Gain				5			5		V/V
GBW	Gain Bandwidth Product				33			33		MHz
SR	Slew Rate				11			11		V/µs
	Settling Time	0.1%	G = 5, 10 V Step, C_L = 100 pF, C_F = 12 pF		1.5			1.5		µs
		0.01%	G = 5, 10 V Step, C_L = 100 pF, C_F = 12 pF		2			2		µs
	Overload Recovery Time		V_{IN} × G = V_S		0.6			0.6		µs
THD+N	Total Harmonic Distortion + Noise		f = 1 kHz, G = 5, V_O = 3.5 Vrms		0.00005%			0.00005%		
OUTPUT										
	Voltage Output		R_L = 10 kΩ	(V–)+2		(V+)–2	(V–)+2		(V+)–2	V
			R_L = 10 kΩ T_A = –40°C to 85°C	(V–)+2		(V+)–2	(V–)+2		(V+)–2	V
			R_L = 600 Ω	(V–)+3.5		(V+)–3.5	(V–)+3.5		(V+)–3.5	V
			R_L = 600 Ω T_A = –40°C to 85°C	(V–)+3.5		(V+)–3.5	(V–)+3.5		(V+)–3.5	V
I_{SC}	Short-Circuit Current				±45			±45		mA
C_{LOAD}	Capacitive Load Drive				See *Typical Characteristics*			See *Typical Characteristics*		
Z_O	Open-loop output impedance		f = 1 MHz		27			27		Ω
POWER SUPPLY										
V_S	Specified Voltage Range			±5		±15	±5		±15	V
	Operating Voltage Range			±2.5		±18	±2.5		±18	V
I_Q	Quiescent Current (per amplifier)		I_O = 0		±3.7	±3.8		±3.7	±3.8	mA
			I_O = 0 T_A = –40°C to 85°C			±4.2			±4.2	mA
TEMPERATURE RANGE										
	Specified Range			–40		85	–40		85	°C
	Operating Range			–55		125	–55		125	°C
	Storage Range			–65		150	–65		150	°C
$θ_{JA}$	Thermal Resistance									
	SO-8 Surface Mount				150			150		°C/W
	DIP-8				100			100		°C/W
	DIP-14				80			80		°C/W
	SO-14 Surface Mount				100			100		°C/W

6.8 Typical Characteristics

At T_A = 25°C, R_L = 10 kΩ, and V_S = ±15 V, unless otherwise noted.

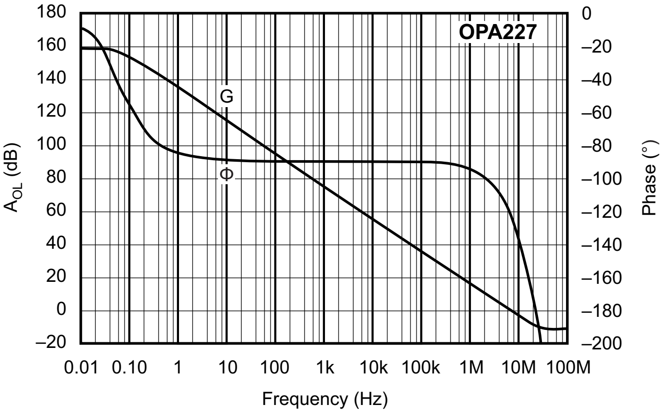


Figure 1. Open-Loop Gain and Phase vs Frequency

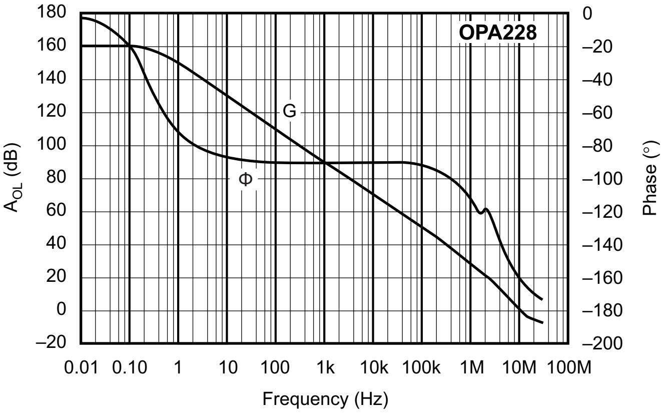


Figure 2. Open-Loop Gain and Phase vs Frequency

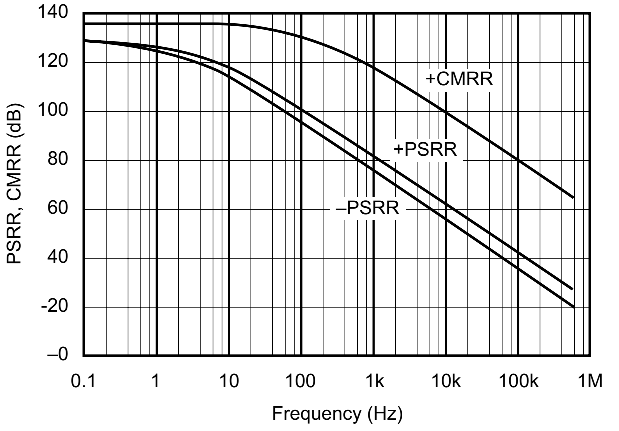


Figure 3. Power Supply and Common-Mode Rejection Ratio vs Frequency

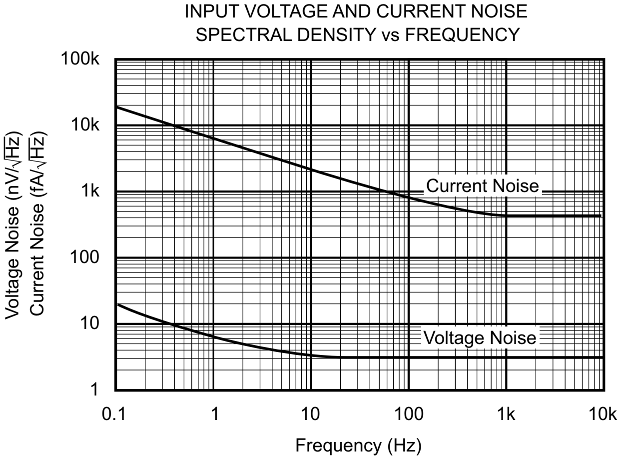


Figure 4. Input Voltage and Current Noise Spectral Density vs Frequency

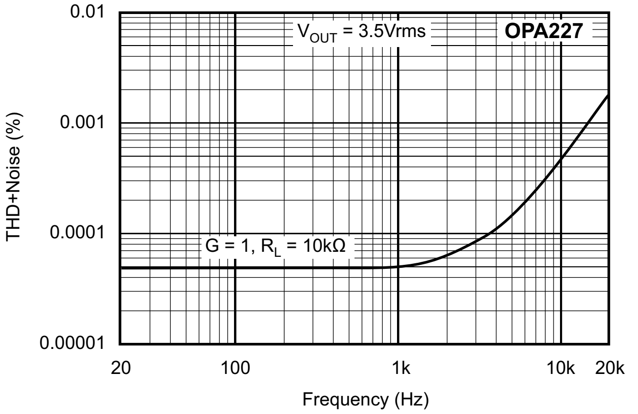


Figure 5. Total Harmonic Distortion + Noise vs Frequency

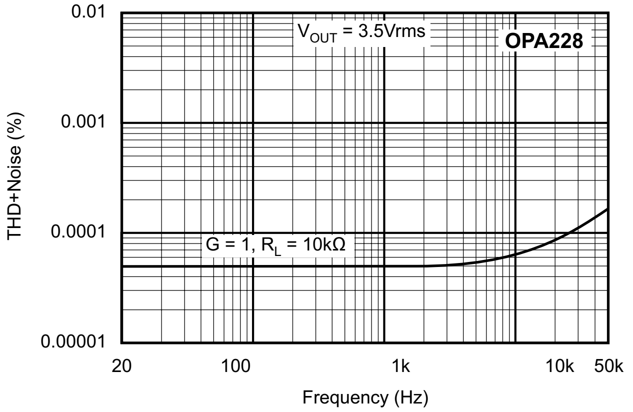


Figure 6. Total Harmonic Distortion + Noise vs Frequency

Typical Characteristics (continued)

At T_A = 25°C, R_L = 10 kΩ, and V_S = ±15 V, unless otherwise noted.

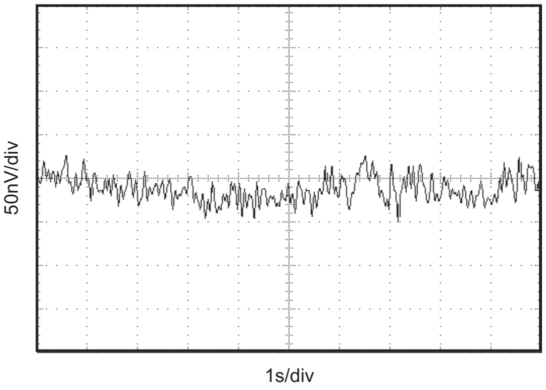


Figure 7. Input Noise Voltage vs Time

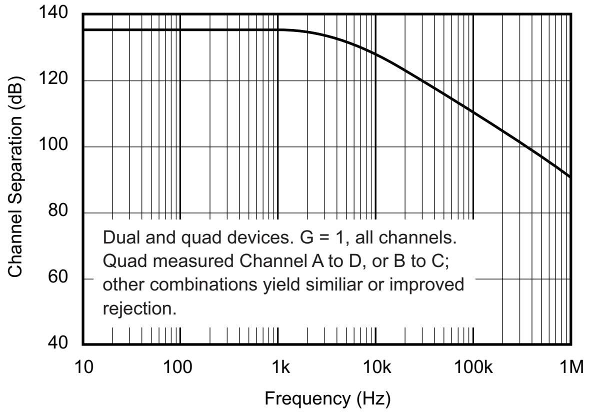


Figure 8. Channel Separation vs Frequency

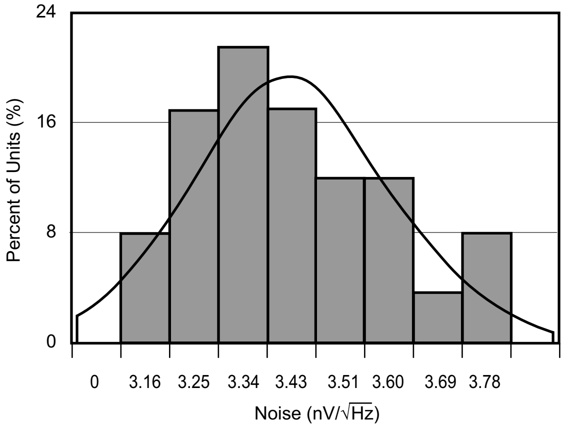


Figure 9. Voltage Noise Distribution (10 Hz)

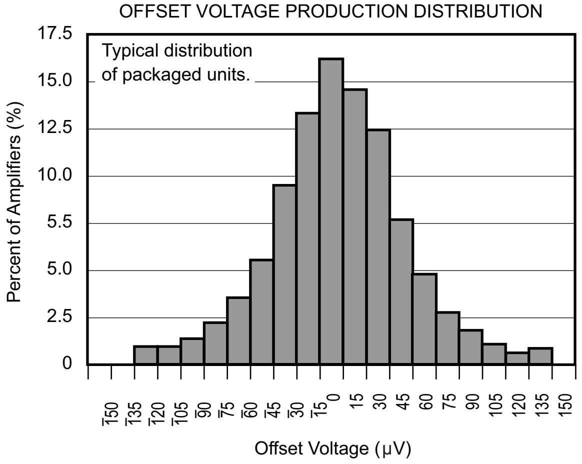


Figure 10. Offset Voltage Production Distribution

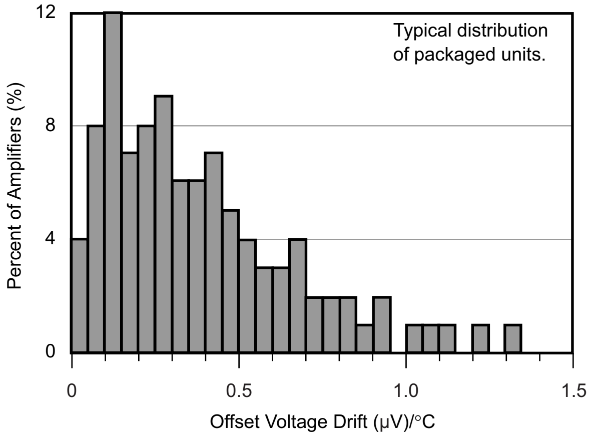


Figure 11. Offset Voltage Drift Production Distribution

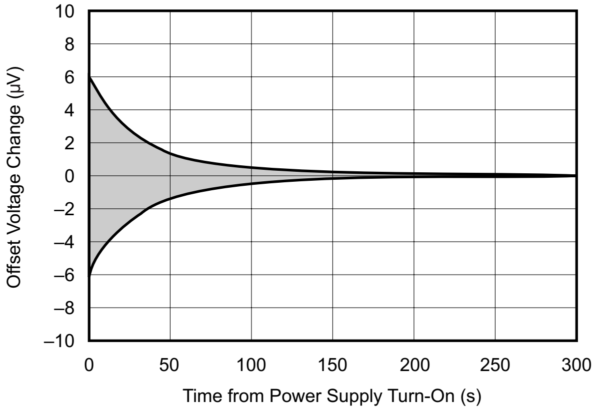


Figure 12. Warm-Up Offset Voltage Drift

Typical Characteristics (continued)

At T_A = 25°C, R_L = 10 kΩ, and V_S = ±15 V, unless otherwise noted.

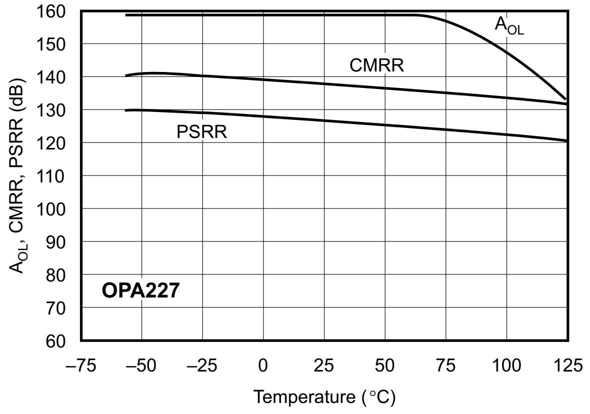


Figure 13. A_{OL}, CMRR, PSRR vs Temperature

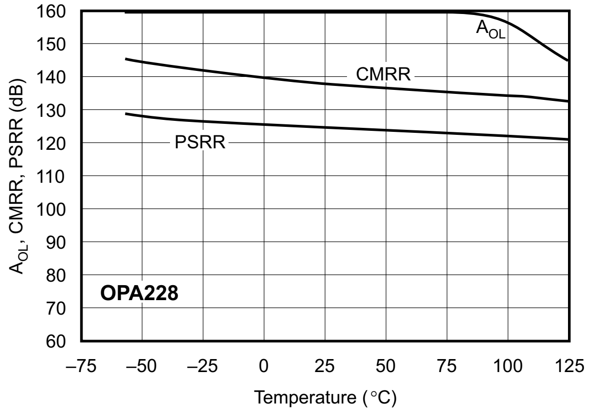


Figure 14. A_{OL}, CMRR, PSRR vs Temperature

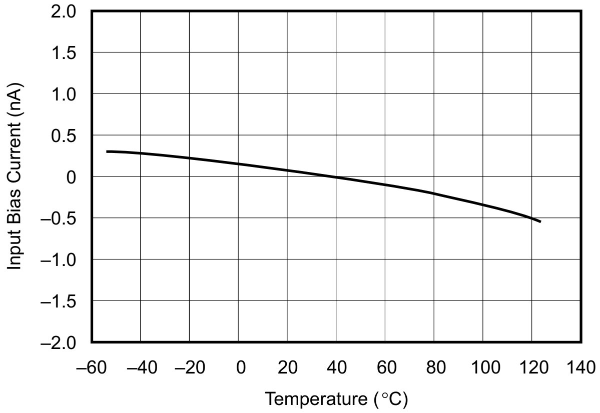


Figure 15. Input Bias Current vs Temperature

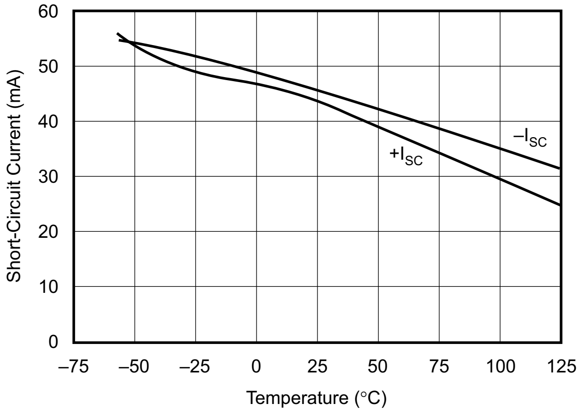


Figure 16. Short-Circuit Current vs Temperature

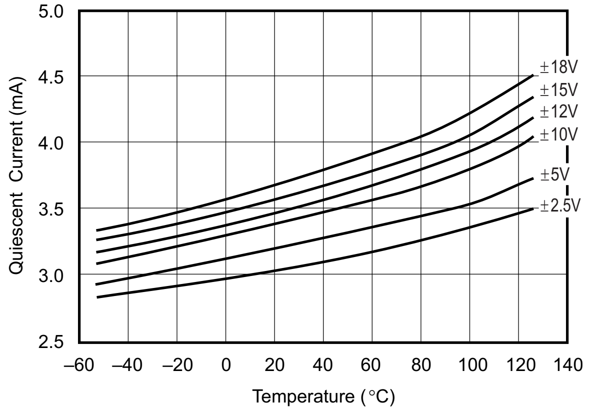


Figure 17. Quiescent Current vs Temperature

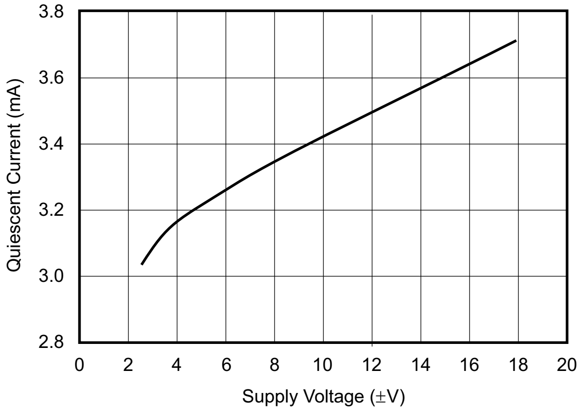


Figure 18. Quiescent Current vs Supply Voltage

Typical Characteristics (continued)

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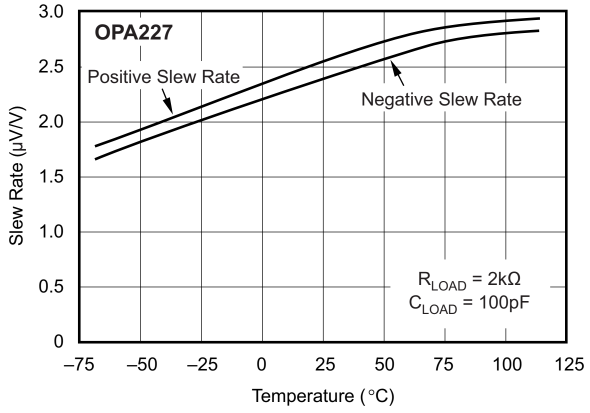


Figure 19. Slew Rate vs Temperature

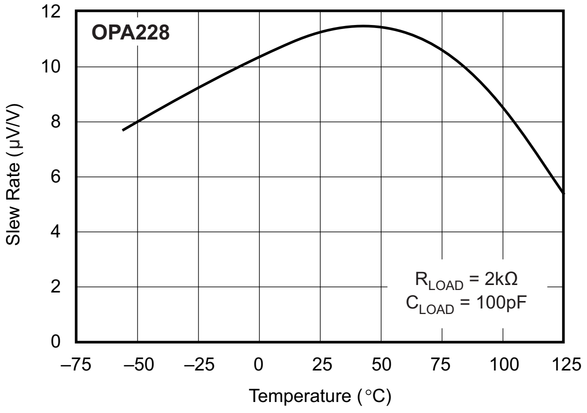


Figure 20. Slew Rate vs Temperature

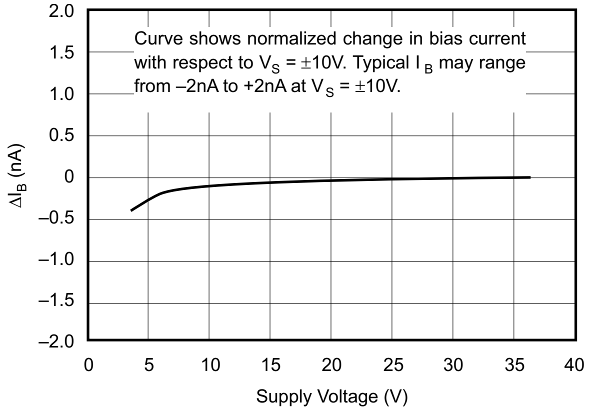


Figure 21. Change in Input Bias Current vs Power Supply Voltage

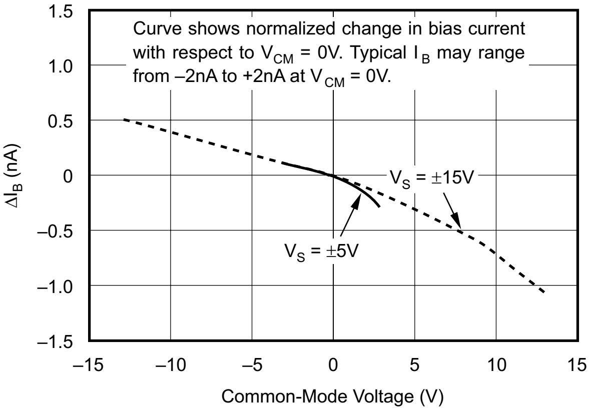


Figure 22. Change in Input Bias Current vs Common-Mode Voltage

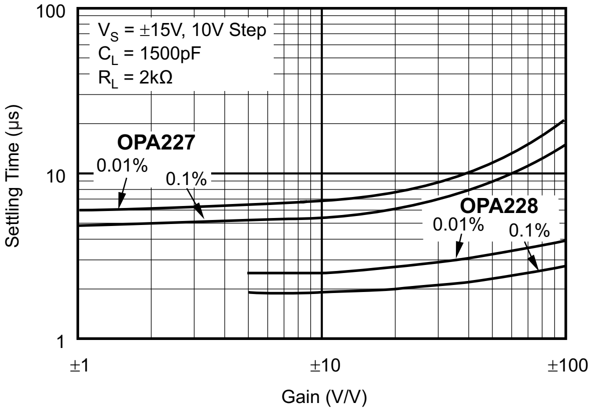


Figure 23. Settling Time vs Closed-Loop Gain

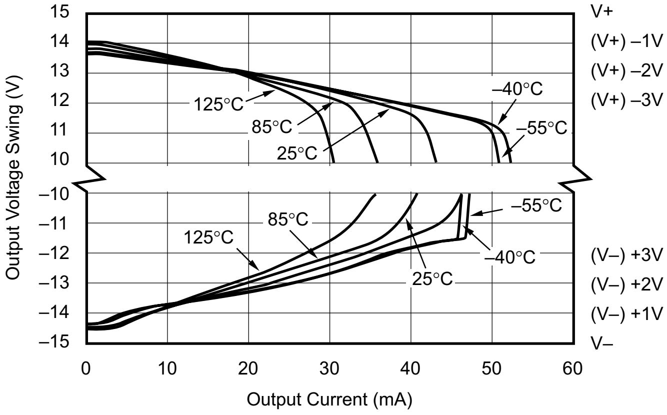


Figure 24. Output Voltage Swing vs Output Current

Typical Characteristics (continued)

At T_A = 25°C, R_L = 10 kΩ, and V_S = ±15 V, unless otherwise noted.

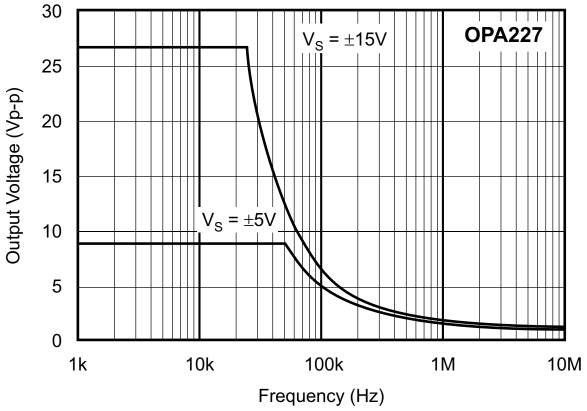


Figure 25. Maximum Output Voltage vs Frequency

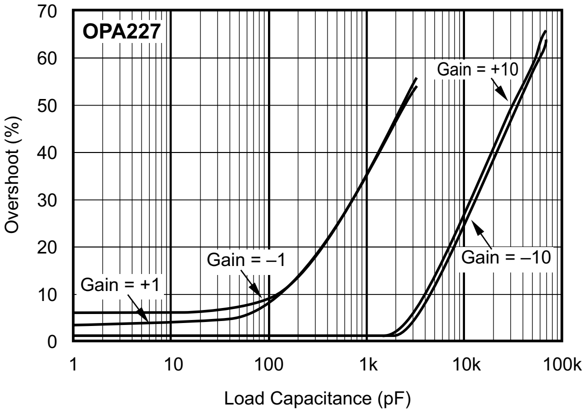
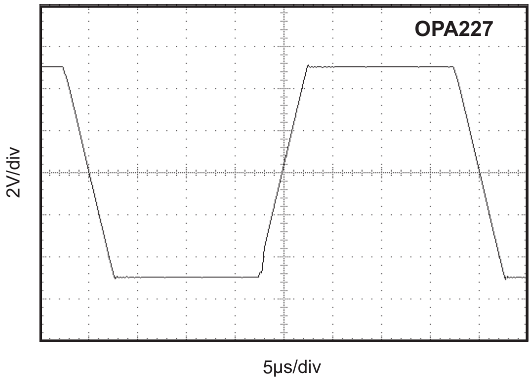
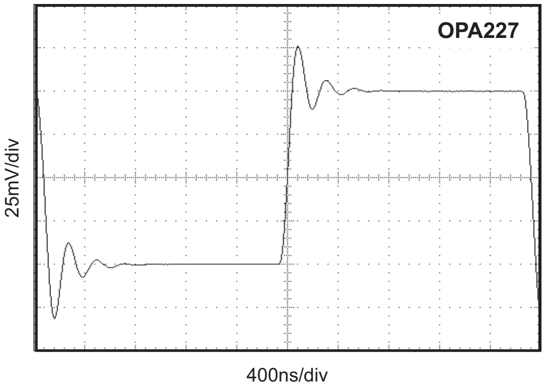


Figure 26. Small-Signal Overshoot vs Load Capacitance



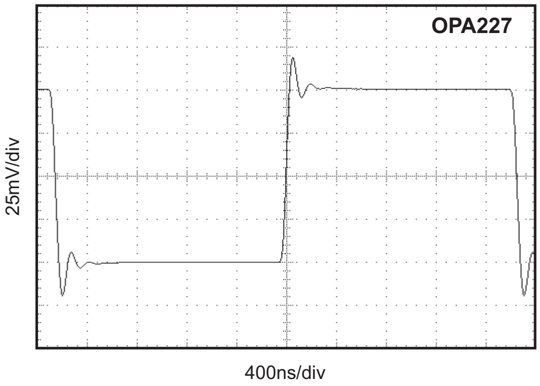
G = –1, C_L = 1500 pF

Figure 27. Large-Signal Step Response



G = 1, C = 1000 pF

Figure 28. Small-Signal Step Response



G = 1, C_L = 5 pF

Figure 29. Small-Signal Step Response

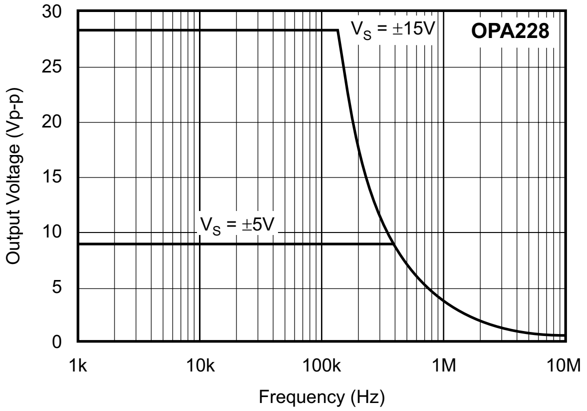


Figure 30. Maximum Output Voltage vs Frequency

Typical Characteristics (continued)

At T_A = 25°C, R_L = 10 kΩ, and V_S = ±15 V, unless otherwise noted.

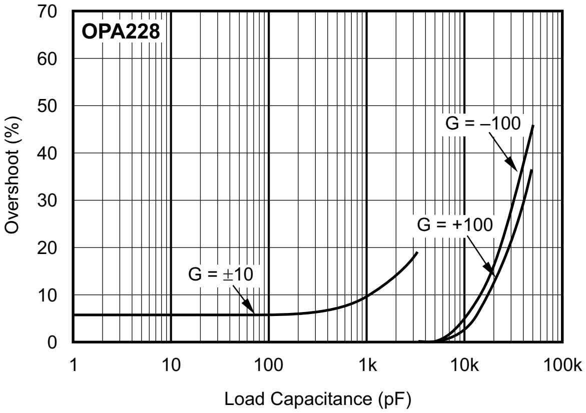
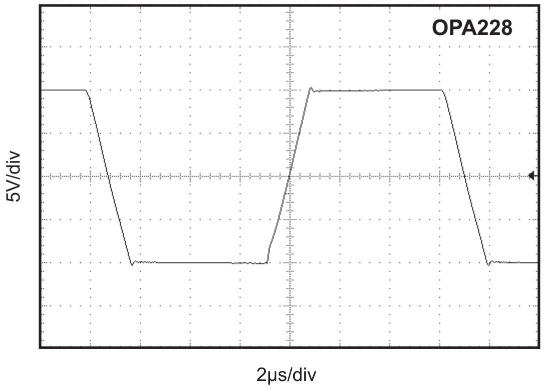
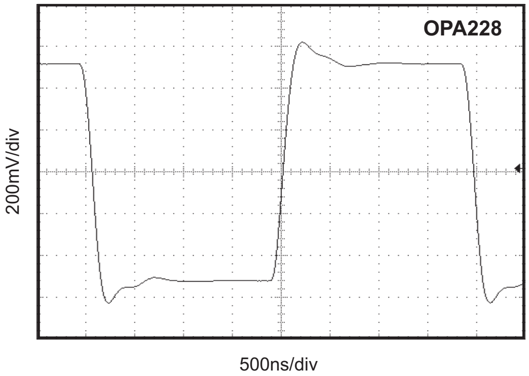


Figure 31. Small-Signal Overshoot vs Load Capacitance



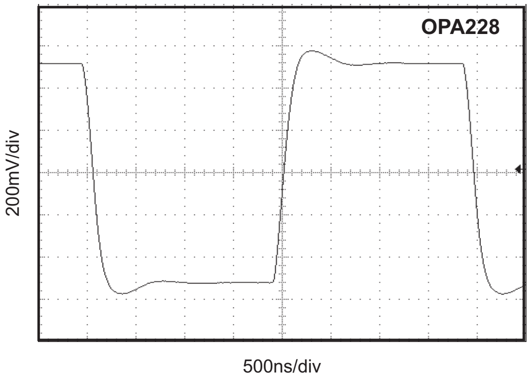
G = –10, C_L = 100 pF

Figure 32. Large-Signal Step Response



G = 10, C_L = 1000 pF R_L = 1.8 kΩ

Figure 33. Small-Signal Step Response



G = 10, C_L = 1000 pF R_L = 1.8 kΩ

Figure 34. Small-Signal Step Response

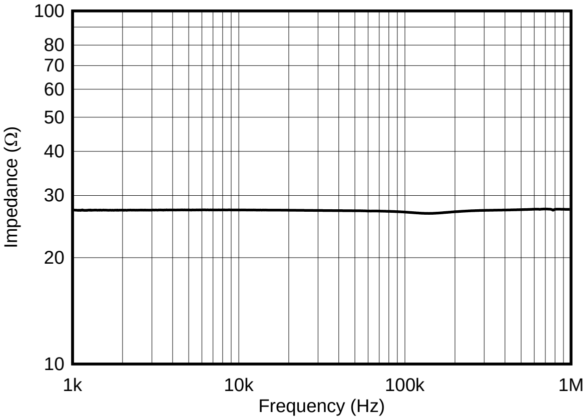


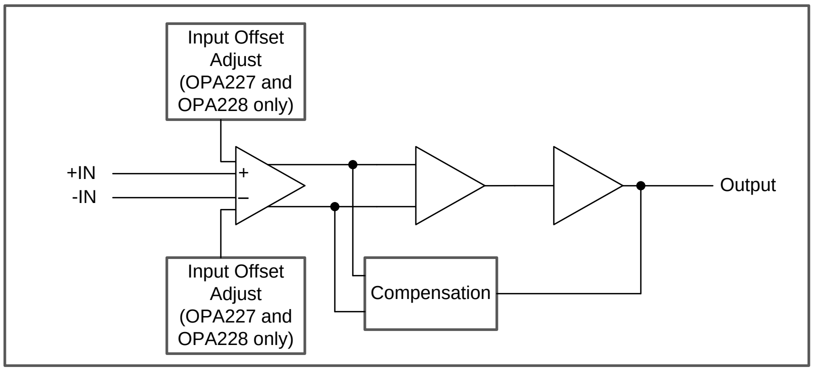
Figure 35. Open-loop Output Impedance

7 Detailed Description

7.1 Overview

The OPAx22x series operational amplifiers combine low noise and wide bandwidth with high precision to make them the ideal choice for applications requiring both AC and precision DC performance. The OPAx227 is unity-gain stable and features high slew rate (2.3 V/µs) and wide bandwidth (8 MHz). The OPAx228 is optimized for closed-loop gains of 5 or greater, and offers higher speed with a slew rate of 10 V/µs and a bandwidth of 33 MHz.

7.2 Functional Block Diagram



7.3 Feature Description

The OPAx22x series are unity-gain stable and free from unexpected output phase reversal, making it easy to use in a wide range of applications. Applications with noisy or high-impedance power supplies may require decoupling capacitors close to the device pins. In most cases 0.1-µF capacitors are adequate.

7.3.1 Offset Voltage and Drift

The OPAx22x series have very low offset voltage and drift. To achieve highest DC precision, circuit layout and mechanical conditions should be optimized. Connections of dissimilar metals can generate thermal potentials at the operational amplifier inputs, which can degrade the offset voltage and drift. These thermocouple effects can exceed the inherent drift of the amplifier and ultimately degrade its performance. The thermal potentials can be made to cancel by assuring that they are equal at both input terminals. In addition:

- Keep thermal mass of the connections made to the two input terminals similar.
- Locate heat sources as far as possible from the critical input circuitry.
- Shield operational amplifier and input circuitry from air currents such as those created by cooling fans.

7.3.2 Operating Voltage

The OPAx22x series of operational amplifiers operate from ±2.5 V to ±18 V supplies with excellent performance. Unlike most operational amplifiers that are specified at only one supply voltage, the OPA227 series is specified for real-world applications; a single set of specifications applies over the ±5-V to ±15-V supply range. Specifications are assured for applications from ±5-V to ±15-V power supplies. Some applications do not require equal positive and negative output voltage swing. Power supply voltages do not need to be equal. The OPAx22x series can operate with as little as 5 V between the supplies and with up to 36 V between the supplies. For example, the positive supply could be set to 25 V with the negative supply at –5 V or vice-versa. In addition, key parameters are assured over the specified temperature range, –40°C to 85°C. Parameters which vary significantly with operating voltage or temperature are shown in the *Typical Characteristics*.

Feature Description (continued)

7.3.3 Offset Voltage Adjustment

The OPAx22x series are laser-trimmed for very low offset and drift so most applications will not require external adjustment. However, the OPA227 and OPA228 (single versions) provide offset voltage trim connections on pins 1 and 8. Offset voltage can be adjusted by connecting a potentiometer as shown in Figure 36. This adjustment should be used only to null the offset of the operational amplifier. This adjustment should not be used to compensate for offsets created elsewhere in the system because this can introduce additional temperature drift.

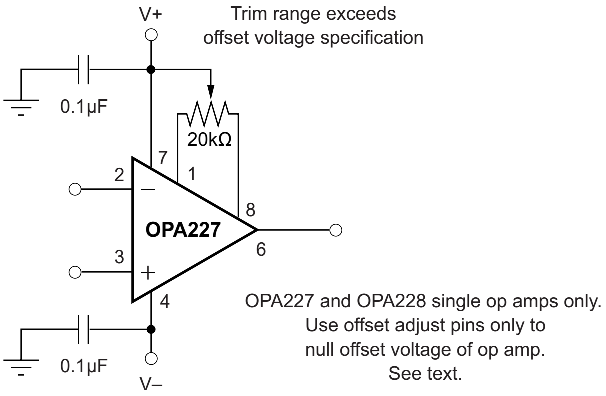


Figure 36. OPA227 Offset Voltage Trim Circuit

7.3.4 Input Protection

Back-to-back diodes (see Figure 37) are used for input protection on the OPAx22x. Exceeding the turnon threshold of these diodes, as in a pulse condition, can cause current to flow through the input protection diodes due to the amplifier's finite slew rate. Without external current limiting resistors, the input devices can be destroyed. Sources of high-input current can cause subtle damage to the amplifier. Although the unit may still be functional, important parameters such as input offset voltage, drift, and noise may shift.

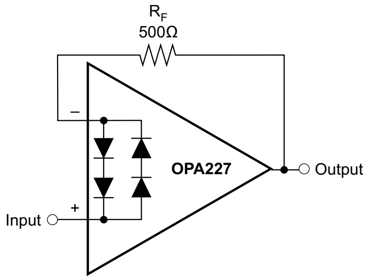


Figure 37. Pulsed Operation

When using the OPA227 as a unity-gain buffer (follower), the input current should be limited to 20 mA. This can be accomplished by inserting a feedback resistor or a resistor in series with the source. Use Equation 1 to calculate sufficient resistor size.

$$R_X = V_S/20mA - R_{SOURCE}$$

where

- R_X is either in series with the source or inserted in the feedback path. (1)

For example, for a 10-V pulse (V_S = 10 V), total loop resistance must be 500 Ω. If the source impedance is large enough to sufficiently limit the current on its own, no additional resistors are needed. The size of any external resistors must be carefully chosen because they will increase noise. See the *Noise Performance* section of this data sheet for further information on noise calculation. Figure 37 shows an example implementing a current limiting feedback resistor.

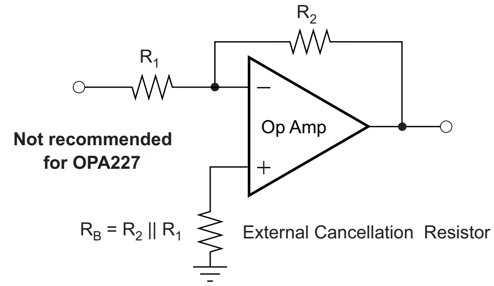
Feature Description (continued)

7.3.5 Input Bias Current Cancellation

The input bias current of the OPAx22x series is internally compensated with an equal and opposite cancellation current. The resulting input bias current is the difference between with input bias current and the cancellation current. The residual input bias current can be positive or negative.

When the bias current is cancelled in this manner, the input bias current and input offset current are approximately equal. A resistor added to cancel the effect of the input bias current (as shown in Figure 38) may actually increase offset and noise and is therefore not recommended.

Conventional Op Amp Configuration



Recommended OPA227 Configuration

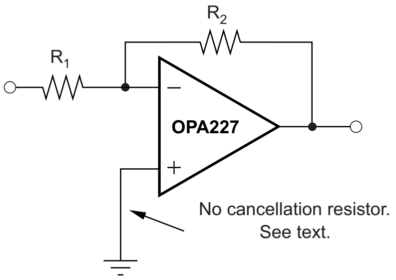


Figure 38. Input Bias Current Cancellation

7.3.6 Noise Performance

Figure 39 shows total circuit noise for varying source impedances with the operational amplifier in a unity-gain configuration (no feedback resistor network, therefore no additional noise contributions). Two different operational amplifiers are shown with total circuit noise calculated. The OPA227 has very low voltage noise, making it ideal for low source impedances (less than 20 kΩ). A similar precision operational amplifier, the OPA277, has somewhat higher voltage noise but lower current noise. It provides excellent noise performance at moderate source impedance (10 kΩ to 100 kΩ). Above 100 kΩ, a FET-input operational amplifier such as the OPA132 (very low current noise) may provide improved performance. Use the equation in Figure 39 for calculating the total circuit noise. e_n = voltage noise, i_n = current noise, R_S = source impedance, k = Boltzmann's constant = 1.38×10^{-23} J/K and T is temperature in K. For more details on calculating noise, see *Basic Noise Calculations*.

Feature Description (continued)

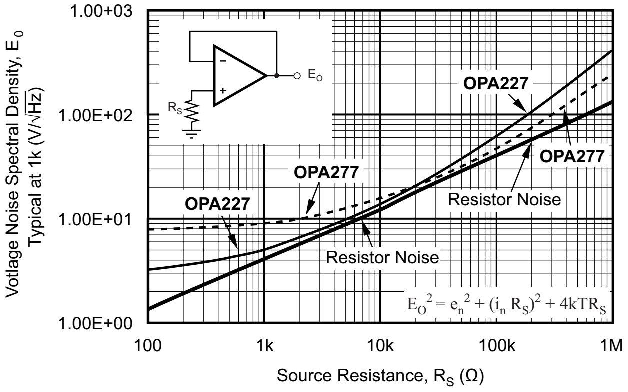


Figure 39. Noise Performance of the OPA227 in Unity-Gain Buffer Configuration

7.3.7 Basic Noise Calculations

Design of low noise operational amplifier circuits requires careful consideration of a variety of possible noise contributors: noise from the signal source, noise generated in the operational amplifier, and noise from the feedback network resistors. The total noise of the circuit is the root-sum-square combination of all noise components.

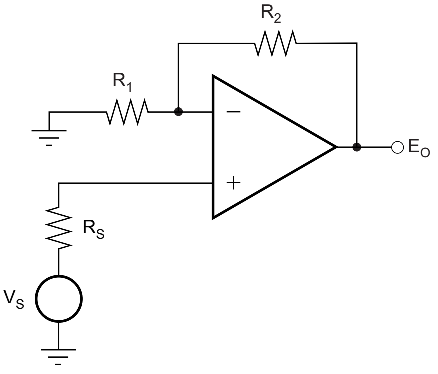
The resistive portion of the source impedance produces thermal noise proportional to the square root of the resistance. This function is shown plotted in Figure 39. Because the source impedance is usually fixed, select the operational amplifier and the feedback resistors to minimize their contribution to the total noise.

Figure 39 shows total noise for varying source impedances with the operational amplifier in a unity-gain configuration (no feedback resistor network and therefore no additional noise contributions). The operational amplifier itself contributes both a voltage noise component and a current noise component. The voltage noise is commonly modeled as a time-varying component of the offset voltage. The current noise is modeled as the time-varying component of the input bias current and reacts with the source resistance to create a voltage component of noise. Consequently, the lowest noise operational amplifier for a given application depends on the source impedance. For low source impedance, current noise is negligible and voltage noise generally dominates. For high source impedance, current noise may dominate.

Figure 40 shows both inverting and noninverting operational amplifier circuit configurations with gain. In circuit configurations with gain, the feedback network resistors also contribute noise. The current noise of the operational amplifier reacts with the feedback resistors to create additional noise components. The feedback resistor values can generally be chosen to make these noise sources negligible. The equations for total noise are shown in the following images for both configurations.

Feature Description (continued)

Noise in Noninverting Gain Configuration



Noise at the output:

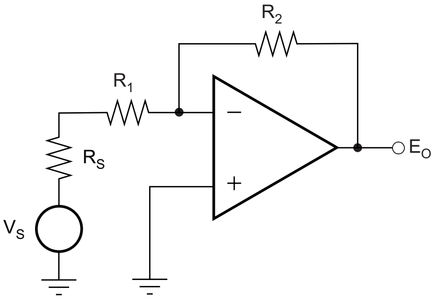
$$E_O^2 = \left(1+\frac{R_2}{R_1}\right)^2 e_n^2 + e_1^2 + e_2^2 + (i_n R_2)^2 + e_S^2 + (i_n R_S)^2\left(1+\frac{R_2}{R_1}\right)^2$$

Where $e_S = \sqrt{4kTR_S} \cdot \left(1+\frac{R_2}{R_1}\right)$ = thermal noise of R_S

$e_1 = \sqrt{4kTR_1} \cdot \left(\frac{R_2}{R_1}\right)$ = thermal noise of R_1

$e_2 = \sqrt{4kTR_2}$ = thermal noise of R_2

Noise in Inverting Gain Configuration



Noise at the output:

$$E_O^2 = \left(1+\frac{R_2}{R_1+R_S}\right)^2 e_n^2 + e_1^2 + e_2^2 + (i_n R_2)^2 + e_S^2$$

Where $e_S = \sqrt{4kTR_S} \cdot \left(\frac{R_2}{R_1+R_S}\right)$ = thermal noise of R_S

$e_1 = \sqrt{4kTR_1} \cdot \left(\frac{R_2}{R_1+R_S}\right)$ = thermal noise of R_1

$e_2 = \sqrt{4kTR_2}$ = thermal noise of R_2

For the OPA227 and OPA228 series op amps at 1kHz, $e_n = 3nV/\sqrt{Hz}$ and $i_n = 0.4pA/\sqrt{Hz}$.

Figure 40. Noise Calculation in Gain Configurations

Feature Description (continued)

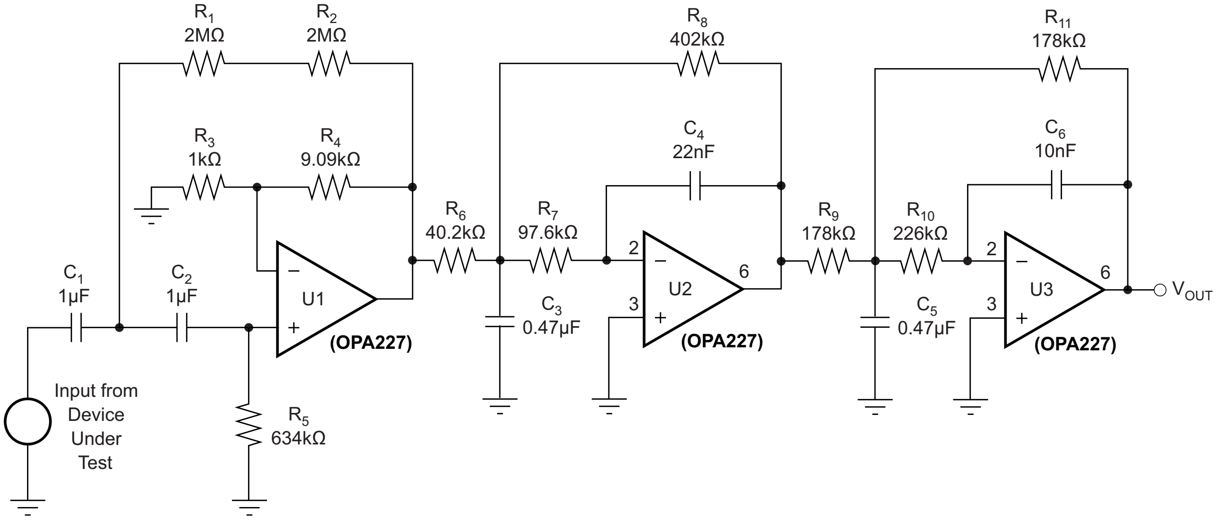


Figure 41. 0.1 Hz to 10 Hz Bandpass Filter Used to Test Wideband Noise of the OPAx22x Series

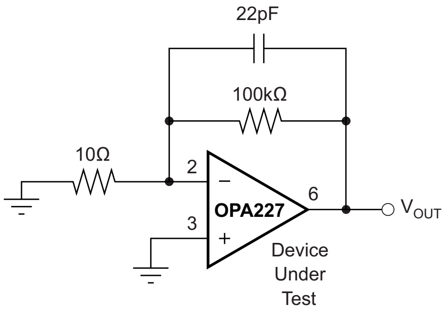


Figure 42. Noise Test Circuit

Figure 41 shows the 0.1 Hz 10 Hz bandpass filter used to test the noise of the OPA227 and OPA228. The filter circuit was designed using Texas Instruments' FilterPro software (available at www.ti.com). Figure 42 shows the configuration of the OPA227 and OPA228 for noise testing.

7.3.8 EMI Rejection Ratio (EMIRR)

The electromagnetic interference (EMI) rejection ratio, or EMIRR, describes the EMI immunity of operational amplifiers. An adverse effect that is common to many operational amplifiers is a change in the offset voltage as a result of RF signal rectification. An operational amplifier that is more efficient at rejecting this change in offset as a result of EMI has a higher EMIRR and is quantified by a decibel value. Measuring EMIRR can be performed in many ways, but this section provides the EMIRR IN+, which specifically describes the EMIRR performance when the RF signal is applied to the noninverting input pin of the operational amplifier. In general, only the noninverting input is tested for EMIRR for the following three reasons:

1. Operational amplifier input pins are known to be the most sensitive to EMI, and typically rectify RF signals better than the supply or output pins.
2. The noninverting and inverting operational amplifier inputs have symmetrical physical layouts and exhibit nearly matching EMIRR performance.
3. EMIRR is easier to measure on noninverting pins than on other pins because the noninverting input terminal can be isolated on a printed-circuit-board (PCB). This isolation allows the RF signal to be applied directly to the noninverting input terminal with no complex interactions from other components or connecting PCB traces.

Feature Description (continued)

A more formal discussion of the EMIRR IN+ definition and test method is provided in application report SBOA128, EMI Rejection Ratio of Operational Amplifiers, available for download at www.ti.com. The EMIRR IN+ of the OPA227 is plotted versus frequency as shown in Figure 43.

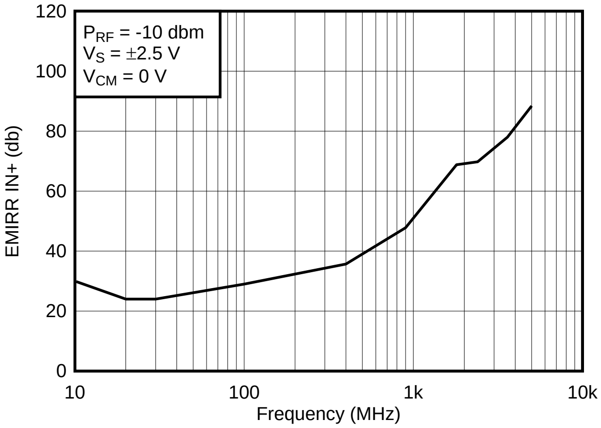


Figure 43. OPA227 EMIRR IN+ vs Frequency

If available, any dual and quad operational amplifier device versions have nearly similar EMIRR IN+ performance. The OPAx227 unity-gain bandwidth is 8 MHz. EMIRR performance below this frequency denotes interfering signals that fall within the operational amplifier bandwidth.

Table 1 shows the EMIRR IN+ values for the OPA227 at particular frequencies commonly encountered in real-world applications. Applications listed in Table 1 may be centered on or operated near the particular frequency shown. This information may be of special interest to designers working with these types of applications, or working in other fields likely to encounter RF interference from broad sources, such as the industrial, scientific, and medical (ISM) radio band.

Table 1. OPAx227 EMIRR IN+ for Frequencies of Interest

FREQUENCY	APPLICATION/ALLOCATION	EMIRR IN+
400 MHz	Mobile radio, mobile satellite/space operation, weather, radar, UHF	35.7 dB
900 MHz	GSM, radio com/nav./GPS (to 1.6 GHz), ISM, aeronautical mobile, UHF	47.8 dB
1.8 GHz	GSM, mobile personal comm. broadband, satellite, L-band	68.8 dB
2.4 GHz	802.11b/g/n, Bluetooth™, mobile personal comm., ISM, amateur radio/satellite, S-band	69.8 dB
3.6 GHz	Radiolocation, aero comm./nav., satellite, mobile, S-band	78 dB
5 GHz	802.11a/n, aero comm./nav., mobile comm., space/satellite operation, C-band	88.4 dB

7.3.8.1 EMIRR IN+ Test Configuration

Figure 44 shows the circuit configuration for testing the EMIRR IN+. An RF source is connected to the operational amplifier noninverting input terminal using a transmission line. The operational amplifier is configured in a unity gain buffer topology with the output connected to a low-pass filter (LPF) and a digital multimeter (DMM). A large impedance mismatch at the operational amplifier input causes a voltage reflection; however, this effect is characterized and accounted for when determining the EMIRR IN+. The resulting DC offset voltage is sampled and measured by the multimeter. The LPF isolates the multimeter from residual RF signals that may interfere with multimeter accuracy. Refer to SBOA128 for more details.

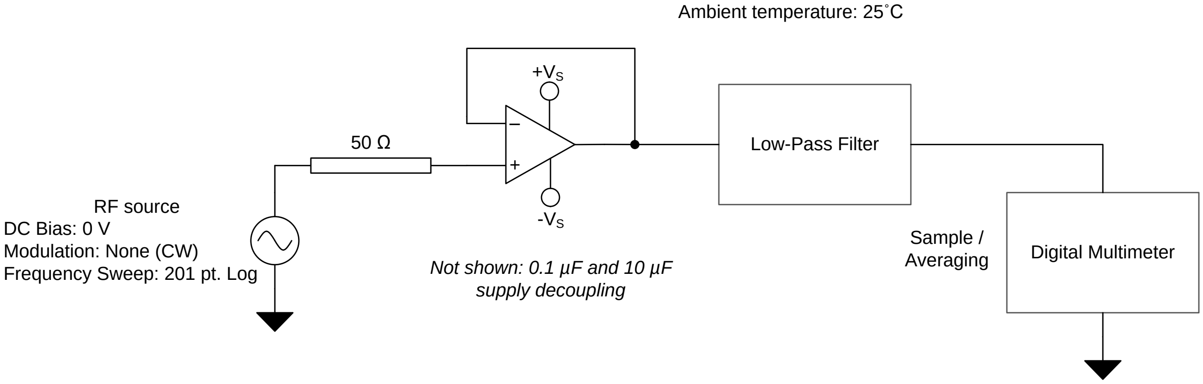


Figure 44. EMIRR IN+ Test Configuration Schematic

7.4 Device Functional Modes

The OPAx22x has a single functional mode and are operational when the power-supply voltage is greater than 5 V (±2.5 V). The maximum power supply voltage for the OPAx22x is 36 V (±18 V).

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The OPAx22x series are precision operational amplifiers with very low noise. The OPAx227 series is unity-gain stable with a slew rate of 2.3 V/μs and 8 MHz bandwidth. The OPAx228 series is optimized for higher-speed applications with gains of 5 or greater, featuring a slew rate of 10 V/μs and 33-MHz bandwidth. Applications with noisy or high impedance power supplies may require decoupling capacitors close to the device pins. In most cases, 0.1-μF capacitors are adequate.

8.1.1 Three-Pole, 20 kHz Low Pass, 0.5-dB Chebyshev Filter

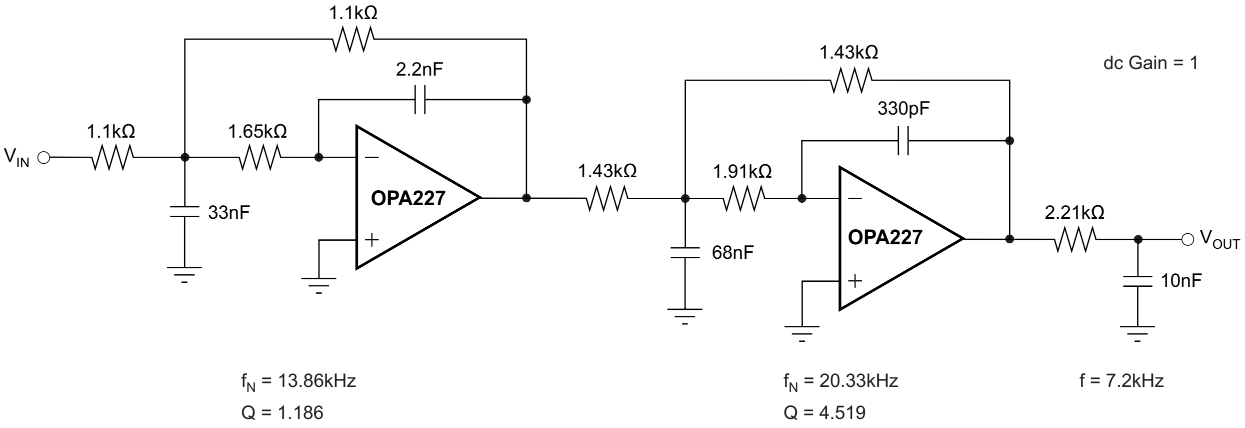
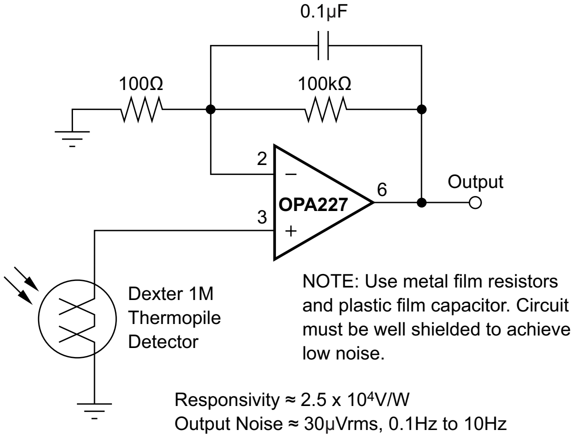


Figure 45. Three-Pole, 20 kHz Low Pass, 0.5-dB Chebyshev Filter

8.1.2 Long-Wavelength Infrared Detector Amplifier



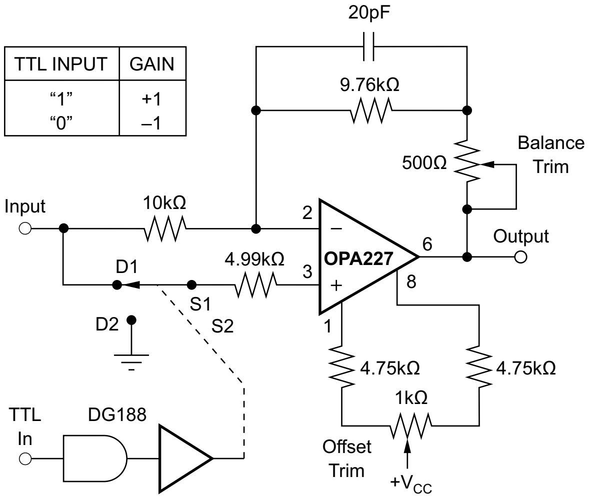
NOTE: Use metal film resistors and plastic film capacitor. Circuit must be well shielded to achieve low noise.

Responsivity ≈ 2.5×10^4V/W
Output Noise ≈ 30μVrms, 0.1Hz to 10Hz

Figure 46. Long-Wavelength Infrared Detector Amplifier

Application Information (continued)

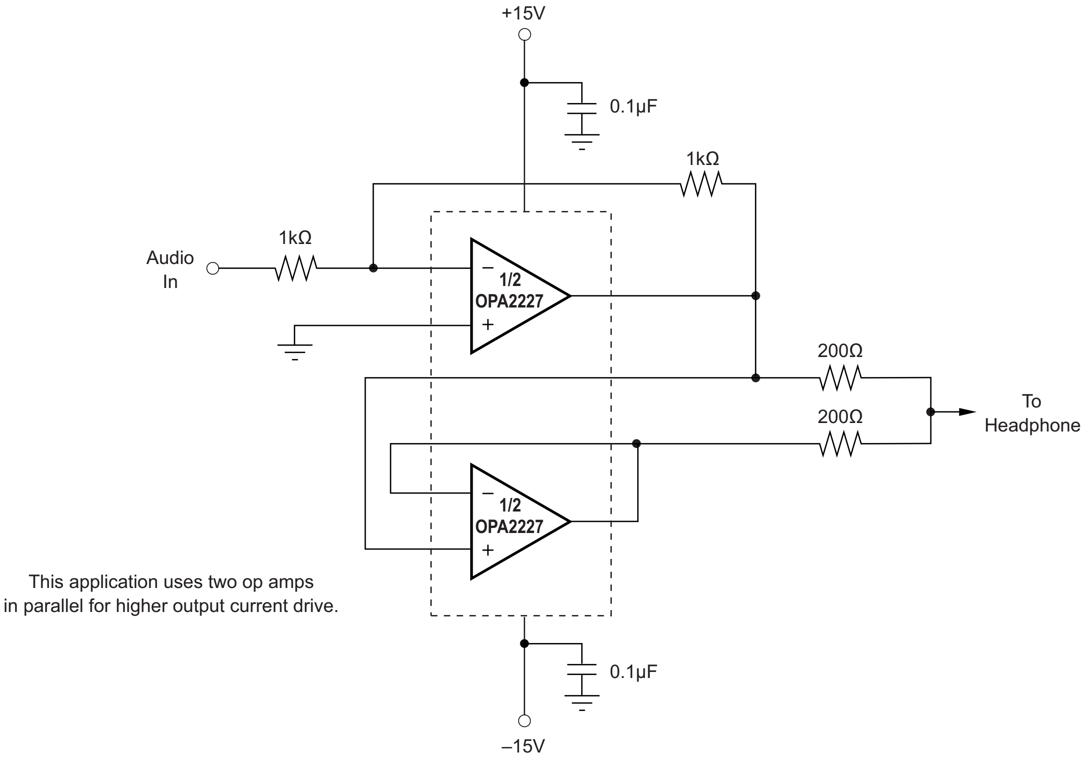
8.1.3 High Performance Synchronous Demodulator



TTL INPUT	GAIN
"1"	+1
"0"	–1

Figure 47. High Performance Synchronous Demodulator

8.1.4 Headphone Amplifier



This application uses two op amps
in parallel for higher output current drive.

Figure 48. Headphone Amplifier

Application Information (continued)

8.1.5 Three-Band Active Tone Control (Bass, Midrange, and Treble)

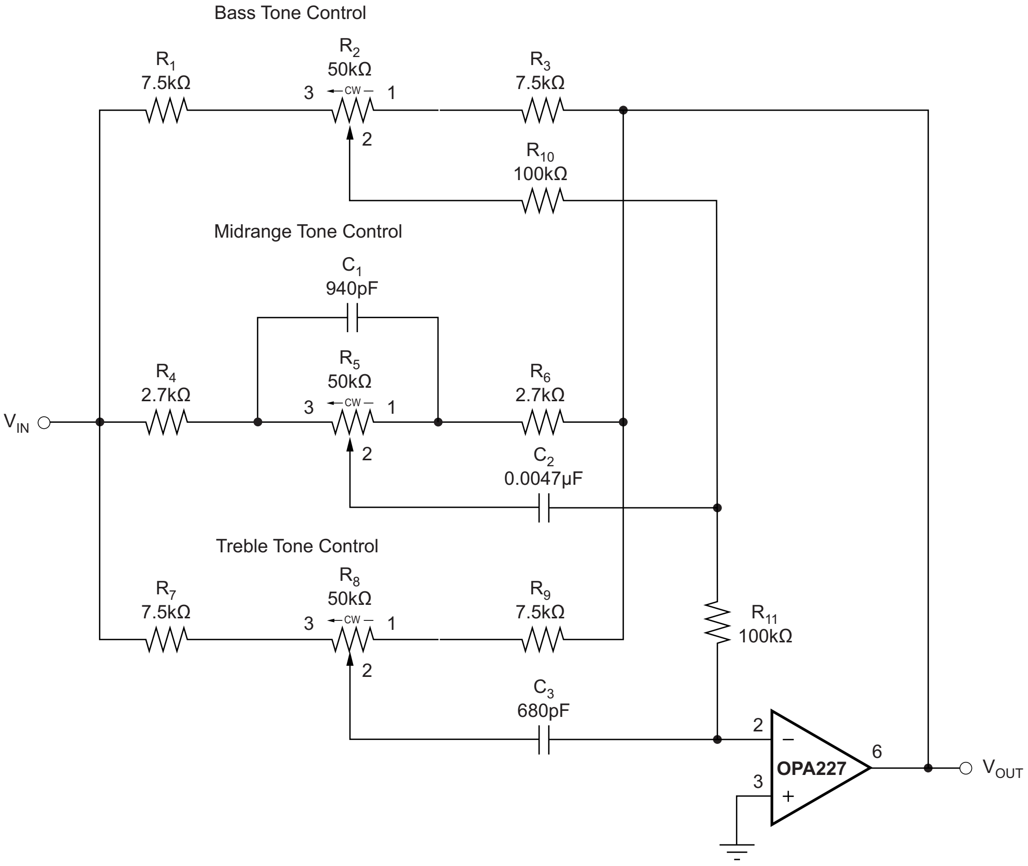


Figure 49. Three-Band Active Tone Control (Bass, Midrange, and Treble)

8.2 Typical Application

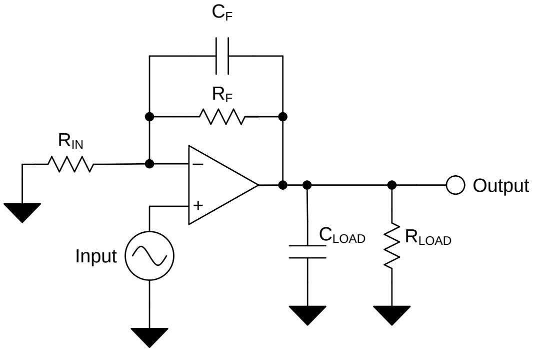


Figure 50. Typical Application Schematic

8.2.1 Design Requirements

1. Operate OPAx228 gain is less than 5 V/V
2. Stable operation with capacitive load

Typical Application (continued)

8.2.2 Detailed Design Procedure

8.2.2.1 Using the OPAx228 in Low Gains

The OPAx228 family is intended for applications with signal gains of 5 or greater, but it is possible to take advantage of their high-speed in lower gains. Without external compensation, the OPA228 has sufficient phase margin to maintain stability in unity gain with purely resistive loads. However, the addition of load capacitance can reduce the phase margin and destabilize the operational amplifier.

A variety of compensation techniques have been evaluated specifically for use with the OPA228. The recommended configuration consists of an additional capacitor (C_F) in parallel with the feedback resistance, as shown in Figure 51 and Figure 52. This feedback capacitor serves two purposes in compensating the circuit. The operational amplifier's input capacitance and the feedback resistors interact to cause phase shift that can result in instability. C_F compensates the input capacitance, minimizing peaking. Additionally, at high frequencies, the closed-loop gain of the amplifier is strongly influenced by the ratio of the input capacitance and the feedback capacitor. Thus, C_F can be selected to yield good stability while maintaining high-speed.

Without external compensation, the noise specification of the OPA228 is the same as that for the OPA227 in gains of 5 or greater. With the additional external compensation, the output noise of the of the OPA228 will be higher. The amount of noise increase is directly related to the increase in high-frequency closed-loop gain established by the C_{IN}/C_F ratio.

Figure 51 and Figure 52 show the recommended circuit for gains of 2 and –2, respectively. The figures suggest approximate values for C_F. Because compensation is highly dependent on circuit design, board layout, and load conditions, C_F should be optimized experimentally for best results. Figure 53 and Figure 55 show the large- and small-signal step responses for the G = 2 configuration with 100-pF load capacitance.Figure 54 and Figure 56 show the large- and small-signal step responses for the G = –2 configuration with 100-pF load capacitance.

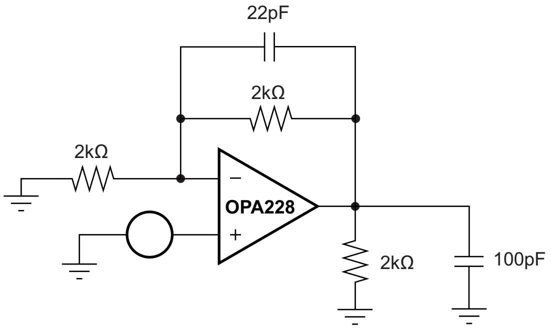


Figure 51. Compensation of the OPA228 for G = 2

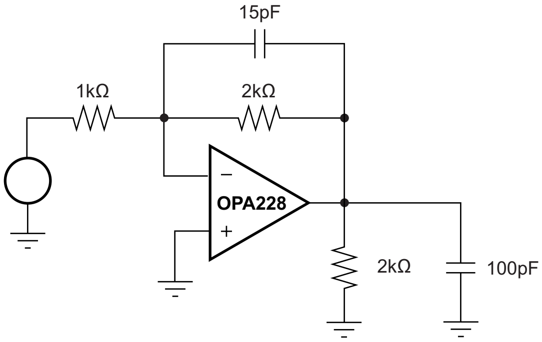


Figure 52. Compensation for OPA228 for G = –2

8.2.3 Application Curves

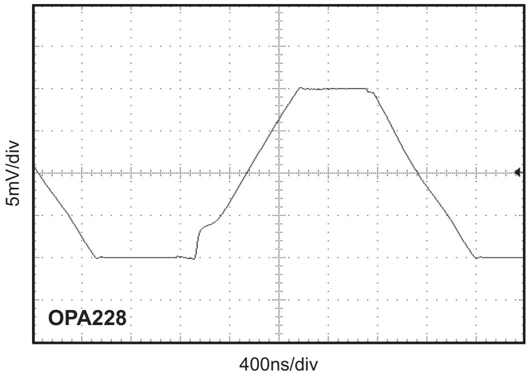


Figure 53. Large-Signal Step Response, G = 2, C_{LOAD} = 100 pF, Input Signal = 5 Vp-p

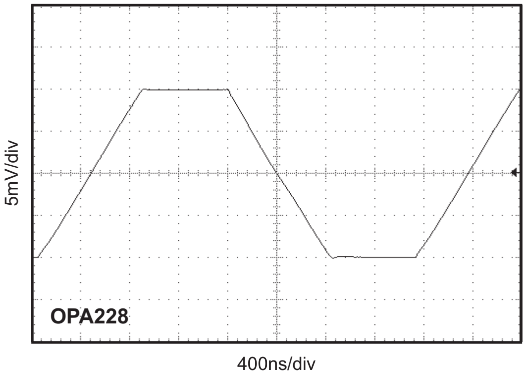


Figure 54. Large-Signal Step Response, G = –2, CLOAD = 100 pF, Input Signal = 5 Vp-p

Typical Application (continued)

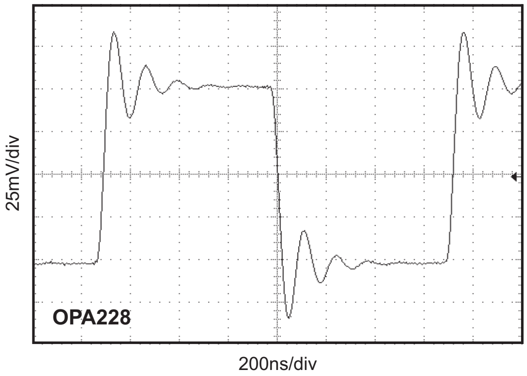


Figure 55. Small-Signal Step Response, G = 2, C_{LOAD} = 100 pF, Input Signal = 50 mVp-p.

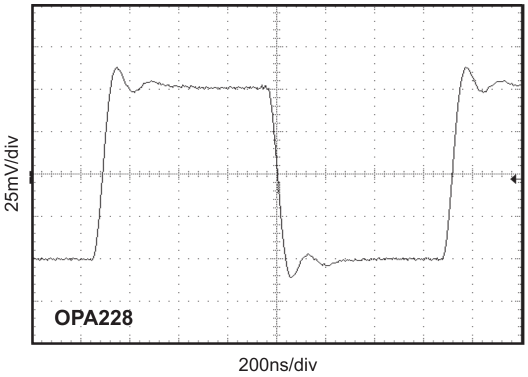


Figure 56. Small-Signal Step Response, G = –2, C_{LOAD} = 100 pF, Input Signal = 50 mVp-p.

9 Power Supply Recommendations

The OPAx22x series are specified for operation from 5 V to 36 V (±2.5 V to ±18 V); many specifications apply from –40°C to 85°C. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in the *Electrical Characteristics: OPAx227 Series (V_S = ±5 V to ±15 V)*.

CAUTION

Supply voltages larger than 36 V can permanently damage the device; see the *Absolute Maximum Ratings*.

Place 0.1-µF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, refer to the *Layout Guidelines*.

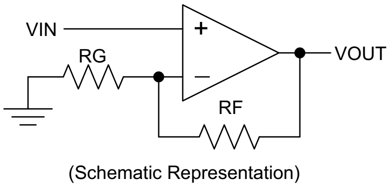
10 Layout

10.1 Layout Guidelines

For best operational performance of the device, use good PCB layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and operational amplifier itself. Bypass capacitors are used to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1-µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds paying attention to the flow of the ground current. For more detailed information refer to *Circuit Board Layout Techniques* (SLOA089).
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace perpendicular is much better as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible. As shown in *Layout Example*, keeping RF and RG close to the inverting input minimizes parasitic capacitance.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.
- Cleaning the PCB following board assembly is recommended for best performance.
- Any precision integrated circuit may experience performance shifts due to moisture ingress into the plastic package. Following any aqueous PCB cleaning process, baking the PCB assembly is recommended to remove moisture introduced into the device packaging during the cleaning process. A low temperature, post cleaning bake at 85°C for 30 minutes is sufficient for most circumstances.

10.2 Layout Example



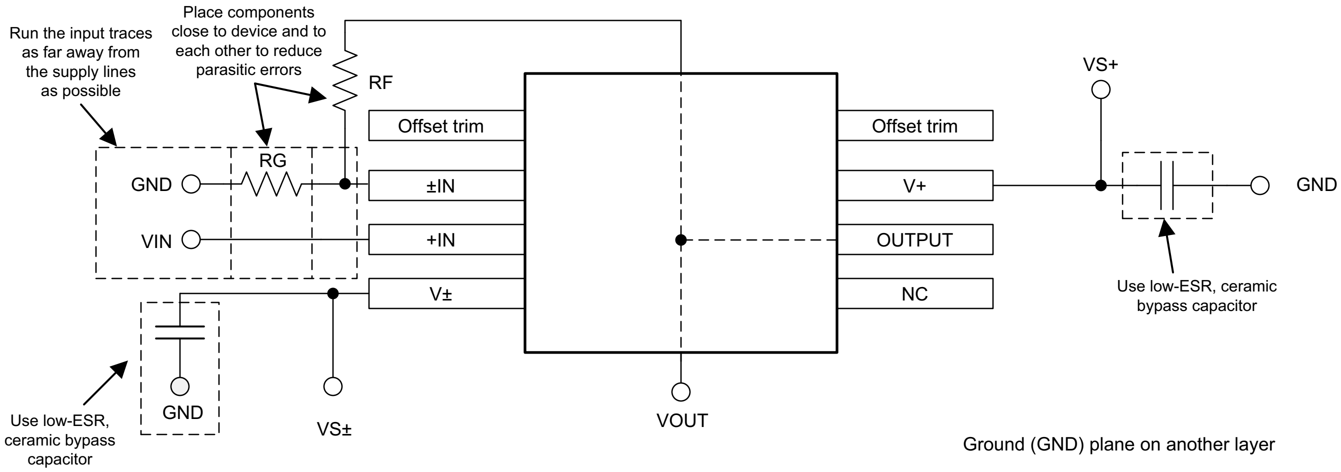


Figure 57. OPAx227 Layout Example

11 Device and Documentation Support

11.1 Device Support

11.1.1 Development Support

11.1.1.1 TINA-TI™ (Free Software Download)

TINA™ is a simple, powerful, and easy-to-use circuit simulation program based on a SPICE engine. TINA-TI is a free, fully-functional version of the TINA software, preloaded with a library of macro models in addition to a range of both passive and active models. TINA-TI provides all the conventional DC, transient, and frequency domain analysis of SPICE, as well as additional design capabilities.

Available as a free download from the Analog eLab Design Center, TINA-TI offers extensive post-processing capability that allows users to format results in a variety of ways. Virtual instruments offer the ability to select input waveforms and probe circuit nodes, voltages, and waveforms, creating a dynamic quick-start tool.

NOTE

These files require that either the TINA software (from DesignSoft™) or TINA-TI software be installed. Download the free TINA-TI software from the TINA-TI folder.

11.1.1.2 TI Precision Designs

The OPAx22x are featured in several TI Precision Designs, available online at http://www.ti.com/ww/en/analog/precision-designs/. TI Precision Designs are analog solutions created by TI's precision analog applications experts and offer the theory of operation, component selection, simulation, complete PCB schematic and layout, bill of materials, and measured performance of many useful circuits.

11.2 Documentation Support

11.2.1 Related Documentation

Circuit Board Layout Techniques, SLOA089

EMI Rejection Ratio of Operational Amplifiers, SBOA128

11.3 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 2. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
OPA227	Click here	Click here	Click here	Click here	Click here
OPA2227	Click here	Click here	Click here	Click here	Click here
OPA4227	Click here	Click here	Click here	Click here	Click here
OPA228	Click here	Click here	Click here	Click here	Click here
OPA2228	Click here	Click here	Click here	Click here	Click here
OPA4228	Click here	Click here	Click here	Click here	Click here

11.4 Trademarks

TINA-TI is a trademark of Texas Instruments, Inc.
TINA, DesignSoft are trademarks of DesignSoft, Inc.
All other trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA2227P	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type		OPA2227P	Samples
OPA2227PA	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type		OPA2227P A	Samples
OPA2227PAG4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type		OPA2227P A	Samples
OPA2227PG4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type		OPA2227P	Samples
OPA2227U	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	OPA 2227U	Samples
OPA2227U/2K5	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	OPA 2227U	Samples
OPA2227U/2K5G4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	OPA 2227U	Samples
OPA2227UA	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	OPA 2227U A	Samples
OPA2227UA/2K5	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	OPA 2227U A	Samples
OPA2227UA/2K5E4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	OPA 2227U A	Samples
OPA2227UAE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	OPA 2227U A	Samples
OPA2227UAG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	OPA 2227U A	Samples
OPA2227UE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	OPA 2227U	Samples
OPA2227UG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	OPA 2227U	Samples
OPA2228P	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type		OPA2228P	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA2228PA	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type		OPA2228P A	Samples
OPA2228PAG4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type		OPA2228P A	Samples
OPA2228PG4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type		OPA2228P	Samples
OPA2228U	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR		OPA 2228U	Samples
OPA2228U/2K5	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR		OPA 2228U	Samples
OPA2228U/2K5E4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR		OPA 2228U	Samples
OPA2228UA	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR		OPA 2228U A	Samples
OPA2228UA/2K5	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR		OPA 2228U A	Samples
OPA2228UA/2K5E4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR		OPA 2228U A	Samples
OPA2228UAE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR		OPA 2228U A	Samples
OPA2228UE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR		OPA 2228U	Samples
OPA227P	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type		OPA227P	Samples
OPA227PA	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type		OPA227P A	Samples
OPA227PAG4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type		OPA227P A	Samples
OPA227PG4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type		OPA227P	Samples
OPA227U	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR		OPA 227U	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA227U/2K5	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR		OPA 227U	Samples
OPA227U/2K5E4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR		OPA 227U	Samples
OPA227UA	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR		OPA 227U A	Samples
OPA227UA/2K5	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR		OPA 227U A	Samples
OPA227UA/2K5G4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR		OPA 227U A	Samples
OPA227UAG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR		OPA 227U A	Samples
OPA227UE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR		OPA 227U	Samples
OPA228P	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type		OPA228P	Samples
OPA228PA	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type		OPA228P A	Samples
OPA228PAG4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type		OPA228P A	Samples
OPA228PG4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type		OPA228P	Samples
OPA228U	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR		OPA 228U	Samples
OPA228UA	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR		OPA 228U A	Samples
OPA228UA/2K5	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR		OPA 228U A	Samples
OPA228UAG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR		OPA 228U A	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA228UG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR		OPA 228U	Samples
OPA4227PA	ACTIVE	PDIP	N	14	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type		OPA4227PA	Samples
OPA4227PAG4	ACTIVE	PDIP	N	14	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type		OPA4227PA	Samples
OPA4227UA	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU-DCC	Level-3-260C-168 HR		OPA4227UA	Samples
OPA4227UA/2K5	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU-DCC	Level-3-260C-168 HR		OPA4227UA	Samples
OPA4227UA/2K5G4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU-DCC	Level-3-260C-168 HR		OPA4227UA	Samples
OPA4227UAG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU-DCC	Level-3-260C-168 HR		OPA4227UA	Samples
OPA4228PA	ACTIVE	PDIP	N	14	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type		OPA4228PA	Samples
OPA4228PAG4	ACTIVE	PDIP	N	14	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type		OPA4228PA	Samples
OPA4228UA	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU-DCC	Level-3-260C-168 HR		OPA4228UA	Samples
OPA4228UA/2K5	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU-DCC	Level-3-260C-168 HR		OPA4228UA	Samples
OPA4228UA/2K5G4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU-DCC	Level-3-260C-168 HR		OPA4228UA	Samples
OPA4228UAE4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU-DCC	Level-3-260C-168 HR		OPA4228UA	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF OPA2227 :

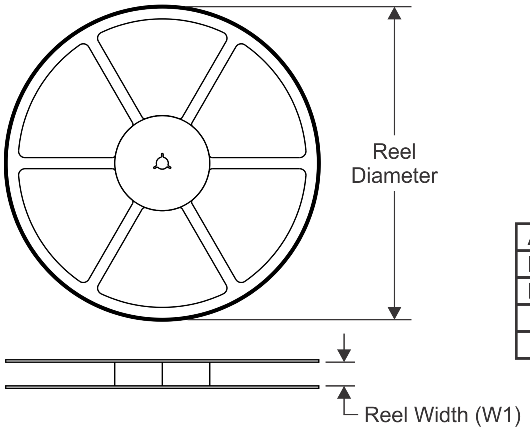
- Enhanced Product: OPA2227-EP

NOTE: Qualified Version Definitions:

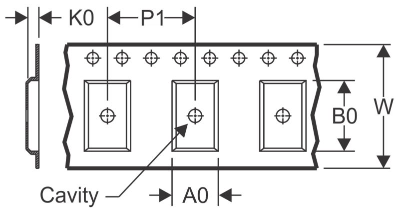
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

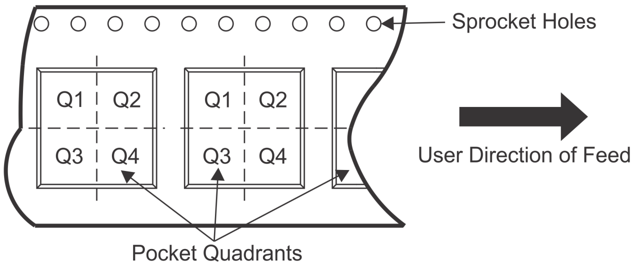


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

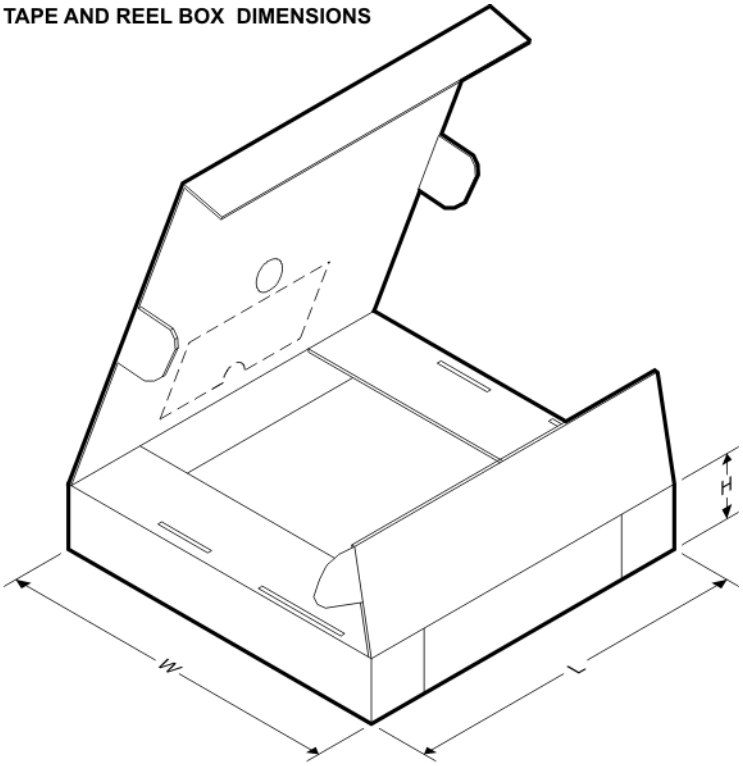
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA2227U/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA2227UA/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA2228U/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA2228UA/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA227U/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA227UA/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA228UA/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA4227UA/2K5	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
OPA4228UA/2K5	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

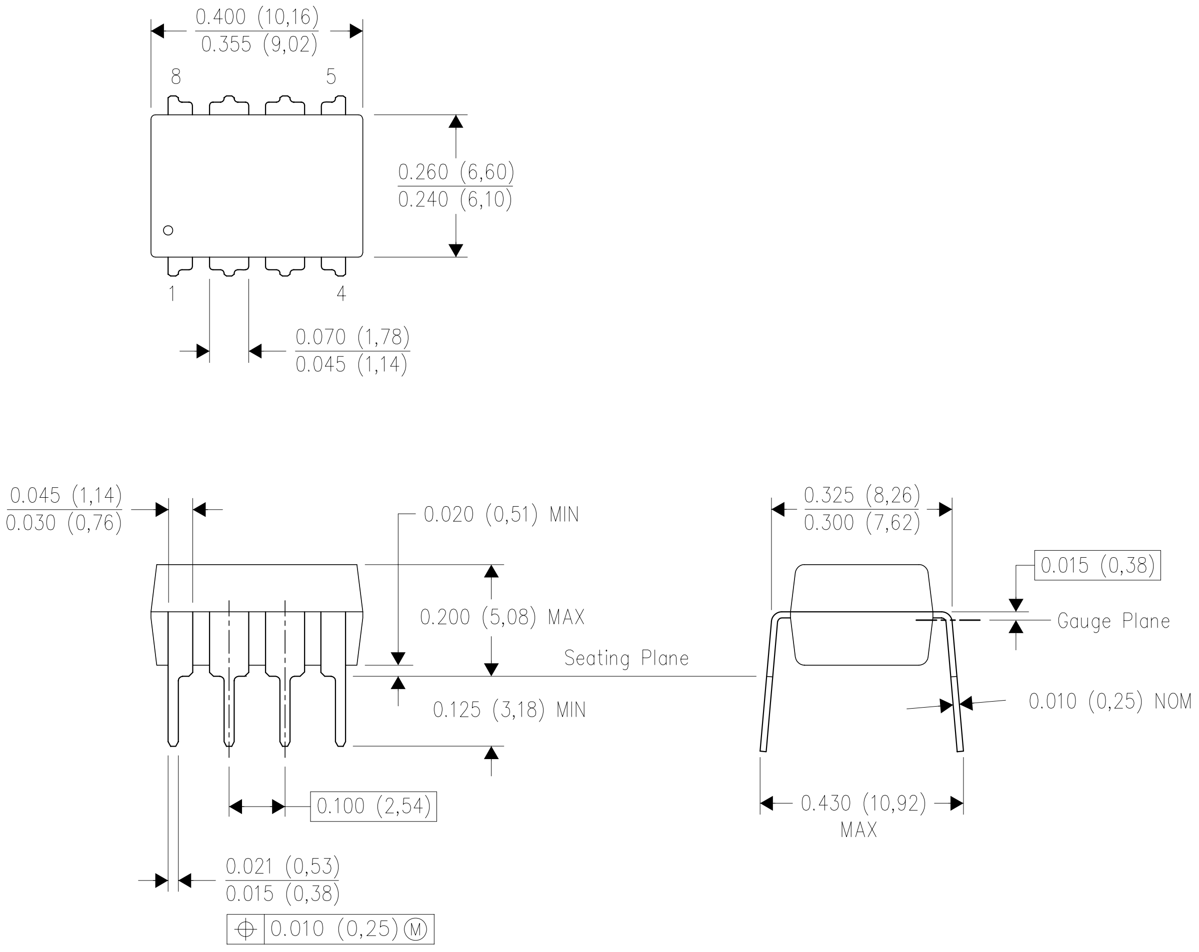
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA2227U/2K5	SOIC	D	8	2500	367.0	367.0	35.0
OPA2227UA/2K5	SOIC	D	8	2500	367.0	367.0	35.0
OPA2228U/2K5	SOIC	D	8	2500	367.0	367.0	35.0
OPA2228UA/2K5	SOIC	D	8	2500	367.0	367.0	35.0
OPA227U/2K5	SOIC	D	8	2500	367.0	367.0	35.0
OPA227UA/2K5	SOIC	D	8	2500	367.0	367.0	35.0
OPA228UA/2K5	SOIC	D	8	2500	367.0	367.0	35.0
OPA4227UA/2K5	SOIC	D	14	2500	367.0	367.0	38.0
OPA4228UA/2K5	SOIC	D	14	2500	367.0	367.0	38.0

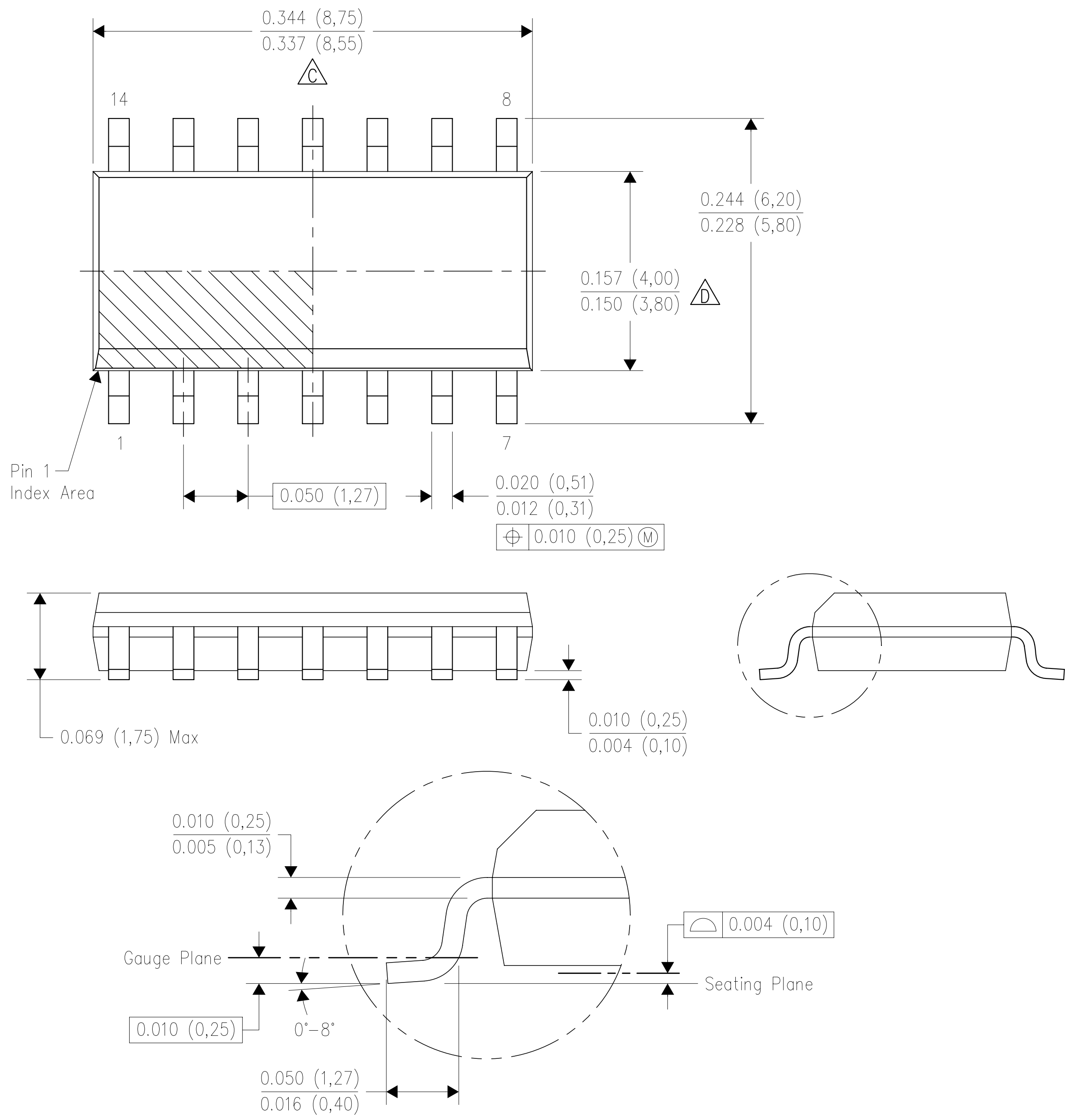
P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



4040082/E 04/2010

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

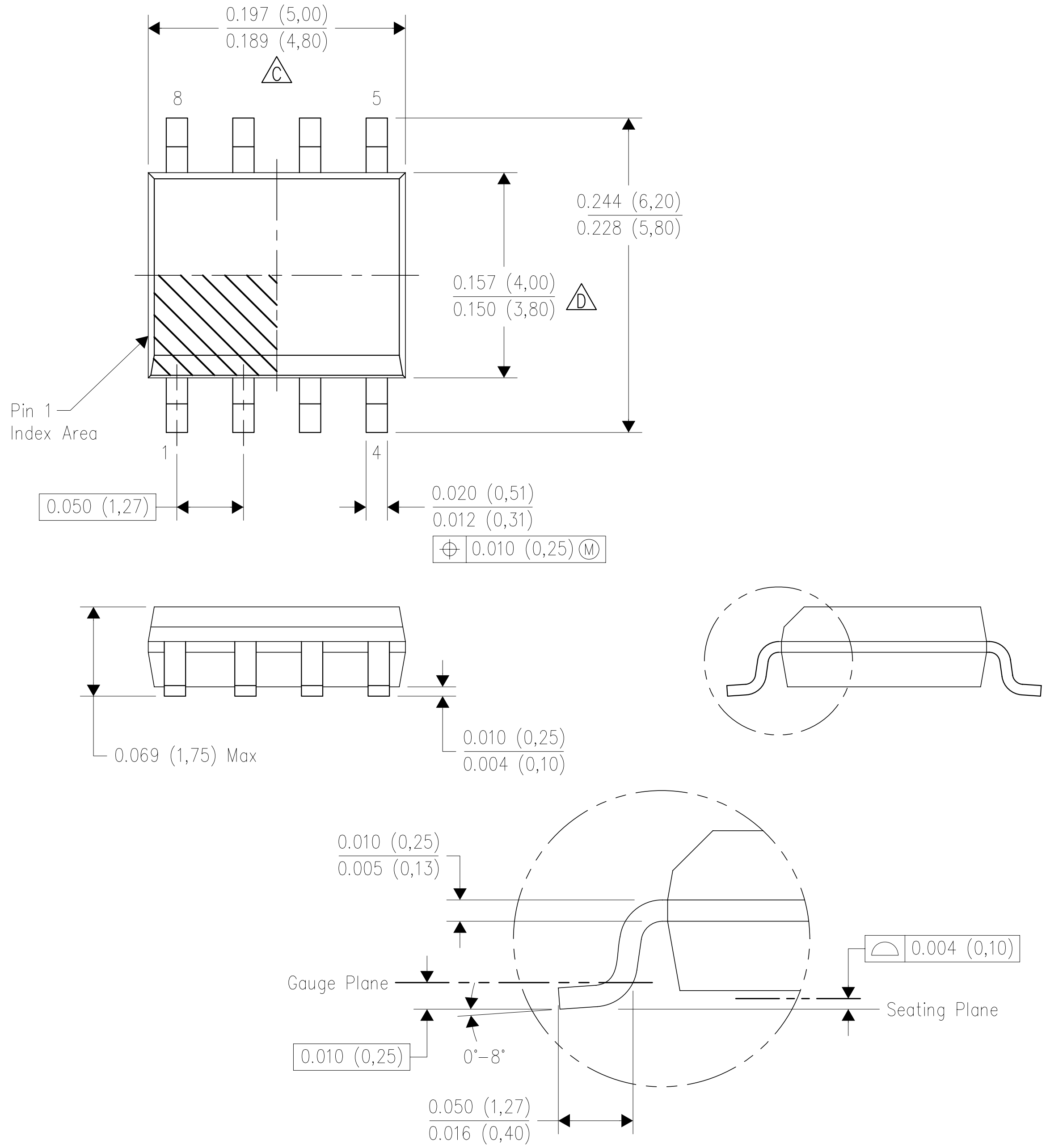
D (R-PDSO-G14) PLASTIC SMALL OUTLINE



4040047-5/M 06/11

NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- D Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G8) PLASTIC SMALL OUTLINE



4040047-3/M 06/11

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS-012 variation AA.

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