6ED2742S01Q
160 V pre-regulated three phase SOI gate driver with integrated charge pump, current sense amplifier, over-current protection, and bootstrap diodes

Features

- Bootstrap voltage (VB node) of +160 V
- Floating channel designed for bootstrap operation
- Integrated power management unit (PMU) with;
  - Linear pre-regulator to enable wide input VIN range
  - Integrated charge pump for stable V_{CC}
- Integrated current sense amplifier (CSA) with selectable gain
- Integrated over-current protection with selectable V_{REF} threshold
- 100% duty cycle operation with trickle charge pump per high side
- Integrated low R_{ON}, ultra-fast bootstrap diodes
- Independent under voltage lockout for both high and low side
- Integrated shoot-through protection with built-in dead time
- Multi-function RFE pin (Enable, Fault, and automatic Fault clear)
- Integrated short pulse / noise rejection input filter
- Schmitt trigger inputs with hysteresis
- 3.3 V, 5 V input logic compatible, outputs in phase with inputs
- Available in small footprint QFN32 lead, 5x5 mm package
- 2kV HBM ESD, RoHS compliant

Product summary

V_{B_OFFSET} = 160 V max
I_{O+_pk} / I_{O-_pk} (typ) = + 1 A / - 2 A
Deadtime (typ) = 100 ns
t_{ON} / t_{OFF} (typ) = 100 ns/ 100 ns
Delay matching = 20 ns max

Package

32-Lead QFN
5x5mm

Applications

General purpose three phase gate driver for N-Channel MOSFETs

- Servo Drives in Robotics and Factory Automation
- General Purpose Low Voltage Drives or inverters
- e-Scooters, e-Bikes, and other e-Vehicles that do not require Automotive Qualification (LSEV)
- Battery operated Small Home Appliances (SHA)
- Commercial and Agricultural Drones
- Professional and Consumer Service Robotics
- Logistics Vehicles (eForklifts, Autonomous warehouse robotics)
- Battery operated hand-held power tools
- Gardening or Outdoor Power Equipment (OPE) Tools

Product validation

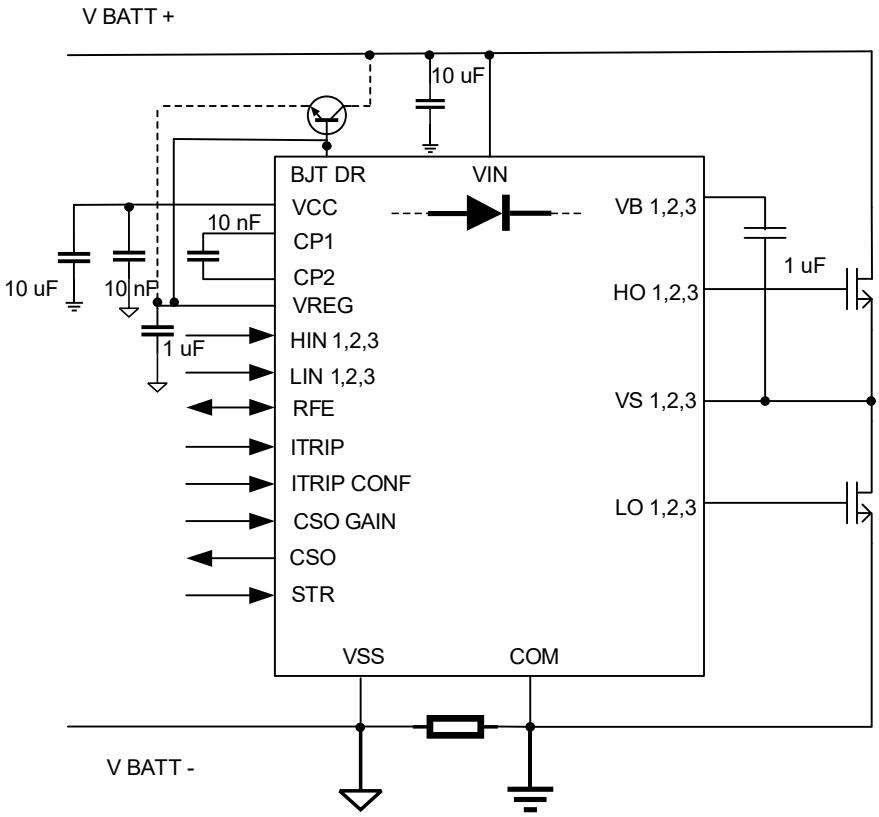
Qualified for industrial applications according to the relevant tests of JEDEC78/20/22

Ordering information

Base part number	Package type	Standard pack		Orderable part number
		Form	Quantity	
6ED2742S01Q	5 x 5mm QFN32	Tape and Reel	2,500	6ED2742S01QXUMA1

1 Description

The 6ED2742S01Q is a 160 V SOI based gate driver designed for three phase BLDC motor drive applications. Integrated bootstrap diodes are used to supply the three external high sides charging bootstrap capacitors and supports 100% duty cycle operation by a trickle charge pump. Protection features include under voltage lockout, over current protection with configurable threshold, fault communication and automatic fault clear. The output drivers feature a high-pulse current buffer stage designed for minimum driver cross-conduction. A current sense operational amplifier (CSA) with selectable gain is integrated between the VSS and COM.



*Bootstrap diode is monolithically integrated.
* For optimal operation use the minimum capacitance values on supply pins as shown here

This diagram shows electrical connections only. Please refer to our application notes and design tips for proper circuit board layout.

Figure 1 Typical application block diagram

2 Table of contents

Electrical parameters

2.1 Absolute maximum ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to VSS unless otherwise stated in the table. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

Table 1 Absolute maximum ratings

Symbol	Definition		Min.	Max.	Units
V_B	High-side floating well supply voltage (Note 1)		-0.3	160	
V_{IN}	Input battery supply voltage		5	140	V
V_S	High-side floating well supply return voltage		-0.3	140	
V_{BS}	Bootstrap supply range		-0.3	20	
V_{HO}	Floating gate drive output voltage		V_S – 0.3	V_B + 0.3	
V_{REG}	Charge pump input voltage		-0.3	20	
V_{CC}	Low side supply voltage		-0.3	20	
V_{LO}	Low-side output voltage		–0.3	V_{cc} + 0.3	
$V_{LOGIC\ IN}$	Logic input voltage (HIN, LIN)		-0.3	5	
BJTDR	Output signal for base drive of external NPN BJT		-0.3	20	
RFE	Enable, Fault and automatic fault clear pin		-0.3	5	
ITRIP	Over current protection input pin		-0.3	5	
ITRIP CONF	Over current protection threshold configuration pin		-0.3	5	
CSO	Current sense op amp output		-0.3	3.6	
CSO GAIN	Current sense op amp gain configuration pin		-0.3	5	
STR	Strobe signal for op amp offset compensation		-0.3	5	
CP1	Charge pump capacitor pin1		-0.3	20	
CP2	Charge pump capacitor pin2		-0.3	20	
COM	Low side power ground return		-5.0	+5.0	
dV_S/dt	Allowable V_S offset supply transient relative to COM		—	50	V / ns
P_D	Package power dissipation @ T_A ≤+25ºC	5 x 5mm QFN-32		3	W
Rth_{JA}	Thermal resistance, junction to ambient	5 x 5mm QFN-32		41	ºC/W
T_J	Junction temperature		—	150	ºC
T_S	Storage temperature		-50	150	
T_L	Lead temperature (soldering, 10 seconds)		—	260	

Note 1: In case VCC > V_B there is an additional power dissipation in the internal bootstrap diode between pins VCC and V_B.

2.2 Recommended operating conditions

For proper operation, the device should be used within the recommended conditions. All voltage parameters are absolute voltages referenced to COM unless otherwise stated below

Table 2 Recommended operating conditions

Symbol	Definition	Min	Max	Units
V_{IN}	Input battery supply voltage	6	140	V
V_B	Bootstrap voltage	V_S + 6	140	
V_{BS}	High-side floating well supply voltage	6	18	
V_S	High-side floating well supply offset voltage	0	122	
V_{HO}	Floating gate drive output voltage	V_S	V_B	
V_{REG}	Charge pump input voltage	5	18	
V_{CC}	Low-side supply voltage (internal PM block)	11	13	
V_{CC}	Low-side supply voltage (external supply)	9	18	
V_{LO}	Low-side output voltage	0	VCC	
$V_{LOGIC\ IN}$	Logic input voltage(HIN, LIN, RFE, STR)	V_{SS}	5	
T_A	Ambient temperature	-40	125	ºC

Note 2: Logic operational for V_S of -8V to +120V. Logic state held for V_S of -8V to -V_{BS}.

2.3 Static electrical characteristics

(V_{CC} – COM) = (V_B – V_S) = 12 V, V_{SS} = COM and T_A = 25 °C unless otherwise specified. The V_{IL}, V_{IH} and I_{IN} parameters are referenced to Vss / COM and are applicable to the respective input leads: HIN and LIN. The V_O and I_O parameters are referenced to V_S / COM and are applicable to the respective output leads HO or LO. The V_{CCUV} parameters are referenced to COM. The V_{BSUV} parameters are referenced to V_S.

Table 3 Static electrical characteristic

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
$V_{CCUVLO+}$	V_{CC} supply undervoltage positive going threshold	6.6	7.5	8.4	V	
$V_{CCUVLO-}$	V_{CC} supply undervoltage negative going threshold	6	6.8	7.6		
$V_{CCUVLOHY}$	V_{CC} supply undervoltage hysteresis	0.2	0.7	1.3		
$V_{BSUVLO+}$	V_{BS} supply undervoltage positive going threshold	4.6	5	5.4		
$V_{BSUVLO-}$	V_{BS} supply undervoltage negative going threshold	4.1	4.5	4.9		
$V_{BSUVLOHY}$	V_{BS} supply undervoltage hysteresis	0.2	0.5	1.3	V	

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
I_{LK}	High-side floating well offset supply leakage	—	—	3	uA	V_B = V_S = 140 V
I_{QCC}	Quiescent supply current	250	350	450		
I_{QBS}	V_{BS} quiescent supply current HO = Off	15	25	40		All input combinations
V_{OH}	High level output voltage LO 1,2,3 HO 1,2,3	—	140	200	V	I_O = 20 mA
V_{OL}	Low level output voltage LO 1,2,3 HO 1,2,3	—	70	120		
I_{opk+}	Peak output current turn-on[1]	—	1000	—	mA	PW ≤ 10 µs
I_{opk-}	Peak output current turn-off[1]	—	2000	—		PW ≤ 10 µs
V_{IH}	Logic “1” input voltage	1.4	1.7	2.0	V	
V_{IL}	Logic “0” input voltage	0.8	1.1	1.4		
$I_{LOGIC\ IN+}$	Input bias current (Output = High)	10	20	30	µA	V_{IN} = 4 V
$I_{LOGIC\ IN-}$	Input bias current (Output = Low)	—	0.15	0.5		V_{IN} = 0 V
R_{BSD}	Bootstrap diode resistance	20	38	55	Ω	
V_{ITRIP}	Over current threshold voltage	950	1000	1050	mV	ITRIP Conf > 3 V
		475	500	525		1.5V < ITRIP Conf < 2V
		225	250	275		0.5V < ITRIP Conf < 1V
		110	130	150		ITRIP Conf < 0.25V

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
G_{CSO}	Current sense amplifier gain	36	40	41	V/V	CSO gain > 3 V
		18	20	21		1.5V < CSO gain< 2V
		9	10	11		0.5V < CSO gain < 1V
		4	5	6		CSO gain < 0.25V
$V_{OFF\_OUT\_40}$	Current sense amplifier output offset @ gain = 40	15	150	285	mV	COM = Vss
$V_{OFF\_OUT\_20}$	Current sense amplifier output offset @ gain = 20	80	150	220		
$V_{OFF\_OUT\_10}$	Current sense amplifier output offset @ gain = 10	110	150	190		
$V_{OFF\_OUT\_5}$	Current sense amplifier output offset @ gain = 5	130	150	170		
V_{OFF_T}[1]	Current sense amplifier output offset drift vs. Temperature	-10		+10	%	COM = Vss, -40 °C < Tj < 150 °C
SR	Slew rate	6.5	—	—	V/us	
V_{RFE+}	RFE positive going threshold	1.4	1.7	2.0	V	
V_{RFE-}	RFE negative going threshold	0.8	1.1	1.4		
I_{RFE+}	Logic “1” Input bias current	—	—	1	uA	
I_{RFE-}	Logic “0” Input bias current	-1	—	—		

[1] Not subjected to production test, verified by characterization.

2.4 Dynamic electrical characteristics

VCC = V_{BS}= 12 V, V_{SS} = COM, T_A = 25 °C and C_L = 1000 pF unless otherwise specified.

Table 4 Dynamic electrical characteristics

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
t_{ON}	Turn-on propagation delay	50	100	190	ns	Cload = 1nF, IN 50% rise to OUT 10% rise
t_{OFF}	Turn-off propagation delay	50	100	190		Cload = 1nF, IN 50% fall to OUT 90% fall
t_R	Turn-on rise time	5	20	40		Cload = 1nF, OUT 10% to OUT 90%
t_F	Turn-off fall time	5	10	40		Cload = 1nF, OUT 90% to OUT 10%
MT	Delay matching time (HS & LS turn-on/off)	—	—	20		Cload = 1nF, OUT 90% to OUT 10%
DT	Deadtime: LO Turn-off to HO Turn-on & HO Turn-off to LO turn-on	70	100	160		
t_{EN}	Enable low to output shutdown propagation delay	60	100	160		
t_{ITRIP}	ITRIP to output shutdown propagation delay	150	100	400		
t_{BL}	ITRIP blanking time	—	150	—		
t_{fil}	Input noise filter time	—	30	—		
t_{FLT}	ITRIP to FAULT propagation delay	150	200	350		
$T_{wakep-up}$	Sleep wake-up time	—	—	2	ms	VIN = 12V, VREG = 1uF, VCC = 1uF, Ccp = 10nF, Tfltclr < 10us, when Vcc is above 8.5V
t_{FLTCLR}	FAULT clear time (R = 2 MΩ, C = 1 nF)	—	1.5	—		R =2 MΩ, C = 1 nF on RFE

3 Block diagram

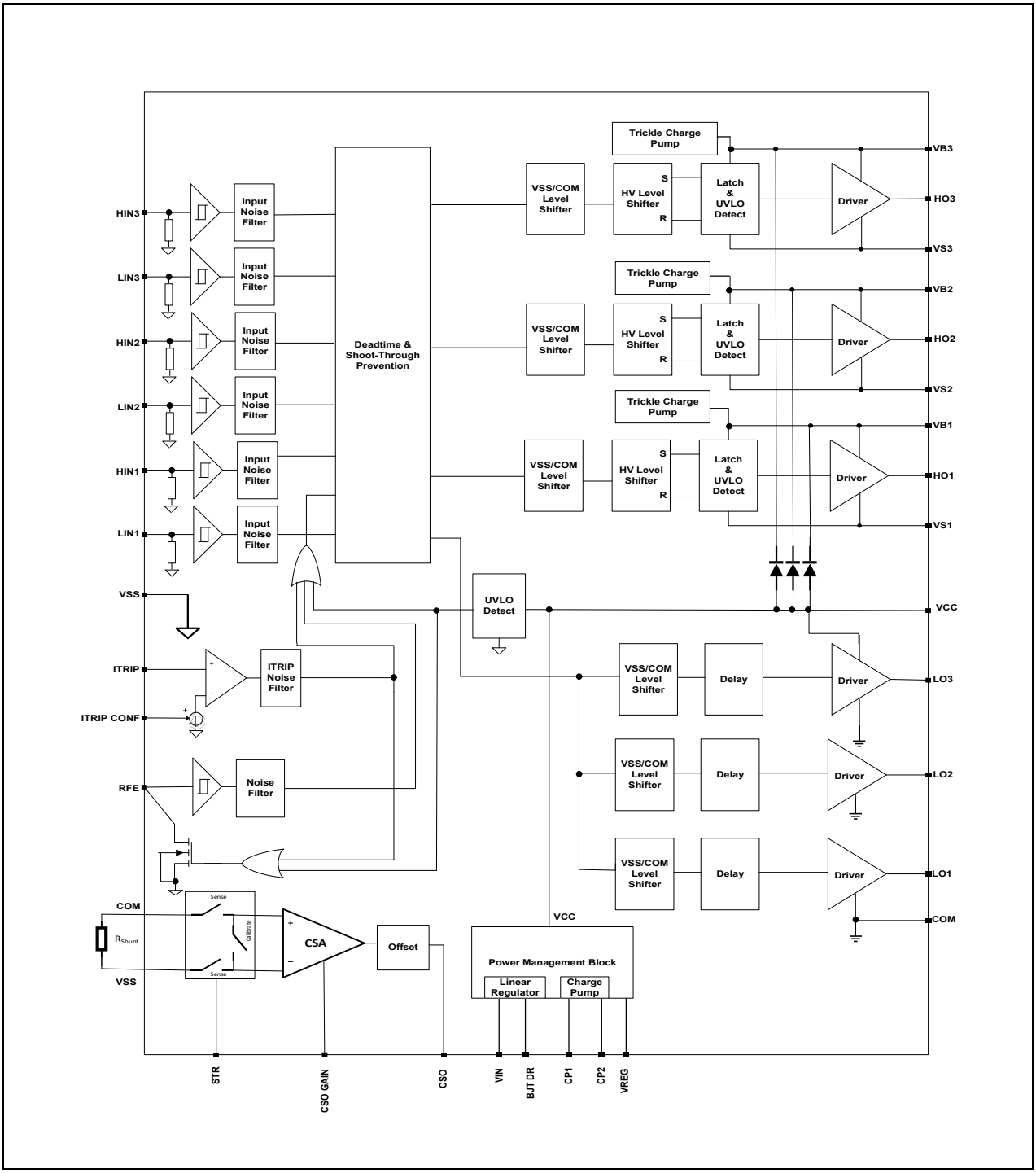


Figure 2 Functional block diagram

4 Pin configuration and functionality

4.1 Pin configuration

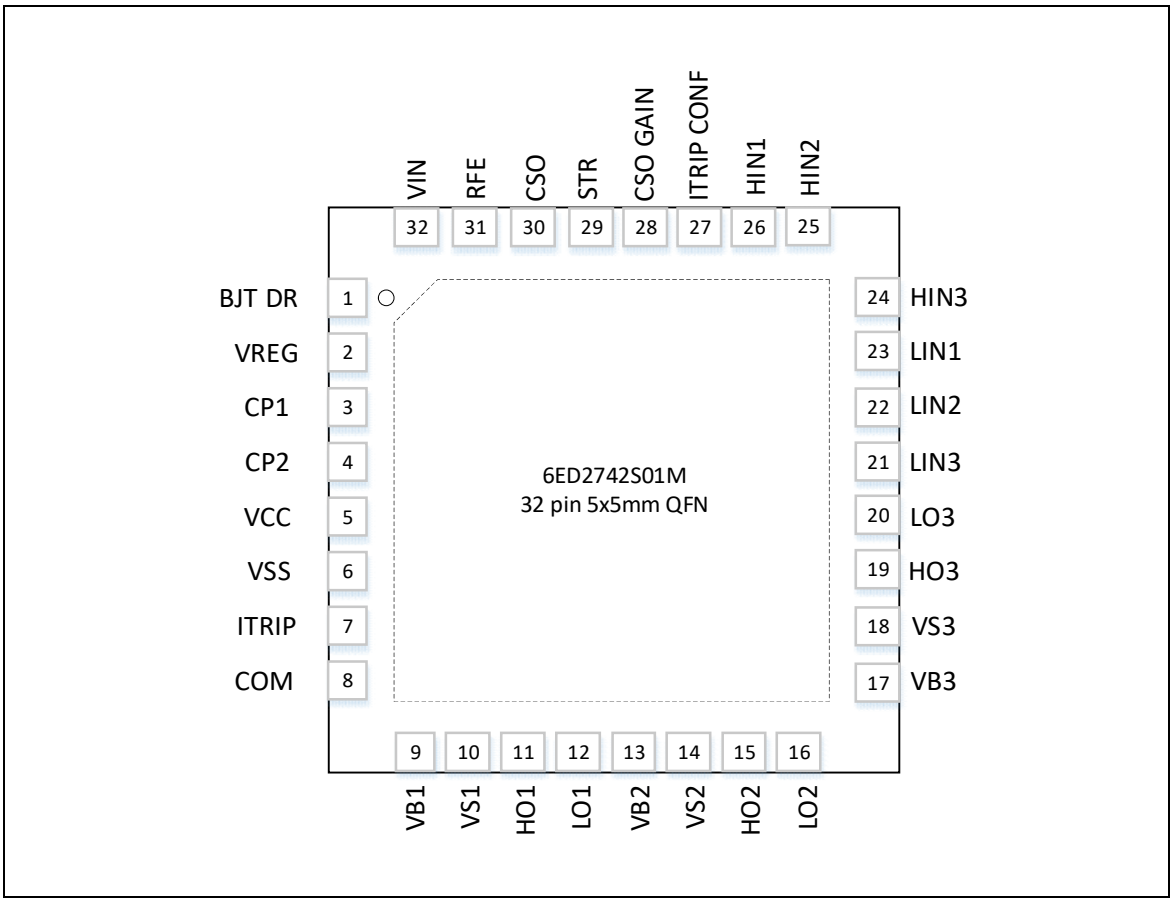


Figure 3 6ED2742S01Q pin assignments (top view)

4.2 Pin functionality

Table 5 Pin descriptions

Symbol	Pin No.	Type	Description
HIN1,2,3	26,25,24	Input	Logic input for high side gate driver output (HOx), in phase
LIN1,2,3	23,22,21	Input	Logic input for low side gate driver output (LOx), in phase
VB1,2,3	9, 13, 17	Output	High side floating supplies
HO1,2,3	11, 15, 19	Output	High side gate drive outputs
VS1,2,3	10, 14, 18	Input	High side floating supply returns
VCC	5	Input	Low side and logic fixed supply
LO1,2,3	12,16,20	Output	Low side gate drive outputs
COM	8	Ground	Low side power ground return
VIN	32	Input	Input voltage (Battery voltage)
VSS	6	Ground	Logic ground
BJT DR	1	Output	Output signal for base drive of external NPN BJT
ITRIP CONF	27	Input	Over current protection threshold configuration pin
ITRIP	7	Input	Over current protection input pin
VREG	2	Output	Charge pump input voltage
CP1	3	Input	Charge pump capacitor pin1
CP2	4	Input	Charge pump capacitor pin2
CSO	30	Output	Current sense op amp output
STR	29	Input	Strobe signal for op amp offset compensation
CSO GAIN	28	Input	Current sense op amp gain configuration pin
RFE	31	Input / Output	Enable, Fault and automatic fault clear pin

5 Application information and additional details

5.1 MOSFET gate drive

The 6ED2742S01Q HVIC is designed to drive MOSFET power devices in battery operated applications. Figures 4 and 5 illustrate several parameters associated with the gate drive functionality of the HVIC. The output current of the HVIC, used to drive the gate of the power switch, is defined as I_O. The voltage that drives the gate of the external power switch is defined as V_{HO} for the high-side power switch and V_{LO} for the low-side power switch; this parameter is sometimes generically called V_{OUT} and in this case does not differentiate between the high-side or low-side output voltage.

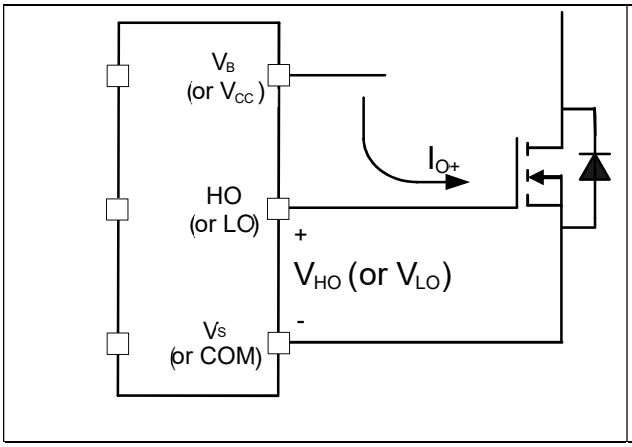


Figure 4 HVIC Sourcing current

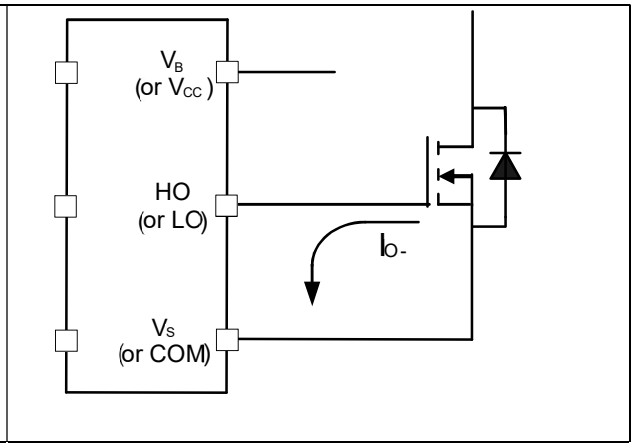


Figure 5 HVIC Sinking current

5.2 Switching relationships

The relationships between the input and output signals of the 6ED2742S01Q are illustrated below in Figure 6. We can see the definitions of several timing parameters (i.e. t_{ON}, t_{OFF}, t_R, and t_F) associated with this device.

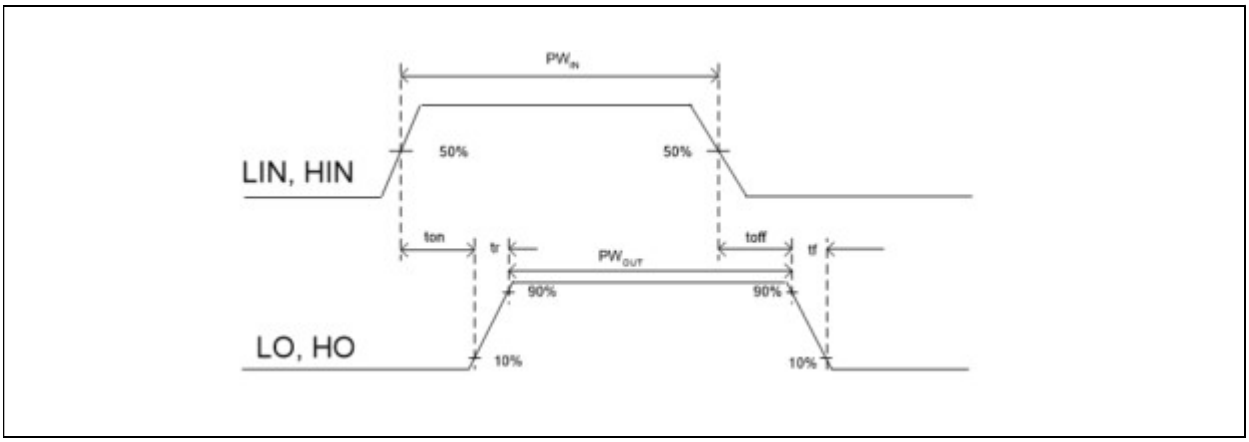


Figure 6 Switching timing diagram

5.3 Timing diagrams

The following two figures illustrate the timing relationships of some of the functionality of the 6ED2742S01Q, in particular over-current protection feature with fault reporting and automatic fault clear.

Interval A of Figures 7 and 8 shows that the signal between Vss and COM has gone from a low to a high state crossing the threshold set up by ITRIP CONF pin; as a result, all of the gate drive outputs have been disabled (i.e., see that HO has returned to the low state; LO is also held low), and a fault condition is reported on the RFE pin, which goes 0V. Once the over-current event has returned to the low state, the output will remain disabled and the fault condition reported until the voltage on the RFE pin charges up to VRFE+ threshold (see interval C in Figure 4); the charging characteristics are dictated by the RC network attached to the RFE pin.

During interval B and D of Figure 7 and 9, we can see that the RFE pin has been pulled low (as is the case when the driver IC has received a command from the control IC to shutdown); these results in the outputs (HO and LO) being held in the low state until the RFE pin is pulled high.over

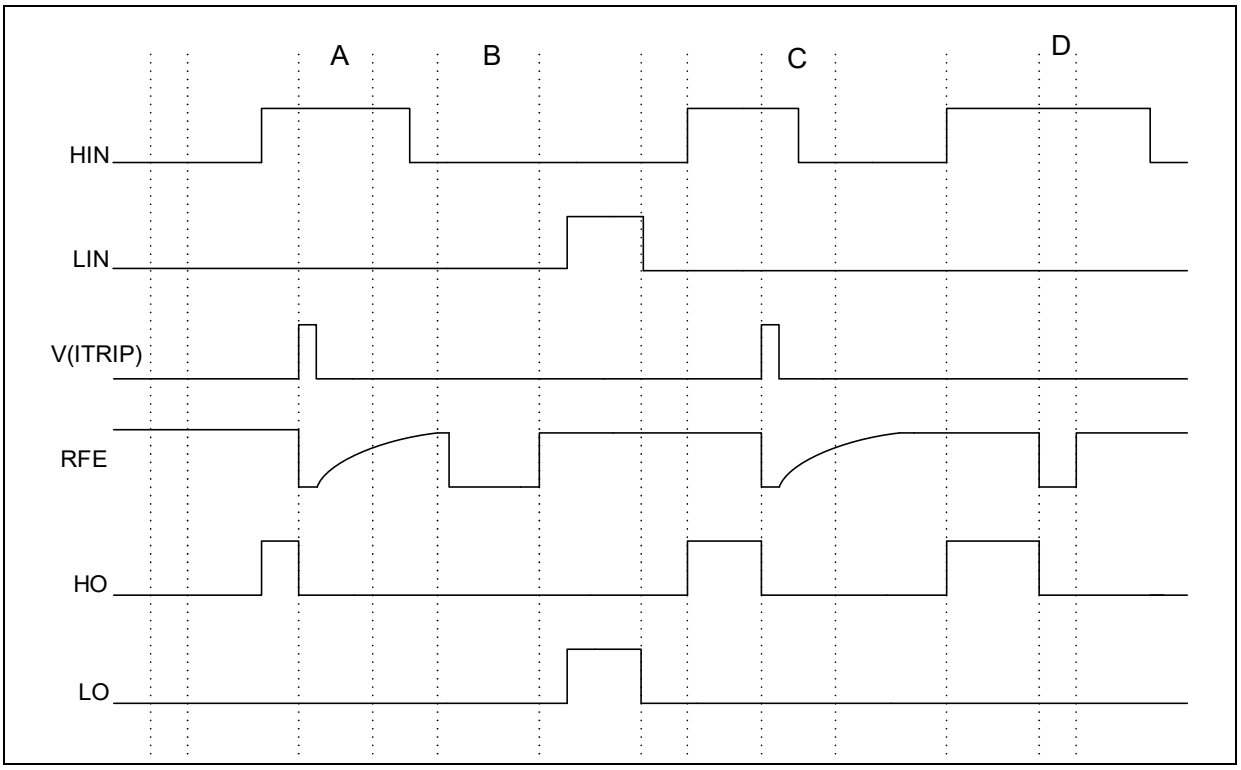


Figure 7 Input/output timing diagram

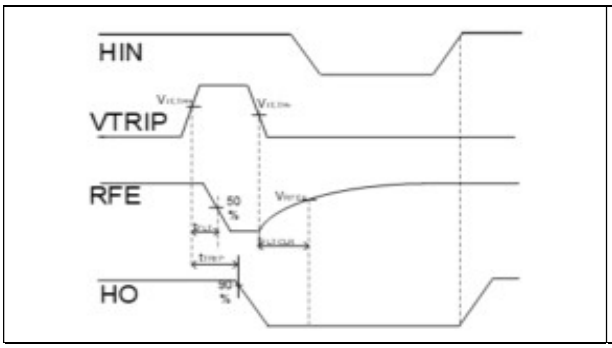


Figure 8 Detailed view of C interval

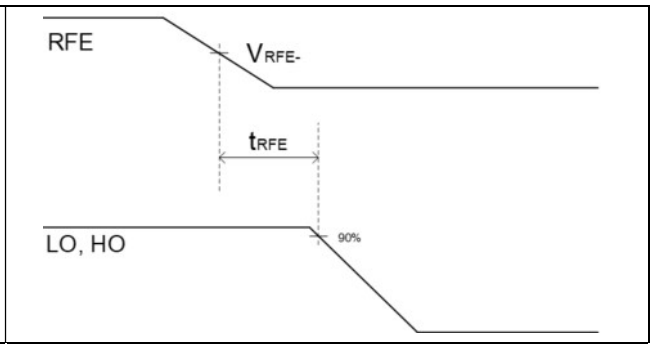


Figure 9 Detailed view of D interval

5.4 Deadtime and matched propagation delays

This 6ED2742S01Q features integrated deadtime protection circuitry. The deadtime feature inserts a time period (a minimum deadtime) in which both the high- and low-side power switches are held off; this is done to ensure that the power switch being turned off has fully turned off before the second power switch is turned on. This minimum deadtime is automatically inserter whenever the external deadtime is shorter than DT; external deadtimes larger than DT are not modified by the gate driver. Figure 10 illustrates the deadtime period and the relationship between the output gate signals.

The deadtime circuitry of 6ED2742S01Q is matched with respect to the high- and low-side outputs. Figure 10 defines the two deadtime parameters (i.e., DTLO-HO and DTHO-LO); the deadtime matching parameter (MDT) associated with the 6ED2742S01Q specifies the maximum difference between DTLO-HO and DTHO-LO.

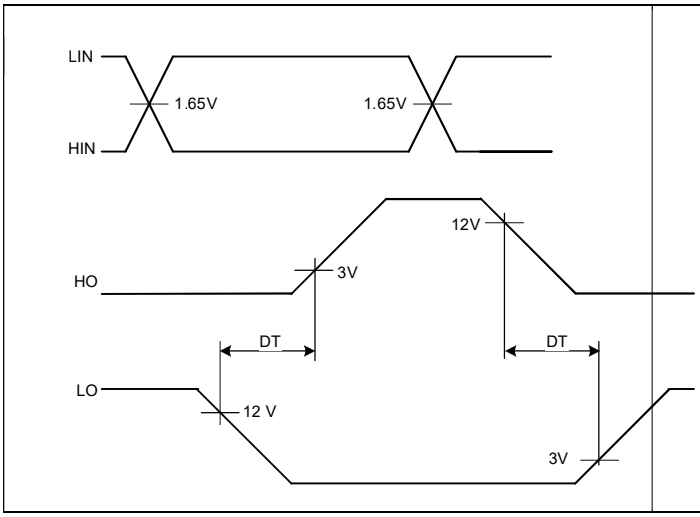


Figure 10 Dead Time Definitions

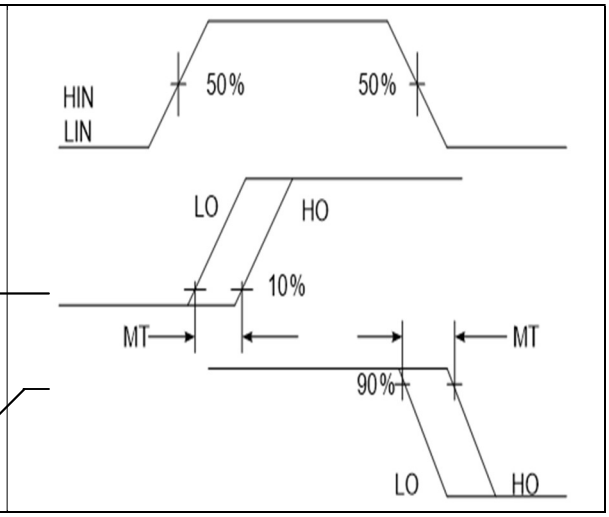


Figure 11 Delay Matching Waveform Definitions

The 6ED2742S01Q is designed with propagation delay matching circuitry. With this feature, the IC's response at the output to a signal at the input requires approximately the same time duration (i.e., tON, tOFF) for both the low-side channels and the high-side channels; the maximum

difference is specified by the delay matching parameter (MT). The propagation turn-on delay (t_{ON}) of the 6ED2742S01Qis matched to the propagation turn-on delay (t_{OFF}).

5.5 Input logic compatibility

The input pins of are based on a TTL and CMOS compatible input-threshold logic that is independent of the Vcc supply voltage. With typical high threshold (V_{IH}) of 2.0 V and typical low threshold (V_{IL}) of 0.8 V, along with very little temperature variation as summarized in Figure 12, the input pins are conveniently driven with logic level PWM control signals derived from 3.3 V and 5 V digital power-controller devices. Wider hysteresis (typically 0.8 V) offers enhanced noise immunity compared to traditional TTL logic implementations, where the hysteresis is typically less than 0.5 V. 6ED2742S01Q also features tight control of the input pin threshold voltage levels which eases system design considerations and ensures stable operation across temperature. The 6ED2742S01Q features floating input protection wherein if any of the input pin is left floating, the output of the corresponding stage is held in the low state. This is achieved using pull-down resistors on all the input pins (HIN, LIN) as shown in the block diagram. The 6ED2742S01Q has input pins that are capable of sustaining voltages higher than the bias voltage applied on the Vcc pin of the device.

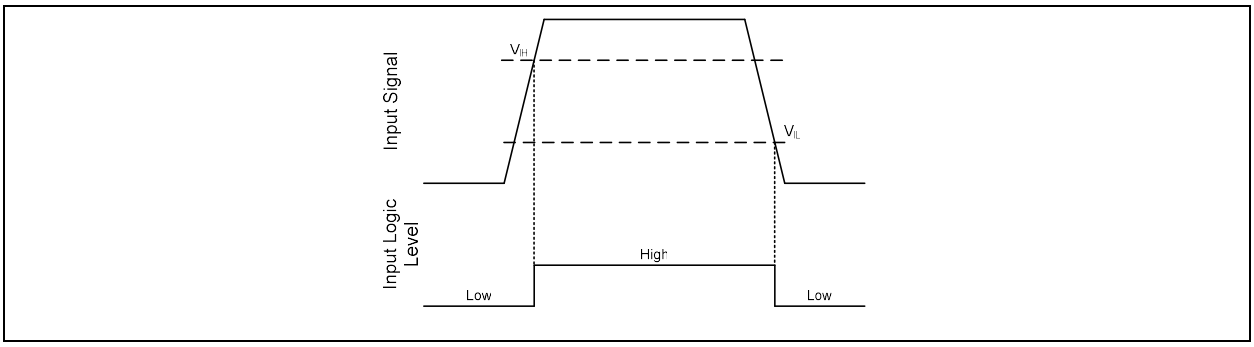


Figure 12 HIN & LIN input thresholds

5.6 Undervoltage lockout

This IC provides undervoltage lockout protection on both the V_{CC} (logic and low-side circuitry) power supply and the V_{BS} (high-side circuitry) power supply. Figure 13 is used to illustrate this concept; V_{CC} (or V_{BS}) is plotted over time and as the waveform crosses the UVLO threshold ($V_{CC\ UVLO+/-}$ or $V_{BSUVLO+/-}$) the undervoltage protection is enabled or disabled.
Upon power-up, should the VCC voltage fail to reach the VCC_{UV+} threshold, the IC won't turn-on. Additionally, if the VCC voltage decreases below the VCC_{UV-} threshold during operation, the undervoltage lockout circuitry will recognize a fault condition and shutdown the high and low-side gate drive outputs.
Upon power-up, should the V_{BS} voltage fail to reach the V_{BSUV+} threshold, the IC won't turn-on. Additionally, if the V_{BS} voltage decreases below the $V_{BSUVLO-}$ threshold during operation, the undervoltage lockout circuitry will recognize a fault condition, and shutdown the high-side gate drive outputs of the IC.

The UVLO protection ensures that the IC drives the external power devices only when the gate supply voltage is sufficient to fully enhance the power devices. Without this feature, the gates of the external power switch could be driven with a low voltage, resulting in the power switch

conducting current while the channel impedance is high; this could result in very high conduction losses within the power device and could lead to power device failure.

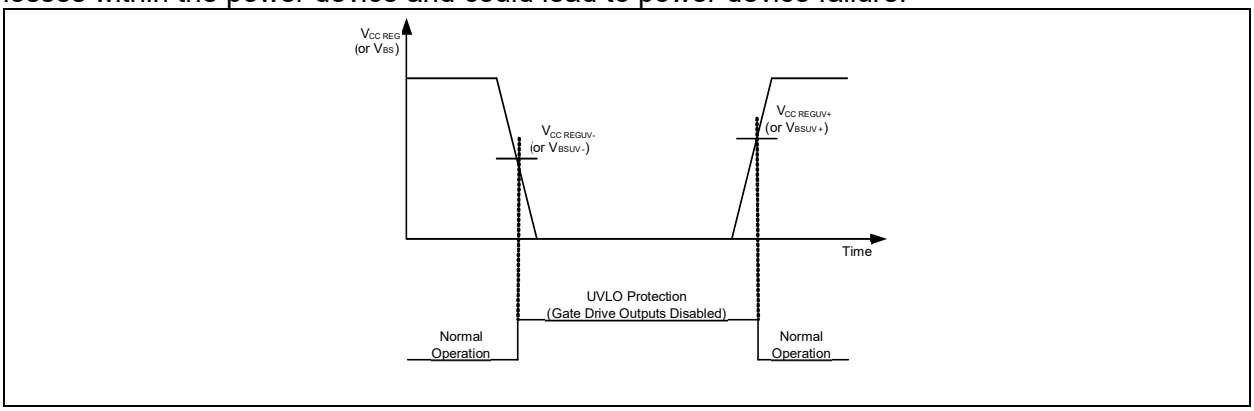


Figure 13 UVLO protection

5.7 Shoot-through protection

The 6ED2742S01Q is equipped with shoot-through protection circuitry (also known as cross-conduction prevention circuitry). Figure 14 shows how this protection circuitry prevents both the high- and low-side switches from conducting at the same time.

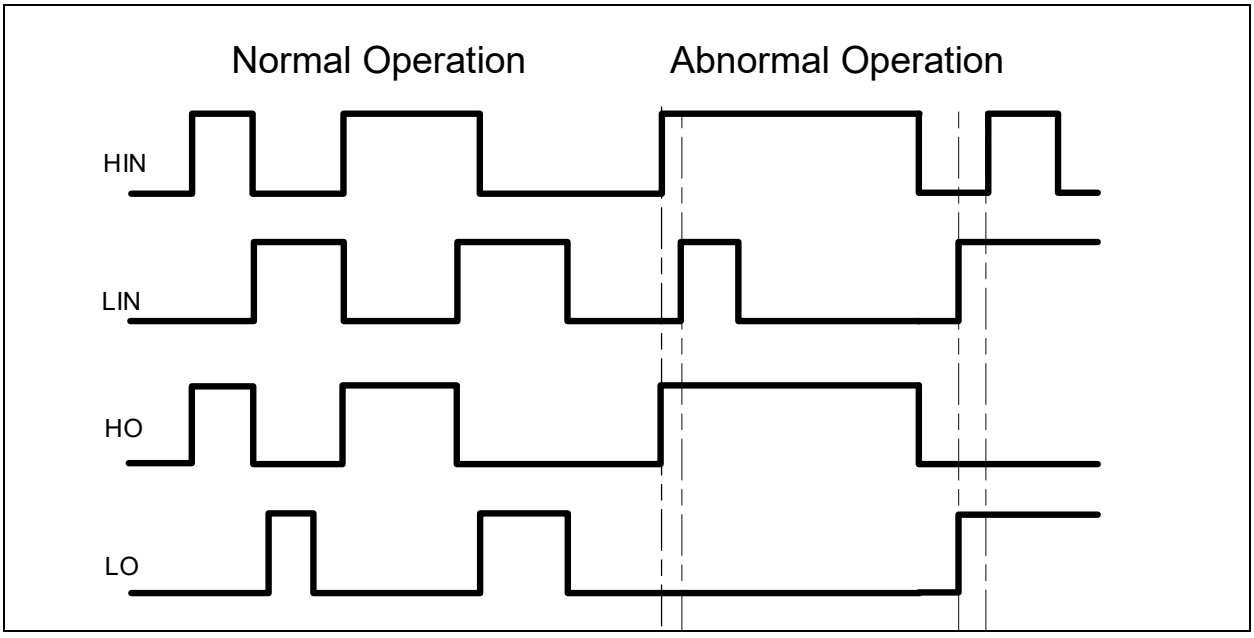


Figure 14 Illustration of shoot-through protection circuitry

5.8 Enable, Fault reporting and programmable fault clear timer

The 6ED2742S01Q provides an enable functionality that allows it to shutdown or enable the HVIC and also provides an integrated fault reporting output along with an adjustable fault clear timer. There are two situations that would cause the IC to report a fault via the RFE pin. The first is an undervoltage condition of VCC and the second is if the over-current feature has recognized a

fault. Once the fault condition occurs, the RFE pin is internally pulled to VSS and the fault clear timer is activated. The RFE output stays in the low state until the fault condition has been removed and the fault clear timer expires; once the fault clear timer expires, the voltage on the RFE pin will return to its external pull-up voltage.

The length of the fault clear time period (t_{FLTCLR}) is determined by exponential charging characteristics of the capacitor where the time constant is set by R_{RFE} and C_{RFE}. Figure 15 shows that R_{RFE} is connected between the external supply (V_{DD}) and the RFE pin, while C_{RFE} is placed between the RFE and VSS pins.

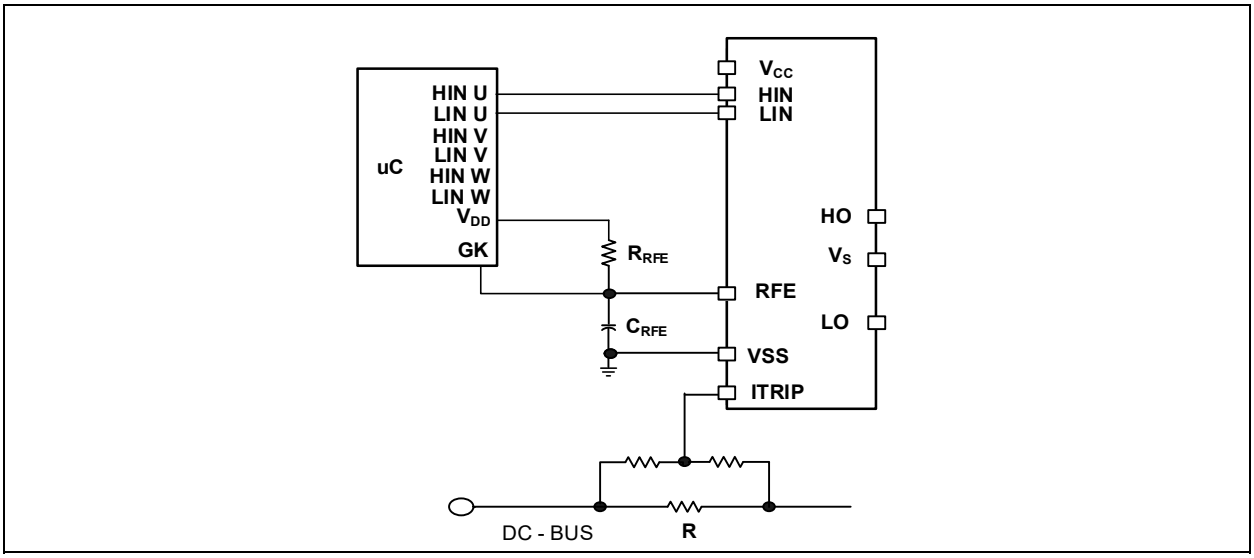


Figure 15 Programming the fault clear timer

The design guidelines for this network are shown in Table 6

Table 6 Design guidelines

C_{RFE}	≤1 nF
	Ceramic
R_{RFE}	0.5 MΩ to 2 MΩ
	>> $R_{ON, RCIN}$

The length of the fault clear time period can be determined by using the formula below.

$v_C(t) = V_{f*}(1-e^{-t/RC})$

$t_{FLTCLR} = -(R_{RFE*}C_{RFE}) *\ln (1-V_{RFE+}/V_{DD}) + 100ns$

The voltage on the RFE pin should not exceed the VDD of the uC power supply.

5.9 Over-current protection

The 6ED2742S01Q is equipped with an over-current feature in addition to the stand-alone Current Sense Amplifier (CSA). This functionality can sense over-current events in the DC- bus. Once the IC detects an over-current event, the outputs are shutdown, and RFE is pulled to VSS.

The level of current at which the over-current protection (OCP) is initiated is determined by the shunt resistor connected between COM pin and VSS pin as shown in Figure 16, and by the threshold configured by ITRIP CONF pin (V_{ITRIP+}). The circuit designer will need to determine the maximum allowable level of current in the DC- bus and select R_0 and V_{ITRIP+}.

$V_{ITRIP+} = R_0 \times I_{DC-}$

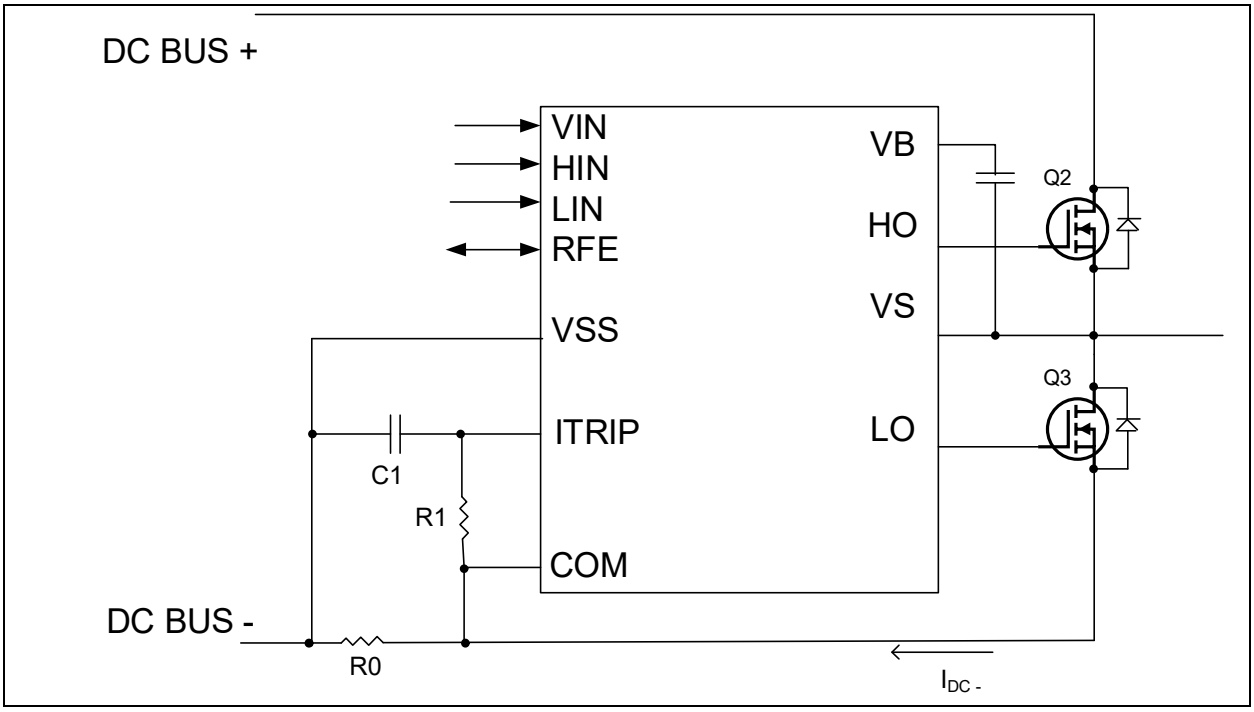


Figure 16 Programming the over-current protection

For example, a typical value for resistor R_0 could be 10 mΩ.

5.10 Current sense operational amplifier

A current sense operational amplifier (CSA) with configurable gain is integrated in the gate driver sensing the voltage between VSS and COM pins. The amplifier has a strobe input signal. When strobe signal is LOW the operational amplifier output signal CSO is following the VSS-COM voltage multiplied by a certain gain, when strobe signal is HIGH CSO signal is reporting the op amp offset. CSO output has an offset added above VSS of 150 mV. This offset ensures the measured current remains positive and does not go negative in any regular operating conditions.

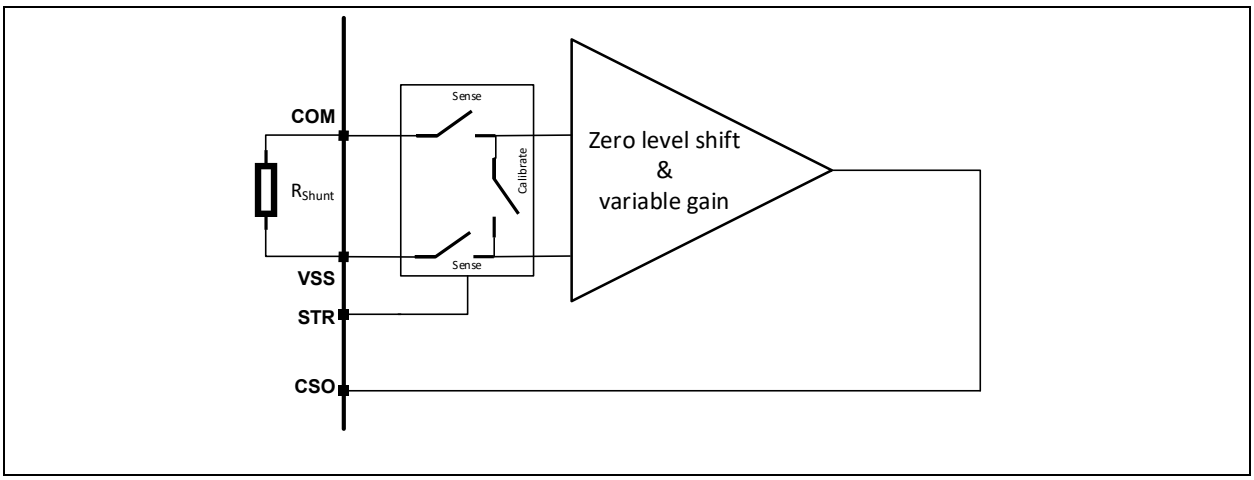


Figure 17 Current sense operational amplifier

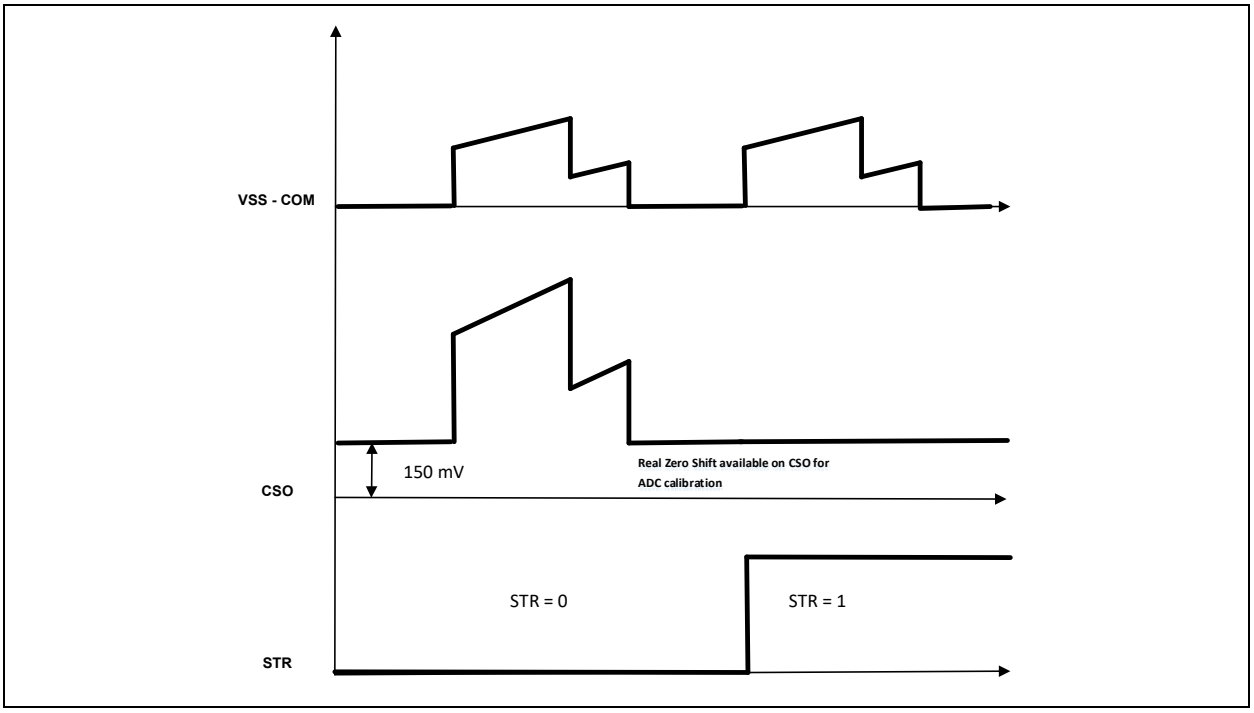


Figure 18 Current sense operational amplifier timing diagram

5.11 Gain settings for the over current protection (ITRIP_Conf) and current sense operational amplifier (CSO)

The gain for the over current protection via ITRIP and current sense operation amplifier output can be set using a simple potential divider network as shown in below figure 19.

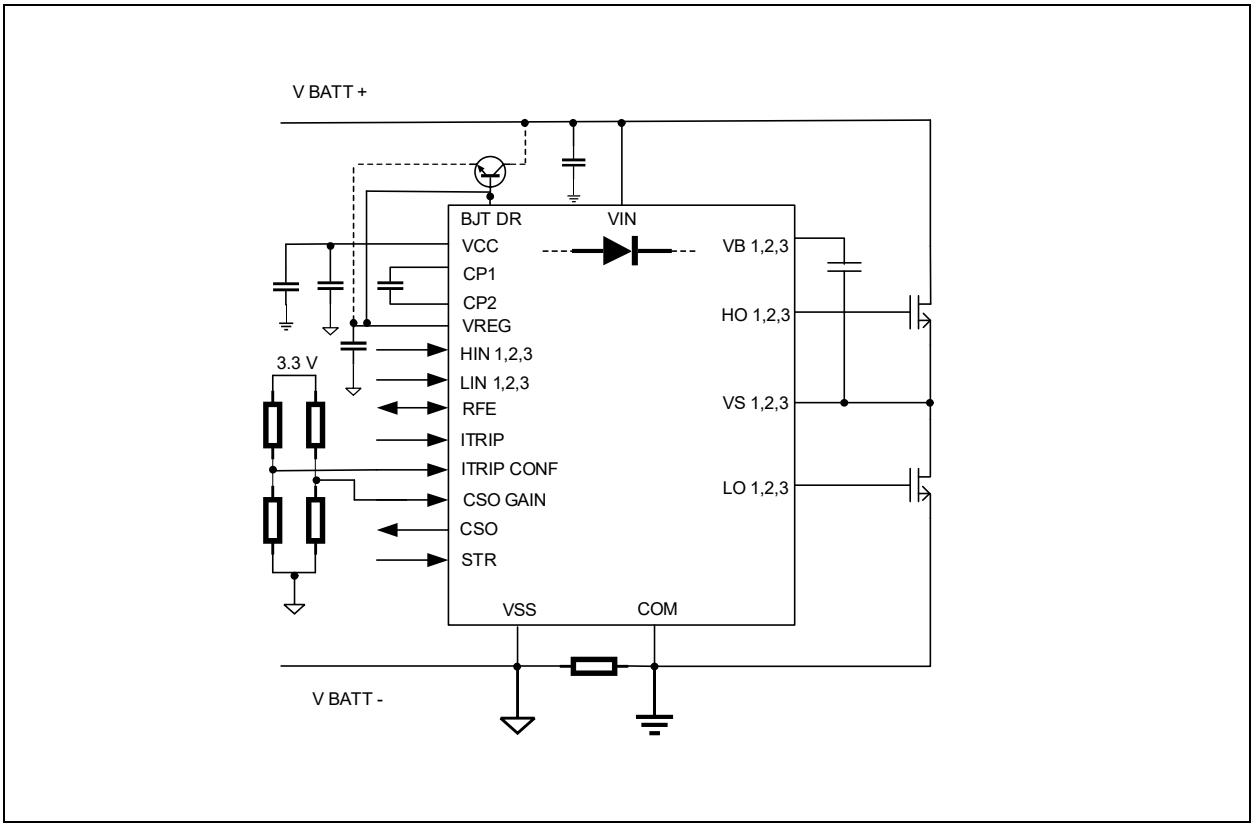


Figure 19 Setting over current protection (ITRIP) gain and current sense operational amplifier gain via the resistor divider

The voltage of the potential divider network can be scaled down from an external 3.3 V. It should be noted that when powering from external 3.3 V the supply sequencing should be such that the 6ED2742 is first powered up via VIN before applying the 3.3 V to the Gain / Config pins. Two use cases are shown in figure 20. Figure “a” shows the option where the 3.3 V input is either ramped up after or along with VIN / VCC. RFE gets asserted (IC gets enabled) after the UVLO of VCC is crossed and V_{RFE+} threshold is crossed. Figure” b” shows use case when the 3.3 V input is already available before VIN / VCC arrive. In this case, RFE gets asserted when the UVLO of VCC is crossed. It is good to note that the RFE pin is held low under two conditions:

a. Under Voltage Lock Out (UVLO) of VCC / V_{RFE}

b. ITRIP threshold as set by ITRIP Config is crossed

In case the 3.3 V arrives before VCC toggling(pulling down and the pulling up) the RFE will re-read the values of ITRIP config and CSO Gain.

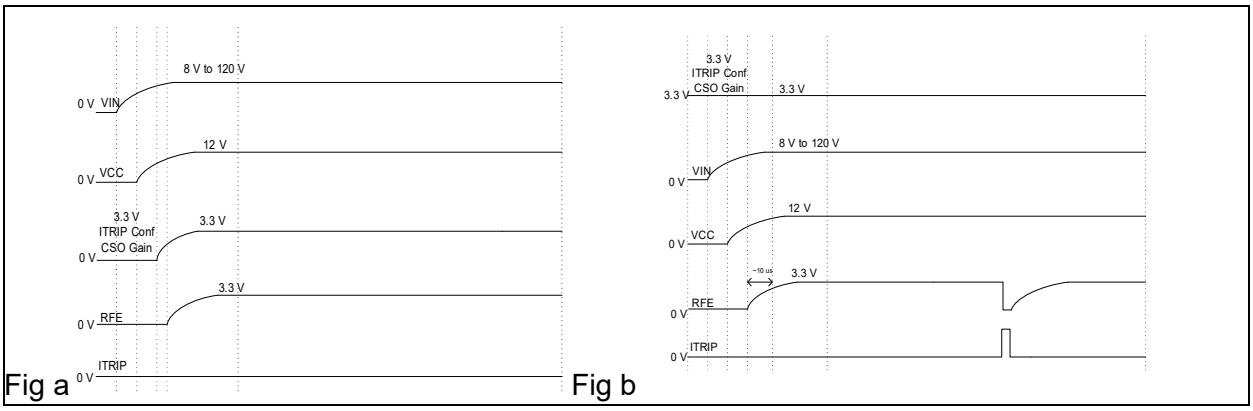


Figure 20 Input voltage sequencing for setting up different gain and ITRIP config

The voltage limits for different gains are as shown in the electrical characterisitics table 3 in page 6 and 7. They are summarized as beow in Table 7 and 8

Table 7 ITRIP Config pin voltage settings for different overcurrent threshold voltages

V_{ITRIP}	Over current threshold voltage	950	1000	1050	mV	**ITRIP Conf > 3 V**
		475	500	525		**1.5V < ITRIP Conf < 2V**
		225	250	275		**0.5V < ITRIP Conf < 1V**
		110	130	150		**ITRIP Conf < 0.25V**

Table 8 CSO gain pin voltage settings for different gain of CSO output

G_{CSO}	Current sense amplifier gain	36	40	41	V/V	**CSO gain > 3 V**
		18	20	21		**1.5V < CSO gain< 2V**
		9	10	11		**0.5V < CSO gain < 1V**
		4	5	6		**CSO gain < 0.25V**

5.12 Advanced input filter

The advanced input filter allows an improvement in the input/output pulse symmetry of the HVIC and helps to reject noise spikes and short pulses. This input filter has been applied to the HIN and LIN inputs.

Figure 19 shows a typical input filter and the asymmetry of the input and output. The upper pair of waveforms (Example 1) show an input signal with a duration much longer then $t_{FIL,IN}$; the

resulting output is approximately the difference between the input signal and $t_{FIL,IN}$. The lower pair of waveforms (Example 2) show an input signal with a duration slightly longer then $t_{FIL,IN}$; the resulting output is approximately the difference between the input signal and $t_{FIL,IN}$.

Figure 20 shows the advanced input filter and the symmetry between the input and output. The upper pair of waveforms (Example 1) show an input signal with a duration much longer then $t_{FIL,IN}$; the resulting output is approximately the same duration as the input signal. The lower pair of waveforms (Example 2) show an input signal with a duration slightly longer then $t_{FIL,IN}$; the resulting output is approximately the same duration as the input signal.

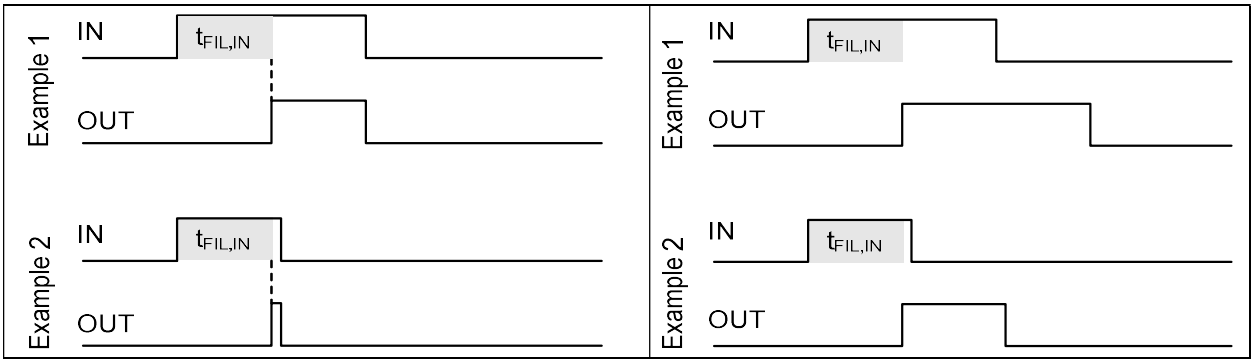


Figure 21 Typical input filter

Figure 22 Advanced input filter

5.13 Short-Pulse / Noise rejection filters

This device's input filter provides protection against short-pulses (e.g., noise) on the input lines. If the duration of the input signal is less than $t_{FIL,IN}$, the output will not change states. Example 1 of Figure 21 shows the input and output in the low state with positive noise spikes of durations less than $t_{FIL,IN}$; the output does not change states. Example 2 of Figure 21 shows the input and output in the high state with negative noise spikes of durations less than $t_{FIL,IN}$; the output does not change states.

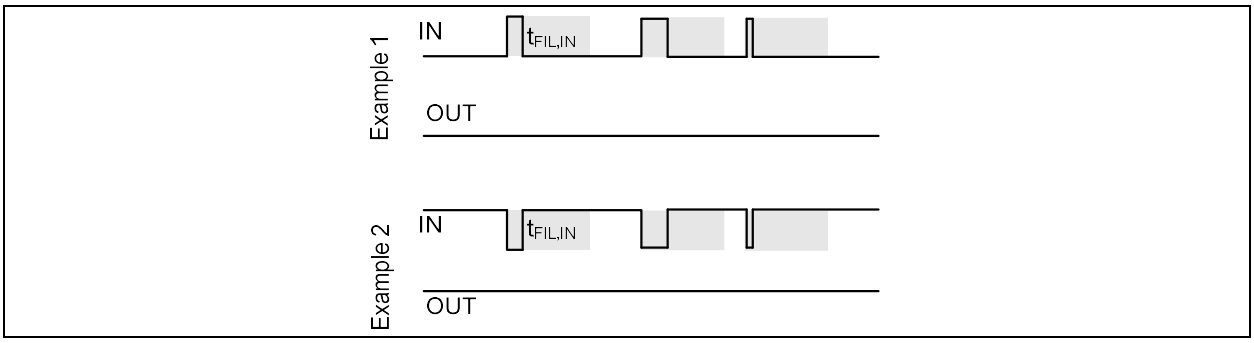


Figure 23 Noise rejecting input filters

5.14 Power Management Unit (PMU)

The integrated power management unit enables the gate driver to operate across a wide range of input voltages without requiring and external VCC supply. For some applications requiring higher VCC voltages above 12 V, such as 15 V, the driver can also be driven with an external VCC voltage supply.

Four possible configurations are as shown in Figure 22 to Figure 25. The four different configurations support different values of I_{CP_AVG} from the Power Management Unit (PMU) depending on the input voltage range and whether an external BJT is used to enable higher power and voltage operation.

5.14.1 Internal linear pre-regulator

A linear pre-regulated circuit with the charge pump supplies a voltage of approximately 12 V to VCC via the VIN voltage. This regulated VCC voltage is used for the low-side gate drive supply as well as for the high-side gate driver circuit supplied through the integrated bootstrap diodes and external bootstrap capacitors.

5.14.2 Internal charge pump

Depending on the configuration and setup, the 6ED2742S01Q can provide a gate drive voltage (VCC) of 12 V, even if the input supply voltage drops as low as 8 V. This gate drive voltage is generated by an internal charge pump, which requires an external capacitor. The charge pump requires external capacitors between CP1 and CP2 and from VREG to ground.

The charge pump flying capacitor between CP1 and CP2 should have a capacitance of 10nF. The capacitor must be rated to withstand the maximum VIN power supply voltage. An X7R or X5R ceramic capacitor is recommended. With a 10nF capacitor, internal charge pump can output approximately 10 mA when VIN is 6 V.

5.14.3 Config #1 - Charge pump only: V_{BATT} connected directly to VREG

Configuration #1 provides the smallest form factor and highest efficiency operating mode for input voltages from 12 V to 18 V. This configuration would be typically used for 12 V nominal battery voltage power tools.

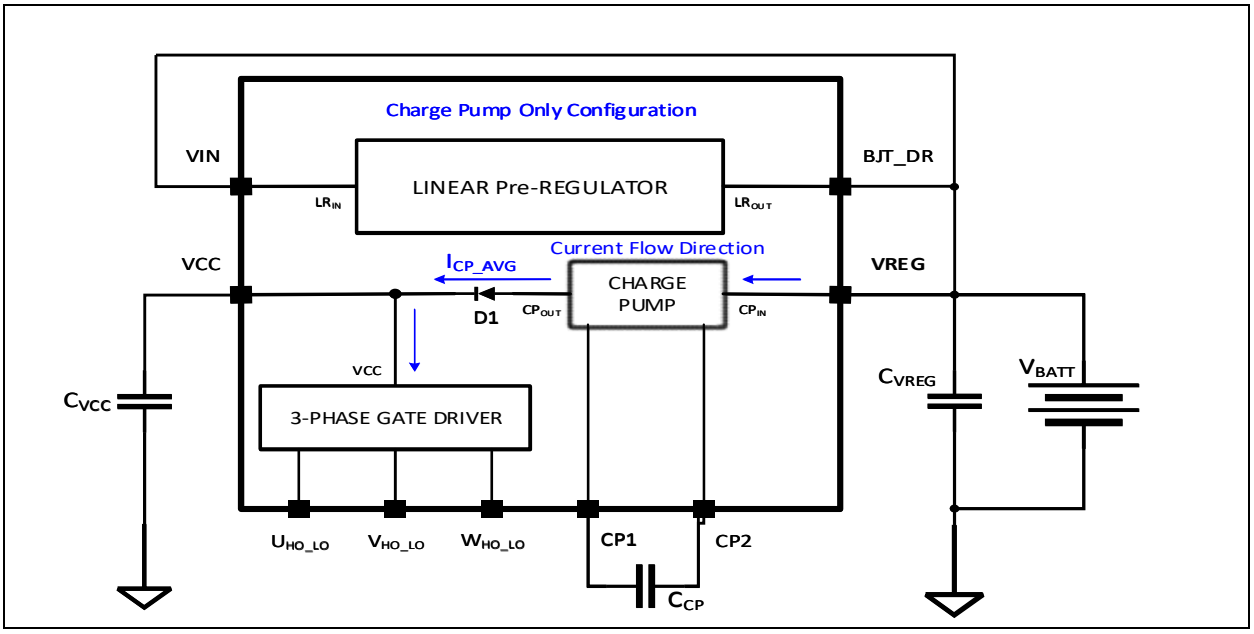
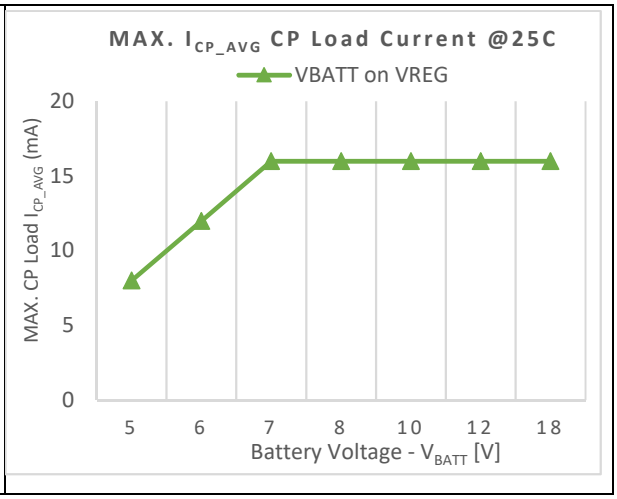


Figure 24 Typical configuration for 8.4 V to 18 V applications

Table 9 Charge pump only operating conditions (typical)

VREG[1] = V_{BATT} (V)	VCC (V)	I_{CP_AVG} Max. (mA @ 25 °C)
18	12	15
12	12	15
8	12	10
7	11	10
6	10	10

Note 1: Maximum absolute VREG voltage = 20V (including transients)



Please note that for configuration #1, there is an optimal operating range that strongly depends on the supplied input voltage to the VREG pin. Exceeding 20V input to the VREG pin may permanently damage the device.

5.14.4 Config #2 - Pre-regulator / charge pump: V_{BATT} connected to VIN

Configuration #2 provides wider input voltage flexibility with the smallest form factor since an external BJT is not used. Typical input voltage range operation up to 96 V is possible.

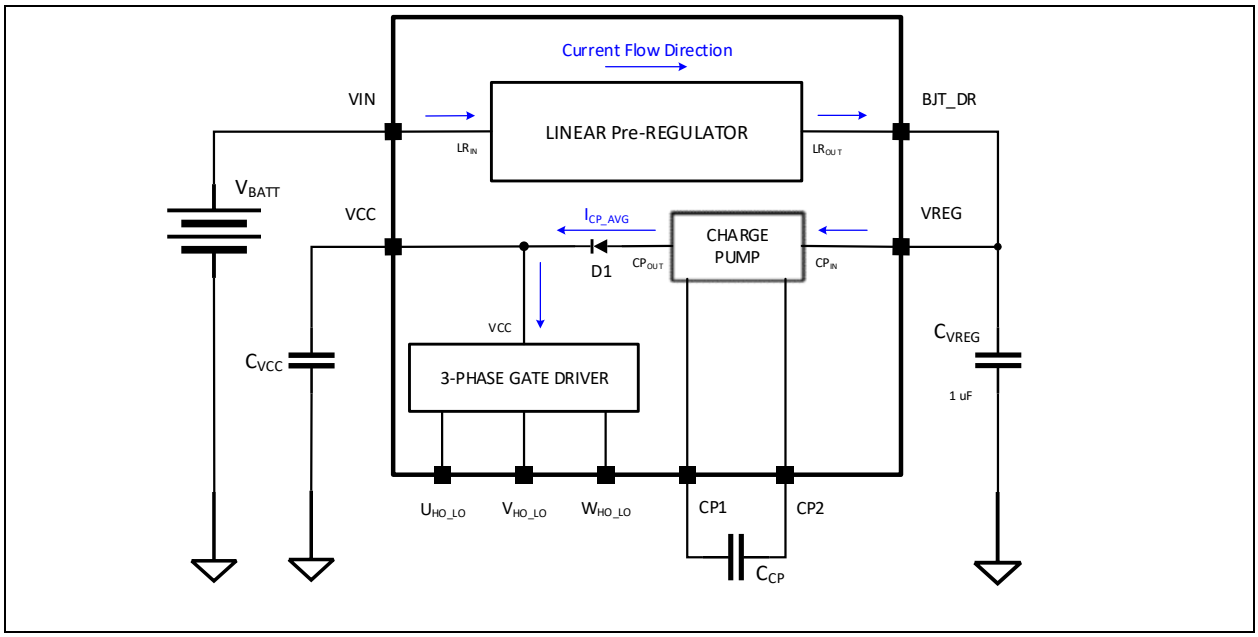
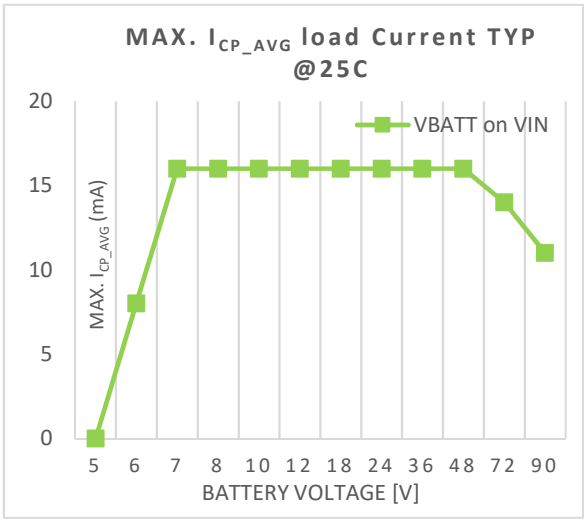


Figure 25 Typical configuration for 12 V to 90 V applications

Table 10 Charge pump only operating conditions (typical)

V_{BATT} = VIN (V)	BJT_DR = VREG (V)	VCC ()	I_{CP_AVG} Max. (mA @ 25 °C)
90	15.5	12	11
72			14
60			15
48			
36			
24			
12	10.5		
9	7.5		



5.14.5 Config #3: V_{BATT} connected to VIN and external BJT

Configuration #3 provides the widest input voltage range with the addition of an external NPN BJT to share the power dissipation between the internal PMU blocks and BJT.

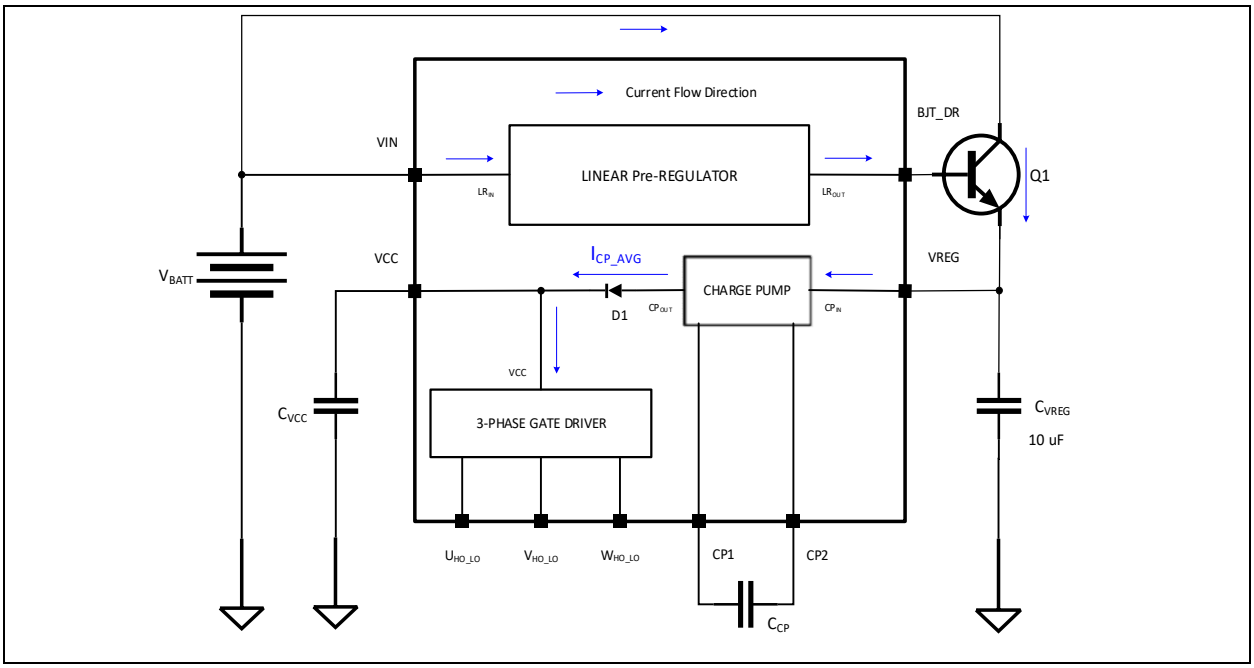


Figure 26 Typical configuration for VIN > 60 V_{DC} applications. For stability reasons VREG capacitor needs to be 10 uF in this configuration

Table 11 Pre-regulator, Charge pump, external BJT operating conditions (typ – 25°C)

VIN (V)	BJT_DR (V)	VREG (V)	VCC (V)
120	16.5	15.5	12
90			
80			
36			
24			
18		14.5	
12	10.5	9.5	
8	6.7	5.7	10

Typical input voltage range recommended is up to 120 V. I_{CP_AVG} of 15 mA for VIN operating range of 10 V - 120 V.

5.14.6 Config #4: Direct External VCC drive

An external VCC power supply (< 18 V) can be connected to the VCC pin to power the gate driver circuit directly with a voltage greater than 12 V (eg. 15V). This can be useful for applications where the MOSFET is driven with a gate voltage greater than 12 V.

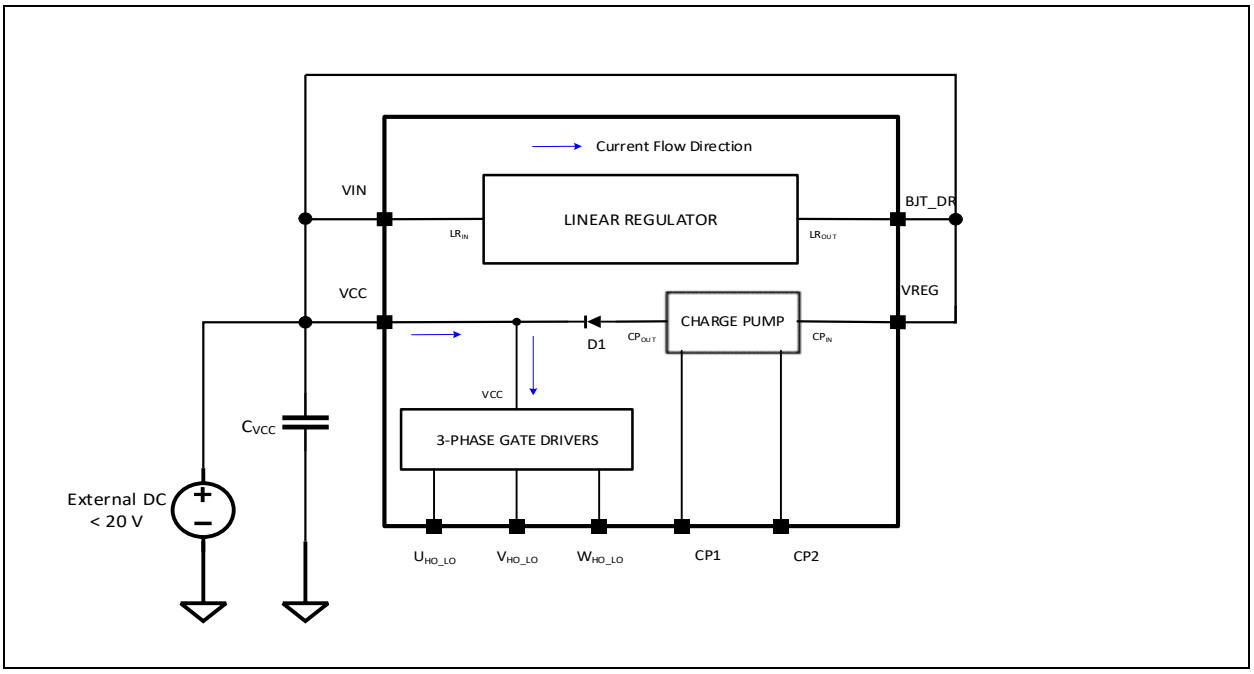


Figure 27 Typical configuration for direct gate drive using an external VCC power supply

5.15 Bootstrap diode

An ultra-fast bootstrap diode is monolithically integrated for establishing the high side supply. The differential resistor of the diode helps to avoid extremely high inrush currents when initially charging the bootstrap capacitor. The integrated diode with its low ohmic resistance helps save cost and improve reliability by reducing external components as shown below figure 26.

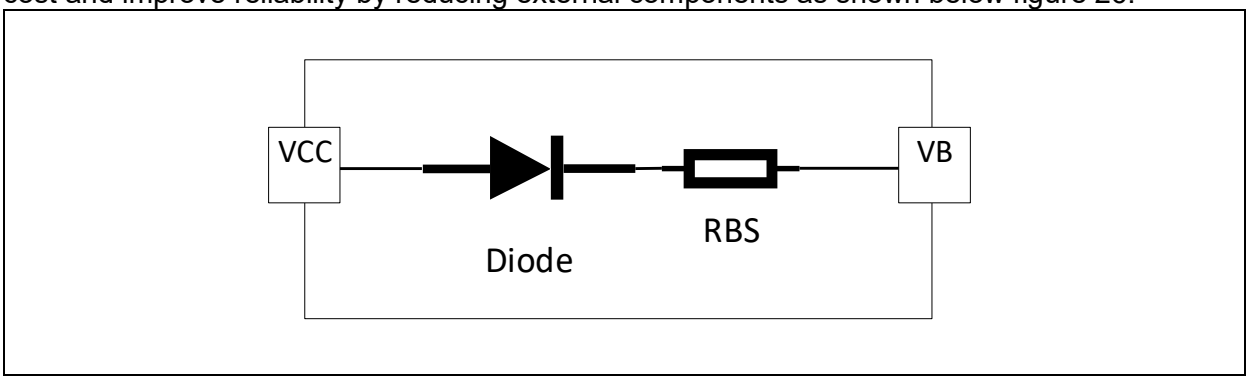


Figure 28 6ED2742S01Q with integrated components

The low ohmic current limiting resistor (typically 38 Ω) provides essential advantages over other competitor devices with high ohmic bootstrap structures. A low ohmic resistor such as in the 6ED2742S01Q allows faster recharging of the bootstrap capacitor during periods of small duty cycles on the low side transistor. The bootstrap diode is usable for all kind power electronic converters. The bootstrap diode is a real uni-directional PN-diode and is temperature robust. It can be used at high temperatures with a low duty cycle of the low side transistor.

The bootstrap diode of the 6ED2742S01Q works with all control algorithms of modern power electronics, such as trapezoidal or sinusoidal motor drives control.

5.16 Internal trickle charge pumps – 100% duty cycle operation

External bootstrap capacitors are charged to VCC via the integrated bootstrap diodes when the lowside MOSFET (LS-FET) is turned on. This charge is then used to drive the high-side MOSFET (HS-FET) gate when it is turned on.

To keep the bootstrap capacitors charged and allow for operation at 100% duty cycle, internal trickle charge pumps for each high side well supply a small current to overcome leakages that would discharge the bootstrap capacitors.

Bootstrap capacitor charging and its optimal value are explained in the subsequent sections.

5.17 Calculating the bootstrap capacitance C_{BS}

Bootstrapping is a common method of pumping charges from a low potential to a higher one. With this technique a supply voltage for the floating high side sections of the gate drive can be easily established according to Figure 27. This method has the advantage of being simple and low cost but may force some limitations on duty-cycle and on-time since they are limited by the requirement to refresh the charge in the bootstrap capacitor. Proper capacitor choice can reduce drastically these limitations.

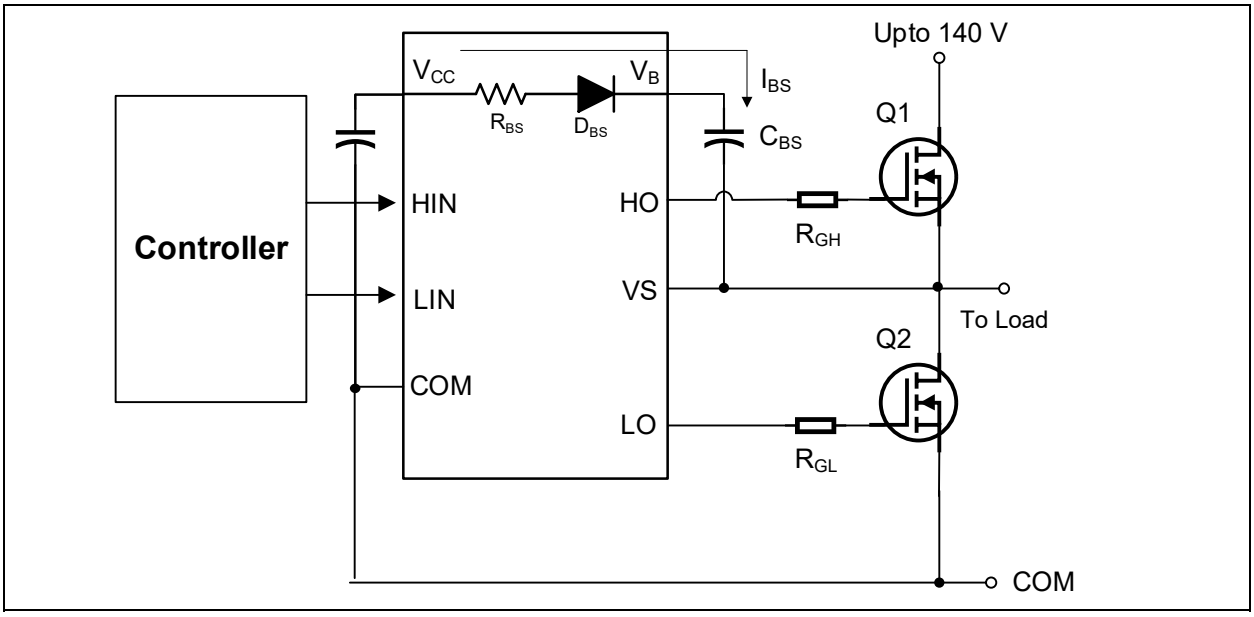


Figure 29 Half bridge bootstrap circuit in 6ED2742S01Q

When the low side MOSFET turns on, it will force the potential of pin V_S to GND. The existing difference between the voltage of the bootstrap capacitor V_{CBS} and VCC results in a charging

current I_{BS} into the capacitor C_{BS}. The current I_{BS} is a pulse current and therefore the ESR of the capacitor C_{BS} must be very small in order to avoid losses in the capacitor that result in lower lifetime of the capacitor. This pin is on high potential again after low side is turned off and high side is conducting current. But now the bootstrap diode D_{BS} blocks a reverse current, so that the charges on the capacitor cannot flow back to the capacitor C_{VCC}. The bootstrap diode D_{BS} also takes over the blocking voltage between pin V_B and VCC. The voltage of the bootstrap capacitor can now supply the high side gate drive sections. It is a general design rule for the location of bootstrap capacitors C_{BS}, that they must be placed as close as possible to the IC. Otherwise, parasitic resistors and inductances may lead to voltage spikes, which may trigger the undervoltage lockout threshold of the individual high side driver section. However, all parts of the 6ED2742S01Q, which have the UVLO also contain a filter at each supply section in order to actively avoid such undesired UVLO triggers.

The current limiting resistor R_{BS} according to Figure 27 reduces the peak of the pulse current during the low side MOSFET turn-on. The pulse current will occur at each turn-on of the low side MOSFET, so that with increasing switching frequency, the capacitor C_{BS} is charged more frequently. Therefore, a smaller capacitor is suitable at higher switching frequencies. The bootstrap capacitor is mainly discharged by two effects: the high side quiescent current and gate charge of the high side MOSFET to be turned on.

The minimum size of the bootstrap capacitor is given by

$$C_{BS} = \frac{Q_{GTOT}}{\Delta V_{BS}}$$

ΔV_{BS} is the maximum allowable voltage drop at the bootstrap capacitor within a switching period, typically 1 V. It is recommended to keep the voltage drop below the undervoltage lockout (UVLO) of the high side and limit

$$\Delta V_{BS} \leq (VCC - V_F - V_{GSmin} - V_{DSon})$$

$V_{GSmin} > V_{BSUV-}$, V_{GSmin} is the minimum gate source voltage we want to maintain and V_{BSUV-} is the high-side supply undervoltage negative threshold.

VCC is the IC voltage supply, V_F is bootstrapdiode forward voltage and V_{DSon} is drain-source voltage of low side MOSFET.

Please note, that the value Q_{GTOT} may vary to a maximum value based on different factors as explained below and the capacitor shows voltage dependent derating behavior of its capacitance.

The influencing factors contributing V_{BS} to decrease are:

- MOSFET turn on required Gate charge (Q_G)
- MOSFET gate-source leakage current (I_{LK_GS})
- Floating section quiescent current (I_{QBS})
- Floating section leakage current (I_{LK})
- Bootstrap diode leakage current (I_{LK_DIODE})
- Charge required by the internal level shifters (Q_{LS}): typical 1nC
- Bootstrap capacitor leakage current (I_{LK_CAP})
- High side on time (T_{HON})

Considering the above,

$$Q_{GTOT} = Q_G + Q_{LS} + \left(I_{QBS} + I_{LK_{GS}} + I_{LK} + I_{LK_{DIODE}} + I_{LK_{CAP}}\right) * T_{HON}$$

I_{LK_CAP} is only relevant when using an electrolytic capacitor and can be ignored if other types of capacitors are used. It is strongly recommend using at least one low ESR ceramic capacitor (paralleling electrolytic capacitor and low ESR ceramic capacitor may result in an efficient solution).

The above C_{BS} equation is valid for pulse by pulse considerations. It is easy to see, that higher capacitance values are needed, when operating continuously at small duty cycles of low side. The recommended bootstrap capacitance is therefore in the range up to 4.7 µF for most switching frequencies. The performance of the integrated bootstrap diode supports the requirement for small bootstrap capacitances.

5.18 PCB layout tips

Distance between high and low voltage components: It's strongly recommended to place the components tied to the floating voltage pins (V_B and V_S) near the respective high voltage portions of the device. Please see the Case Outline information in this datasheet for the details.

Ground Plane: In order to minimize noise coupling, the ground plane should not be placed under or near the high voltage floating side.

Gate Drive Loops: Current loops behave like antennas and are able to receive and transmit EM noise (see Figure 29). In order to reduce the EM coupling and improve the power switch turn on/off performance, the gate drive loops must be reduced as much as possible. Moreover, current can be injected inside the gate drive loop via the MOSFET collector-to-gate parasitic capacitance. The parasitic auto-inductance of the gate loop contributes to developing a voltage across the gate-emitter, thus increasing the possibility of a self turn-on effect.

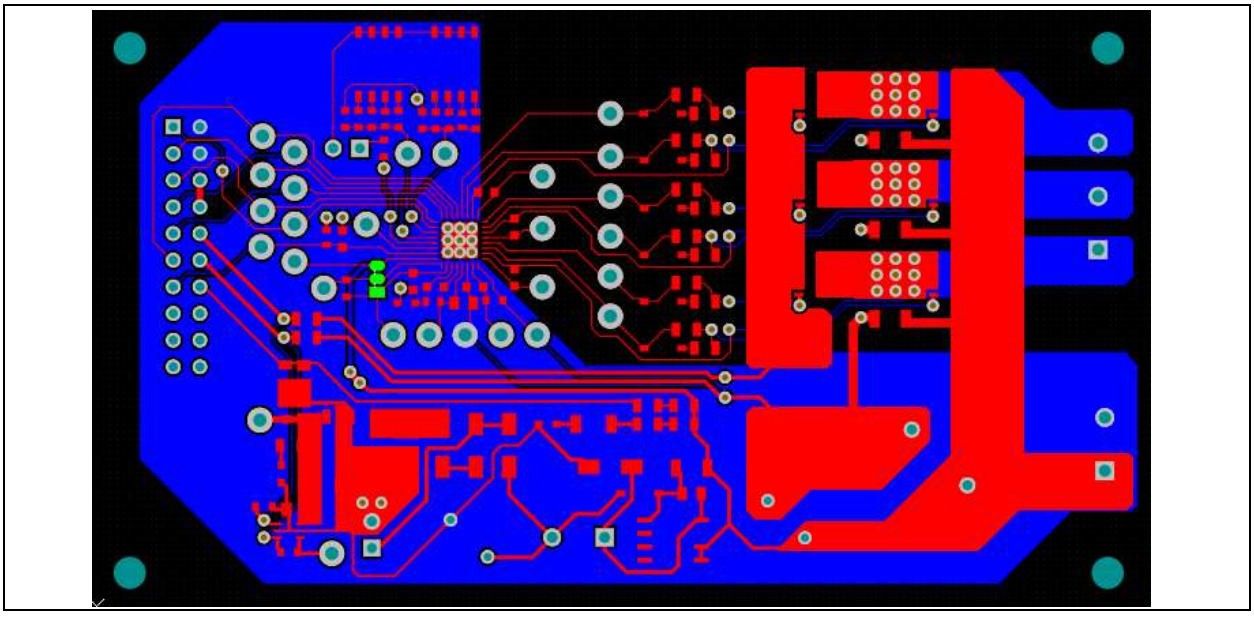


Figure 30 Optimal layout of 6ED2742 driving three phases of OptiMOS™ MOSFETs

Supply Capacitor: It is recommended to place a bypass capacitor (C_{IN}) between the VCC and COM pins. A ceramic 1µF ceramic capacitor is suitable for most applications. This component should be placed as close as possible to the pins in order to reduce parasitic elements.

Routing and Placement: Power stage PCB parasitic elements can contribute to large negative voltage transients at the switch node; it is recommended to limit the phase voltage negative transients. See figure 30 for optimal placement of components. Ceramic capacitors close to the VCC, VIN, VREG, Charge pump and VB pins.

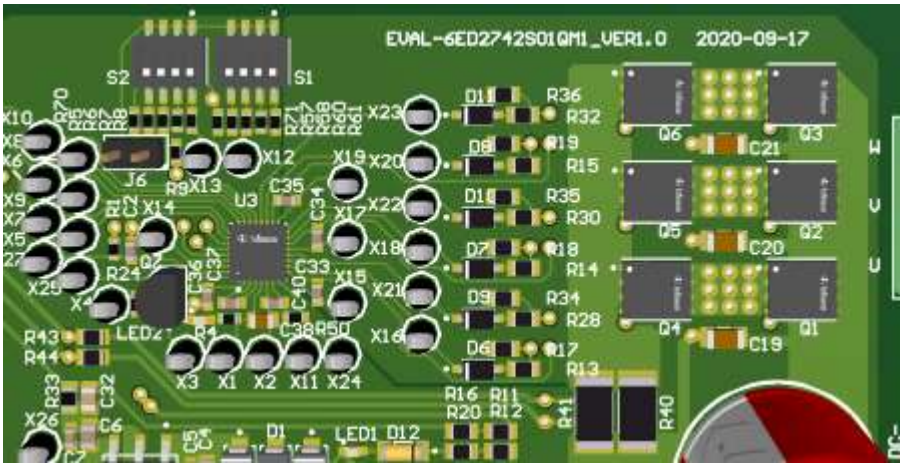


Figure 31 6ED2742S01Q and its surrounding components optimal placement

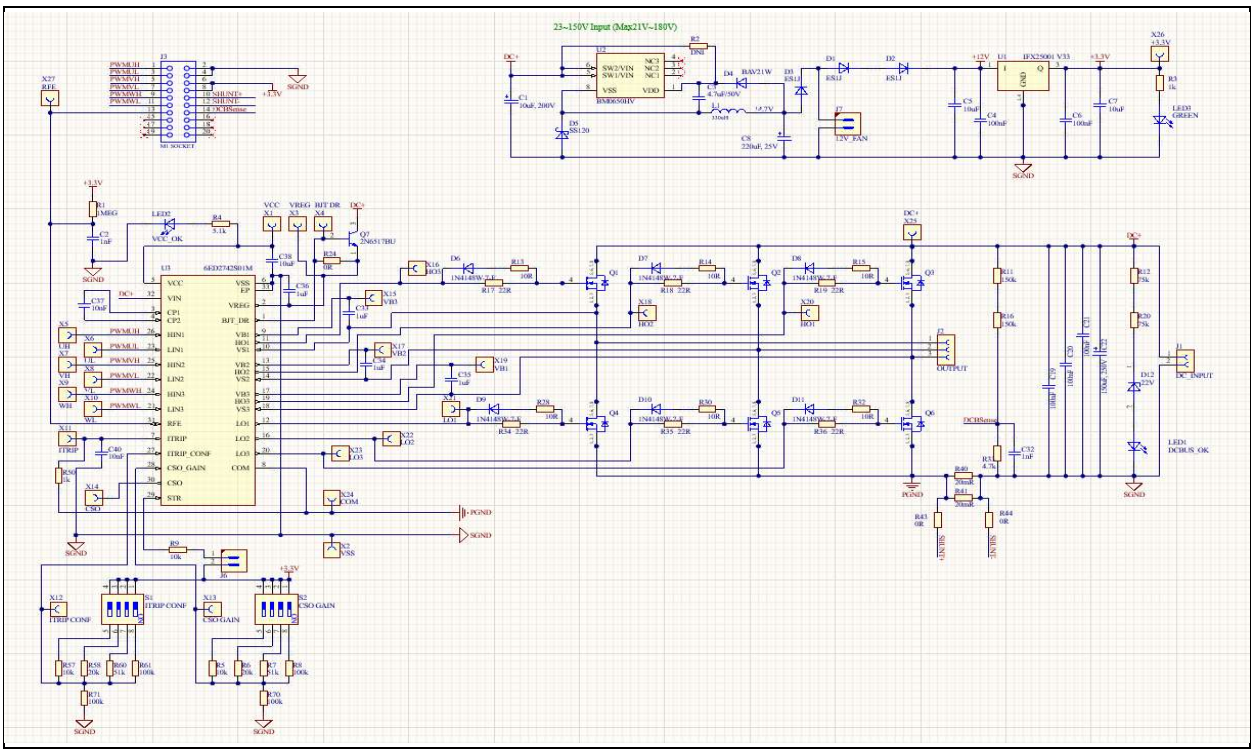


Figure 32 6ED2742S01Q 500 W demo board schematic

Qualification information[1]

Table 12 Qualification information

Qualification level		Industrial[2] Note: This family of ICs has passed JEDEC's Industrial qualification. Consumer qualification level is granted by extension of the higher Industrial level.	
Moisture sensitivity level		VQFN-32	MSL1, 260 °C (per IPC/JEDEC J-STD-020)
ESD	Charged device model	Class C3 (1.0 kV) (per JEDEC JS-002-2018)	
	Human body model	Class 2 (2 kV) (per JEDEC JS-001-2017)	
IC latch-up test		Class II Level A (per JESD78E)	
RoHS compliant		Yes	

6 Related products

Table 13

Product	Description
Gate Driver ICs	
6EDL04I06 / 6EDL04N06	600 V, 3 phase level shift thin-film SOI gate driver with integrated high speed, low $R_{DS(ON)}$ bootstrap diodes with over-current protection (OCP), 240/420 mA source/sink current drive, fault reporting, and Enable for MOSFET or MOSFET switches.
6EDL04N02PR	200 V, 3 phase level shift thin-film SOI gate driver with integrated high speed, low $R_{DS(ON)}$ bootstrap diodes with over-current protection (OCP), 240/420 mA source/sink current drive, fault reporting, and Enable for MOSFET or MOSFET switches.
iMOTION™ Controllers	
IRMCK099	iMOTION™ Motor control IC for variable speed drives utilizing sensor-less Field Oriented Control (FOC) for Permanent Magnet Synchronous Motors (PMSM).
IMC101T	High performance Motor Control IC for variable speed drives based on field oriented control (FOC) of permanent magnet synchronous motors (PMSM).

[1] Qualification standards can be found at Infineon's web site www.infineon.com
[2] Higher qualification ratings may be available should the user have such requirements. Please contact your Infineon sales representative for further information.

7 Packaging information

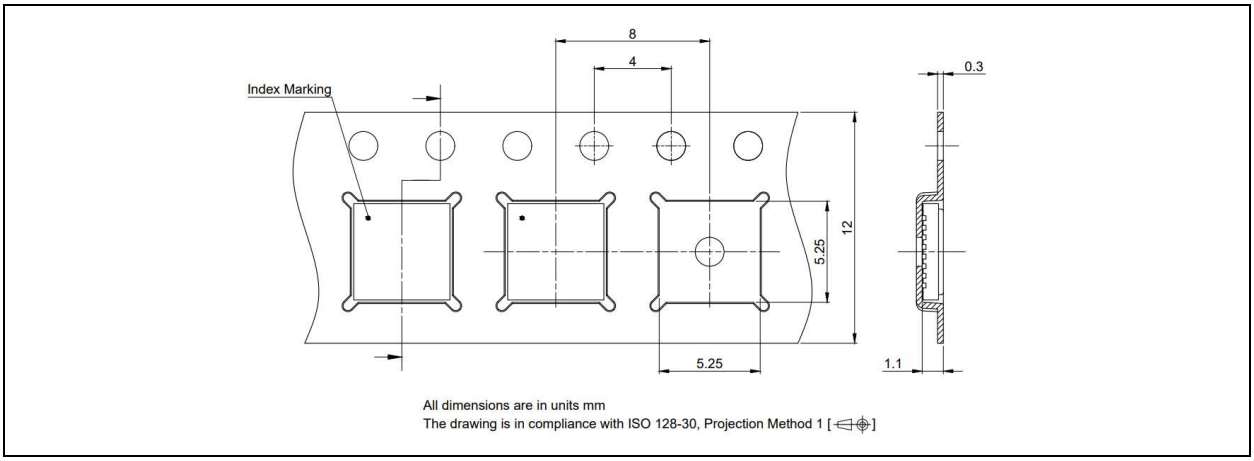


Figure 33 Target Packaging outline PG- VQFN-32-13 (6ED2742S01Q)

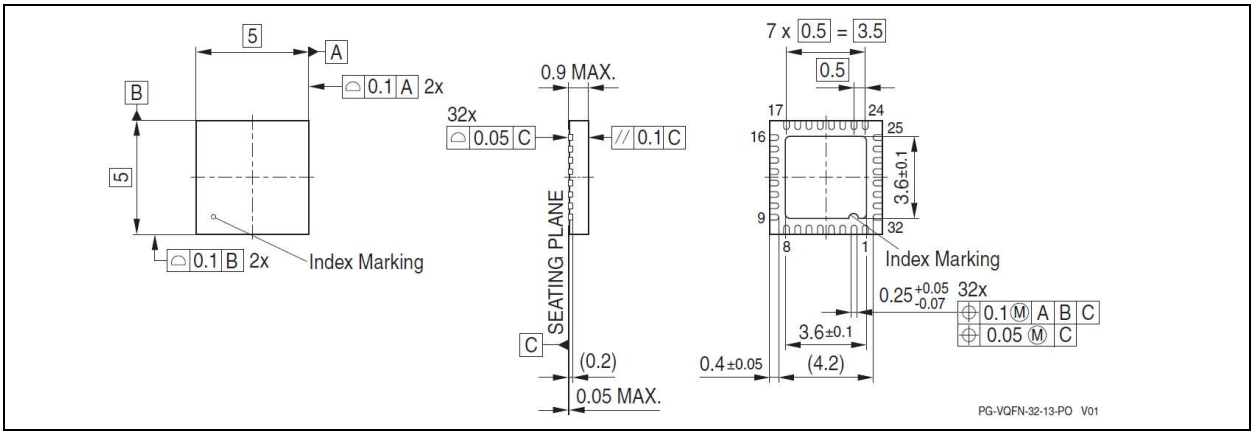


Figure 34 Target Package Dimensions PG-VQFN-32-13 (6ED2742S01Q)

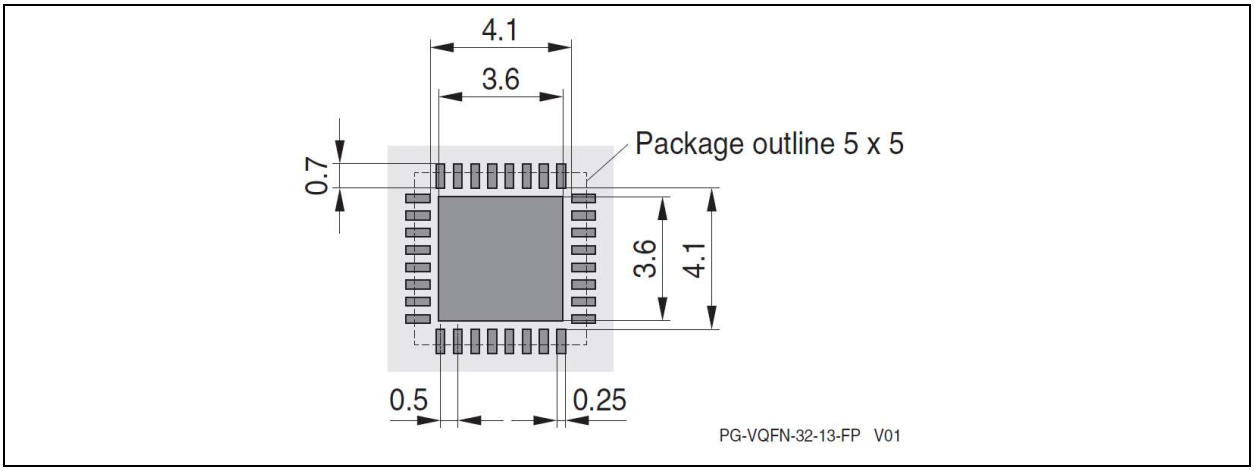


Figure 35 Recommended Footprint PG-VQFN-32-13 (6ED2742S01Q)

8 Additional documentation and resources

Several technical documents related to the use of HVICs are available at www.infineon.com; use the Site Search function and the document number to quickly locate them.

Below is a short list of some of these documents.

Application Notes:
Understanding HVIC Datasheet Specifications
HV Floating MOS-Gate Driver ICs
Use Gate Charge to Design the Gate Drive Circuit for Power MOSFETs and MOSFETs
Bootstrap Network Analysis: Focusing on the Integrated Bootstrap Functionality

Design Tips:
Using Monolithic High Voltage Gate Drivers
Alleviating High Side Latch on Problem at Power Up
Keeping the Bootstrap Capacitor Charged in Buck Converters
Managing Transients in Control IC Driven Power Stages
Simple High Side Drive Provides Fast Switching and Continuous On-Time

8.1 Infineon online forum resources

The Gate Driver Forum is live at Infineon Forums (www.infineonforums.com). This online forum is where the Infineon gate driver IC community comes to the assistance of our customers to provide technical guidance – how to use gate drivers ICs, existing and new gate driver information, application information, availability of demo boards, online training materials for over 500 gate driver ICs. The Gate Driver Forum also serves as a repository of FAQs where the user can review solutions to common or specific issues faced in similar applications.

Register online at the Gate Driver Forum and learn the nuances of efficiently driving a power switch in any given power electronic application.

9 Revision history

Document version	Date of release	Description of changes
1.0	April 10, 2022	Final Datasheet

Trademarks
All referenced product or service names and trademarks are the property of their respective owners.

Edition 2020-09-22

Published by

Infineon Technologies AG

81726 Munich, Germany

Do you have a question about this document?

Email: erratum@infineon.com

Document reference

IMPORTANT NOTICE

The information given in this document shall in no event be regarded as a guarantee of conditions or characteristics ("Beschaffenheitsgarantie") .

With respect to any examples, hints or any typical values stated herein and/or any information regarding the application of the product, Infineon Technologies hereby disclaims any and all warranties and liabilities of any kind, including without limitation warranties of non-infringement of intellectual property rights of any third party.

In addition, any information given in this document is subject to customer's compliance with its obligations stated in this document and any applicable legal requirements, norms and standards concerning customer's products and any use of the product of Infineon Technologies in customer's applications.

The data contained in this document is exclusively intended for technically trained staff. It is the responsibility of customer's technical departments to evaluate the suitability of the product for the intended application and the completeness of the product information given in this document with respect to such application.

For further information on the product, technology delivery terms and conditions and prices please contact your nearest Infineon Technologies office (**www.infineon.com**).

WARNINGS

Due to technical requirements products may contain dangerous substances. For information on the types in question please contact your nearest Infineon Technologies office.

Except as otherwise explicitly approved by Infineon Technologies in a written document signed by authorized representatives of Infineon Technologies, Infineon Technologies' products may not be used in any applications where a failure of the product or any consequences of the use thereof can reasonably be expected to result in personal injury.