

ACPL-K71T, ACPL-K72T, ACPL-K74T and ACPL-K75T

Automotive High Speed Low Power Digital Optocouplers

with R²Coupler™ Isolation and AEC-Q100 Grade 1 Qualification



Data Sheet



Lead (Pb) Free
RoHS 6 fully
compliant

RoHS 6 fully compliant options available;
-xxxE denotes a lead-free product

Description

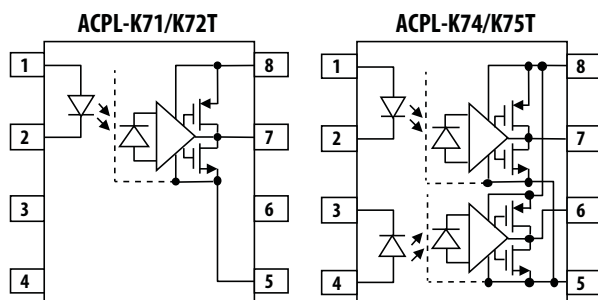
The ACPL-K71T and ACPL-K72T are high speed digital CMOS optocouplers package suitable for emerging electric vehicle applications. The ACPL-K74T and ACPL-K75T are dual channel equivalent of the ACPL-K71T and ACPL-K72T respectively. All products are available in the stretched SO-8 package outline, designed to be compatible with standard surface mount processes.

ACPL-K71T and ACPL-K74T are high speed mode with fastest propagation delay (max 35ns at $I_F=10\text{mA}$) while ACPL-K72T and ACPL-K75T are low power mode with lowest LED drive current of 4mA for standard digital isolation switching.

Each channel of the digital optocoupler has a CMOS detector IC with an integrated photodiode, a high speed trans-impedance amplifier, and a voltage comparator with an output driver.

Avago R²Coupler provides with reinforced insulation and reliability that delivers safe signal isolation critical in automotive and high temperature industrial applications.

Functional Diagram



Note: The connection of a 0.1 μF bypass capacitor between pins 5 and 8 is recommended.

Features

- Qualified to AEC-Q100 Grade 1 Test Guidelines
- Automotive Wide Temperature Range: -40°C to 125°C
- High Temperature and Reliability, High Speed Digital Interface for Automotive Application.
- 5 V CMOS compatibility
- 40 kV/ μs Common-Mode Rejection at $V_{\text{CM}}=1000\text{V}$ Typ.
- Low Propagation Delay :
 - ACPL-K71T, ACPL-K74T: 25ns Typ.@ $I_F = 10\text{mA}$
 - ACPL-K72T, ACPL-K75T: 60ns Typ.@ $I_F = 4\text{mA}$
- Worldwide Safety Approval:
 - UL 1577 approval, 5kV_{RMS} /1 min.
 - CSA Approval
 - IEC/EN/DIN EN 60747-5-5

Applications

- CAN Bus and SPI Communications Interface
- High Temperature Digital/Analog Signal Isolation
- Automotive IPM Driver for DC-DC converters and motor inverters
- Power Transistor Isolation

Truth Table

| LED | V _o |
|-----|----------------|
| ON | LOW |
| OFF | HIGH |

CAUTION: It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.

Ordering Information

| Part number | Option (RoHS Compliant) | Package | Surface Mount | Tape & Reel | UL 5000 V _{RMS} / 1 Minute rating | IEC/EN/DIN EN 60747-5-5 | Quantity |
|-------------|----------------------------|-------------------|------------------|----------------|---|----------------------------|---------------|
| ACPL-K71T | -000E | Stretched SO-8 | X | | X | | 80 per tube |
| | -060E | | X | | X | X | 80 per tube |
| | -500E | | X | X | X | | 1000 per reel |
| | -560E | | X | X | X | X | 1000 per reel |
| ACPL-K72T | -000E | Stretched SO-8 | X | | X | | 80 per tube |
| | -060E | | X | | X | X | 80 per tube |
| | -500E | | X | X | X | | 1000 per reel |
| | -560E | | X | X | X | X | 1000 per reel |
| ACPL-K74T | -000E | Stretched SO-8 | X | | X | | 80 per tube |
| | -060E | | X | | X | X | 80 per tube |
| | -500E | | X | X | X | | 1000 per reel |
| | -560E | | X | X | X | X | 1000 per reel |
| ACPL-K75T | -000E | Stretched SO-8 | X | | X | | 80 per tube |
| | -060E | | X | | X | X | 80 per tube |
| | -500E | | X | X | X | | 1000 per reel |
| | -560E | | X | X | X | X | 1000 per reel |

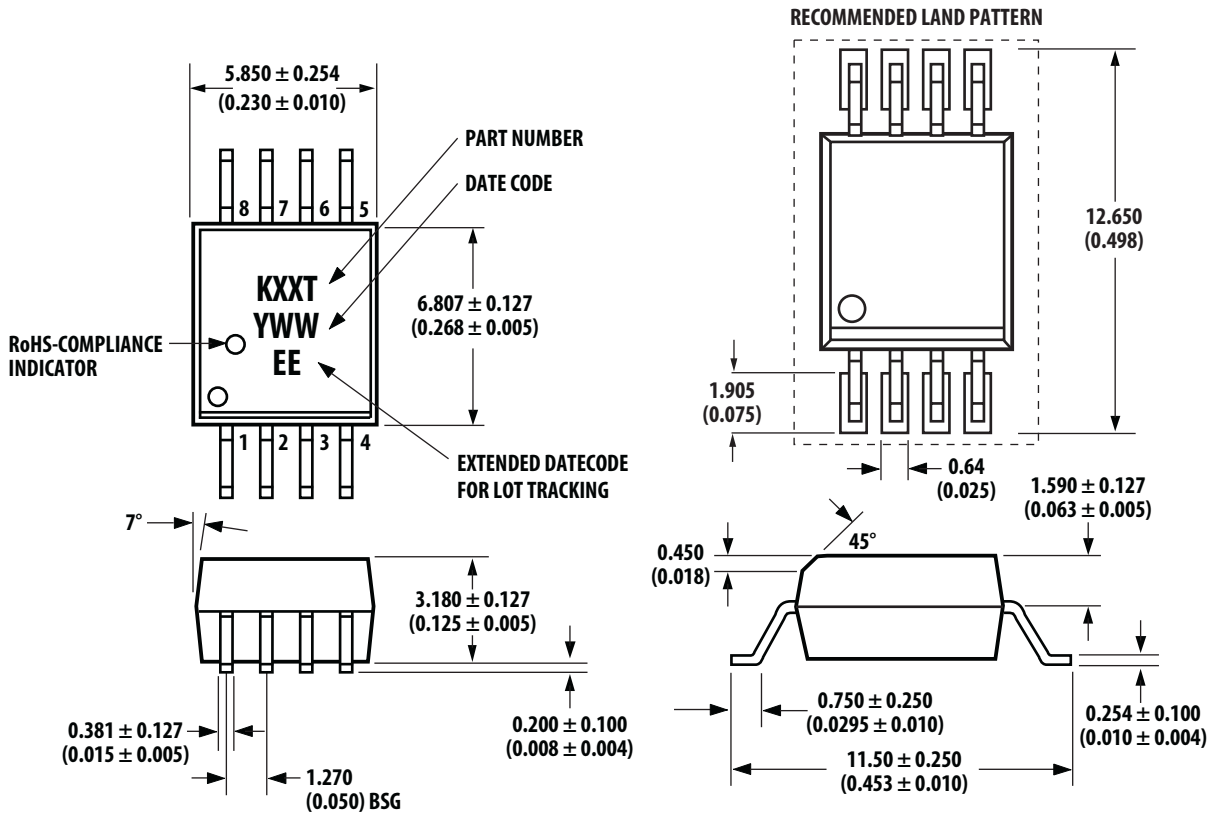
To order, choose a part number from the part number column and combine with the desired option from the option column to form an order entry.

Example 1:

ACPL-K71T-560E to order product of SSO-8 Surface Mount package in Tape and Reel packaging with IEC/EN/DIN EN 60747-5-5 Safety Approval in RoHS compliant.

Option datasheets are available. Contact your Avago sales representative or authorized distributor for information.

Package Outline Dimensions (Stretched S08)



Dimensions in millimeters and (inches).

Note:
Lead coplanarity = 0.1 mm (0.004 inches).
Floating lead protrusion = 0.25mm (10mils) max.

Recommended Pb-Free IR Profile

Recommended reflow condition as per JEDEC Standard, J-STD-020 (latest revision).

Note: Non-halide flux should be used.

Regulatory Information

The ACPL-K71T, ACPL-K72T, ACPL-K74T and ACPL-K75T are approved by the following organizations:

UL

Approval under UL 1577, component recognition program up to $V_{ISO} = 5kV_{RMS}$.

CSA

Approval under CSA Component Acceptance Notice #5.

IEC/EN/DIN EN 60747-5-5

Approval under IEC/EN/DIN EN 60747-5-5.

Insulation and Safety Related Specifications

| Parameter | Symbol | | Units | Conditions |
|---|--------|------|-------|--|
| Minimum External Air Gap (Clearance) | L(101) | 8 | mm | Measured from input terminals to output terminals, shortest distance through air. |
| Minimum External Tracking (Creepage) | L(102) | 8 | mm | Measured from input terminals to output terminals, shortest distance path along body. |
| Minimum Internal Plastic Gap (Internal Clearance) | | 0.08 | mm | Through insulation distance conductor to conductor, usually the straight line distance thickness between the emitter and detector. |
| Tracking Resistance (Comparative Tracking Index) | CTI | 175 | V | DIN IEC 112/VDE 0303 Part 1 |
| Isolation Group (DIN VDE0109) | | IIIa | | Material Group (DIN VDE 0109) |

IEC/EN/DIN EN 60747-5-5 Insulation Related Characteristic (Option 060 only)

| Description | Symbol | Characteristic | Units |
|---|----------------|----------------|-------------|
| Installation classification per DIN VDE 0110/1.89, Table 1 for rated mains voltage ≤ 600 V rms for rated mains voltage ≤ 1000 V rms | | I-IV I-III | |
| Climatic Classification | | 40/125/21 | |
| Pollution Degree (DIN VDE 0110/1.89) | | 2 | |
| Maximum Working Insulation Voltage | V_{IORM} | 1140 | V_{PEAK} |
| Input to Output Test Voltage, Method b $V_{IORM} \times 1.875 = V_{PR}$, 100% Production Test with $t_m = 1$ sec Partial Discharge < 5 pC | V_{PR} | 2137 | V_{PEAK} |
| Input to Output Test Voltage, Method a $V_{IORM} \times 1.6 = V_{PR}$, Type and sample test, $t_m = 10$ sec, Partial Discharge < 5 pC | V_{PR} | 1824 | V_{PEAK} |
| Highest Allowable Overvoltage (Transient Overvoltage, $t_{ini} = 60$ sec) | V_{IOTM} | 8000 | V_{PEAK} |
| Safety Limiting Values (Maximum values allowed in the event of a failure) | | | |
| Case Temperature | T_S | 175 | $^{\circ}C$ |
| Input Current | $I_{S,INPUT}$ | 230 | mA |
| Output Power | $P_{S,OUTPUT}$ | 600 | mW |
| Insulation Resistance at $T_S, V_{IO} = 500$ V | R_S | 10^9 | Ω |

Absolute Maximum Ratings

| Parameter | Symbol | Min. | Max. | Units | Test Conditions |
|-----------------------------------|---------------|---|----------------|-------|--|
| Storage Temperature | T_S | -55 | 130 | °C | |
| Ambient Operating Temperature | T_A | -40 | 125 | °C | |
| Supply Voltages | V_{DD} | 0 | 6.5 | V | |
| Output Voltage | V_O | -0.5 | $V_{DD} + 0.5$ | V | |
| Average Forward Input Current | I_F | | 20.0 | mA | |
| Peak Transient Input Current | $I_{F(TRAN)}$ | | 1 | A | $\leq 1\mu s$ Pulse Width, 300pps |
| | | | 80 | mA | $\leq 1\mu s$ Pulse Width, <10% Duty Cycle |
| Reverse Input Voltage | V_r | | 5 | V | |
| Input Power Dissipation | P_I | | 40 | mW | |
| Output Power Dissipation | P_o | | 30 | mW | |
| Lead Solder Temperature | | 260°C for 10 sec., 1.6 mm below seating plane | | | |
| Solder Reflow Temperature Profile | | See Solder Reflow Temperature Profile Section | | | |

Recommended Operating Conditions

| Parameter | Symbol | Min. | Max. | Units | Note |
|---------------------------|--------------|------|------|-------|------|
| Supply Voltage | V_{CC} | 3.0 | 5.5 | V | |
| Operating Temperature | T_A | -40 | 125 | °C | |
| Forward Input Current | $I_{F(ON)}$ | 4 | 15 | mA | |
| Forward Off State Voltage | $V_{F(OFF)}$ | | 0.8 | V | |
| Input Threshold Current | I_{TH} | | 3.5 | mA | |

Electrical Specifications

Over recommended temperature $T_A = -40^\circ\text{C}$ to 125°C , $3.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$. All typical specifications are at $T_A = 25^\circ\text{C}$, $V_{DD} = 5\text{ V}$.

| Parameter | Symbol | Min. | Typ. | Max. | Units | Test Conditions | Fig | Notes |
|--|-----------|----------------|------|------|-------|---|-----|-------|
| LED Forward Voltage | V_F | 1.45 | 1.5 | 1.75 | V | $I_F = 10\text{ mA}$, $T_A = 25^\circ\text{C}$ | | |
| | | 1.25 | 1.5 | 1.85 | V | | | |
| Vf Temperature Coefficient | | | -1.5 | | mV/°C | | | |
| Input Capacitance | C_{IN} | | 90 | | pF | | | |
| Input Reverse Breakdown Voltage | BV_R | 5.0 | | | V | $I_R = 10\mu\text{A}$ | | |
| Logic High Output Voltage | V_{OH} | $V_{DD} - 0.6$ | | | V | $I_{OH} = -3.2\text{ mA}$ | 4 | |
| Logic Low Output Voltage | V_{OL} | | | 0.6 | V | $I_{OL} = 4\text{ mA}$ | 3 | |
| Logic Low Output Supply Current (per channel) | I_{DDL} | | 0.9 | 1.5 | mA | | | |
| Logic High Output Supply Current (per channel) | I_{DDH} | | 0.9 | 1.5 | mA | | | |

ACPL-K71T, ACPL-K74T High Speed Mode Switching Specifications

Over recommended temperature $T_A = -40^{\circ}\text{C}$ to 125°C , $4.5\text{ V} \leq V_{DD} \leq 5.5\text{ V}$. All typical specifications are at $T_A=25^{\circ}\text{C}$, $V_{DD}=5\text{ V}$.

| Parameter | Symbol | Min. | Typ. | Max. | Units | Test Conditions | Fig | Notes |
|---|-----------|------|------|------|-------------------|--|--------|-------|
| Propagation Delay Time to Logic Low Output | t_{PHL} | | 25 | 35 | ns | $V_{IN} = 4.5\text{V}-5.5\text{V}$, $R_{IN} = 390\Omega \pm 5\%$, $C_{IN} = 100\text{pF}$, $C_L = 15\text{pF}$ $V_{THL} = 0.8\text{V}$ $V_{TLH} = 80\%$ of V_{DD} | 5,6,11 | 1,2,3 |
| Propagation Delay Time to Logic High Output | t_{PLH} | | 25 | 35 | ns | | | |
| Pulse Width Distortion | PWD | | 0 | 12 | ns | | | |
| Propagation Delay Skew | t_{PSK} | | | 15 | ns | | | |
| Output Rise Time (10% – 90%) | t_R | | 10 | | ns | | | |
| Output Fall Time (90% - 10%) | t_F | | 10 | | ns | | | |
| Common Mode Transient Immunity at Logic High Output | $ CM_H $ | 15 | 25 | | kV/ μs | $V_{IN} = 0\text{V}$, $R_{IN} = 390\Omega \pm 5\%$, $C_{IN} = 100\text{pF}$, $V_{CM} = 1000\text{V}$, $T_A = 25^{\circ}\text{C}$ | 12 | 4 |
| Common Mode Transient Immunity at Logic High Output | $ CM_L $ | 15 | 25 | | kV/ μs | $V_{IN} = 4.5\text{V}-5.5\text{V}$, $R_{IN} = 390\Omega \pm 5\%$, $C_{IN} = 100\text{pF}$, $V_{CM} = 1000\text{V}$, $T_A = 25^{\circ}\text{C}$ | 12 | 5 |

ACPL-K72T, ACPL-K75T Low Power Mode Switching Specifications

Over recommended temperature $T_A = -40^{\circ}\text{C}$ to 125°C , $3.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$. All typical specifications are at $T_A=25^{\circ}\text{C}$, $V_{DD}=5\text{ V}$.

| Parameter | Symbol | Min. | Typ. | Max. | Units | Test Conditions | Fig | Notes |
|---|-----------|------|------|------|-------------------|---|--------------------|-------|
| Propagation Delay Time to Logic Low Output | t_{PHL} | | 60 | 100 | ns | $I_F = 4\text{mA}$, $C_L = 15\text{pF}$ $V_{THL} = 0.8\text{V}$ $V_{TLH} = 80\%$ of V_{DD} | 7, 8, 9, 10, 13 | 1,2,3 |
| Propagation Delay Time to Logic High Output | t_{PLH} | | 35 | 100 | ns | | | |
| Pulse Width Distortion | PWD | | 25 | 50 | ns | | | |
| Propagation Delay Skew | t_{PSK} | | | 60 | ns | | | |
| Output Rise Time (10% – 90%) | t_R | | 10 | | ns | | | |
| Output Fall Time (90% - 10%) | t_F | | 10 | | ns | | | |
| Common Mode Transient Immunity at Logic High Output | $ CM_H $ | 25 | 40 | | kV/ μs | LED Driving Circuit Fig 13, $V_{IN} = 0\text{V}$, $R_1 = 350\Omega \pm 5\%$, $R_2 = 350\Omega \pm 5\%$, $V_{CM} = 1000\text{V}$, $T_A = 25^{\circ}\text{C}$ | 14 | 4 |
| Common Mode Transient Immunity at Logic High Output | $ CM_L $ | 25 | 40 | | kV/ μs | LED Driving Circuit Fig 14, $V_{IN} = 4.5-5.5\text{V}$, $R_1 = 350\Omega \pm 5\%$, $R_2 = 350\Omega \pm 5\%$, $V_{CM} = 1000\text{V}$, $T_A = 25^{\circ}\text{C}$ | 14 | 5 |

Package Characteristics

All Typical at $T_A = 25^\circ\text{C}$.

| Parameter | Symbol | Min. | Typ. | Max. | Units | Test Conditions | Notes |
|--|-----------|------|-----------|------|-----------|--|-------|
| Input-Output Momentary Withstand Voltage | V_{ISO} | 5000 | | | V_{RMS} | $RH \leq 50\%$, $t = 1$ minute, $T_A = 25^\circ\text{C}$ | 6, 7 |
| Input-Output Resistance | R_{I-O} | | 10^{14} | | Ω | $V_{I-O} = 500$ V dc | 6 |
| Input-Output Capacitance | C_{I-O} | | 0.6 | | pF | $f = 1$ MHz, $T_A = 25^\circ\text{C}$ | 6 |

Notes:

- t_{PHL} propagation delay is measured from the 50% (V_{IN} or I_F) on the rising edge of the input pulse to the 0.8V of V_{DD} of the falling edge of the V_O signal. t_{PLH} propagation delay is measured from the 50% (V_{IN} or I_F) on the falling edge of the input pulse to the 80% level of the rising edge of the V_O signal.
- PWD is defined as $|t_{PHL} - t_{PLH}|$.
- t_{PSK} is equal to the magnitude of the worst case difference in t_{PHL} and/or t_{PLH} that will be seen between units at any given temperature within the recommended operating conditions.
- CM_H is the maximum tolerable rate of rise of the common mode voltage to assure that the output will remain in a high logic state.
- CM_L is the maximum tolerable rate of fall of the common mode voltage to assure that the output will remain in a low logic state.
- Device considered a two terminal device: pins 1, 2, 3 and 4 shorted together, and pins 5, 6, 7 and 8 shorted together.
- In accordance with UL 1577, each optocoupler is proof tested by applying an insulation test voltage $> 6000V_{RMS}$ for 1 second.

Performance Plots

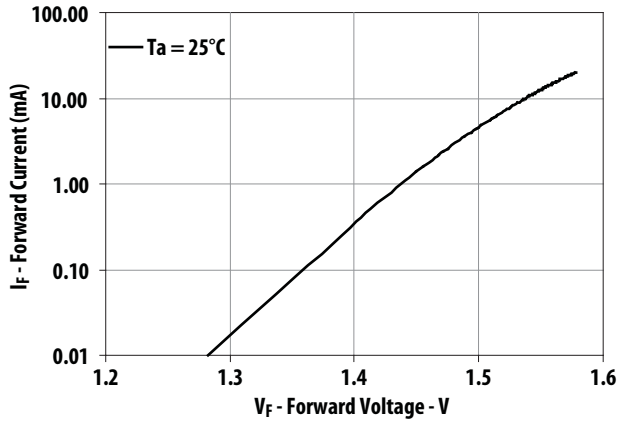


Figure 1. Typical Diode Input Forward Current Characteristic

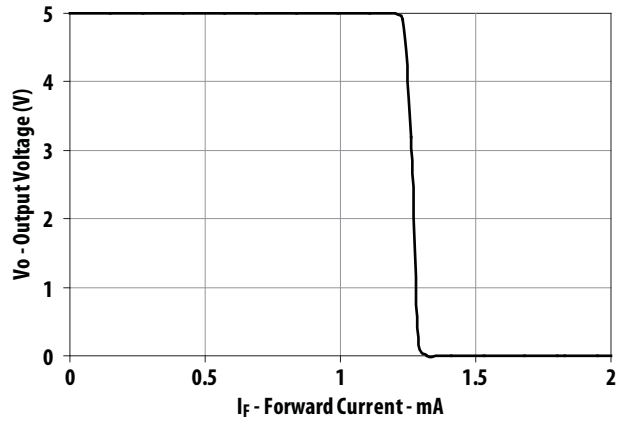


Figure 2. Typical Output Voltage vs Input Forward Current

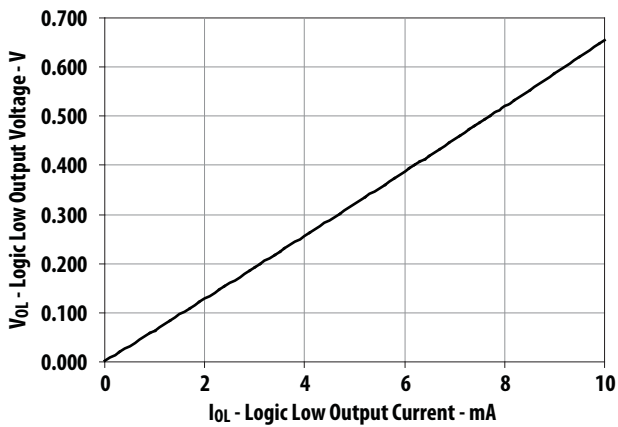


Figure 3 Typical Logic Low Output Voltage vs Low Output Current

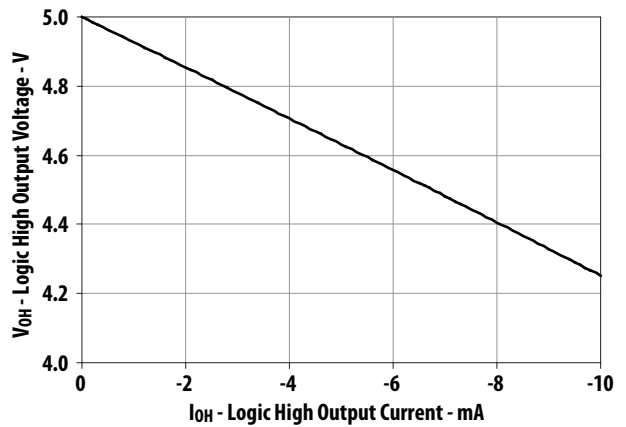


Figure 4. Typical Logic High Output Voltage vs Logic High Output Current

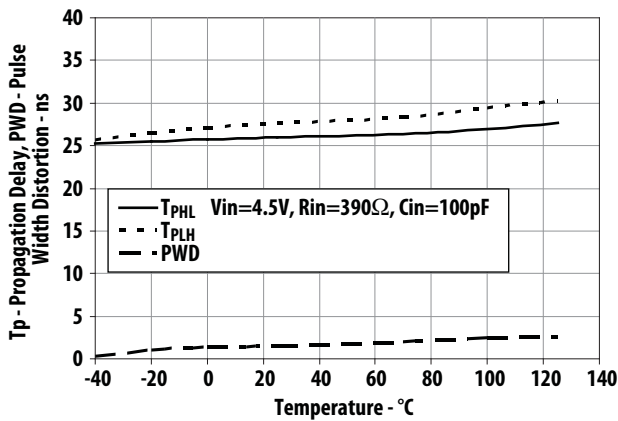


Figure 5. ACPL-K71T/K74T (High Speed) Typical Propagation Delay vs Temperature

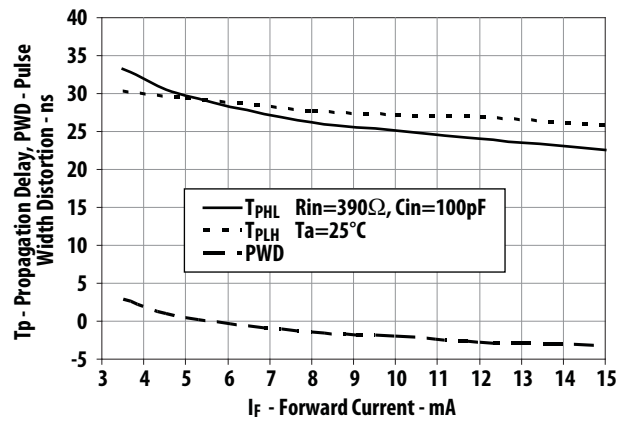


Figure 6. ACPL-K71T/K74T (High Speed) Typical Propagation Delay vs Input Forward Current

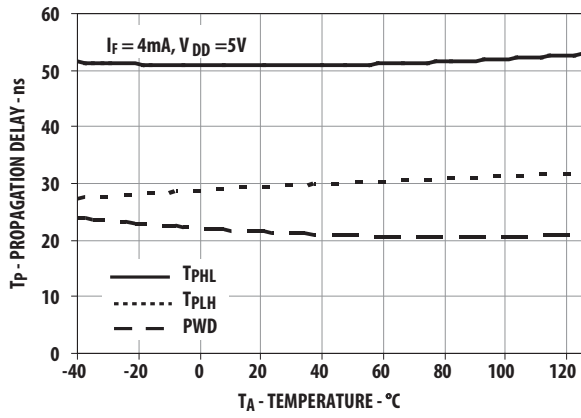


Figure 7. ACPL-K72T/K75T (5V) Typical Propagation Delay vs Temperature

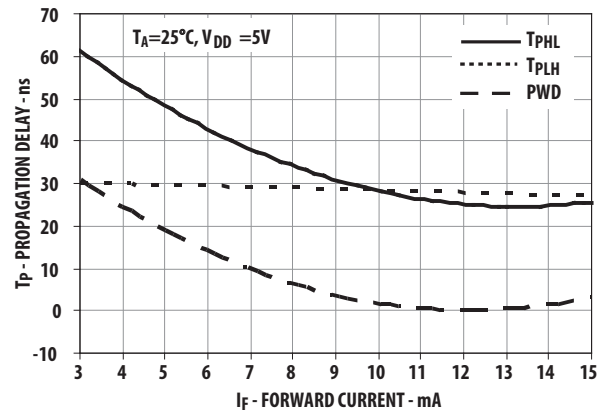


Figure 8. ACPL-K72T/K75T (5V) Typical Propagation Delay vs Input Forward Current

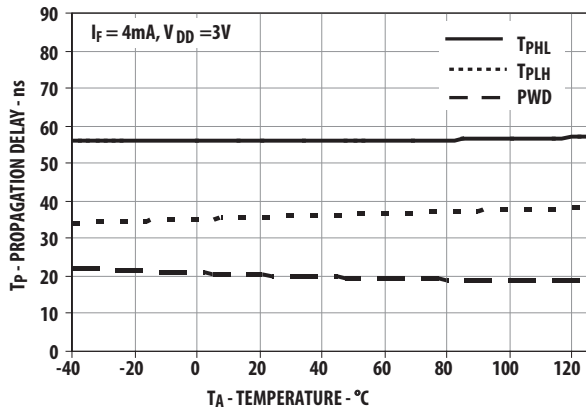


Figure 9. ACPL-K72T/K75T (3V) Typical Propagation Delay vs Temperature

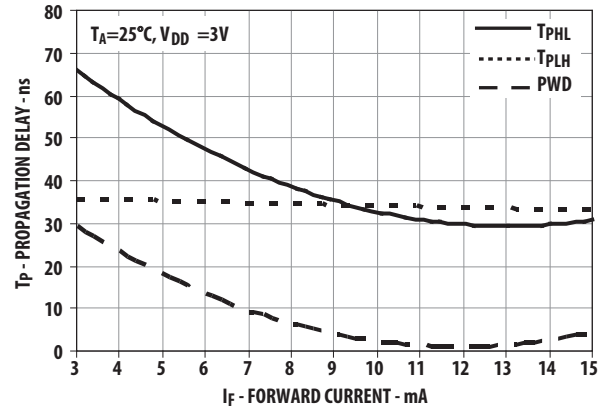


Figure 10. ACPL-K72T/K75T (3V) Typical Propagation Delay vs Input Forward Current

ACPL-K71T/K74T High Speed Mode:

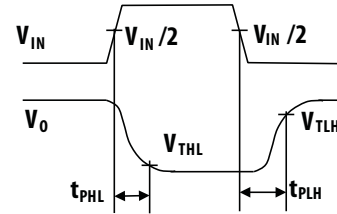
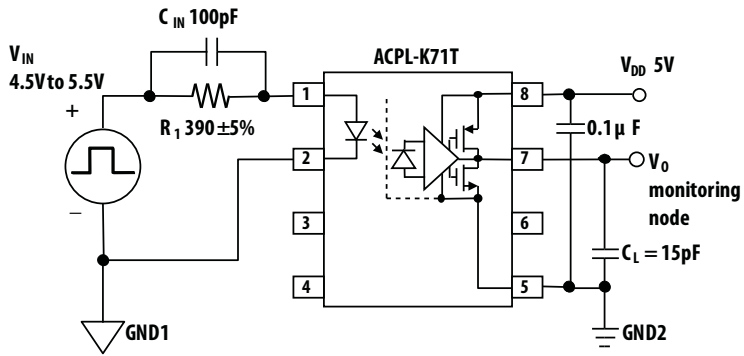


Figure 11. High Speed Mode Switching Test Circuit and Typical Waveform

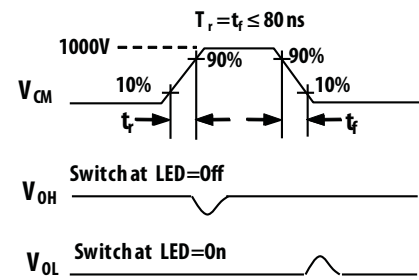
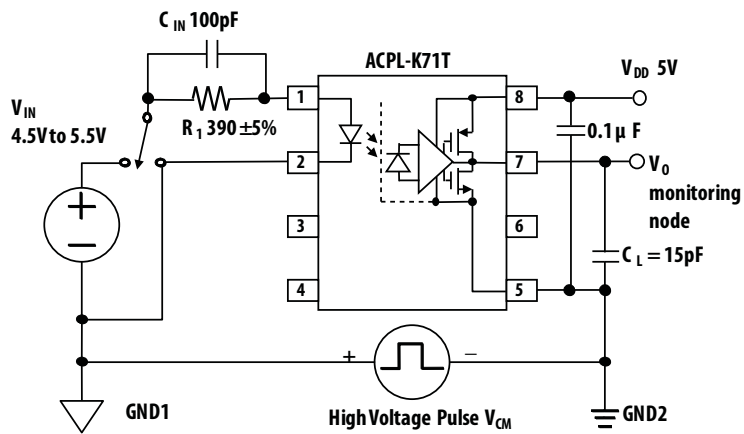


Figure 12. High Speed Mode CMR Test Circuit and Typical Waveform

ACPL-K72T/K75T Low Power Mode:

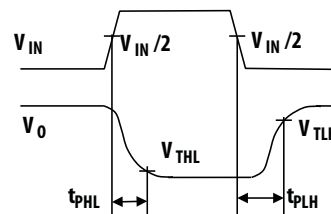
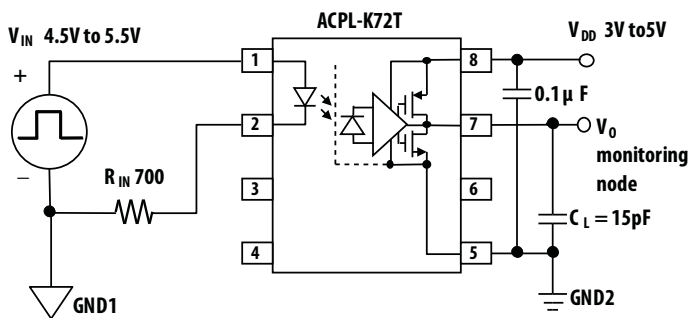


Figure 13. Low Power Mode Switching Test Circuit and Typical Waveform

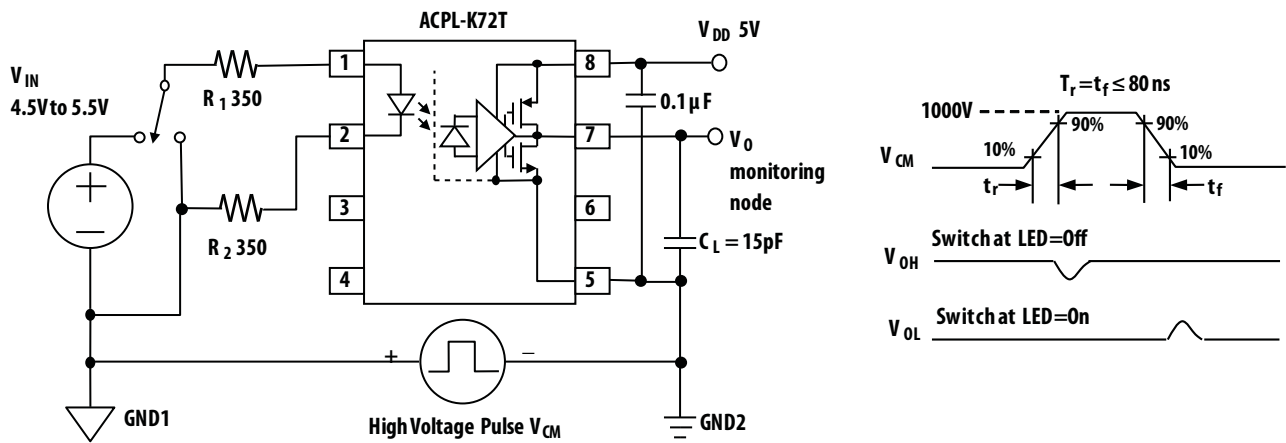
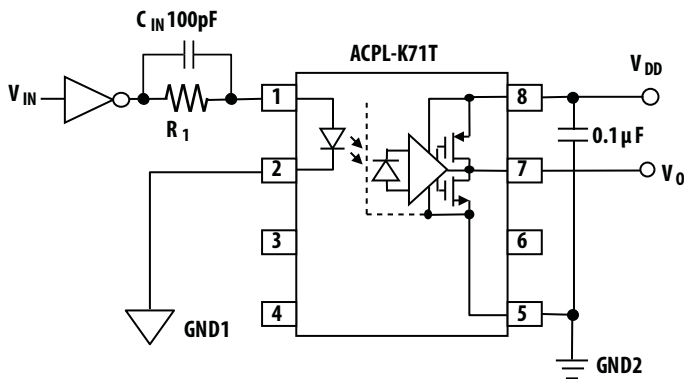


Figure 14. Low Power Mode CMR Test Circuit

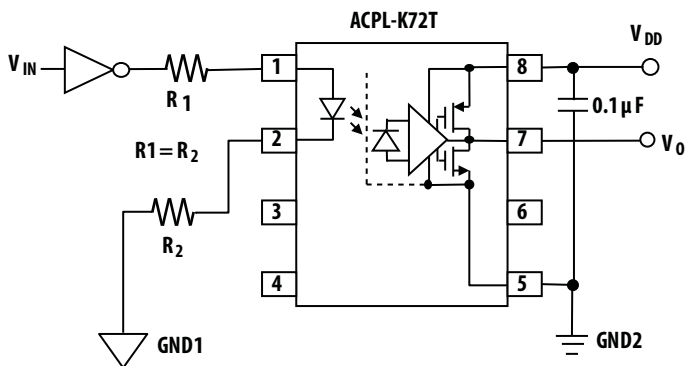
Recommended Application Circuits



Truth Table

| V _{IN} | LED | V _o |
|-----------------|-----|----------------|
| LOW | ON | LOW |
| HIGH | OFF | HIGH |

Figure 15. Recommended Application Circuit for ACPL-K71T/K74T High Speed Performance



Truth Table

| V _{IN} | LED | V _o |
|-----------------|-----|----------------|
| LOW | ON | LOW |
| HIGH | OFF | HIGH |

Figure 16. Recommended Application Circuit for ACPL-K72T/K75T Low Power Performance

Thermal Resistance Model for ACPL-K71T/K72T

The diagram of ACPL-K71T/K72T for measurement is shown in Figure 17. Here, one die is heated first and the temperatures of all the dice are recorded after thermal equilibrium is reached. Then, the 2nd die is heated and all the dice temperatures are recorded. With the known ambient temperature, the die junction temperature and power dissipation, the thermal resistance can be calculated. The thermal resistance calculation can be cast in matrix form. This yields a 2 by 2 matrix for our case of two heat sources.

$$\begin{vmatrix} R_{11} & R_{12} \\ R_{21} & R_{22} \end{vmatrix} \times \begin{vmatrix} P_1 \\ P_2 \end{vmatrix} = \begin{vmatrix} \Delta T_1 \\ \Delta T_2 \end{vmatrix}$$

- R₁₁ : Thermal Resistance of Die1 due to heating of Die1 (°C/W)
- R₁₂ : Thermal Resistance of Die1 due to heating of Die2 (°C/W)
- R₂₁ : Thermal Resistance of Die2 due to heating of Die1 (°C/W)
- R₂₂ : Thermal Resistance of Die2 due to heating of Die2 (°C/W)

- P₁ : Power dissipation of Die1 (W)
- P₂ : Power dissipation of Die2 (W)

- T₁ : Junction temperature of Die1 due to heat from all dice (°C)
- T₂ : Junction temperature of Die2 due to heat from all dice (°C)

T_a : Ambient temperature (°C)

- ΔT₁ : Temperature difference between Die1 junction and ambient (°C)
- ΔT₂ : Temperature difference between Die2 junction and ambient (°C)

$$T_1 = (R_{11} \times P_1 + R_{12} \times P_2) + T_a$$

$$T_2 = (R_{21} \times P_1 + R_{22} \times P_2) + T_a$$

Measurement data on a low K board:

$$R_{11} = 160 \text{ °C/W}, R_{12} = R_{21} = 74 \text{ °C/W}, R_{22} = 115 \text{ °C/W}$$

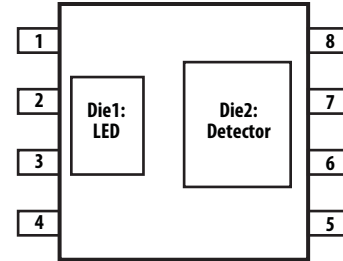


Figure 17. Diagram of ACPL-K71T/K72T for measurement

Thermal Resistance Model for ACPL-K74T/K75T

The diagram of ACPL-K74T/K75T for measurement is shown in Figure 18. Here, one die is heated first and the temperatures of all the dice are recorded after thermal equilibrium is reached. Then, the 2nd, 3rd and 4th die is heated and all the dice temperatures are recorded. With the known ambient temperature, the die junction temperature and power dissipation, the thermal resistance can be calculated. The thermal resistance calculation can be cast in matrix form. This yields a 4 by 4 matrix for our case of two heat sources.

$$\begin{vmatrix} R_{11} & R_{12} & R_{13} & R_{14} \\ R_{21} & R_{22} & R_{23} & R_{24} \\ R_{31} & R_{32} & R_{33} & R_{34} \\ R_{41} & R_{42} & R_{43} & R_{44} \end{vmatrix} \times \begin{vmatrix} P_1 \\ P_2 \\ P_3 \\ P_4 \end{vmatrix} = \begin{vmatrix} \Delta T_1 \\ \Delta T_2 \\ \Delta T_3 \\ \Delta T_4 \end{vmatrix}$$

- R₁₁ : Thermal Resistance of Die1 due to heating of Die1 (°C/W)
- R₁₂ : Thermal Resistance of Die1 due to heating of Die2 (°C/W)
- R₁₃ : Thermal Resistance of Die1 due to heating of Die3 (°C/W)
- R₁₄ : Thermal Resistance of Die1 due to heating of Die4 (°C/W)

- R₂₁ : Thermal Resistance of Die2 due to heating of Die1 (°C/W)
- R₂₂ : Thermal Resistance of Die2 due to heating of Die2 (°C/W)
- R₂₃ : Thermal Resistance of Die2 due to heating of Die3 (°C/W)
- R₂₄ : Thermal Resistance of Die2 due to heating of Die4 (°C/W)

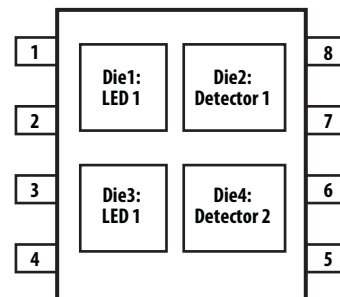


Figure 18. Diagram of ACPL-K74T/K75T for measurement

R₃₁ : Thermal Resistance of Die3 due to heating of Die1 (°C/W)
 R₃₂ : Thermal Resistance of Die3 due to heating of Die2 (°C/W)
 R₃₃ : Thermal Resistance of Die3 due to heating of Die3 (°C/W)
 R₃₄ : Thermal Resistance of Die3 due to heating of Die4 (°C/W)

R₄₁ : Thermal Resistance of Die4 due to heating of Die1 (°C/W)
 R₄₂ : Thermal Resistance of Die4 due to heating of Die2 (°C/W)
 R₄₃ : Thermal Resistance of Die4 due to heating of Die3 (°C/W)
 R₄₄ : Thermal Resistance of Die4 due to heating of Die4 (°C/W)

P₁ : Power dissipation of Die1 (W)
 P₂ : Power dissipation of Die2.
 P₃ : Power dissipation of Die3 (W)
 P₄ : Power dissipation of Die4.

T₁ : Junction temperature of Die1 due to heat from all dice (°C)
 T₂ : Junction temperature of Die2 due to heat from all dice (°C)
 T₃ : Junction temperature of Die3 due to heat from all dice (°C)
 T₄ : Junction temperature of Die4 due to heat from all dice (°C)

T_a : Ambient temperature (°C)

ΔT₁ : Temperature difference between Die1 junction and ambient (°C)
 ΔT₂ : Temperature difference between Die2 junction and ambient (°C)
 ΔT₃ : Temperature difference between Die3 junction and ambient (°C)
 ΔT₄ : Temperature difference between Die4 junction and ambient (°C)

$$T_1 = (R_{11} \times P_1 + R_{12} \times P_2 + R_{13} \times P_3 + R_{14} \times P_4) + T_a \text{ -- (1)}$$

$$T_2 = (R_{21} \times P_1 + R_{22} \times P_2 + R_{23} \times P_3 + R_{24} \times P_4) + T_a \text{ -- (2)}$$

$$T_3 = (R_{31} \times P_1 + R_{32} \times P_2 + R_{33} \times P_3 + R_{34} \times P_4) + T_a \text{ -- (3)}$$

$$T_4 = (R_{41} \times P_1 + R_{42} \times P_2 + R_{43} \times P_3 + R_{44} \times P_4) + T_a \text{ -- (4)}$$

Measurement data on a low K board:

| | | | | | | | | | | | | | | | |
|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|
| R ₁₁ | R ₁₂ | R ₁₃ | R ₁₄ | R ₂₁ | R ₂₂ | R ₂₃ | R ₂₄ | R ₃₁ | R ₃₂ | R ₃₃ | R ₃₄ | R ₄₁ | R ₄₂ | R ₄₃ | R ₄₄ |
| 160 | 76 | 76 | 76 | 76 | 115 | 76 | 76 | 76 | 76 | 160 | 76 | 76 | 76 | 76 | 115 |

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