



Product Change Notification / SYST-22ULJY515

Date:

01-Feb-2021

Product Category:

8-bit Microcontrollers

PCN Type:

Silicon Die Revision

Notification Subject:

ERRATA - PIC18F27/47/57Q84 Silicon Errata and Data Sheet Clarifications Silicon Die Revision Addition

Affected CPNs:

[SYST-22ULJY515_Affected_CPN_02012021.pdf](#)

[SYST-22ULJY515_Affected_CPN_02012021.csv](#)

Notification Text:

SYST-22ULJY515

Microchip has released a new Product Documents for the PIC18F27/47/57Q84 Silicon Errata and Data Sheet Clarifications of devices. If you are using one of these devices please read the document located at [PIC18F27/47/57Q84 Silicon Errata and Data Sheet Clarifications](#) .

Notification Status: Final

Description of Change: 1) Added new silicon Rev B4 and silicon erratum item 1.3. Minor editorial corrections

Impacts to Data Sheet: None

Reason for Change: To Improve manufacturability

Change Implementation Status: Complete

Estimated First Ship Date: 01 Feb 2021

NOTE: Please be advised that after the estimated first ship date customers may receive pre and post change parts.

Markings to Distinguish Revised from Unrevised Devices: Traceability Code

Attachments:

[PIC18F27/47/57Q84 Silicon Errata and Data Sheet Clarifications](#)

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Affected Catalog Part Numbers (CPN)

PIC18F27Q84-E/5N
PIC18F27Q84-E/SO
PIC18F27Q84-E/SP
PIC18F27Q84-E/SS
PIC18F27Q84-I/5N
PIC18F27Q84-I/SO
PIC18F27Q84-I/SP
PIC18F27Q84-I/SS
PIC18F27Q84T-I/5N
PIC18F27Q84T-I/SO
PIC18F27Q84T-I/SS
PIC18F57Q84-E/6MX
PIC18F57Q84-E/PT
PIC18F57Q84-I/6MX
PIC18F57Q84-I/PT
PIC18F57Q84T-I/6MX
PIC18F57Q84T-I/PT

PIC18F27/47/57Q84 Silicon Errata and Data Sheet Clarifications

The PIC18F27/47/57Q84 devices that you have received conform functionally to the current device data sheet (DS40002213C), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in the table below.

The errata described in this document will be addressed in future revisions of the PIC18F27/47/57Q84 silicon.

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current.

Table 1. Silicon Device Identification

Part Number	Device ID	Revision ID	
		B3	B4
PIC18F27Q84	0x9903	0xA043	0xA044
PIC18F47Q84	0x9904	0xA043	0xA044
PIC18F57Q84	0x9905	0xA043	0xA044



Important: Refer to the **Device/Revision ID** section in the current “**PIC18FXXQ84 Family Programming Specification**” (DS40002137C) for more detailed information on Device Identification and Revision IDs for your specific device.

Table 2. Silicon Issue Summary

Module	Feature	Item No.	Issue Summary	Affected Revisions	
				B3	B4
UTMR	Hardware Reset condition	1.1.1	Reset does not happen at period match when the prescaler > 0	X	
	Level-triggered ERS Start/Reset condition	1.1.2	Dead zone exists in level-triggered Start/Reset condition when an ERS signal is generated due to an SFR access	X	X
	Hardware Reset condition	1.1.3	Reset does not happen at period match when the prescaler > 0 and the timer stops at period match (includes One Shot mode)	X	X
Note: Only those issues indicated in the last column apply to the current silicon revision.					

1. Silicon Errata Issues



Notice: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated by the bold font in the following tables apply to the current silicon revision.

1.1 Module: Universal Timer (UTMR) Module

1.1.1 Reset Does Not Happen at Period Match When the Prescaler > 0

When the prescaler > 0 and a hardware-based Reset event is selected (RESET = `b01 or `b10 or `b11), the timer does not reset at period match.

Work around

1. Use prescaler = 0, or
2. When using prescaler > 0, clear the timer in software using the CLR command at every PR match interrupt.

Affected Silicon Revisions

B3	B4
X	

1.1.2 Dead Zone Exists in Level-Triggered Start/Reset Condition When an ERS Signal Is Generated Due to an SFR Access

When a level-triggered Start/Reset condition (START = `b11 or RESET = `b01) is triggered by an ERS signal generated by an SFR access such as TUxyPRL_Write or TUxyTMRL_Read or TUxyCRL_Read (TUxyERS = 0x3E or 0x3F), there exists a dead zone in which subsequent SFR accesses will be missed. This dead zone is the period between the ZIF flag being set and the timer starting to count again. This can be monitored by checking either the RUN status bit or the level output of the timer.

Work around

The user must wait for the timer to start counting before accessing the period, counter and capture registers again.

Affected Silicon Revisions

B3	B4
X	X

1.1.3 Reset Does Not Happen at Period Match When the Prescaler > 0 and the Timer Stops at Period Match

When the prescaler > 0 and the UTMR is configured to both stop and reset at period match, the timer will stop immediately at the period value and will not reset (no pulse output and the ZIF bit will not be set).

This issue also occurs when One Shot mode is enabled (OSEN = 1) and the prescaler > 0. In this mode, the timer will stop and clear the ON bit as soon as the period is reached, but no pulse output will occur and the ZIF bit will not be set.

Work around

1. Use prescaler = 0, or
2. When using prescaler > 0, clear the timer in software using the CLR command at every PR match interrupt.

Affected Silicon Revisions

B3	B4
X	X

2. Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (40002213C):

Note:

Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

2.1 None

There are no known data sheet clarifications as of this publication date.

3. Appendix A: Revision History

Doc. Rev.	Date	Comments
C	01/2021	Added new silicon Rev B4 and silicon erratum item 1.3. Minor editorial corrections.
B	11/2020	Changed to released silicon revision.
A	06/2020	Initial document release.

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