NXP Semiconductors
User's Guide

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FRDM-KL28Z User's Guide

1. Introduction

The Freedom development platform is a set of software and hardware tools for evaluation and development. It is an ideal tool for the rapid prototyping of microcontroller-based applications.

The FRDM-KL28Z supports power supply voltage range from 1.71 V to 3.6 V. It features a KL28Z, a device boasting a maximum operating frequency of 96 MHz, up to 512 KB Flash and numerous analog and digital peripherals.

The FRDM-KL28Z includes the NXP open standard embedded serial and debug adapter known as OpenSDA. This circuit offers the user several options for serial communications, flash programming and run-control debugging.

The FRDM-KL28Z hardware is form-factor compatible with the Arduino™ R3 pin layout, providing a broad range of expansion board options. The on-board interfaces include an RGB LED, a 6-axis digital sensor (combining a 3D accelerometer and 3D magnetometer), a 3-axis digital angular rate gyroscope, an ambient light sensor, and a capacitive touch slider.

There are many software development tool options available to the user. Choices include Kinetis Design Studio (KDS), IAR Embedded Workbench, Keil MDK featuring the µVision IDE, and so on.

All of these features combine to give users the freedom needed to rapidly prototype many embedded designs: a

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powerful microcontroller built on a very low-power core and SOC platform, easy-access to I/O with a large ecosystem of compatible hardware, a flexible programming and debug interface, and a large ecosystem of software development environments.

2. Getting Started

Refer to the FRDM-KL28Z *Quick Start Package* for step-by-step instructions for getting started with the freedom board. See the "Jump Start Your Design" section at nxp.com/FREDEVPLA for the Quick Start Package and software lab guides.

3. FRDM-KL28Z Features

The FRDM-KL28Z hardware is a Freedom development board assembled with the following features:

- MKL28Z512VLL7 MCU (96 MHz, 512 KB Flash, 128 KB RAM, 32 KB ROM,100 LQFP package)
- 3-Axis Digital Angular Rate Gyroscope, FXAS21002CQ (U2)
- Accelerometer and magnetometer, FXOS8700CQ (U10)
- OpenSDA: On-board serial and debug adapter (U7)
- I/O headers for easy access to MCU I/O pins
- Ambient light sensor (Q1)
- Flexible power supply options: USB, coin cell battery, external source
- Capacitive touch slider
- Reset push button (SW1)
- NMI and LLWU buttons (SW2, SW3)
- RGB LED (D2)

The FRDM-KL28Z features two MCUs: The target MCU is the MKL28Z512VLL7. The OpenSDA MCU is the MK20DX128VFM5.

The primary components and their location on the hardware assembly are pointed out in *Figure 1*. *Figure 2* shows a block diagram of the FRDM-KL28Z board.

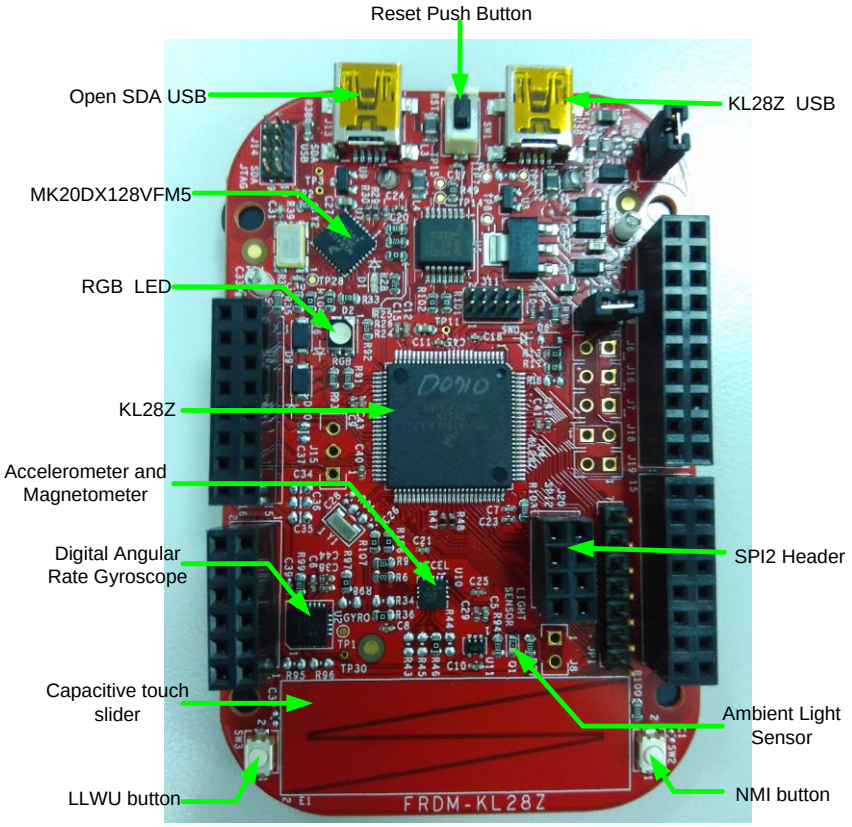

Figure 1. FRDM-KL28Z feature call-outs

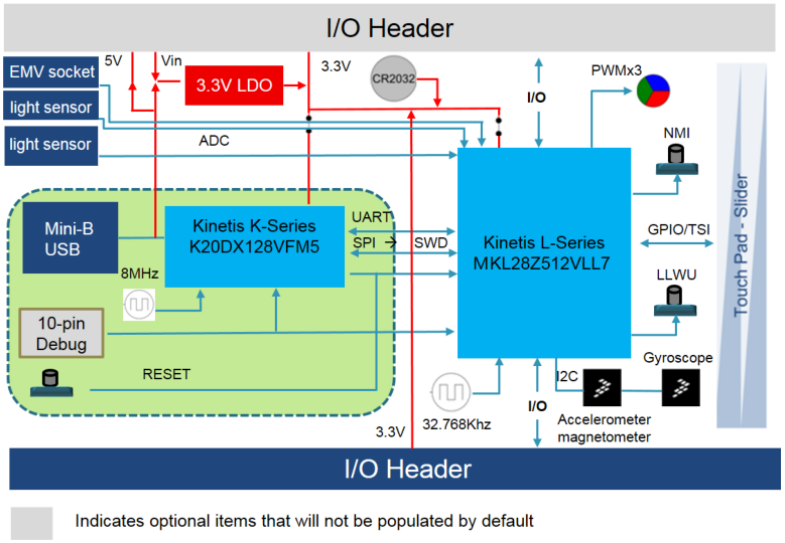

Figure 2. FRDM-KL28Z block diagram

4. FRDM-KL28Z Hardware Description

4.1. Power supply

The FRDM-KL28Z offers a design with multiple power supply options. It can be powered from the USB connector, battery on the board, the VIN pin on the I/O header, or an off-board 1.71-3.6 V supply from the 3.3 V pin on the I/O header. The USB and VIN supplies are regulated on-board using a 3.3 V linear regulator to produce the main power supply. Other sources are not regulated on-board.

The following table provides the operational details and requirements for the power supplies.

Table 1. Tags Power supply requirements

Supply Source & Location	Valid Range	OpenSDA Operational?	Regulated on-board?
OpenSDA USB (J13)	5 V	Yes	Yes
KL28Z USB (J10)	5 V	No	Yes
P5V0-9V0_VIN (J3 PIN16)	4.3-9 V	No	Yes
P3V3 Pin（J3 PIN8）	1.71-3.6 V	No	No
Battery	2-3.6 V	No	No

Figure 3 shows the schematic drawing for the power supply inputs and the on-board voltage regulator. In addition, regulated power can be supplied to J3 pin 16 from an external source through P5-9V_VIN by populating the board with an optional voltage regulator (for instance a 7805 style regulator) in a TO-220 package, thus providing a high current supply to external devices. To prevent voltage sag under a high load, C34, C35, C36, and C37 should be populated with appropriately sized capacitors to match the regulator chosen.

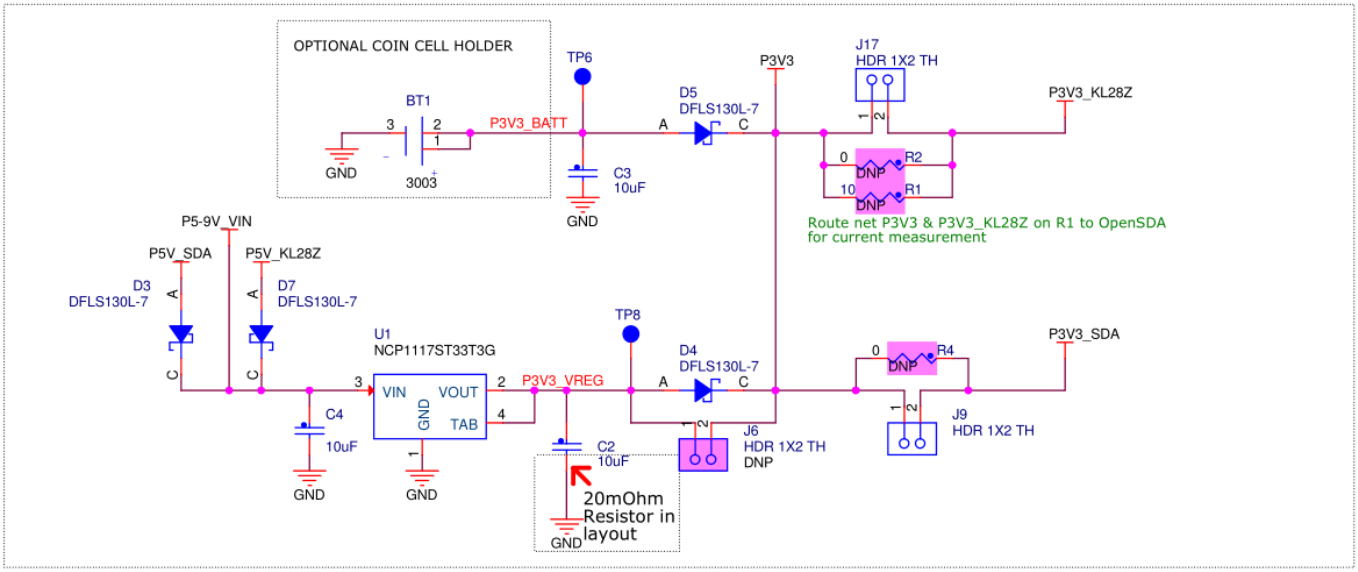

Figure 3. Power supply schematic

NOTE

The OpenSDA circuit is operational only when a USB cable is connected and supplying power to J13. However, the protection circuitry is in place to allow multiple sources to be powered at once.

Table 2. FRDM-KL28Z power supplies

Power Supply Name	Description
P5V0-9V0_VIN	Power supplied from the VIN pin of the I/O headers (J3 pin 16).
P5V_SDA	Power supplied from the OpenSDA USB connector
P5V_USB	Nominal 5 V is supplied to the I/O headers (J3 pin 10). Sourced from either the P5V_KL28Z or P5V_SDA through a back drive protection Schottky diode.
P5V_KL28Z	Power supplied from the Mini USB connector.
P3V3_VREG	Regulated 3.3 V supply. Sources power to the P3V3 supply rail through an optional back drive protection Schottky diode.
P3V3	Main supply rail for the FRDM-KL28Z. Can be sourced from P3V3_VREG (J3 pin 8).
P3V3_KL28Z	KL28Z MCU power supply. Header J17 provides a convenient means for KL28Z energy consumption measurements.
P3V3_SDA	OpenSDA circuit power supply.
P3V3_BATT	Coin cell battery supply voltage. Sources power to the P3V supply rail with the option of adding a Schottky diode.

NOTE

J9 and J17 are populated by default. It is very convenient to measure the energy consumption of the KL28Z by a parallel voltmeter or a series ammeter.

4.2. Serial and debug adapter (OpenSDA)

OpenSDA is an open-standard serial and debug adapter. It bridges serial and debug communications between a USB host and an embedded target processor as shown in *Figure 4*. OpenSDA features a mass storage device (MSD) bootloader, which provides a quick and easy mechanism for loading different OpenSDA Applications such as flash programmers, run-control debug interfaces, serial-to-USB converters, and more. Two or more OpenSDA applications can run simultaneously. For example, run-control debug application and serial-to-USB converter runs in parallel to provide a virtual COM communication interface while allowing code debugging via OpenSDA with just single USB connection. These two applications are provided in a single code package. Refer to the OpenSDA User's Guide for more details.

OpenSDA is managed by a Kinetis K20 MCU built on the ARM Cortex-M4 core. The OpenSDA circuit includes a status LED (D1) and a RESET pushbutton (SW1). The pushbutton asserts the Reset signal to the KL28Z target MCU. It can also be used to place the OpenSDA circuit into bootloader mode by holding down the RESET pushbutton while plugging the USB cable to USB connector J13. Once the OpenSDA enters bootloader mode, other OpenSDA applications such as debug app can be programmed. SPI and GPIO signals provide an interface to the SWD debug port of the KL28Z. Additionally, signal connections are available to implement a UART serial channel. The OpenSDA circuit receives power when the USB connector J13 is plugged into a USB host.

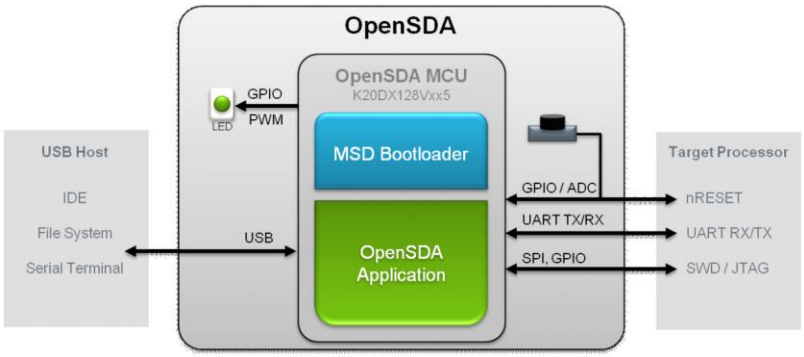

Figure 4. OpenSDA block diagram

4.2.1. Debugging interface

Signals with SPI and GPIO capability are used to connect directly to the SWD of the KL28Z. These signals are also brought out to a standard 10-pin Cortex Debug connector (J11) as shown in *Figure 5*.

In order to isolate the KL28Z MCU from the OpenSDA circuit and use J11 to connect to an off-board MCU, cut the trace between pin1 and pin2 of J18 on bottom layer. This will disconnect the SWD_CLK pin to the KL28Z so that it will interfere with the communications to an off-board MCU connected to J11. *Figure 5* shows SWD connector signals description for KL28Z.

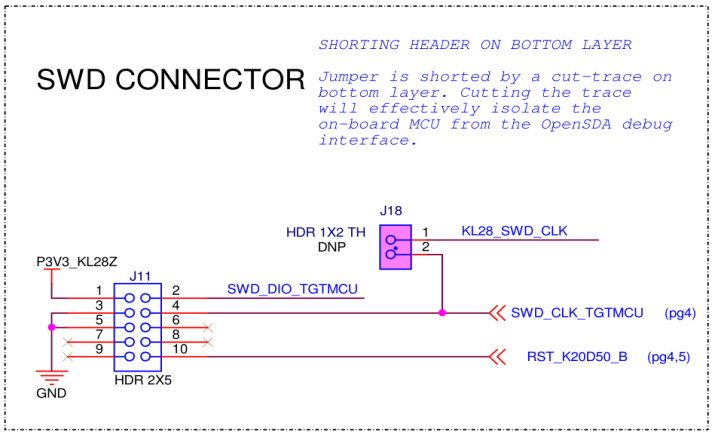

Figure 5. SWD debug connector to KL28Z

4.2.2. Virtual serial port

A serial port connection is available between the OpenSDA MCU and pins PTB16 and PTB17 of the KL28Z.Several of the default OpenSDA applications provided by Freescale, including the MSD Flash programmer and the P&E debug application, providing a USB communications device class (CDC) interface that bridges serial communications between the USB host and this serial interface.

4.3. Microcontroller

The FRDM-KL28Z is a MCU module featuring the MKL28Z512VLL7, a Kinetis microcontroller with USB 2.0 full-speed OTG controller in a 100 LQFP package. An on-board debug circuit, OpenSDA, provides a SWD interface and a power supply input through a mini-USB connector, as well as serial to USB and CDC class compliant UART interface. The KL28Z MCU features as shown in *Table 3*.

Table 3. Features of MKL28Z512VLL7

Feature	Description
Ultra-low-power	- 10 low-power modes with power and clock gating for optimal peripheral activity and recovery times. Stop currents of <190 nA (VLLS0), run currents of <280 uA/MHz, 4 s wake-up from Stop mode - Full memory and analog operation down to 1.71V for extended battery life - Low-leakage wake-up unit with up to eight internal modules and eight pins as wake-up sources in low-leakage stop (LLS)/very low-leakage stop (VLLS) modes - Low-power timer for continual system operation in reduced power states
Flash, SRAM, ROM	- 512 KB flash featuring fast access times, high reliability, and four levels of security protection. No user or system intervention to complete programming and erase functions and full operation down to 1.71 V - 128 KB of SRAM - 32 KB of ROM with Kinetis bootloader included (UART, SPI, I^2C, USB-HID)
Mixed-signal capability	- SAR 16-bit analog-to-digital converter (ADC) - High-speed comparator (CMP) with internal 6-bit digital-to-analog converter (DAC) - 12-bit digital-to-analog converter (DAC) - VREF module 1.2 V output
Performance	- 72 MHz ARM Cortex-M0+ core - Up to 16 channel DMA for peripheral and memory servicing with reduced CPU loading and faster system throughput - Cross bar switch enables concurrent multi-master bus accesses, increasing bus bandwidth - Independent flash banks allowing concurrent code execution and firmware updating with no performance degradation or complex coding routines - Bit manipulation engine (BME) allows execution of single-instruction atomic bit-modify-write operations on the peripheral address space
Timing and control	- Three timer/PWM modules – one with six channel, and two with two channels - Low-power timer - Real-time clock - 4-channel 32-bit periodic interrupt timer provides time base for RTOS task scheduler or trigger source for ADC conversion, provides lifetime timer capability
Human-machine interface Connectivity and communications	- Touch sensing input - General-purpose input/output up to 54 - USB full-speed OTG controller with on-chip transceiver and 5 V to 3.3 V regulator, supporting crystal-less recovery - USB low-voltage regulator supplies up to 120 mA off chip at 3.3 volts to power external components from 5-volt input - Three 32-bit LPSPI modules - Three LPUART modules - Three LPI2C modules supporting Ultra-Fast mode - One I^2S (SAI) module - FlexIO module

4.3.1. Clock source

KL28Z start up to the default reset clock for core/system clock, which is 8 MHz from SIRC. Software can enable the main external oscillator (EXTAL/XTAL), or to high frequency internal reference (FIRC) 48 MHz if desired. The external oscillator/resonator can range from 32.768 KHz up to 32 MHz. A 32.768 KHz crystal is the default external source for the SCG oscillator inputs (XTAL/EXTAL).

4.3.2. Serial port

The primary serial port interface signals are PTB16 and PTB17. These signals are connected to both the OpenSDA and to the J1 I/O connector. Note that the OpenSDA connection can be isolated from J1 by removing R47 and R48, if required.

4.3.3. USB port

The Kinetis KL28 microcontroller features a dual-role USB controller with on-chip full-speed and low-speed transceivers. The USB interface on the FRDM-KL28Z is configured as a full-speed USB device. J10 is the USB connector for this interface. As shown in *Figure 6.*

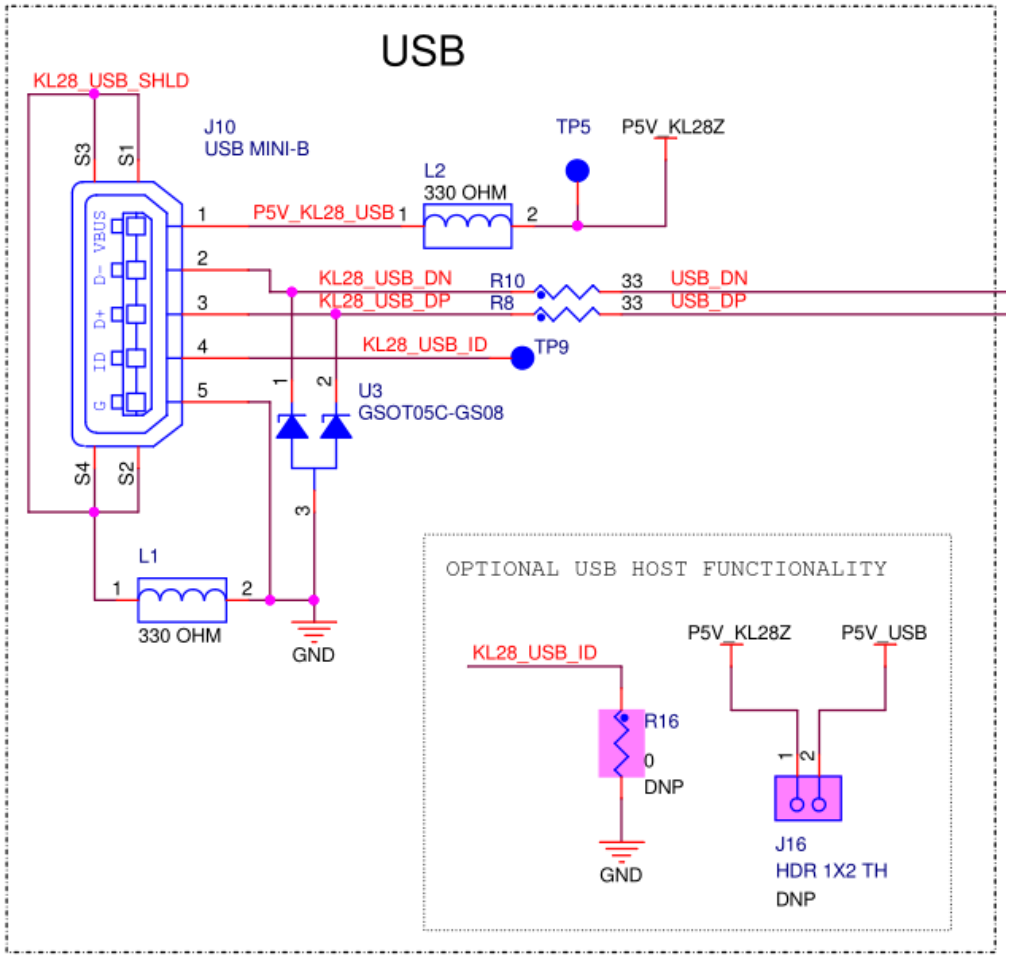

Figure 6. USB connector schematic

4.3.4. Reset

The PTA20/RESET signal on the KL28Z is connected externally to a pushbutton, SW1, and also to the OpenSDA circuit. However, R76 should be removed when isolating the OpenSDA MCU from SW1 or to do power consumption testing for KL28Z. Isolating the RESET line allows a more accurate measurement of the target device's power consumption in low-power modes. The reset button can be used to force an external reset event in the target MCU.

4.3.5. Debug

The sole debug interface on all Kinetis L series devices is a Serial Wire Debug (SWD) port. The primary controller of this interface on the FRDM-KL28Z is the onboard OpenSDA circuit. However, a 2x5-pin Cortex Debug connector, J11, provides access to the SWD signals for the KL28Z MCU. The following table shows SWD connector signals description for KL28Z.

Table 4. ARM JTAG/SWD mini connector description

Pin	Function	Connection to KL28Z
1	VTref	P3V3_MCU
2	SWDIO/TMS	PTA3
3	GND	GND
4	SWDCLK/TCK	PTA0
5	GND	GND
6	SWO/TDO	NC
7	NC	NC
8	TDI	NC
9	NC	NC
10	RESET	PTA20

4.4. Capacitive touch slider

Two GPIO pins functioning as Touch Sense Input (TSI) signals, are connected to capacitive electrodes configured as a touch slider as shown in *Figure 7*.

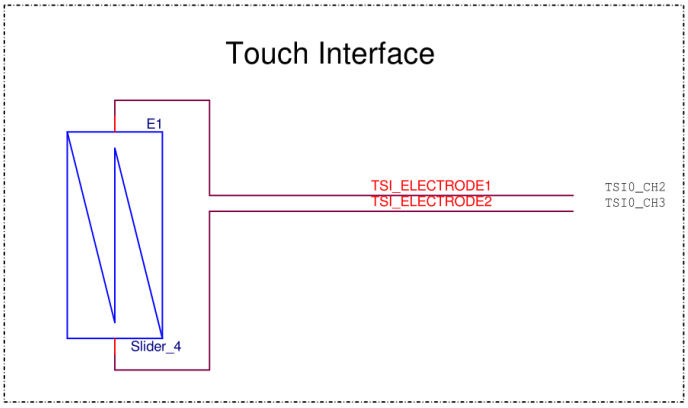

Figure 7. Touch slider connection

4.5. I2C Inertial Sensor

4.5.1. 6-axis accelerometer and magnetometer

FXOS8700CQ is a small, low-power, 3-axis, linear accelerometer, and 3-axis magnetometer combined into a single package. The device features a selectable I^2C or point-to-point SPI serial interface with 14-bit accelerometer and 16-bit magnetometer ADC resolution along with smart-embedded functions. It is interfaced through an I^2C bus and two GPIO signals as shown in *Figure 8* and the table below.

By default, the I^2C address is 0x1E (As SA0 and SA1 were pulled low).

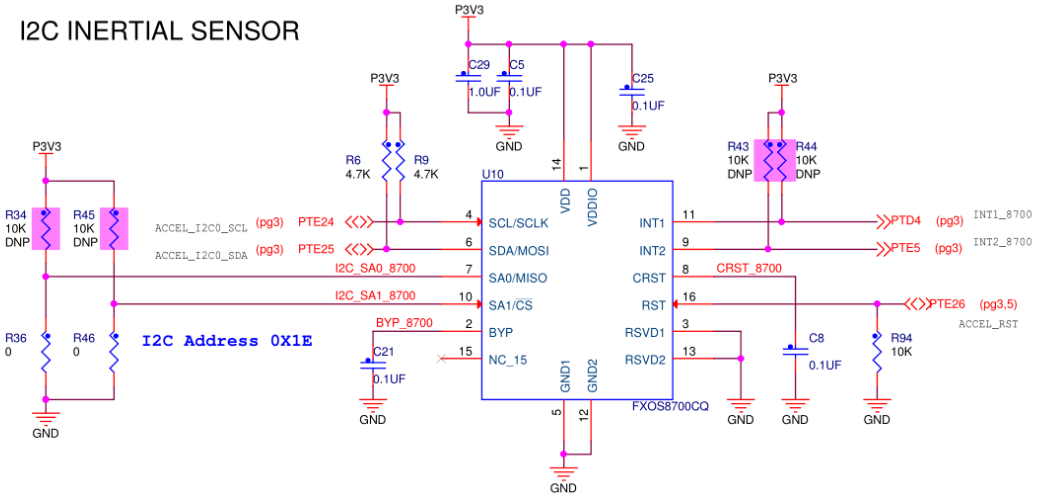

Figure 8. FXOS8700CQ schematic diagram

Table 5. Accelerometer FXOS8700CQ signal connections

FX0S8700CQ	KL28Z
SCL	PTE24
SDA	PTE25
INT1	PTD4
INT2	PTE5

4.5.2. 3-Axis Digital Angular Rate Gyroscope

FXAS21002C is a small, low-power, pitch, and roll angular rate gyroscope with 16 bit ADC resolution. The full-scale range is adjustable from ±250°/s to ±2000°/s. It features both I2C and SPI interfaces. It is interfaced through an I2C bus and two GPIO signals as shown in the following table and *Figure 9*. By default, the I2C address is 0x20 (As SA0 pulled low).

Table 6. Gyroscope FXAS21002CQ signal connections

FXAS21002CQ	KL28Z
SCL	PTE24
SDA	PTE25
INT1	PTE0
INT2	PTE1

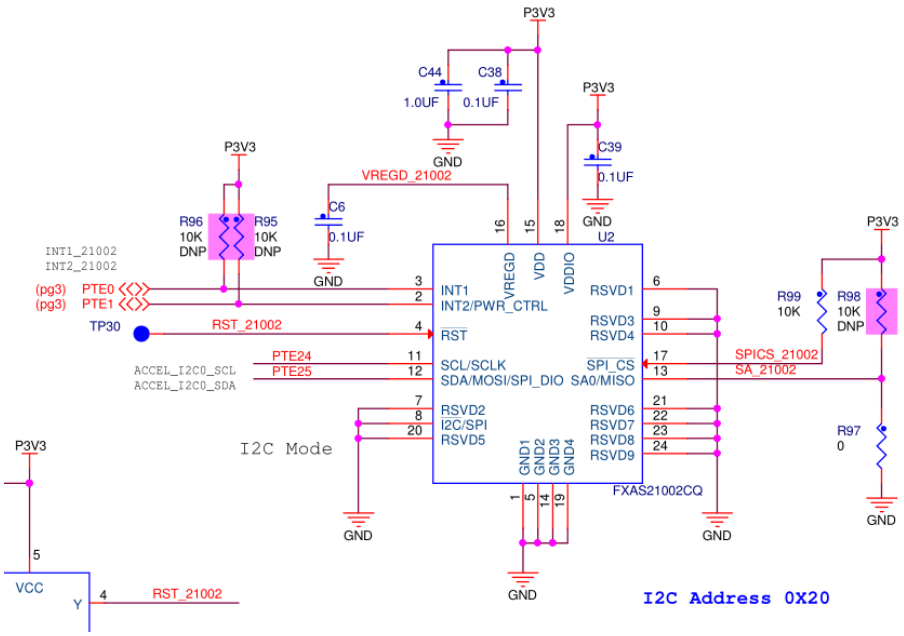

Figure 9. FXAS21002C schematic diagram

4.6. RGB LED

Three PWM-capable KL28Z signals are connected to a red, green, and blue LED.

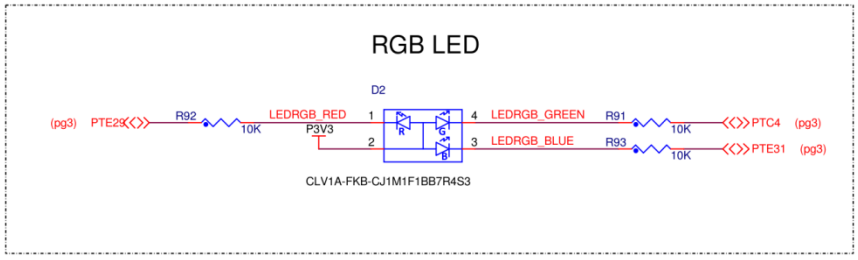

Figure 10. RGB schematic diagram

As is shown in *Figure 10*, the signal connections are shown in the following table.

Table 7. Gyroscope FXAS21002CQ signal connections

RGB LED	KL28Z
Red Cathode	PTE29
Green Cathode	PTC4
Blue Cathode	PTE31

4.7. Visible light sensor

An ambient light sensor is connected to PTD5, which is shown in *Figure 11*.

This sensor may be isolated from PTE22 by removing J8.

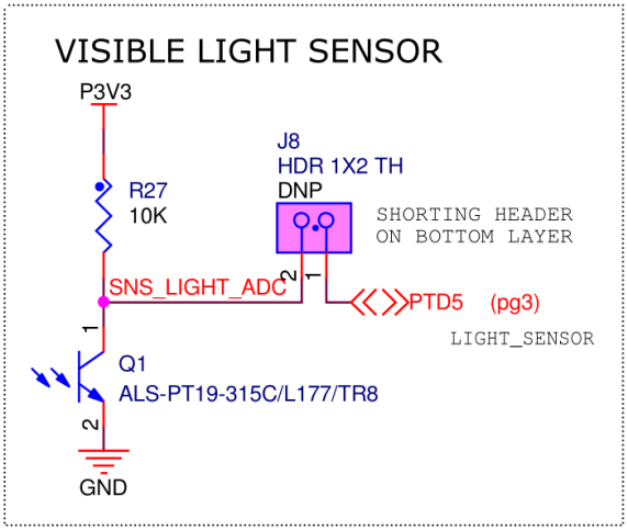

Figure 11. Visible light sensor schematic diagram

4.8. EMVSIM Header

The EMVSIM (Euro/Mastercard/Visa/SIM Serial Interface Module) is a standalone ISO 7816 module that is connected to the AIPS0 Peripheral Bridge. The EMVSIM module's clock source is the CPU/platform clock (as shown in *Figure 12*). The following table shows the user-accessible signals available on EMVSIM. These signals are actually connected to the external pins by JP1.

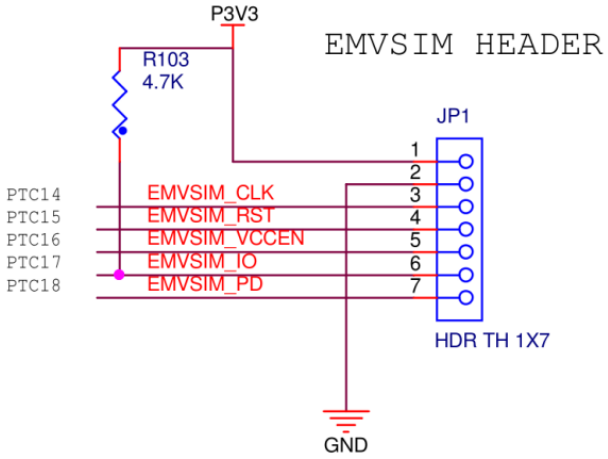

Figure 12. Visible light EMVSIM Header

Table 8. User-accessible signals available on EMVSIM

JP1 pin	KL28Z	Signal name	Description
1	—	Vcc	3.3 V source
2	—	GND	—
3	PTC14	EMVSIM_SCLK	Card Clock. Clock to Smart Card
4	PTC15	EMVSIM_SRST	Card Reset. Reset signal to Smart Card
5	PTC16	EMVSIM_VCC_EN	Card Power Enable. This signal controls the power to Smart Card
6	PTC17	EMVSIM_IO	Card Data Line. Bi-directional data line
7	PTC18	EMVSIM_PD	Card Presence Detect. Signal indicating presence or removal of card

4.9. SPI2 Header

The LPSPI is a low power Serial Peripheral Interface (SPI) module that supports an efficient interface to an SPI bus as a master and/or a slave. *Figure 13* and the following table show the output connections and its functions.

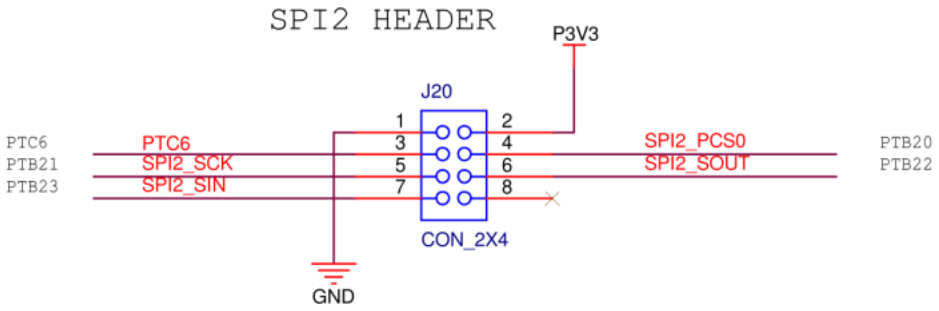

Figure 13. Header SPI2 Header

Table 9. SPI2 Header connections

J20 pin	Signal name	Connected to KL28Z pin	Description
1	GND	—	—
2	VCC3.3V	—	—
3	NC	PTC6	—
4	SPI2_PCS0	PTB20	Peripheral Chip Select
5	SPI2_SCK	PTB21	Serial clock
6	SPI2_SOUT	PTB22	Serial Data Output
7	SPI2_SIN	PTB23	Serial Data Input
8	NC	—	—

4.10. Analog reference voltage

The onboard ADC of the FRDM KL28Z uses the Reference Voltage High (VREFH) and Reference Voltage Low (VREFL) pins to set high and low voltage references for the analog modules. By default VREFH is attached to P3V3_KL28Z (3.3 V Supply). VREFL is connected to GND.

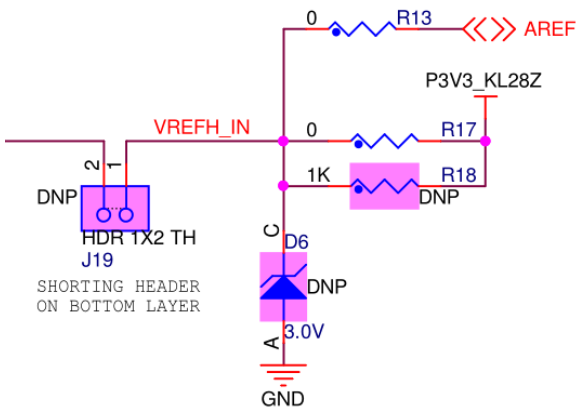

Figure 14. VREFH circuit schematic

If desired, VREFH can use a VDDA independent reference by adding R18 and a Zener diode (D6). R17 (0 Ω resistor) must be removed when implementing this option. Alternatively, VREFH can be attached to an external source through AREF by removing R17 and populating R13 with a 0 Ω resistor.

4.11. Input/output headers

The MKL28 MCU is packaged in a 100-pin LQFP. Some pins are utilized by on-board circuitry, but many are directly connected to one of four I/O headers (J1, J2, J3, and J4) as shown in the following image.

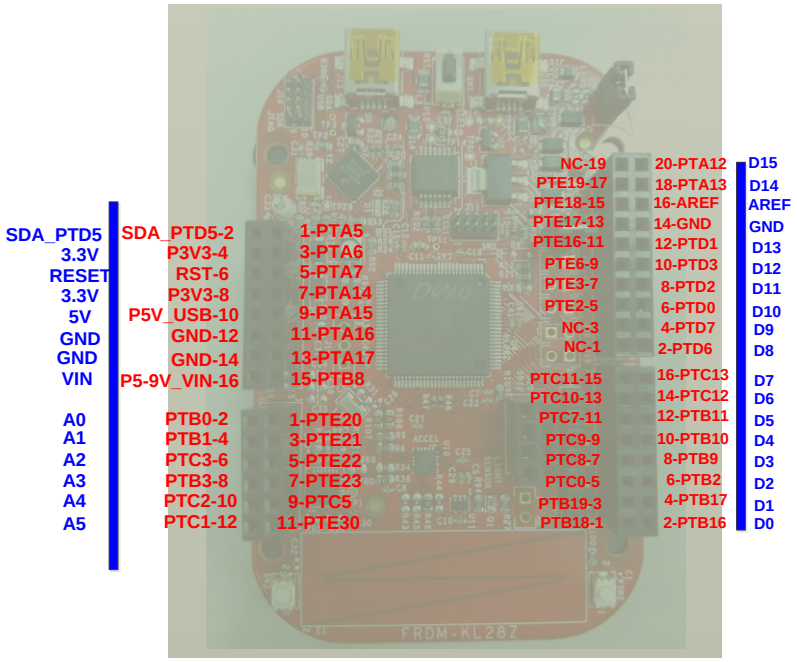

Figure 15. Input/output headers

5. References

The reference documents for the FRDM-KL28Z hardware are shown below. All documents can be found at nxp.com

- FRDM-KL28Z Quick Start Guide
- FRDM-KL28Z User's Guide
- FRDM-KL28Z Schematics PDF
- OpenSDA User's Guide (document OPENSDAUG)
- KL28 Sub-Family Reference Manual

6. Revision History

Table 10. Revision history

Revision number	Date	Substantive changes
0	06/2016	Initial release

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