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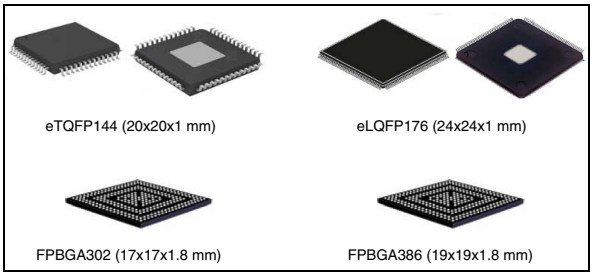
SPC58EHx, SPC58NHx

A scalable approach for high-end body, networking and security platforms for Automotive

Data brief



Features

- AEC-Q100 qualified
- High performance e200z4 triple core:
  - 32-bit Power Architecture technology CPU
  - Core frequency as high as 200 MHz
  - Variable Length Encoding (VLE)
  - Floating Point, End-to-End Error Correction
- 10496 KB (10240 KB code Flash + 256 KB data Flash) on-chip Flash memory:
  - Supports read during program and erase operations, and multiple blocks allowing EEPROM emulation
  - Supports read while read between the two code Flash partitions
  - Hardware support for Flash context switching (for FOTA with multi software versions)
- 1088 KB on-chip general-purpose SRAM (in addition to 192 KB core local data RAM):
  - 64 KB in CPU_0, 64 KB in CPU_1 and 64 KB in CPU_2
- 224 KB HSM dedicated Flash memory (192 KB code + 32 KB data)
- Multi-channel direct memory access controller (eDMA):
  - One eDMA with 64 channels
  - One eDMA with 16 channels
- One interrupt controller (INTC)
- Comprehensive new generation ASIL-D safety concept:
  - ASIL-D of ISO 26262
  - One CPU channel in lockstep
  - Logic BIST
  - FCCU for collection and reaction to failure notifications
  - Memory BIST
  - Cyclic redundancy check (CRC) unit
  - Memory Error Management Unit (MEMU) for collection and reporting of error events in memories
- Crossbar switch architecture for concurrent access to peripherals, Flash, or RAM from multiple bus masters with end-to-end ECC
- Body cross triggering unit (BCTU):
  - Triggers ADC conversions from any eMIOS channel
  - Triggers ADC conversions from up to 2 dedicated PIT_RTIs
- Enhanced modular IO subsystem (eMIOS):
  - up to 96 timed IO channels with 16-bit counter resolution
- Enhanced analog-to-digital converter system with:
  - 4 independent fast 12-bit SAR analog converters
  - One supervisor 12-bit SAR analog converter
  - One standby 10-bit SAR analog converter
  - 100 ADC channels
- Communication interfaces:
  - 24 LINFlexD modules
  - 10 deserial serial peripheral interface (DSPI) modules
  - 1 deserial serial peripheral interface (DSPI_LP) module available in low power mode

  - 16 MCAN interfaces with advanced shared memory scheme and ISO CAN-FD support
  - Dual-channel FlexRay controller
  - One SD/SDIO/eMMC module
  - One OctalSPI module with double Chip Select
  - Two independent Ethernet controllers, one 10/100Mbps and the other one 10/100Mbps or 1Gbps, compliant IEEE 802.3-2008 and OPEN RGMII EPL v2.3
  - Four I^2C modules
  - Two PSI5 modules
- Low power capabilities:
  - Versatile low power modes
  - Ultra low power standby with RTC
  - Smart Wake-up Unit for contact monitoring
  - Fast wakeup schemes
- Dual phase-locked loops with stable clock domain for peripherals and FM modulation domain for computational shell
- Nexus development interface (NDI) per IEEE-ISTO 5001-2003 standard, with some support for 2010 standard
- Boot assist Flash (BAF) supports factory programming using a serial bootload through the asynchronous CAN or LIN/UART
- Low power supply options:
  - Single internal linear regulator with external ballast
  - External low voltage supply (1.2 V)
- Temperature range:
  - -40 °C to 105 °C
  - -40 °C to 125 °C

Table 1. Device summary

Package	Part number					
	6 MB		8 MB		10 MB	
	Dual core	Triple core	Dual core	Triple core	Dual core	Triple core
eTQFP144	SPC58EH84E5	SPC58NH84E5	SPC58EH90E5	SPC58NH90E5	SPC58EH92E5	SPC58NH92E5
eLQFP176	SPC58EH84E7	SPC58NH84E7	SPC58EH90E7	SPC58NH90E7	SPC58EH92E7	SPC58NH92E7
FPBGA302	SPC58EH84C3	SPC58NH84C3	SPC58EH90C3	SPC58NH90C3	SPC58EH92C3	SPC58NH92C3
FPBGA386	SPC58EH84C5	SPC58NH84C5	SPC58EH90C5	SPC58NH90C5	SPC58EH92C5	SPC58NH92C5

1 Description

The SPC58 H Line is a general-purpose MCU targeting high-end Body, Networking and Security applications. SPC58 H Line extends the Chorus Series of successful 40nm Automotive MCUs. and offers a seamless extension with compatible devices from 2 M up to 10 Mbytes Flash. Combining the 3x PowerPC cores (200Mhz) with a rich set of communication interfaces like 2x Ethernet, 16x ISO CAN FD and 24x LIN, it introduces new features to support Connected Gateway applications with Gigabit ethernet MAC for fast download, an hyperbus interface to extend the internal RAM and the eMMC interface to allow big data file storage.

To manage OTA update while the application keeps running, the 10 Mbyte flash can be programmed in background and its context swapped on reset.

The Smart Standby domain including RAM, RTC, ADC and a new low power SPI module increases the contact monitoring capability keeping the consumption extremely low (< 160 µA) and guaranteeing a fast start-up on wake-up event (< 500 µs).

The SPC58 H Line offers the highest performance and integrated devices available in high-efficiency pin count packages like eTQFP144 fully scalable up to FPBGA386. Designed according to ISO 26262, the SPC58 H Line supports ASIL-B/D offering 1 lockstep core as well as a EVITA full Security supporting asymmetric keys. With its 100 Mbit IPC the Chorus H Line is designed for system scalability coupling 2 Chorus H devices to build a system with 6 cores, 20 Mbytes flash and 2x Gigabit ethernet.

2 Software Library and Tools

The product family is provided as a set of software libraries to enable application development. The libraries are available on *www.st.com* and they include:

- Flash drivers for run-time and off-line device programming
- MCAL drivers
- Core Self Test
- Security Firmware for HSM

Additional software components and tools are available by selected 3rd parties:

Figure 1. Software components and tools

3 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: *www.st.com*.

ECOPACK is an ST trademark.

4 Revision history

Table 2. Document revision history

Date	Revision	Changes
17-Oct-2018	1	Initial release.
15-Jul-2020	2	Updated: – *Features on page 1* – *Figure 1: Software components and tools*