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NTE74LS112A
Integrated Circuit
TTL – Dual J–K Negative Edge Triggered Flip–Flop with Preset and Clear

Description:

The NTE74LS112A contains two independent J–K negative–edge–triggered flip–flops in a 16–Lead plastic DIP type package. A low level at the preset or clear inputs sets or resets the outputs regardless of the levels of the other inputs. When preset and clear are inactive (high), data at the J and K inputs meeting the setup time requirements are transferred to the outputs on the negative–going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold time interval, data at the J and K inputs may be changed without affecting the levels at the outputs. This versatile flip–flop can perform as a toggle flip–flop by tying J and K high.

Absolute Maximum Ratings: (Note 1)

Supply Voltage, V_{CC} 7V

DC Input Voltage, V_{IN} 7V

Operating Temperature Range, T_A . . . . . 0°C to +70°C

Storage Temperature Range, T_{stg} . . . . . –65°C to +150°C

Note 1. Unless otherwise specified, all voltages are referenced to GND.

Recommended Operating Conditions:

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.75	5.0	5.25	V
High–Level Input Voltage	V_{IH}	2.0	–	–	V
Low–Level Input Voltage	V_{IL}	–	–	0.8	V
High–Level Output Current	I_{OH}	–	–	–1	mA
Low–Level Output Current	I_{OL}	–	–	20	mA
Clock Frequency	f_{clock}	0	–	25	MHz
Pulse Duration CLK High	t_w	6.0	–	–	ns
CLK Low		6.5	–	–	ns
$\overline{PRE}$ or $\overline{CLR}$ Low		8.0	–	–	ns
Setup Time before CLK↓ (Data High or Low)	t_{su}	3	–	–	ns
Hold Time Data after CLK↓	t_h	0	–	–	ns
Operating Temperature Range	T_A	0	–	+70	°C

Electrical Characteristics: (Note 2, Note 3)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Clamp Voltage	V_{IK}	V_{CC} = MIN, I_I = −18mA	–	–	−1.2	V
High Level Output Voltage	V_{OH}	V_{CC} = MIN, V_{IH} = 2V, V_{IL} = 0.8V, I_{OH} = −1mA	2.7	3.4	–	V
Low Level Output Voltage	V_{OL}	V_{CC} = MIN, V_{IH} = 2V, V_{IL} = 0.8V, I_{OL} = 20mA	–	–	0.5	V
Input Current	I_I	V_{CC} = MAX, V_I = 5.5V	–	–	1	mA
High Level Input Current J or K	I_{IH}	V_{CC} = MAX, V_I = 2.7V	–	–	50	μA
All Other			–	–	100	μA
Low Level Input Current J or K	I_{IL}	V_{CC} = MAX, V_I = 0.5V	–	–	−1.6	mA
$\overline{CLR}$ (Note 6)			–	–	−7	mA
$\overline{PRE}$ (Note 6)			–	–	−7	mA
CLK			–	–	−4	mA
Short−Circuit Output Current	I_{OS}	V_{CC} = MAX, Note 4	−40	–	−100	mA
Supply Current	I_{CC}	V_{CC} = MAX, Note 5	–	15	25	mA

Note 2. .For conditions shown as MIN or MAX, use the appropriate value specified under “Recommended Operation Conditions”.

Note 3. All typical values are at V_{CC} = 5V, T_A = +25°C.

Note 4. For certain devices where state commutation can be caused by shorting an output to GND, an equivalent test may be performed with V_O = 2.125V and the minimum and maximum limits reduced to one half of their stated values.

Note 5. With all outputs open, I_{CC} is measured with the Q and $\overline{Q}$ outputs high in turn. At the time of measurement, the clock input is grounded.

Note 6. Clear is tested with preset high and preset is tested with clear high.

Switching Characteristics: (V_{CC} = 5V, T_A = +25°C unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Maximum Clock Frequency	t_{max}	R_L = 280Ω, C_L = 15pF	80	125	–	MHz
Propagation Delay Time From $\overline{PRE}$ or $\overline{CLR}$ Input to Q or $\overline{Q}$ Output	t_{PLH}		–	4	7	ns
From $\overline{PRE}$ or $\overline{CLR}$ (CLK High) Input to Q or $\overline{Q}$ Output	t_{PHL}		–	5	7	ns
From $\overline{PRE}$ or $\overline{CLR}$ (CLK Low) Input to Q or $\overline{Q}$ Output			–	5	7	ns
Propagation Delay Time (From CLK Input to Q or $\overline{Q}$ Output)	t_{PLH}		–	4	7	ns
	t_{PHL}		–	5	7	ns

Function Table (Each Flip−Flop):

Inputs					Outputs	
$\overline{PRE}$	$\overline{CLR}$	CLK	J	K	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H†	H†
H	H	↓	L	L	Q_0	$\overline{Q}_0$
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	Toggle	
H	H	H	X	X	Q_0	$\overline{Q}_0$

† The output levels in this configuration are not guaranteed to meet the minimum levels for V_{OH} if the lows at preset and clear are near V_{IL} maximum. Furthermore, this configuration is nonstable; that is, it will not persist when preset or clear return to their inactive (high) level.

Pin Connection Diagram