

High Sound Quality Audio D/A Converters

32-bit, 768 kHz Sampling

Stereo Audio D/A Converter

BD34352EKV

General Description

BD34352EKV is 32-bit high sound quality Stereo Audio D/A converter with ROHM original sound quality design, realizing excellent numerical performance (SNR: 126 dB (Typ), THD+N: -112 dB (Typ)) suitable for high-end audio. Favourite sound is selectable by switching 2 kinds of digital FIR filters (Sharp Roll-Off, Slow Roll-Off). PCM I/F supports up to 768 kHz and DSD I/F supports up to 22.4 MHz.

Features

- SNR 126 dB (Typ), THD+N -112 dB (Typ) (Note 1)
- Sampling Frequency 32 kHz to 768 kHz (Note 1)
- 2 Kinds of Digital FIR Filters (Note 1)
- DSD 2.8 MHz, 5.6 MHz, 11.2 MHz, 22.4 MHz Available
- Supports Stereo Mode (2ch) and Mono Mode (1ch)
- Selectable 4 Device Addresses (38h, 3Ah, 3Ch, 3Eh)

Applications

- CD/SACD Player
- Digital Audio Player (DAP)
- USB-DAC and Others

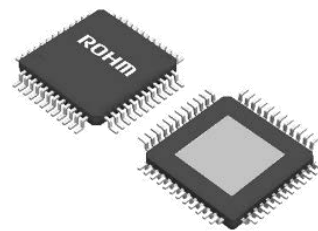
Key Specifications

- Supply Voltage Range of AVCC (Note 2) 4.5 V to 5.5 V
- Supply Voltage Range of DVDD 1.4 V to 1.6 V
- Supply Voltage Range of DVDDIO 3.0 V to 3.6 V
- SNR (Note 1) 126 dB (Typ)
- THD+N (Note 1) -112 dB (Typ)
- Dynamic Range (Note 1) 126 dB (Typ)
- Operation Temperature Range -25 °C to +85 °C

Package

HTQFP64BV

W (Typ) x D (Typ) x H (Max)
12.0 mm x 12.0 mm x 1.0 mm



(Note 1) PCM mode

(Note 2) AVCC, AVCC_R and AVCC_L in Typical Application Circuit

Typical Application Circuit

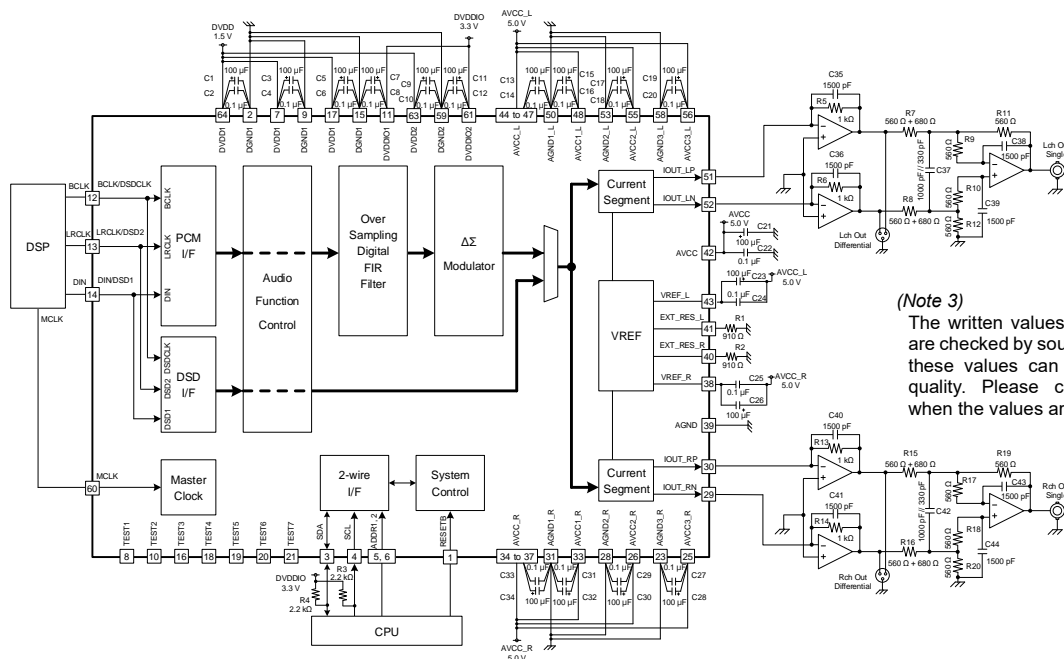


Figure 1. Typical Application Circuit

(Note 3)

The written values of external parts are checked by sound test. Changing these values can affect the sound quality. Please check the sound when the values are changed.

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Pin Configuration

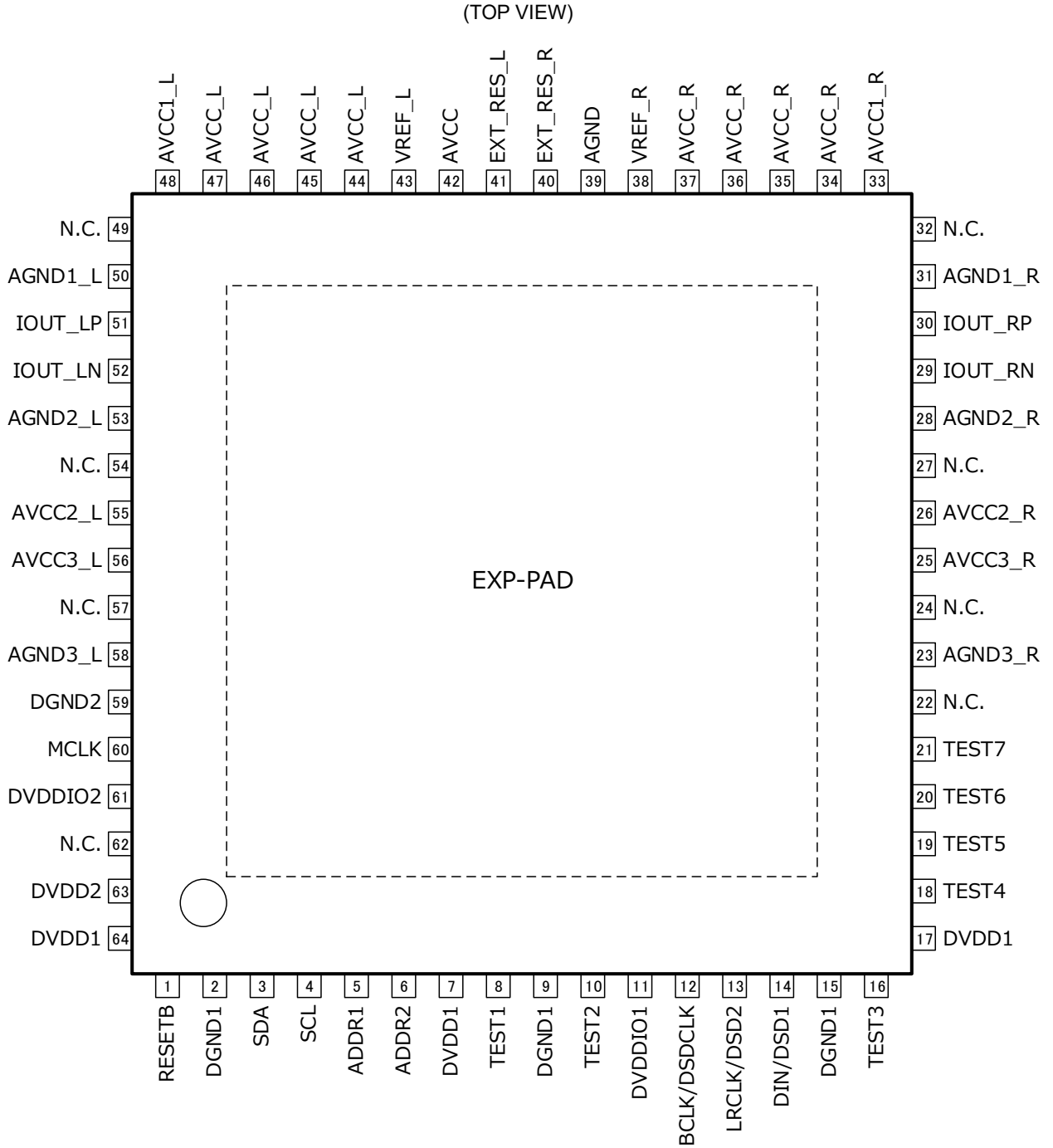


Figure 2. Pin Configuration

Caution:

Open the N.C. pins and the TEST pins (TEST1 to TEST7).
The EXP-PAD should be connect to AGND.

Pin Descriptions

Pin No.	Pin Name	D/A ^(Note 1)	I/O ^(Note 2)	Function
1	RESETB	D	I	Reset (L: Reset)
2	DGND1	D	-	Digital ground
3	SDA	D	I/O	2-wire I/F data ^(Note 3)
4	SCL	D	I	2-wire I/F clock
5	ADDR1	D	I	2-wire I/F device address selector1 (38h/3Ah/3Ch/3Eh)
6	ADDR2	D	I	2-wire I/F device address selector2 (38h/3Ah/3Ch/3Eh)
7	DVDD1	D	-	Digital core power supply (1.5 V)
8	TEST1	D	I	The TEST pin ^(Note 4)
9	DGND1	D	-	Digital ground
10	TEST2	D	I	The TEST pin ^(Note 4)
11	DVDDIO1	D	-	Digital I/O power supply (3.3 V)
12	BCLK/DSDCLK	D	I	PCM I/F bit clock / DSD clock
13	LRCLK/DSD2	D	I	PCM I/F LR clock / DSD2 data
14	DIN/DSD1	D	I	PCM I/F serial data / DSD1 data
15	DGND1	D	-	Digital ground
16	TEST3	D	I	The TEST pin ^(Note 4)
17	DVDD1	D	-	Digital core power supply (1.5 V)
18	TEST4	D	I	The TEST pin ^(Note 4)
19	TEST5	D	I	The TEST pin ^(Note 4)
20	TEST6	D	I	The TEST pin ^(Note 4)
21	TEST7	D	I	The TEST pin ^(Note 4)
22	N.C.	-	-	No connection ^(Note 4)
23	AGND3_R	A	-	Rch analog ground
24	N.C.	-	-	No connection ^(Note 4)
25	AVCC3_R	A	-	Rch analog power supply (5.0 V)
26	AVCC2_R	A	-	Rch analog power supply (5.0 V)
27	N.C.	-	-	No connection ^(Note 4)
28	AGND2_R	A	-	Rch analog ground
29	IOUT_RN	A	O	Rch negative output
30	IOUT_RP	A	O	Rch positive output
31	AGND1_R	A	-	Rch analog ground
32	N.C.	-	-	No connection ^(Note 4)

Pin Descriptions - continued

Pin No.	Pin Name	D/A ^(Note 1)	I/O ^(Note 2)	Function
33	AVCC1_R	A	-	Rch analog power supply (5.0 V)
34	AVCC_R	A	-	Rch analog power supply for Current Segment (5.0 V)
35	AVCC_R	A	-	Rch analog power supply for Current Segment (5.0 V)
36	AVCC_R	A	-	Rch analog power supply for Current Segment (5.0 V)
37	AVCC_R	A	-	Rch analog power supply for Current Segment (5.0 V)
38	VREF_R	A	O	Rch external capacitor (Recommended: 0.1 μ F + 100 μ F)
39	AGND	A	-	Analog ground
40	EXT_RES_R	A	O	Rch external register (Recommended: 910 Ω)
41	EXT_RES_L	A	O	Lch external register (Recommended: 910 Ω)
42	AVCC	A	-	Analog power supply (5.0 V)
43	VREF_L	A	O	Lch external capacitor (Recommended: 0.1 μ F + 100 μ F)
44	AVCC_L	A	-	Lch analog power supply for Current Segment (5.0 V)
45	AVCC_L	A	-	Lch analog power supply for Current Segment (5.0 V)
46	AVCC_L	A	-	Lch analog power supply for Current Segment (5.0 V)
47	AVCC_L	A	-	Lch analog power supply for Current Segment (5.0 V)
48	AVCC1_L	A	-	Lch analog power supply (5.0 V)
49	N.C.	-	-	No connection ^(Note 4)
50	AGND1_L	A	-	Lch analog ground
51	IOUT_LP	A	O	Lch positive output
52	IOUT_LN	A	O	Lch negative output
53	AGND2_L	A	-	Lch analog ground
54	N.C.	-	-	No connection ^(Note 4)
55	AVCC2_L	A	-	Lch analog power supply (5.0 V)
56	AVCC3_L	A	-	Lch analog power supply (5.0 V)
57	N.C.	-	-	No connection ^(Note 4)
58	AGND3_L	A	-	Lch analog ground
59	DGND2	D	-	Digital ground for MCLK
60	MCLK	D	I	Master clock
61	DVDDIO2	D	-	Digital I/O power supply for MCLK (3.3 V)
62	N.C.	-	-	No connection ^(Note 4)
63	DVDD2	D	-	Digital power supply for MCLK (1.5 V)
64	DVDD1	D	-	Digital core power supply (1.5 V)
-	EXP_PAD	-	-	Connect the EXP-PAD to AGND.

(Note 1) D/A means D: Digital pin, A: Analog pin.

(Note 2) I/O means I: Input, O: Output.

(Note 3) In 2-wire I/F operation, this pin becomes open-drain output.

(Note 4) Open the N.C. pins and TEST pins (TEST1 to TEST7)

Block Diagram

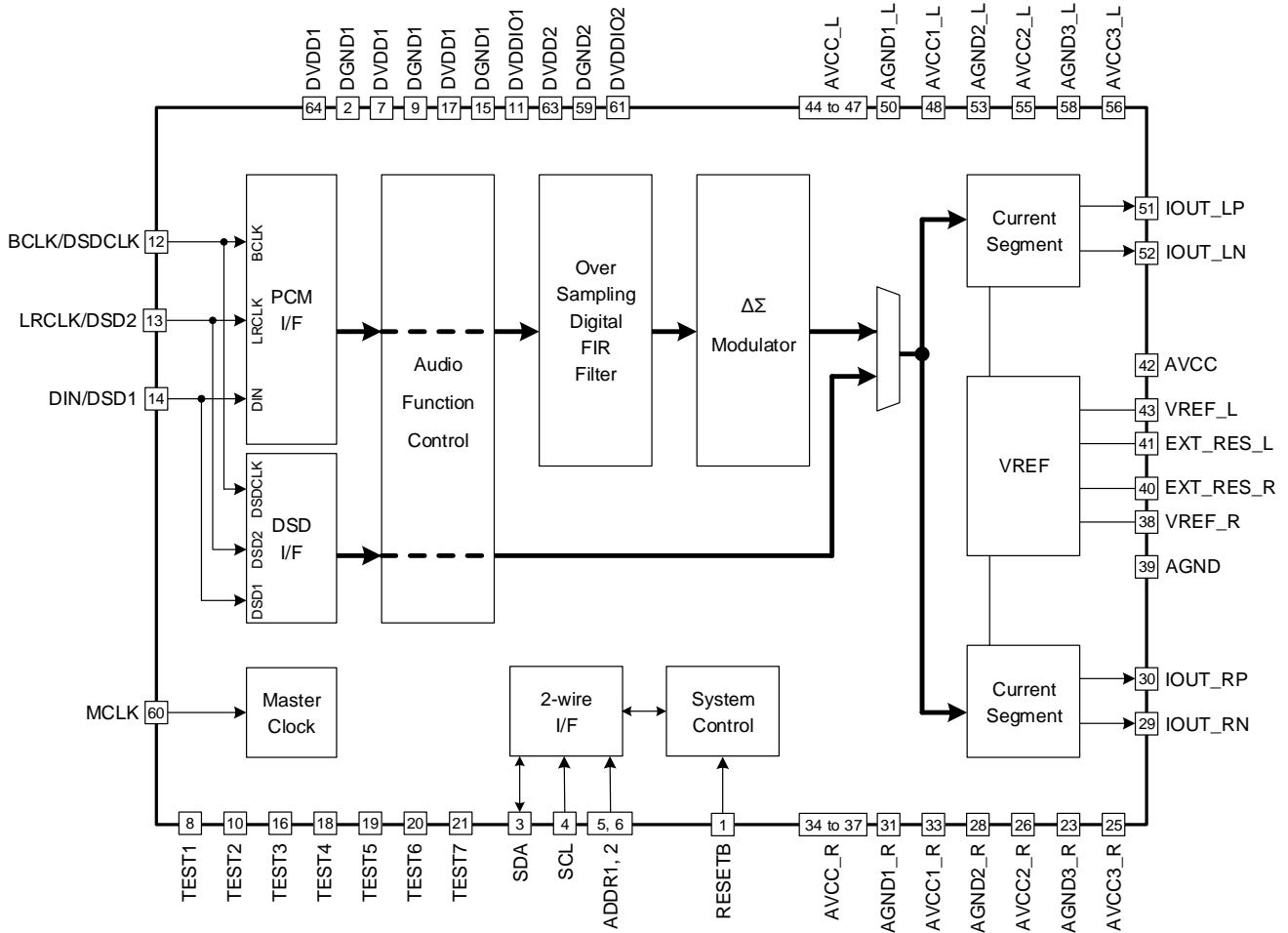


Figure 3. Block Diagram

Table 1. Description of Blocks

Block	Description
PCM I/F	Digital audio interface for PCM audio format 2ch stereo Supports 32 kHz to 768 kHz input sampling frequency Supports 16-bit to 32-bit data formats BCLK = 64 fs
DSD I/F	Digital audio interface for DSD audio format 2ch stereo Supports 2.8 MHz, 5.6 MHz, 11.2 MHz, 22.4 MHz DSD
Master Clock	Clock control
2-wire I/F	2-wire interface block for register settings Supports 400 kHz data transmission speed 4 device addresses (38h, 3Ah, 3Ch, 3Eh) are selectable
System Control	System control by register setting
Audio Function Control	Audio format control PCM mode: LR swap -> stereo/mono -> polarity inversion DSD mode: stereo/mono -> LR swap -> polarity inversion
Over Sampling Digital FIR Filter	Over sampling digital FIR filter Sharp Roll-Off / Slow Roll-Off filter are selectable
ΔΣ Modulator	ΔΣ modulator
Current Segment	Current segment
VREF	Voltage reference

Absolute Maximum Ratings (Ta = 25 °C)

Parameter	Symbol	Rating	Unit
Supply Voltage	AVCC	7.0	V
	DVDDIO	7.0	
	DVDD	2.1	
Input Voltage	Vin	-0.3 to DVDDIO + 0.3	V
Storage Temperature Range	Tstg	-55 to +150	°C
Maximum Junction Temperature	Tjmax	150	°C

Caution 1: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

Caution 2: Should by any chance the maximum junction temperature rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, design a PCB with thermal resistance taken into consideration by increasing board size and copper area so as not to exceed the maximum junction temperature rating.

Thermal Resistance^(Note 1)

Parameter	Symbol	Thermal Resistance (Typ)		Unit
		1s ^(Note 3)	2s2p ^(Note 4)	
HTQFP64BV				
Junction to Ambient	θ_{JA}	64.5	16.1	°C/W
Junction to Top Characterization Parameter ^(Note 2)	Ψ_{JT}	3	2	°C/W

(Note 1) Based on JESD51-2A(Still-Air).

(Note 2) The thermal characterization parameter to report the difference between junction temperature and the temperature at the top center of the outside surface of the component package.

(Note 3) Using a PCB board based on JESD51-3.

(Note 4) Using a PCB board based on JESD51-7.

Layer Number of Measurement Board	Material	Board Size
Single	FR-4	114.3 mm x 76.2 mm x 1.57 mmt

Top	
Copper Pattern	Thickness
Footprints and Traces	70 μ m

Layer Number of Measurement Board	Material	Board Size	Thermal Via ^(Note 5)		
			Pitch	Diameter	
4 Layers	FR-4	114.3 mm x 76.2 mm x 1.6 mmt	1.20 mm	Φ 0.30 mm	
Top		2 Internal Layers		Bottom	
Copper Pattern	Thickness	Copper Pattern	Thickness	Copper Pattern	Thickness
Footprints and Traces	70 μ m	74.2 mm x 74.2 mm	35 μ m	74.2 mm x 74.2 mm	70 μ m

(Note 5) This thermal via connects with the copper pattern of all layers.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Operating Supply Voltage	AVCC	4.5	5.0	5.5	V
	DVDDIO	3.0	3.3	3.6	
	DVDD	1.4	1.5	1.6	
Operating Temperature	Topr	-25	+25	+85	°C

Caution: Operating supply voltage and operating temperature are the ranges in which the IC is available for basic operation.

(Basic operation means that the IC operates without emitting unexpected noise or stopping signal.)

Characteristics and rating are not warranted in the whole operating supply voltage and operating temperature.

Electrical Characteristics

Unless otherwise specified $T_a = 25\text{ }^\circ\text{C}$, $AVCC = 5.0\text{ V}$, $DVDDIO = 3.3\text{ V}$, $DVDD = 1.5\text{ V}$, Input signal frequency = 1 kHz, 20-kHz AES17 LPF, Differential output (XLR) measurement, PCM Mode, 24-bit I²S input, $f_s = 44.1\text{ kHz}$, $MCLK = 11.2896\text{ MHz}$, Clock 2 (06h) = 01h, FIR Filter 1 (30h) = 01h, FIR Filter 2 (31h) = 80h, Delta Sigma (40h) = 00h, Volume Transition Time (20h) = 78h

Parameter	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
Power Supply Current						
AVCC Current	I_{AVCC}	-	30.5	45.0	mA	$AVCC_L + AVCC_R + AVCC$ -∞ dBFS (PCM, No signal)
DVDDIO Current	I_{DVDDIO}	-	52	250	μA	-∞ dBFS (PCM, No signal)
DVDD Current 1	I_{DVDD1}	-	10	20	mA	-∞ dBFS (PCM, No signal)
DVDD Current 2	I_{DVDD2}	-	11	22	mA	0 dBFS, $f_s = 44.1\text{ kHz}$
DVDD Current 3	I_{DVDD3}	-	18	36	mA	0 dBFS, $f_s = 96\text{ kHz}$, (30h) = 02h, (31h) = 01h, (40h) = 11h, $MCLK = 24.5760\text{ MHz}$
DVDD Current 4	I_{DVDD4}	-	17	34	mA	0 dBFS, $f_s = 192\text{ kHz}$, (30h) = 04h, (31h) = 02h, (40h) = 11h, $MCLK = 24.5760\text{ MHz}$
DVDD Current 5	I_{DVDD5}	-	10	20	mA	0 dBFS, $f_s = 384\text{ kHz}$, (30h) = 08h, (31h) = 00h, (40h) = 11h, $MCLK = 24.5760\text{ MHz}$
DVDD Current 6	I_{DVDD6}	-	21	42	mA	0 dBFS, $f_s = 44.1\text{ kHz}$, (30h) = 01h, (31h) = 00h, (40h) = 11h, $MCLK = 22.5792\text{ MHz}$ (Max DVDD current setting)
PCM AC Characteristics						
SNR	SNR_P	122	126	-	dB	20-kHz AES17 LPF + A-weight
THD+N	THD_P	-	-112	-97	dB	20-kHz AES17 LPF, -3 dBFS
Dynamic Range	DR_P	122	126	-	dB	20-kHz AES17 LPF + A-weight, -60 dBFS
Channel Gain Mismatch	GM_P	-0.5	0	+0.5	dB	0 dBFS, 20-kHz AES17 LPF
Output Center Current	I_{CN_P}	4.6	5.3	6.0	mA	-∞ dBFS (No signal), Bias current single output
Peak Output Current	I_{PP_P}	5.42	6.25	7.08	mApp	0 dBFS, Current amplitude
Sampling Frequency	f_s	32.0	44.1	768.0	kHz	
Bit Length	Bit	16	-	32	Bit	

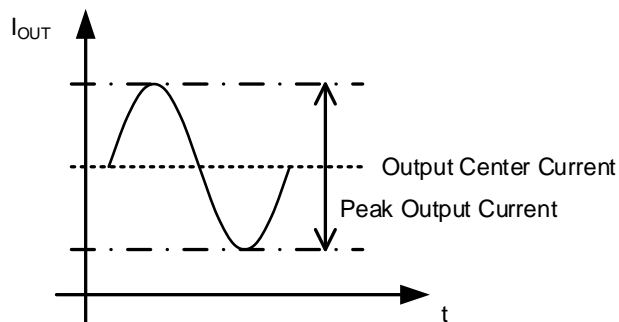


Figure 4. Peak Output Current

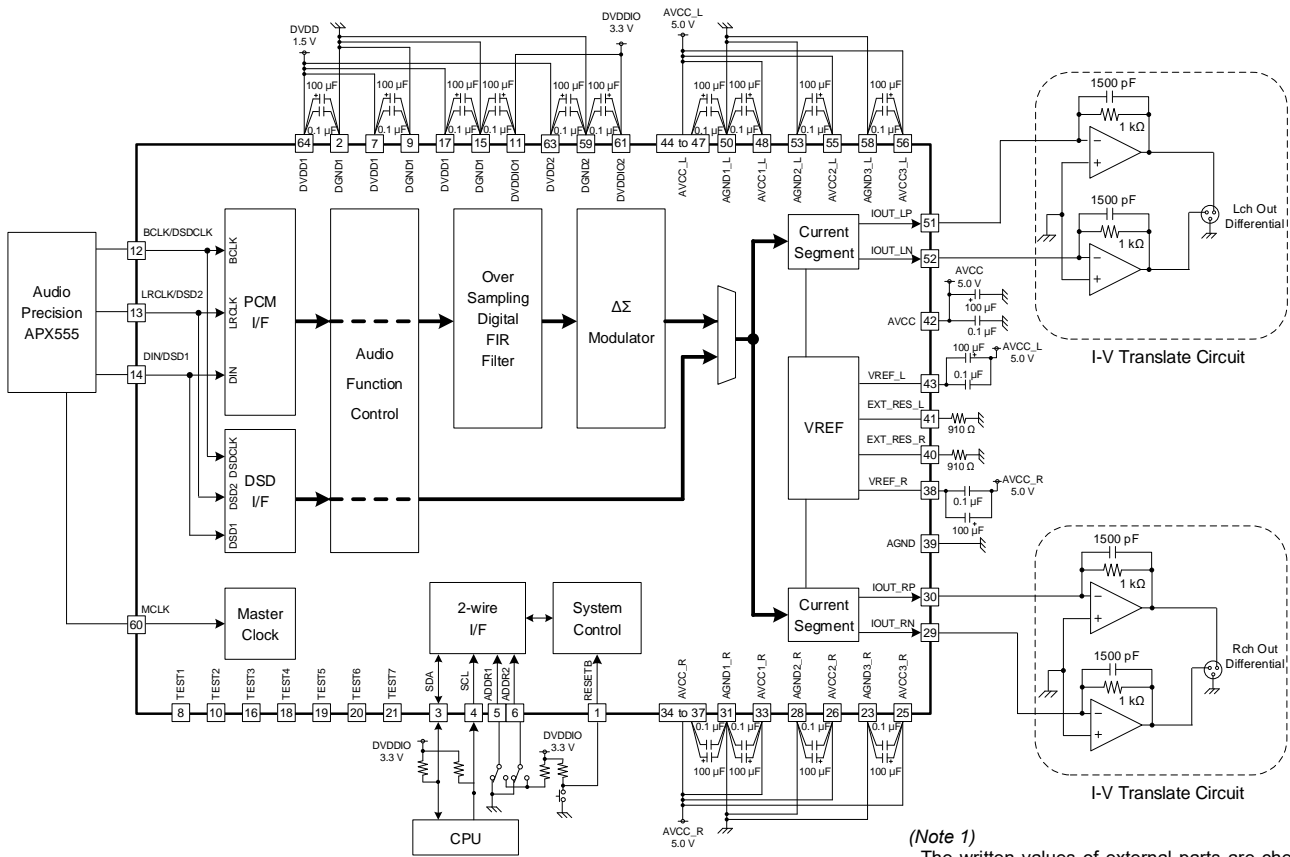
Electrical Characteristics - continued

Unless otherwise specified Ta = 25 °C, AVCC = 5.0 V, DVDDIO = 3.3 V, DVDD = 1.5 V
 Input Signal Frequency = 1 kHz, 20-kHz AES17 LPF, Differential output (XLR) measurement
 DSD Mode, f_{DSD} = 5.6448 MHz, MCLK = 45.1584 MHz, Clock 2 (06h) = 01h, DSD Filter (16h) = 05h

Parameter	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
DSD AC Characteristics						
SNR	SNR _D	112	122	-	dB	20-kHz AES17 LPF + A-weight ^(Note 1)
THD+N	THD _D	-	-110	-95	dB	20-kHz AES17LPF, 0 dBFS
Dynamic Range	DR _D	104	117	-	dB	20-kHz AES17 LPF + A-weight, -60 dBFS
Output Center Current	I _{CN_D}	4.6	5.3	6.0	mA	-∞ dBFS (No signal), Bias current single output
Peak Output Current	I _{PP_D}	3.0	3.5	4.0	mApp	0 dBFS, Current amplitude
DSD Clock	f _{DSD}	2.8224	-	22.5792	MHz	

(Note 1) The silent input pattern of DSD data is a repetition of 5Ah.

Measurement Circuit



(Note 1)
 The written values of external parts are checked by sound test. Changing these values can affect the sound quality. Please check the sound when the values are changed.

Figure 5. Measurement Circuit

DC Characteristics

Unless otherwise specified Ta = 25 °C, AVCC = 5.0 V, DVDDIO = 3.3 V, DVDD = 1.5 V

Parameter	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
High Level Input Voltage	V _{IH}	0.8 x DVDDIO	-	-	V	MCLK, DIN/DSD1, LRCLK/DSD2, BCLK/DSDCLK, RESETB, SCL, SDA, ADDR1, ADDR2 pin
Low Level Input Voltage	V _{IL}	-	-	0.2 x DVDDIO	V	MCLK, DIN/DSD1, LRCLK/DSD2, BCLK/DSDCLK, RESETB, SCL, SDA pin
Input Leakage Current	I _{IN1}	-10	-	+10	μA	ADDR1, ADDR2 pin
	I _{IN2}	-500	-	+500	μA	ADDR1, ADDR2 pin
Low Level Output Voltage	V _{OL}	-	-	0.4	V	SDA pin, I _o : 3 mA

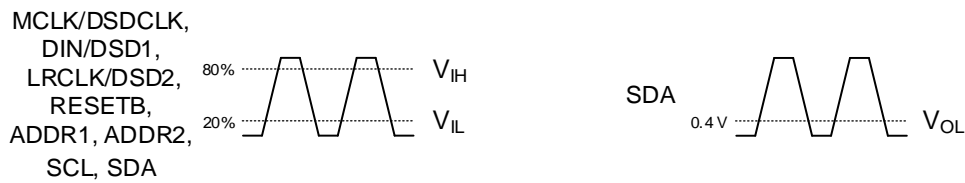


Figure 6. High/Low Level Specifications

AC Characteristics (MCLK, RESETB)

Unless otherwise specified Ta = 25 °C, AVCC = 5.0 V, DVDDIO = 3.3 V, DVDD = 1.5 V

Parameter	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
MCLK Frequency	f _{MCLK}	2.8224	-	49.1520	MHz	
MCLK "H" Length	t _{MCH}	8.1	-	-	ns	
MCLK "L" Length	t _{MCL}	8.1	-	-	ns	
MCLK Duty	DUTY _M	40	50	60	%	t _{MCH} / (t _{MCH} + t _{MCL})
RESETB Pulse Width	t _{RST}	1	-	-	μs	

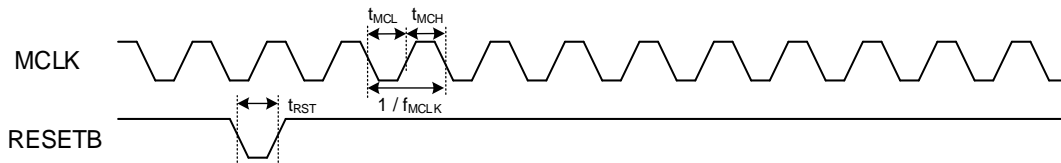


Figure 7. Timing Specifications of MCLK

AC Characteristics (PCM Mode)

Unless otherwise specified Ta = 25 °C, AVCC = 5.0 V, DVDDIO = 3.3 V, DVDD = 1.5 V

Parameter	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
LRCLK Frequency	f _{LRCLK}	32	-	768	kHz	f _{LRCLK} = fs
LRCLK Hold Time	t _{LRH}	8.1	-	-	ns	
LRCLK Setup Time	t _{LRSU}	8.1	-	-	ns	
LRCLK Duty	DUTY _L	40	50	60	%	
BCLK Frequency	f _{BCLK}	2.048	-	49.152	MHz	f _{BCLK} = 64 f _{LRCLK}
BCLK "H" Length	t _{BCH}	8.1	-	-	ns	
BCLK "L" Length	t _{BCL}	8.1	-	-	ns	
BCLK Duty	DUTY _B	40	50	60	%	t _{BCH} / (t _{BCH} + t _{BCL})
DIN Setup Time	t _{DINS}	8.1	-	-	ns	
DIN Hold Time	t _{DINH}	8.1	-	-	ns	

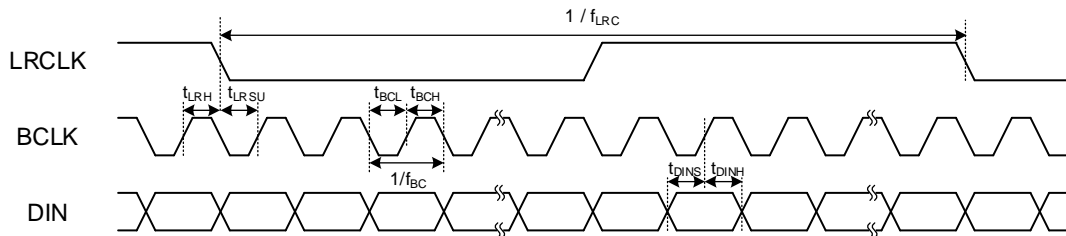


Figure 8. Timing Specifications of I²S

AC Characteristics (DSD Mode)

Unless otherwise specified Ta = 25 °C, AVCC = 5.0 V, DVDDIO = 3.3 V, DVDD = 1.5 V

Parameter	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
DSDCLK Frequency	f _{DSD}	2.8224	-	22.5792	MHz	
DSDCLK Duty	DUTY _D	40	50	60	%	t _{DCH} / (t _{DCH} + t _{DCL})
DSDCLK "H" Length	t _{DCH}	17.7	-	-	ns	
DSDCLK "L" Length	t _{DCL}	17.7	-	-	ns	
DSD data Setup Time	t _{DSDS}	17.7	-	-	ns	
DSD data Hold Time	t _{DSDH}	17.7	-	-	ns	

DSD1 data and DSD2 data are output from Lch and Rch respectively.

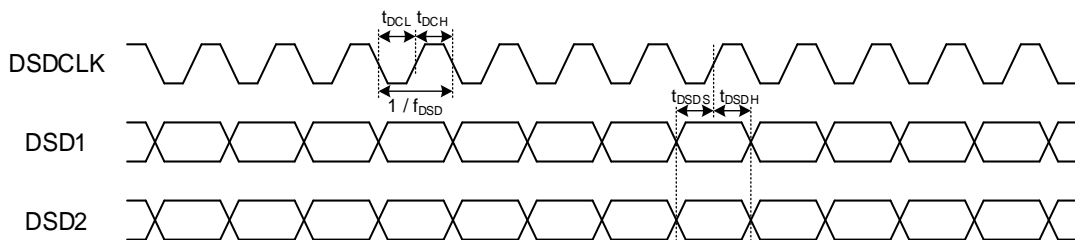


Figure 9. Timing Specifications of DSD

AC Characteristics (2-wire I/F)

Unless otherwise specified Ta = 25 °C, AVCC = 5.0 V, DVDDIO = 3.3 V, DVDD = 1.5 V

Parameter	Symbol	Limit		Unit
		Min	Max	
SCL Clock Frequency	f _{SCL}	-	400	kHz
Bus Free Time between a STOP and START Condition	t _{BUF}	0.8	-	μs
Hold Time (Repeated) START Condition	t _{HD_STA}	0.4	-	μs
LOW Period of the SCL Clock	t _{LOW}	0.8	-	μs
HIGH Period of the SCL Clock	t _{HIGH}	0.4	-	μs
Setup Time for a Repeated START Condition	t _{SU_STA}	0.4	-	μs
Data Hold Time	t _{HD_DAT}	0	-	μs
Data Setup Time	t _{SU_DAT}	100	-	Ns
Setup Time for STOP Condition	t _{SU_STO}	0.4	-	Ms

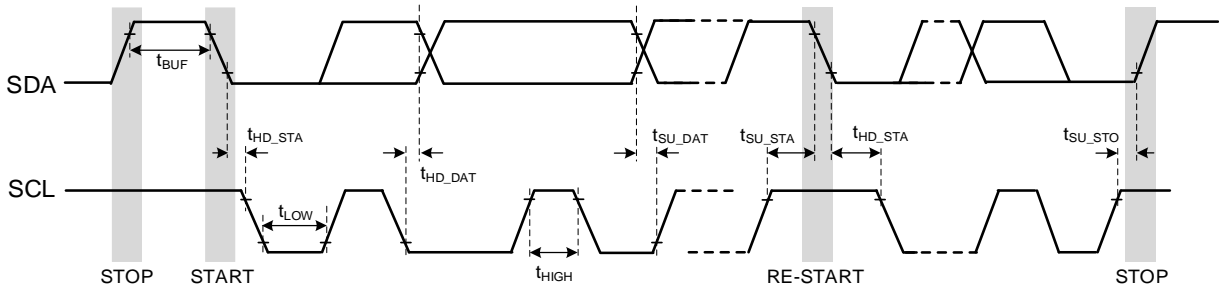


Figure 10. Timing Specifications of 2-wire I/F

Typical Performance Curves

Unless otherwise specified Ta = 25 °C, AVCC = 5.0 V, DVDDIO = 3.3 V, DVDD = 1.5 V, Input signal frequency = 1 kHz, 20-kHz AES17 LPF, Differential output (XLR) measurement, PCM Mode, 24-bit I²S input, fs = 44.1 kHz, MCLK = 11.2896 MHz, Clock 2 (06h) = 01h, FIR Filter 1 (30h) = 01h, FIR Filter 2 (31h) = 80h, Delta Sigma (40h) = 00h, Volume Transition Time (20h) = 78h

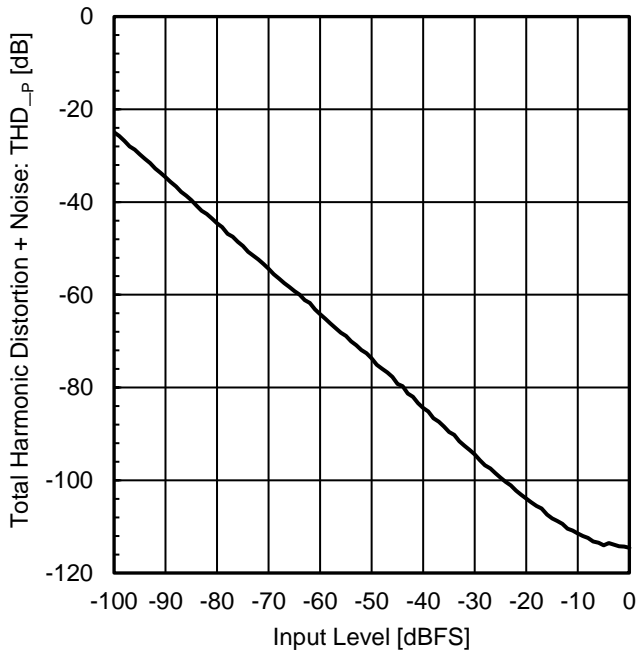


Figure 11. THD+N vs Input Level

(External LPF: AUX-0025 (Audio Precision))

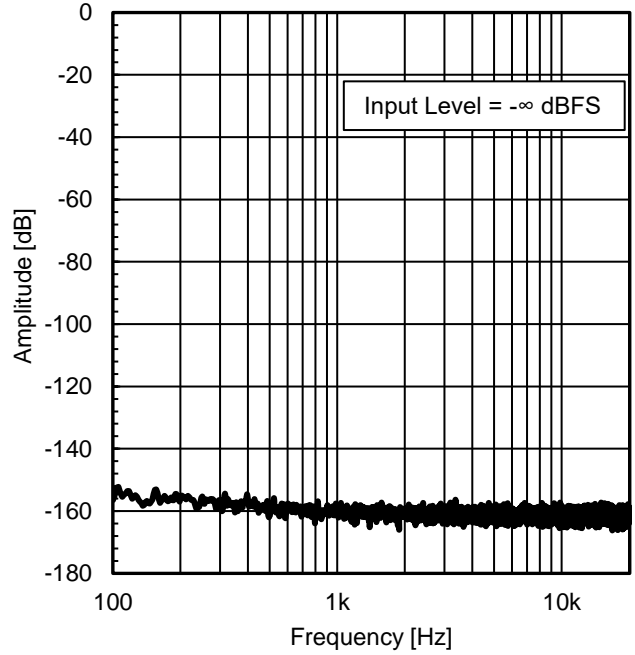


Figure 12. Amplitude vs Frequency

2-wire I/F

Format

Device address and 1 byte of register address are sent in data write-in and data read-out. The format of 2-wire I/F slave mode is shown below.

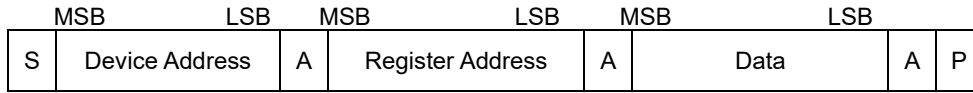


Figure 13. 2-wire I/F Transmission Format

- S : START Condition
- Device Address : Device Address of 8-bit data (MSB first)
- A : Acknowledge. Acknowledge bit is added to send and receive data every byte.
When the correct data is sent and received, acknowledge is "L".
In the case of "H", there is no acknowledge.
- Register Address : Register Address of 8-bit data (MSB first)
- Data : Write-in or Read-out data of 8-bit (MSB first)
- P : STOP Condition

START and STOP Conditions

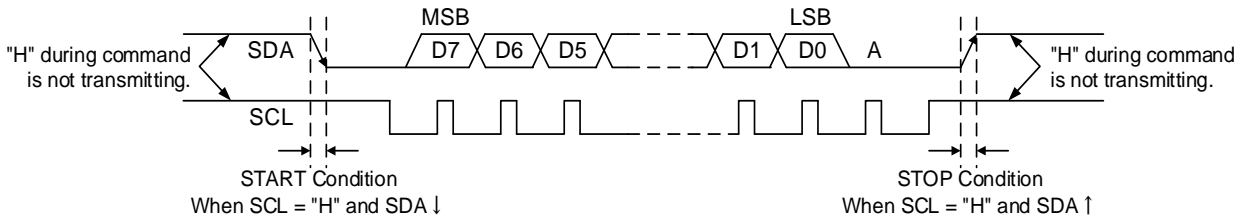


Figure 14. START and STOP Specifications

Device Address

The format of Device Address is shown below. Four Device Addresses are selectable by setting of the ADDR1 and the ADDR2 pins. R/W bit is the mode setting of Write-in (R/W = 0) or Read-out (R/W = 1).

MSB						LSB	
D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	1	1	ADDR2	ADDR1	R/W

Figure 15. Device Address Data Format

The pins setting of Device Address are shown below.

Table 2. Pin Setting of Device Address

Pin Setting		Device Address	
ADDR2	ADDR1	Write-in (R/W = 0)	Read-out (R/W = 1)
L	L	38h	39h
L	H	3Ah	3Bh
H	L	3Ch	3Dh
H	H	3Eh	3Fh

2-wire I/F - continued

Write Operation

In case of write-in, after sending a device address and a register address, send write data. Auto incremental function allows consecutive data transmission. In case of forwarding data, repeat Step 6 to 7 of below table so that address will automatically be +1. When the register address reaches FFh, it does not increase and repeats FFh. In the example shown below, N consecutive registers from 20h are written.

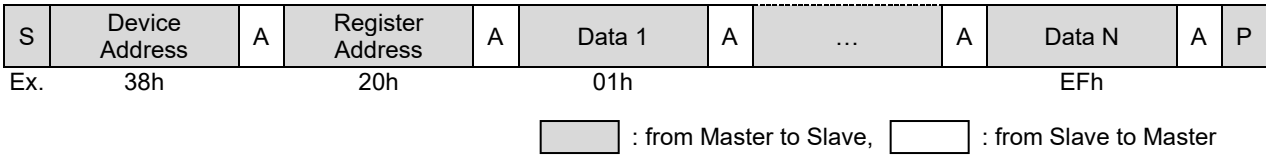


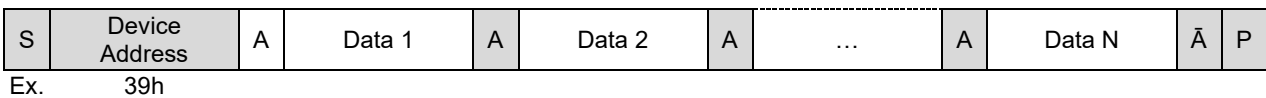
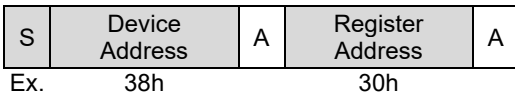
Figure 16. Data Write-in format

Table 3. Write Operation Sequence

Step	Bit	Master	Slave	Note
1		START Condition		
2	8	Device Address		38h, 3Ah, 3Ch or 3Eh
3	1		Acknowledge	
4	8	Register Address		Register Address 8-bit
5	1		Acknowledge	
6	8	Write-in Data		Write Data 8-bit
7	1		Acknowledge	
8		STOP Condition		

Read Operation

In case of read-out, at first send device address and a register address. Next send device address again and data is read. Acknowledge should not be returned after finishing the command. Auto incremental function allows consecutive data transmission. In case of forwarding consecutive data, repeat Step 9 to 10 of below table so that address will automatically be +1. When the register address reaches FFh, it does not increase and repeats FFh. In the example shown below, N consecutive registers from 30h are read.



: from Master to Slave,
 : from Slave to Master,
 A : Acknowledge, Ā : No acknowledge

Figure 17. Data Read-out format

Table 4. Read Operation Sequence

Step	Bit	Master	Slave	Note
1		START Condition		
2	8	Device Address		38h, 3Ah, 3Ch or 3Eh
3	1		Acknowledge	
4	8	Register Address		
5	1		Acknowledge	
6	1	START Condition		
7	8	Device Address		39h, 3Bh, 3Dh or 3Fh
8	1		Acknowledge	
9	8		Read-out Data	
10	1	Acknowledge		
11		STOP Condition		

Register Map

Do not change the setting which 0 or 1 is assigned in register map. Otherwise, normal operation is not guaranteed.

Add ress	Register Name	R/W	Initial	D7	D6	D5	D4	D3	D2	D1	D0
00h	Software Reset	R/W	00h	0	0	0	0	0	0	0	SoftRst_X
01h	Chip Version	R	52h	52h							
02h	Digital Power	R/W	00h	0	0	0	0	0	0	0	DigPon
03h	Analog Power	R/W	00h	0	0	0	0	0	0	0	AnaPon
04h	Clock 1	R/W	00h	0	0	0	0	0	0	MclkDiv[1:0]	
05h	(Reserved)	R/W	00h	0	0	0	0	0	0	0	0
06h	Clock 2	R/W	00h	0	0	0	0	0	0	0	PhaseAdj
07h	(Reserved)	R/W	04h	0	0	0	0	0	1	0	0
08h	(Reserved)	R/W	00h	0	0	0	0	0	0	0	0
↓	(Reserved)	R/W	00h	0	0	0	0	0	0	0	0
0Fh	(Reserved)	R/W	00h	0	0	0	0	0	0	0	0
10h	Audio I/F 1	R/W	0Bh	DsdOn	0	0	DsdMute Mode	Fmt[1:0]		WLen[1:0]	
11h	(Reserved)	R/W	00h	0	0	0	0	0	0	0	0
12h	Audio I/F 2	R/W	00h	0	0	0	0	0	0	MonoSel[1:0]	
13h	Audio I/F 3	R/W	00h	0	0	0	0	0	0	0	LrSwap
14h	Audio Output Polarity	R/W	00h	0	0	0	0	0	0	OutPol2	OutPol1
15h	(Reserved)	R/W	00h	0	0	0	0	0	0	0	0
16h	DSD Filter	R/W	02h	0	0	0	0	0	DfSetting	DsdFilter[1:0]	
17h	Audio Input Polarity	R/W	00h	0	0	0	0	0	0	InPol2	InPol1
18h	(Reserved)	R/W	00h	0	0	0	0	0	0	0	0
19h	(Reserved)	R/W	11h	0	0	0	1	0	0	0	1
1Ah	(Reserved)	R/W	00h	0	0	0	0	0	0	0	0
↓	(Reserved)	R/W	00h	0	0	0	0	0	0	0	0
1Fh	(Reserved)	R/W	00h	0	0	0	0	0	0	0	0
20h	Volume Transition Time	R/W	48h	0	VttSetting[2:0]			VolTranTime[3:0]			
21h	Volume 1	R/W	00h	Vol1[7:0]							
22h	Volume 2	R/W	00h	Vol2[7:0]							
23h	(Reserved)	R/W	00h	0	0	0	0	0	0	0	0
↓	(Reserved)	R/W	00h	0	0	0	0	0	0	0	0
28h	(Reserved)	R/W	00h	0	0	0	0	0	0	0	0
29h	Mute Transition Time	R/W	08h	0	0	0	0	MuteTranTime[3:0]			
2Ah	Mute	R/W	00h	0	0	0	0	0	0	Mute2_X	Mute1_X
2Bh	(Reserved)	R/W	00h	0	0	0	0	0	0	0	0
↓	(Reserved)	R/W	00h	0	0	0	0	0	0	0	0
2Eh	(Reserved)	R/W	00h	0	0	0	0	0	0	0	0
2Fh	RAM Clear	R/W	00h	RamClr	0	0	0	0	0	0	0
30h	FIR Filter 1	R/W	00h	0	0	0	0	FirAlgo[3:0]			
31h	FIR Filter 2	R/W	00h	HpcMode	0	0	0	0	FirCoeff[2:0]		
32h	(Reserved)	R/W	00h	0	0	0	0	0	0	0	0
33h	De-Emphasis 1	R/W	00h	0	0	0	0	0	DempFs[1:0]		
34h	De-Emphasis 2	R/W	00h	0	0	0	0	0	0	Demp2	Demp1
35h	(Reserved)	R/W	00h	0	0	0	0	0	0	0	0
↓	(Reserved)	R/W	00h	0	0	0	0	0	0	0	0
3Fh	(Reserved)	R/W	00h	0	0	0	0	0	0	0	0
40h	Delta Sigma	R/W	00h	0	0	0	DsSetting	0	0	DsOsr[1:0]	
41h	Setting 1	R/W	00h	Setting1[7:0]							
42h	Setting 2	R/W	00h	Setting2[7:0]							
43h	Setting 3	R/W	00h	Setting3[7:0]							
44h	(Reserved)	R/W	00h	0	0	0	0	0	0	0	0
↓	(Reserved)	R/W	00h	0	0	0	0	0	0	0	0
47h	(Reserved)	R/W	00h	0	0	0	0	0	0	0	0
48h	Setting 4	R/W	00h	Setting4[7:0]							
49h	(Reserved)	R/W	00h	0	0	0	0	0	0	0	0
↓	(Reserved)	R/W	00h	0	0	0	0	0	0	0	0
5Fh	(Reserved)	R/W	00h	0	0	0	0	0	0	0	0

Register Map - continued

Do not change the setting which 0 or 1 is assigned in register map. Otherwise, normal operation is not guaranteed.

Add ress	Register Name	R/W	Initial	D7	D6	D5	D4	D3	D2	D1	D0
60h	Setting 5	R/W	00h	Setting5[7:0]							
61h	Setting 6	R/W	00h	Setting6[7:0]							
62h	(Reserved)	R/W	00h	0	0	0	0	0	0	0	0
↓	(Reserved)	R/W	00h	0	0	0	0	0	0	0	0
67h	(Reserved)	R/W	00h	0	0	0	0	0	0	0	0
68h	(Reserved)	R/W	12h	0	0	0	1	0	0	1	0
69h	(Reserved)	R/W	00h	0	0	0	0	0	0	0	0
↓	(Reserved)	R/W	00h	0	0	0	0	0	0	0	0
A2h	(Reserved)	R/W	00h	0	0	0	0	0	0	0	0
A3h	(Reserved)	R/W	03h	0	0	0	0	0	0	1	1
A4h	(Reserved)	R/W	00h	0	0	0	0	0	0	0	0
A5h	(Reserved)	R/W	FFh	1	1	1	1	1	1	1	1
A6h	(Reserved)	R/W	FFh	1	1	1	1	1	1	1	1
A7h	(Reserved)	R/W	FFh	1	1	1	1	1	1	1	1
A8h	(Reserved)	R/W	00h	0	0	0	0	0	0	0	0
↓	(Reserved)	R/W	00h	0	0	0	0	0	0	0	0
AFh	(Reserved)	R/W	00h	0	0	0	0	0	0	0	0
B0h	(Reserved)	R/W	02h	0	0	0	0	0	0	1	0
↓	(Reserved)	R/W	02h	0	0	0	0	0	0	1	0
B7h	(Reserved)	R/W	02h	0	0	0	0	0	0	1	0
B8h	(Reserved)	R/W	00h	0	0	0	0	0	0	0	0
↓	(Reserved)	R/W	00h	0	0	0	0	0	0	0	0
FFh	(Reserved)	R/W	00h	0	0	0	0	0	0	0	0

Register Description

1. Address 00h (Software Reset)

Address	Register Name	R/W	Initial	D7	D6	D5	D4	D3	D2	D1	D0
00h	Software Reset	R/W	00h	0	0	0	0	0	0	0	SoftRst_X

SoftRst_X: Software Reset Control

- 0 Software reset (All registers are not initialized) (default)
- 1 Normal operation

2. Address 01h (Chip Version)

Address	Register Name	R/W	Initial	D7	D6	D5	D4	D3	D2	D1	D0
01h	Chip Version	R	52h	ChipVer = 52h							

ChipVer: Chip Version Register (Read only)

3. Address 02h (Digital Power)

Address	Register Name	R/W	Initial	D7	D6	D5	D4	D3	D2	D1	D0
02h	Digital Power	R/W	00h	0	0	0	0	0	0	0	DigPon

DigPon: Digital Power Control

- 0 Power off and stop clock (default)
- 1 Power on and provide clock

4. Address 03h (Analog Power)

Address	Register Name	R/W	Initial	D7	D6	D5	D4	D3	D2	D1	D0
03h	Analog Power	R/W	00h	0	0	0	0	0	0	0	AnaPon

AnaPon: Analog Power Control

- 0 Power off (Current output off) (default)
- 1 Power on (Current output on)

5. Address 04h (Clock 1)

Address	Register Name	R/W	Initial	D7	D6	D5	D4	D3	D2	D1	D0
04h	Clock 1	R/W	00h	0	0	0	0	0	0	MclkDiv[1:0]	

MclkDiv[1:0]: MCLK Division Ratio Selection for Internal Clock

- 00 1 time (default)
- 01 2/3 times
- 10 1/2 times
- 11 1/3 times

There are some functions that cannot be used due to this setting. See the "[System Clock](#)" section for more details on the available register combinations.

Register Description - continued

6. Address 06h (Clock 2)

Address	Register Name	R/W	Initial	D7	D6	D5	D4	D3	D2	D1	D0
06h	Clock 2	R/W	00h	0	0	0	0	0	0	0	PhaseAdj

PhaseAdj: Phase Adjustment Control for Internal Clock

- 0 Phase adjustment disabled (default) Audio characteristics may be improved.
- 1 Phase adjustment enabled Sound quality may be improved.

(DSD mode)

When this function is enabled, the frequency of MCLK must be twice of DSDCLK frequency.
See the "System Clock" section for the setting of MCLK frequency.

7. Address 10h (Audio I/F 1)

Address	Register Name	R/W	Initial	D7	D6	D5	D4	D3	D2	D1	D0
10h	Audio I/F 1	R/W	0Bh	DsdOn	0	0	DsdMute Mode	Fmt[1:0]		WLen[1:0]	

DsdOn: DSD Mode Selection
 0 PCM mode (default)
 1 DSD mode

DsdMuteMode: DSD Mute Enable (For DSD mode)
 0 DSD Mute enabled (default) Controlled by the setting of Mute (2Ah[1:0]).
 1 DSD Mute disabled Not be muted even if Mute (2Ah[1:0]) on.

Fmt[1:0]: Audio Data Input Format (For PCM mode)
 00 Right justified
 01 Left justified
 10 I²S (default)
 11 Prohibition

WLen[1:0]: Audio Data Input Bit Length (For PCM mode)
 00 16-bit
 01 20-bit
 10 24-bit
 11 32-bit (default)

Right Justified

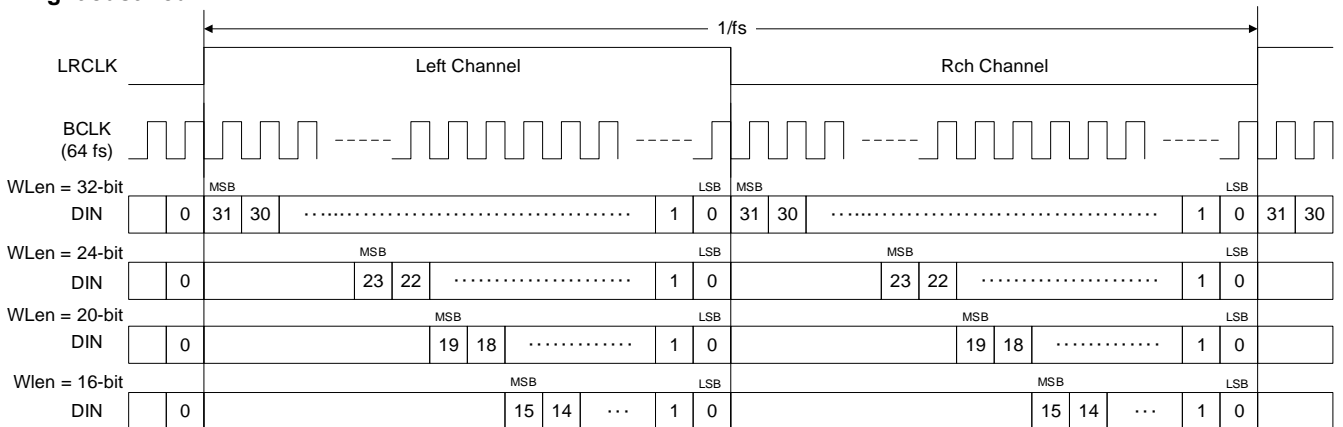


Figure 18. Audio Data Input Format: Right Justified

Address 10h (Audio I/F 1) - continued

Left Justified

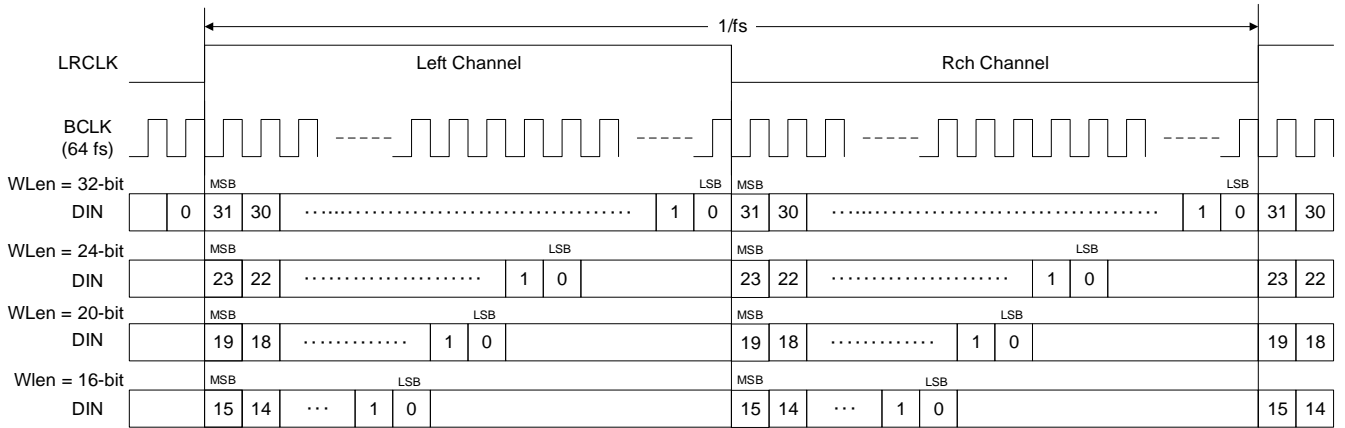


Figure 19. Audio Data Input Format: Left Justified

I²S

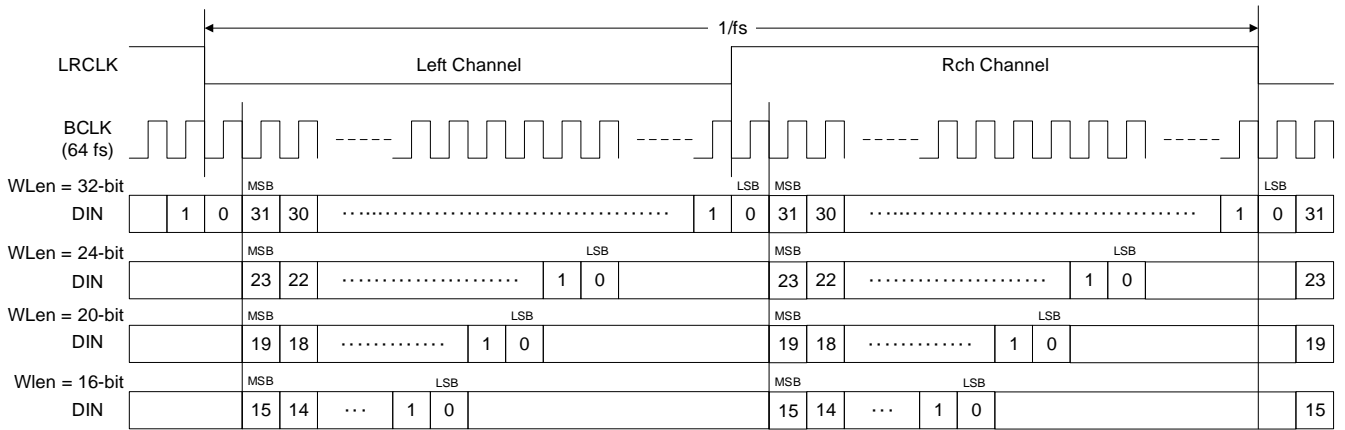


Figure 20. Audio Data Input Format: I²S

8. Address 12h (Audio I/F 2)

Address	Register Name	R/W	Initial	D7	D6	D5	D4	D3	D2	D1	D0
12h	Audio I/F 2	R/W	00h	0	0	0	0	0	0	MonoSel[1:0]	

MonoSel[1:0]: Monaural Mode Selection *(Note 1)*

Table 5. Stereo/Monaural Mode Settings for PCM Mode

MonoSel[1:0]	Mode	Lch output	Rch output	
00	Stereo mode	Lch input	Rch input	(default)
01	Mixing mode	(Lch input + Rch input)/2		
10	Mono mode Lch	Lch input		
11	Mono mode Rch	Rch input		

Table 6. Stereo/Monaural Mode Settings for PCM Mode

MonoSel[1:0]	Mode	Lch output	Rch output	
00	Stereo mode	Lch input	Rch input	(default)
01	Stereo mode	Lch input	Rch input	
10	Mono mode Lch	Lch input		
11	Mono mode Rch	Rch input		

(Note 1) This is the function of Audio Function Control block in the "Block Diagram".

Register Description - continued

9. Address 13h (Audio I/F 3)

Address	Register Name	R/W	Initial	D7	D6	D5	D4	D3	D2	D1	D0
13h	Audio I/F 3	R/W	00h	0	0	0	0	0	0	0	LrSwap

LrSwap: Audio Data Swap Control^(Note 1)

Table 7. LR Swap Setting

LrSwap	Lch output	Rch output
0	Lch input	Rch input
1	Rch input	Lch input

(default)

10. Address 14h (Audio Output Polarity)

Address	Register Name	R/W	Initial	D7	D6	D5	D4	D3	D2	D1	D0
14h	Audio Output Polarity	R/W	00h	0	0	0	0	0	0	OutPol2	OutPol1

OutPol1: Polarity Inversion Control for Lch^(Note 2)

- 0 Normal (default)
- 1 Polarity inversion

OutPol2: Polarity Inversion Control for Rch^(Note 2)

- 0 Normal (default)
- 1 Polarity inversion

11. Address 16h (DSD Filter)

Address	Register Name	R/W	Initial	D7	D6	D5	D4	D3	D2	D1	D0
16h	DSD Filter	R/W	02h	0	0	0	0	0	DfSetting	DsdFilter[1:0]	

DfSetting Set 1. Other values are prohibited.

DsdFilter[1:0]: DSD Filter Selection. (For DSD mode)

Table 8. Cut Off Frequency of DSD Filter

DsdFilter [1:0]	Cut Off Frequency			
	DSD 2.8 MHz	DSD 5.6 MHz	DSD 11.2 MHz	DSD 22.4 MHz
00	19 kHz	39 kHz	78 kHz	157 kHz
01	39 kHz	78 kHz	157 kHz	314 kHz
10	78 kHz	157 kHz	314 kHz	628 kHz
11	Prohibition			

(default)

^(Note 1) This is the function of Audio Function Control block in the "Block Diagram".^(Note 2) This is the function of $\Delta\Sigma$ Modulator block in the "Block Diagram".

Register Description - continued

12. Address 17h (Audio Input Polarity)

Address	Register Name	R/W	Initial	D7	D6	D5	D4	D3	D2	D1	D0
17h	Audio Input Polarity	R/W	00h	0	0	0	0	0	0	InPol2	InPol1

InPol1: Polarity Inversion Control for Lch^(Note 1)

- 0 Normal (default)
- 1 Polarity inversion

InPol2: Polarity Inversion Control for Rch^(Note 1)

- 0 Normal (default)
- 1 Polarity inversion

13. Address 20h (Volume Transition Time)

Address	Register Name	R/W	Initial	D7	D6	D5	D4	D3	D2	D1	D0
20h	Volume Transition Time	R/W	48h	0	VttSetting[2:0]			VolTranTime[3:0]			

VttSetting[2:0] Set 7h. Other values are prohibited.

VolTranTime[3:0]: Volume Transition Time Selection (For PCM mode)

The table below shows the volume transition time when the gain is switched from 0 dB to $-\infty$ dB. The volume transition time depends on the difference between target volume and current volume. For example, the volume transition time when the gain is switched from 0 dB to -6 dB is half the time in the table below.

Table 9. Volume Transition Time

VolTran Time[3:0]	Transition Time	Transition Time (ms)							
		32 kHz	44.1 kHz	48 kHz	96 kHz	192 kHz	384 kHz	768 kHz	
0h	0	0							
1h to 7h	Prohibition	Prohibition							
8h	1024/fs	32.0	23.2	21.3	10.7	5.33	2.67	1.33	(default)
9h	2048/fs	64.0	46.4	42.7	21.3	10.7	5.33	2.67	
Ah	4096/fs	128	92.9	85.3	42.7	21.3	10.7	5.33	
Bh	8192/fs	256	186	171	85.3	42.7	21.3	10.7	
Ch	16384/fs	512	372	341	171	85.3	42.7	21.3	
Dh	32768/fs	1024	743	683	341	171	85.3	42.7	
Eh	65536/fs	2048	1486	1365	683	341	171	85.3	

(Note 1) This is the function of Audio Function Control back in the "Block Diagram".

Register Description - continued

14. Address 21h, 22h (Volume 1, Volume 2)

Address	Register Name	R/W	Initial	D7	D6	D5	D4	D3	D2	D1	D0
21h	Volume 1	R/W	00h	Vol1[7:0]							
22h	Volume 2	R/W	00h	Vol2[7:0]							

Vol1[7:0]: Digital Volume (Attenuation Level) Setting for Lch. (For PCM mode)
 0 dB (00h, default) to -110.0 dB (DCh), -∞ dB (FFh)
 0.5 dB step
 In Mono mode, both Lch and Rch are controlled by Vol1[7:0].

Vol2[7:0]: Digital Volume (Attenuation Level) Setting for Rch (For PCM mode)
 0 dB (00h, default) to -110.0 dB (DCh), -∞ dB (FFh)
 0.5 dB step
 In Mono mode, Vol2[7:0] is not used.

Table 10. Digital Volume (Attenuation Level) Setting

Setting	Gain[dB]	Setting	Gain[dB]	Setting	Gain[dB]	Setting	Gain[dB]	Setting	Gain[dB]	Setting	Gain[dB]	Setting	Gain[dB]
00h	0.0	20h	-16.0	40h	-32.0	60h	-48.0	80h	-64.0	A0h	-80.0	C0h	-96.0
01h	-0.5	21h	-16.5	41h	-32.5	61h	-48.5	81h	-64.5	A1h	-80.5	C1h	-96.5
02h	-1.0	22h	-17.0	42h	-33.0	62h	-49.0	82h	-65.0	A2h	-81.0	C2h	-97.0
03h	-1.5	23h	-17.5	43h	-33.5	63h	-49.5	83h	-65.5	A3h	-81.5	C3h	-97.5
04h	-2.0	24h	-18.0	44h	-34.0	64h	-50.0	84h	-66.0	A4h	-82.0	C4h	-98.0
05h	-2.5	25h	-18.5	45h	-34.5	65h	-50.5	85h	-66.5	A5h	-82.5	C5h	-98.5
06h	-3.0	26h	-19.0	46h	-35.0	66h	-51.0	86h	-67.0	A6h	-83.0	C6h	-99.0
07h	-3.5	27h	-19.5	47h	-35.5	67h	-51.5	87h	-67.5	A7h	-83.5	C7h	-99.5
08h	-4.0	28h	-20.0	48h	-36.0	68h	-52.0	88h	-68.0	A8h	-84.0	C8h	-100.0
09h	-4.5	29h	-20.5	49h	-36.5	69h	-52.5	89h	-68.5	A9h	-84.5	C9h	-100.5
0Ah	-5.0	2Ah	-21.0	4Ah	-37.0	6Ah	-53.0	8Ah	-69.0	AAh	-85.0	CAh	-101.0
0Bh	-5.5	2Bh	-21.5	4Bh	-37.5	6Bh	-53.5	8Bh	-69.5	ABh	-85.5	CBh	-101.5
0Ch	-6.0	2Ch	-22.0	4Ch	-38.0	6Ch	-54.0	8Ch	-70.0	ACH	-86.0	CCh	-102.0
0Dh	-6.5	2Dh	-22.5	4Dh	-38.5	6Dh	-54.5	8Dh	-70.5	ADh	-86.5	CDh	-102.5
0Eh	-7.0	2Eh	-23.0	4Eh	-39.0	6Eh	-55.0	8Eh	-71.0	AEdh	-87.0	CEh	-103.0
0Fh	-7.5	2Fh	-23.5	4Fh	-39.5	6Fh	-55.5	8Fh	-71.5	AFh	-87.5	CFh	-103.5
10h	-8.0	30h	-24.0	50h	-40.0	70h	-56.0	90h	-72.0	B0h	-88.0	D0h	-104.0
11h	-8.5	31h	-24.5	51h	-40.5	71h	-56.5	91h	-72.5	B1h	-88.5	D1h	-104.5
12h	-9.0	32h	-25.0	52h	-41.0	72h	-57.0	92h	-73.0	B2h	-89.0	D2h	-105.0
13h	-9.5	33h	-25.5	53h	-41.5	73h	-57.5	93h	-73.5	B3h	-89.5	D3h	-105.5
14h	-10.0	34h	-26.0	54h	-42.0	74h	-58.0	94h	-74.0	B4h	-90.0	D4h	-106.0
15h	-10.5	35h	-26.5	55h	-42.5	75h	-58.5	95h	-74.5	B5h	-90.5	D5h	-106.5
16h	-11.0	36h	-27.0	56h	-43.0	76h	-59.0	96h	-75.0	B6h	-91.0	D6h	-107.0
17h	-11.5	37h	-27.5	57h	-43.5	77h	-59.5	97h	-75.5	B7h	-91.5	D7h	-107.5
18h	-12.0	38h	-28.0	58h	-44.0	78h	-60.0	98h	-76.0	B8h	-92.0	D8h	-108.0
19h	-12.5	39h	-28.5	59h	-44.5	79h	-60.5	99h	-76.5	B9h	-92.5	D9h	-108.5
1Ah	-13.0	3Ah	-29.0	5Ah	-45.0	7Ah	-61.0	9Ah	-77.0	BAh	-93.0	DAh	-109.0
1Bh	-13.5	3Bh	-29.5	5Bh	-45.5	7Bh	-61.5	9Bh	-77.5	BBh	-93.5	DBh	-109.5
1Ch	-14.0	3Ch	-30.0	5Ch	-46.0	7Ch	-62.0	9Ch	-78.0	BCh	-94.0	DCh	-110.0
1Dh	-14.5	3Dh	-30.5	5Dh	-46.5	7Dh	-62.5	9Dh	-78.5	BDh	-94.5	DDh	prohibition
1Eh	-15.0	3Eh	-31.0	5Eh	-47.0	7Eh	-63.0	9Eh	-79.0	BEh	-95.0	↓	prohibition
1Fh	-15.5	3Fh	-31.5	5Fh	-47.5	7Fh	-63.5	9Fh	-79.5	BFh	-95.5	FEh	prohibition
												FFh	-∞

Example of Volume Switching (fs = 44.1 kHz)

In case of setting VolTranTime (20h[3:0]) = 8h (1024/fs), Vol1 (21h[7:0]) = -∞ dB (FFh), 0 dB (00h)

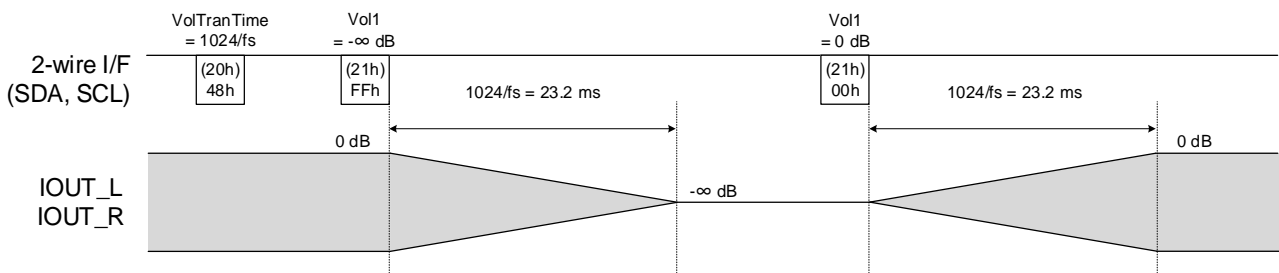


Figure 21. Example of Volume Switching

Register Description - continued

15. Address 29h (Mute Transition Time)

Address	Register Name	R/W	Initial	D7	D6	D5	D4	D3	D2	D1	D0
29h	Mute Transition Time	R/W	08h	0	0	0	0	MuteTranTime[3:0]			

MuteTranTime[3:0]: Mute Transition Time Selection (For PCM mode)

The table below shows the transition time when muting from 0 dB to $-\infty$ dB.

If the setting time is short, pop noise may occur. Please evaluate it carefully before determining the setting value.

Table 11. Mute Transition Time in PCM Mode

MuteTran Time[3:0]	Transition Time	Transition Time (ms)							
		32 kHz	44.1 kHz	48 kHz	96 kHz	192 kHz	384 kHz	768 kHz	
0h	0	0							
1h to 7h	Prohibition	Prohibition							
8h	1024/fs	32	23.2	21.3	10.7	5.33	2.67	1.33	(default)
9h	2048/fs	64	46.4	42.7	21.3	10.7	5.33	2.67	
Ah	4096/fs	128	92.9	85.3	42.7	21.3	10.7	5.33	
Bh	8192/fs	256	186	171	85.3	42.7	21.3	10.7	
Ch	16384/fs	512	372	341	171	85.3	42.7	21.3	
Dh	32768/fs	1024	743	683	341	171	85.3	42.7	
Eh	65536/fs	2048	1486	1365	683	341	171	85.3	

Table 12. Mute Transition Time in DSD Mode

MuteTran Time[3:0]	Transition Time (ms)				
	2.8224 MHz	5.6448 MHz	11.2896 MHz	22.5792 MHz	
0h	0				
1h to 7h	Prohibition				
8h	11.6	5.80	2.90	1.45	(default)
9h	23.2	11.6	5.80	2.90	
Ah	46.4	23.2	11.6	5.80	
Bh	92.9	46.4	23.2	11.6	
Ch	186	92.9	46.4	23.2	
Dh	372	186	92.9	46.4	
Eh	743	372	186	92.9	
Fh	1486	743	372	186	

Register Description - continued

16. Address 2Ah (Mute)

Address	Register Name	R/W	Initial	D7	D6	D5	D4	D3	D2	D1	D0
2Ah	Mute	R/W	00h	0	0	0	0	0	0	Mute2_X	Mute1_X

Mute1_X: Digital Mute Control for Lch

- 0 Mute on (default)
- 1 Mute off

Mute2_X: Digital Mute Control for Rch

- 0 Mute on (default)
- 1 Mute off

Example of Mute switching in PCM mode (fs = 44.1 kHz)

In case of setting MuteTranTime (29h[3:0]) = 8h (1024/fs), Mute (2Ah[1:0])= On (3h), Off (0h)

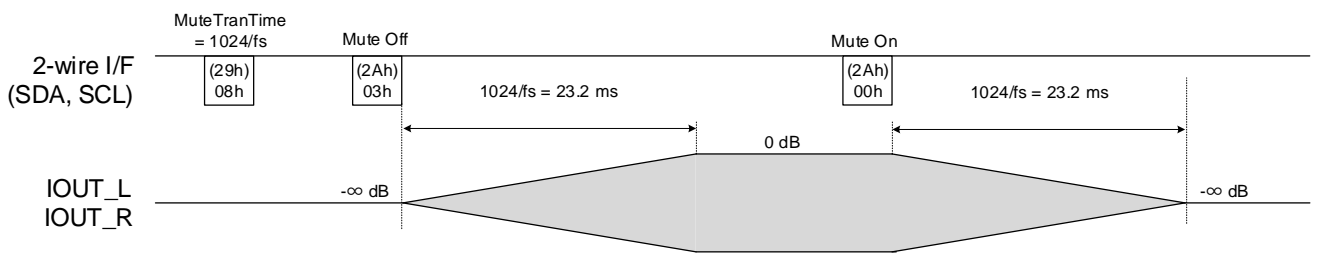


Figure 22. Example of Mute On/Off (PCM Mode)

Example of Mute switching in DSD mode (2.8224 MHz)

In case of setting MuteTranTime (29h[3:0]) = 9h (23.2 ms), Mute (2Ah[1:0])= On (3h), Off (0h)

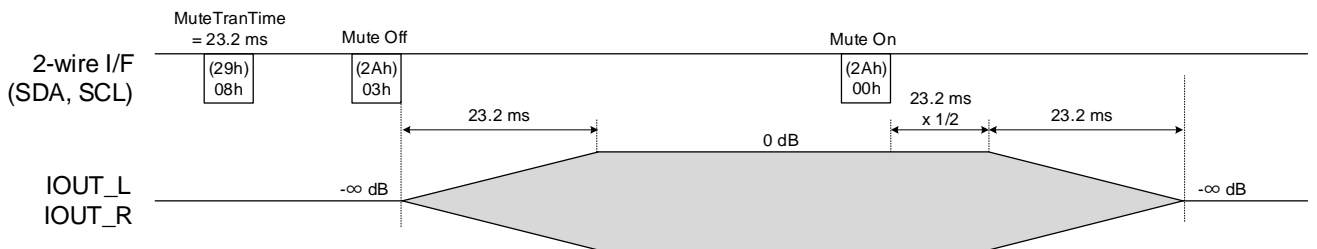


Figure 23. Example of Mute On/Off (DSD Mode)

17. Address 2Fh (RAM Clear)

Address	Register Name	R/W	Initial	D7	D6	D5	D4	D3	D2	D1	D0
2Fh	RAM Clear	R/W	00h	RamClr	0	0	0	0	0	0	0

RamClr: RAM Clear and Initialization Control (For PCM mode)

- 0 RAM clear off (default)
- 1 RAM clear on

It is necessary to turn RAM clear on and off when changing the clock and filter settings. See the “Mode Switching Sequence” section for more details.

Register Description - continued

18. Address 30h, 31h (FIR Filter 1, FIR Filter 2)

Address	Register Name	R/W	Initial	D7	D6	D5	D4	D3	D2	D1	D0
30h	FIR Filter 1	R/W	00h	0	0	0	0	FirAlgo[3:0]			
31h	FIR Filter 2	R/W	00h	HpcMode	0	0	0	0	FirCoeff[2:0]		

FirAlgo[3:0]: FIR Calculation Algorithm Selection (For PCM mode)

FirCoeff[2:0]: FIR Coefficient Selection (For PCM mode)

Please set the FIR filter according to the table below. The frequency responses are shown in "[Frequency Response of FIR Filter](#)" section.

When changing the filter settings, it is necessary to execute the mode switching sequence. The filter settings are reflected when RAM clear in the mode switching sequence is executed. See the "[Mode Switching Sequence](#)" section for more details

Table 13. FIR Filter Setting

FirAlgo[3:0]	FirCoeff[2:0]	fs	Filter Setting	(default)
0h	0h	-	FIR Stop ($-\infty$ dB Output)	
1h	0h	32 kHz, 44.1 kHz, 48 kHz	Sharp Roll-Off	
	3h		Slow Roll-Off	
2h	1h	88.2 kHz, 96 kHz	Sharp Roll-Off	
	4h		Slow Roll-Off	
4h	2h	176.4 kHz, 192 kHz	Sharp Roll-Off	
	5h		Slow Roll-Off	
8h	0h	352.8 kHz, 384 kHz	FIR Bypass	
		705.6 kHz, 768 kHz		
Others		Prohibition		

HpcMode: High Precision Calculation Mode Control (For PCM mode)

- 0 High precision calculation on (default)
- 1 High precision calculation off

Sound quality and audio characteristics can be adjusted with this set up. Please note that when high precision calculation is turned on, the DVDD operating current also increases as the amount of calculation increases accordingly. In case of fs = 705.6 kHz / 768 kHz or MCLK division ratio ($MclkDiv(04h[1:0]) = 10$ or 11, this function is not available and must be turned off. See the "[System Clock](#)" section for more details on the available register combinations.

Address 30h, 31h (FIR Filter 1, FIR Filter 2) - continued

Frequency Response of FIR Filter

Sharp Roll-Off Filter

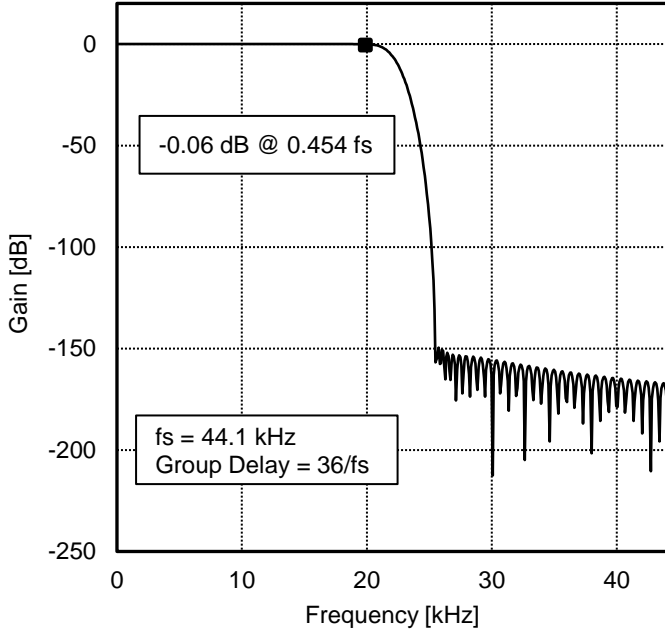


Figure 24. Gain vs Frequency

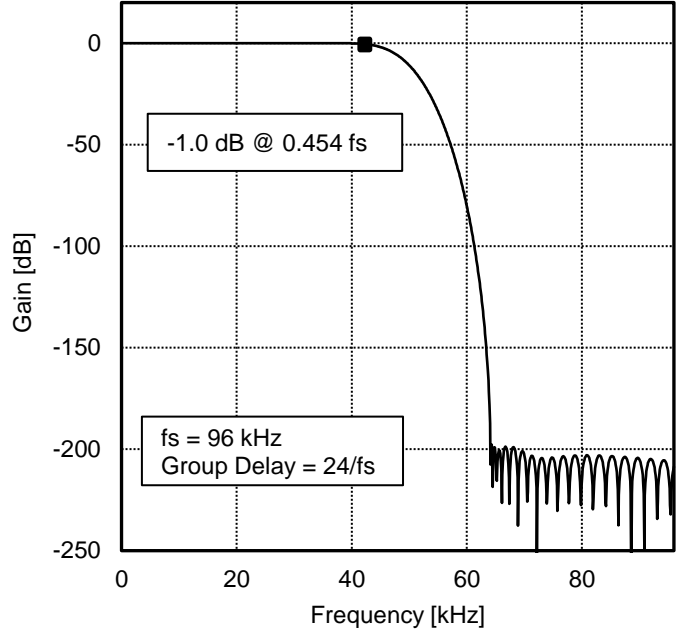


Figure 25. Gain vs Frequency

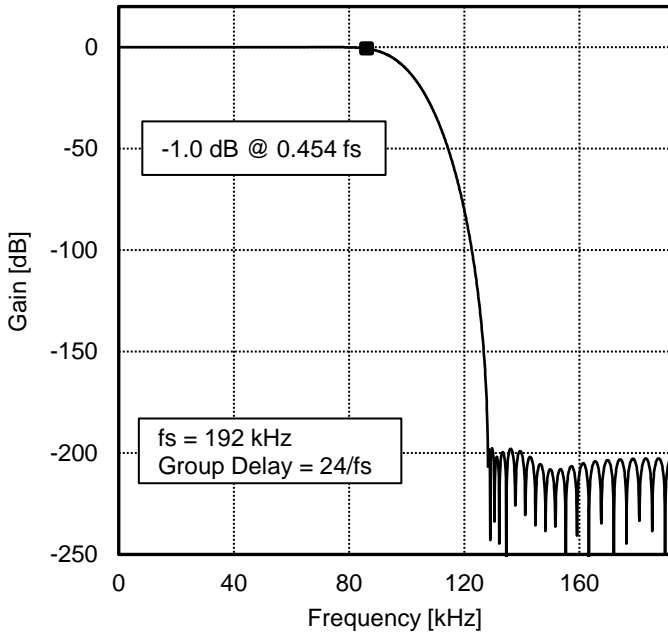


Figure 26. Gain vs Frequency

Address 30h, 31h (FIR Filter 1, FIR Filter 2) - continued

Frequency Response of FIR Filter

Slow Roll-Off Filter

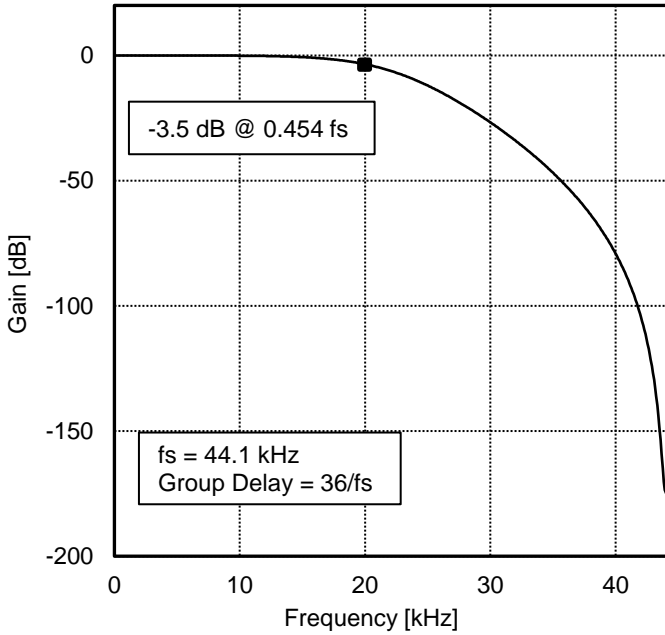


Figure 27. Gain vs Frequency

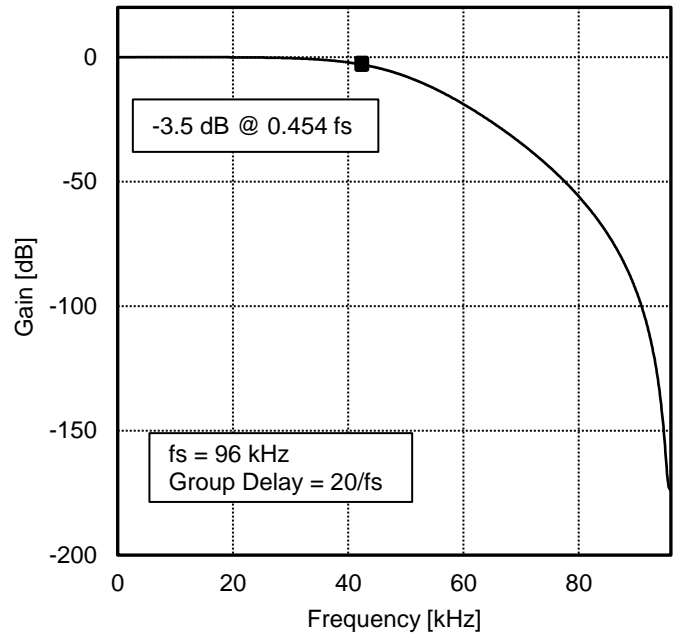


Figure 28. Gain vs Frequency

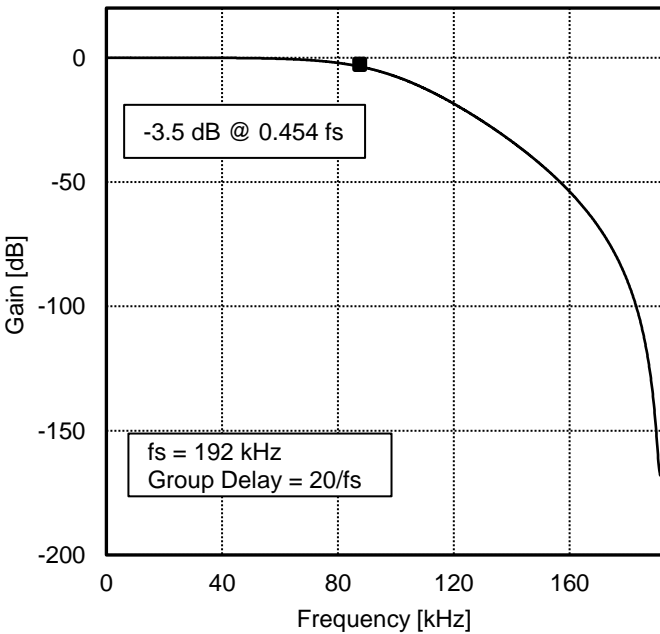


Figure 29. Gain vs Frequency

Register Description - continued

19. Address 33h, 34h (De-Emphasis 1, De-Emphasis 2)

Address	Register Name	R/W	Initial	D7	D6	D5	D4	D3	D2	D1	D0
33h	De-Emphasis 1	R/W	00h	0	0	0	0	0	0	DempFs[1:0]	
34h	De-Emphasis 2	R/W	00h	0	0	0	0	0	0	Demp2	Demp1

DempFs[1:0]: Sampling Frequency Selection for De-Emphasis (For PCM mode)

This register is available when De-Emphasis is enabled by Demp1 / Demp2 setting.

00 Through (De-Emphasis is disabled) (default)

01 fs = 32 kHz

10 fs = 44.1 kHz

11 fs = 48 kHz

The frequency responses are shown in "[Frequency Response of De-Emphasis Filter](#)" section.

Demp1: De-Emphasis Control for Lch (For PCM mode)

0 De-Emphasis disabled (default)

1 De-Emphasis enabled

Demp2: De-Emphasis Control for Rch (For PCM mode)

0 De-Emphasis disabled (default)

1 De-Emphasis enabled

Address 33h, 34h (De-Emphasis 1, De-Emphasis 2) - continued

Frequency Response of De-Emphasis Filter

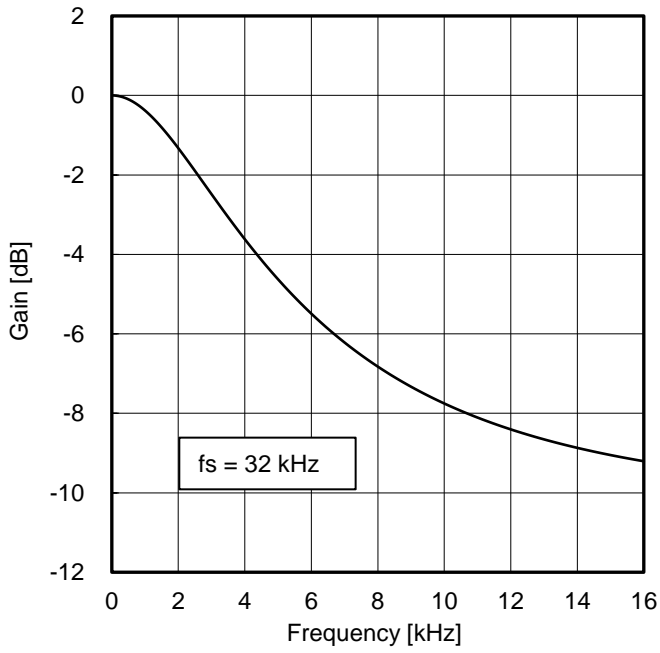


Figure 30. Gain vs Frequency

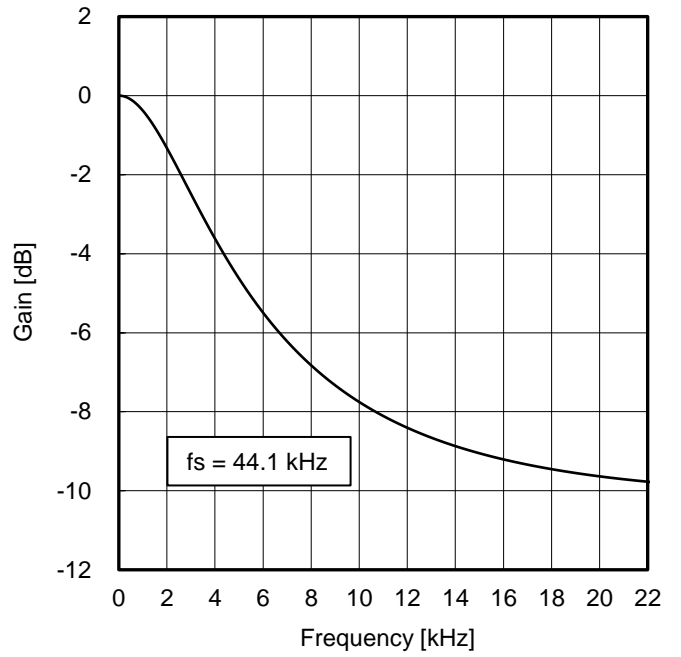


Figure 31. Gain vs Frequency

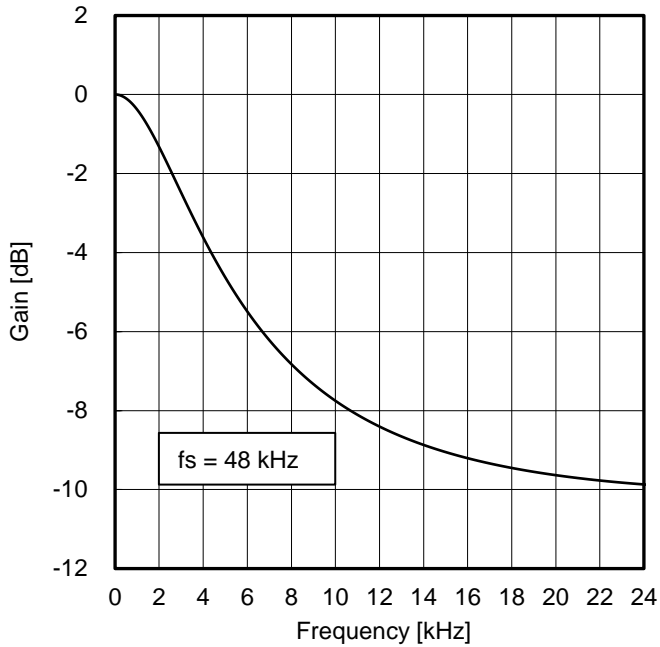


Figure 32. Gain vs Frequency

Register Description - continued

20. Address 40h (Delta Sigma)

Address	Register Name	R/W	Initial	D7	D6	D5	D4	D3	D2	D1	D0
40h	Delta Sigma	R/W	00h	0	0	0	DsSetting	0	0	DsOsr[1:0]	

DsSetting: $\Delta\Sigma$ Modulator Setting

DsOsr[1:0]: Oversampling Rate Selection for $\Delta\Sigma$ Modulator

(PCM mode)

The over sampling rate of $\Delta\Sigma$ Modulator can be changed. The sound quality and audio characteristics are adjustable by this setting.

The setting of over sampling rate should be changed according to the MCLK division ratio setting. See the "System Clock" section for more details on the available register combinations.

Table 14. Over Sampling Rate Setting of $\Delta\Sigma$ Modulator

DsSetting	DsOsr[1:0]	Over Sampling Rate
0	00	x8
	01	x16
	10	x32
	11	Prohibition
1	00	x16
	01	x32
	10	Prohibition
	11	Prohibition

(default)

(DSD mode)

In DSD mode, over sampling rate cannot be changed

Set DsSetting = 0, DsOsr[1:0] = 10.

21. Address 41h, 42h, 43h, 48h (Setting 1, Setting 2, Setting 3, Setting 4)

Address	Register Name	R/W	Initial	D7	D6	D5	D4	D3	D2	D1	D0
41h	Setting 1	R/W	00h	Setting1[7:0]							
42h	Setting 2	R/W	00h	Setting2[7:0]							
43h	Setting 3	R/W	00h	Setting3[7:0]							
48h	Setting 4	R/W	00h	Setting4[7:0]							

Setting1[7:0] Set 00h

Setting2[7:0] Set 16h

Setting3[7:0] Set 2Dh

Setting4[7:0] Set 0Dh

Set these registers in power-on sequence. See the "Power-On Sequence" section for more details.

Register Description - continued

22. Address 60h, 61h (Setting 5, Setting 6)

Address	Register Name	R/W	Initial	D7	D6	D5	D4	D3	D2	D1	D0
60h	Setting 5	R/W	00h	Setting5[7:0]							
61h	Setting 6	R/W	00h	Setting6[7:0]							

Setting5[7:0] In the case of PCM mode, set 16h
In the case of DSD mode, set 9Eh

Setting6[7:0] In the case of PCM mode, set 16h
In the case of DSD mode, set 1Eh

23. Address D0h, D3h (Boot 1, Boot 2)^(Note 3)

Address	Register Name	R/W	Initial	D7	D6	D5	D4	D3	D2	D1	D0
D0h	Boot 1	R/W	00h	Boot1[7:0]							
D3h	Boot 2	R/W	00h	Boot2[7:0]							

(Note 3) These registers are not listed in the register map because they are used only in power-on sequence.

Boot1[7:0] This register is used to prevent pop noise in power-on sequence.

Boot2[7:0] This register is used to prevent pop noise in power-on sequence.

The operation to prevent pop noise is shown below and it is necessary to keep the order.

1. Boot1[7:0] (D0h) = 6Ah
2. Boot2[7:0] (D3h) = 10h
3. Boot2[7:0] (D3h) = 00h
4. Boot1[7:0] (D0h) = 00h

Please refer to the "Power-On Sequence" section for more details.

System Clock

This section describes the system clock setting in PCM mode and DSD mode. When switching the system clock, it is necessary to execute the mode switching sequence. See the “[Mode Switching Sequence](#)” section for more details and see the “[Recommended Settings](#)” section for more details on recommended settings for each fs.

(PCM mode)

The system clocks required for PCM mode are MCLK, BCLK, and LRCLK. These clocks need to be synchronized but not in phase. The frequency of MCLK should be 22.5792 MHz or 24.5760 MHz. When fs = 32 kHz / 44.1 kHz / 48 kHz, the frequency of internal clock is lowered by MCLK division ratio setting ([MclkDiv \(04h\[1:0\]\)](#) = 10 (1/2 times) or 11 (1/3 times)). As a result, DVDD operating current can be reduced. In this case, high precision calculation ([HpcMode \(31h\[7\]\)](#)) function cannot be used and over sampling rate setting of $\Delta\Sigma$ modulator ([DsSetting \(40h\[4\]\)](#), [DsOsr \(40h\[1:0\]\)](#)) must be changed according to the MCLK division ratio setting. The following table shows system clock frequency settings and available combinations of register setting.

Table 15. System Clock Frequency Settings in PCM Mode

LRCLK (kHz)	BCLK (MHz)	MCLK (MHz)		MclkDiv (04h[1:0])		HpcMode (31h[7])		DsSetting (40h[4])	DsOsr (40h[1:0])	
32	2.0480	768 fs	24.5760	01	2/3 times	0/1	On/Off	1	00	x16
									01	x32
				11	1/3 times	1	Off	0	00	x8
									01	x16
								10	x32	
44.1 48	2.8224 3.0720	512 fs	22.5792 24.5760	00	1 time	0/1	On/Off	1	00	x16
									01	x32
				10	1/2 times	1	Off	0	00	x8
									01	x16
								10	x32	
88.2 96	5.6448 6.1440	256 fs	22.5792 24.5760	00	1 time	0/1	On/Off	1	00	x16
									01	x32
176.4 192	11.2896 12.2880	128 fs	22.5792 24.5760	00	1 time	0/1	On/Off	1	00	x16
									01	x32
352.8 384	22.5792 24.5760	64 fs	22.5792 24.5760	00	1 time	1	Off	1	00	x16
									01	x32
705.6 768	45.1584 49.1520	32 fs	22.5792 24.5760	00	1 time	1	Off	0	00	x8
									01	x16

(DSD mode)

The system clocks required for DSD mode are MCLK and DSDCLK. These system clocks need to be synchronized but not in phase. The frequency of MCLK should be same as DSDCLK or double. When the phase adjustment function for internal clock is enabled ([PhaseAdj \(06h \[0\]\)](#) = 1), the frequency of MCLK must be double DSDCLK. The following table shows system clock frequency settings.

Table 16. System Clock Frequency Setting in DSD Mode

DSDCLK (MHz)	MCLK (MHz)	
	PhaseAdj (06h[0])	
	0	1
2.8224	2.8224	5.6448
5.6448	5.6448	11.2896
11.2896	11.2896	22.5792
22.5792	22.5792	45.1584

Power-On Sequence

In the power-on sequence, the power supply is turned on in the order of DVDDIO, DVDD, and AVCC. After all power supply turned on, MCLK inputting, hard reset releasing (RESETB), and register settings with 2-wire I / F must be done. In the power-on sequence, initial setting must be done for all registers. Please execute the power-on sequence according to the following register setting and "Timing Chart". In case these sequences are not followed properly, normal operation cannot be guaranteed.

Table 17. Register Settings in Power-On Sequence

Step	Operations	Register Address	Register Settings
1	Initial Setting	04h	Clock 1
		06h	Clock 2
		10h	Audio I/F 1
		12h	Audio I/F 2
		13h	Audio I/F 3
		14h	Audio Output Polarity
		16h	DSD Filter ^(Note 1)
		17h	Audio Input Polarity
		20h	Volume Transition Time ^(Note 2)
		21h	Volume 1
		22h	Volume 2
		29h	Mute Transition Time
		30h	FIR Filter 1
		31h	FIR Filter 2
		33h	De-Emphasis 1
		34h	De-Emphasis 2
		40h	Delta Sigma
		41h	= 00h
		42h	= 16h
		43h	= 2Dh
48h	= 0Dh		
60h	Setting 5		
61h	Setting 6		
2	Software Reset Off	00h	= 01h
3	Digital Power On	02h	= 01h
4	Pop Nose Prevention	D0h	= 6Ah
		D3h	= 10h
		D3h	= 00h
		D0h	= 00h
5	Analog Power On	03h	= 01h
6	RAM Clear On	2Fh	= 80h
7	RAM Clear Off	2Fh	= 00h
8	Mute Off	2Ah	= 03h

(Note 1) DfSetting (16h[2]) must be set to 1.

(Note 2) VttSetting (20h[6:4]) must be set to 7h.

Power-On Sequence - continued

Timing Chart

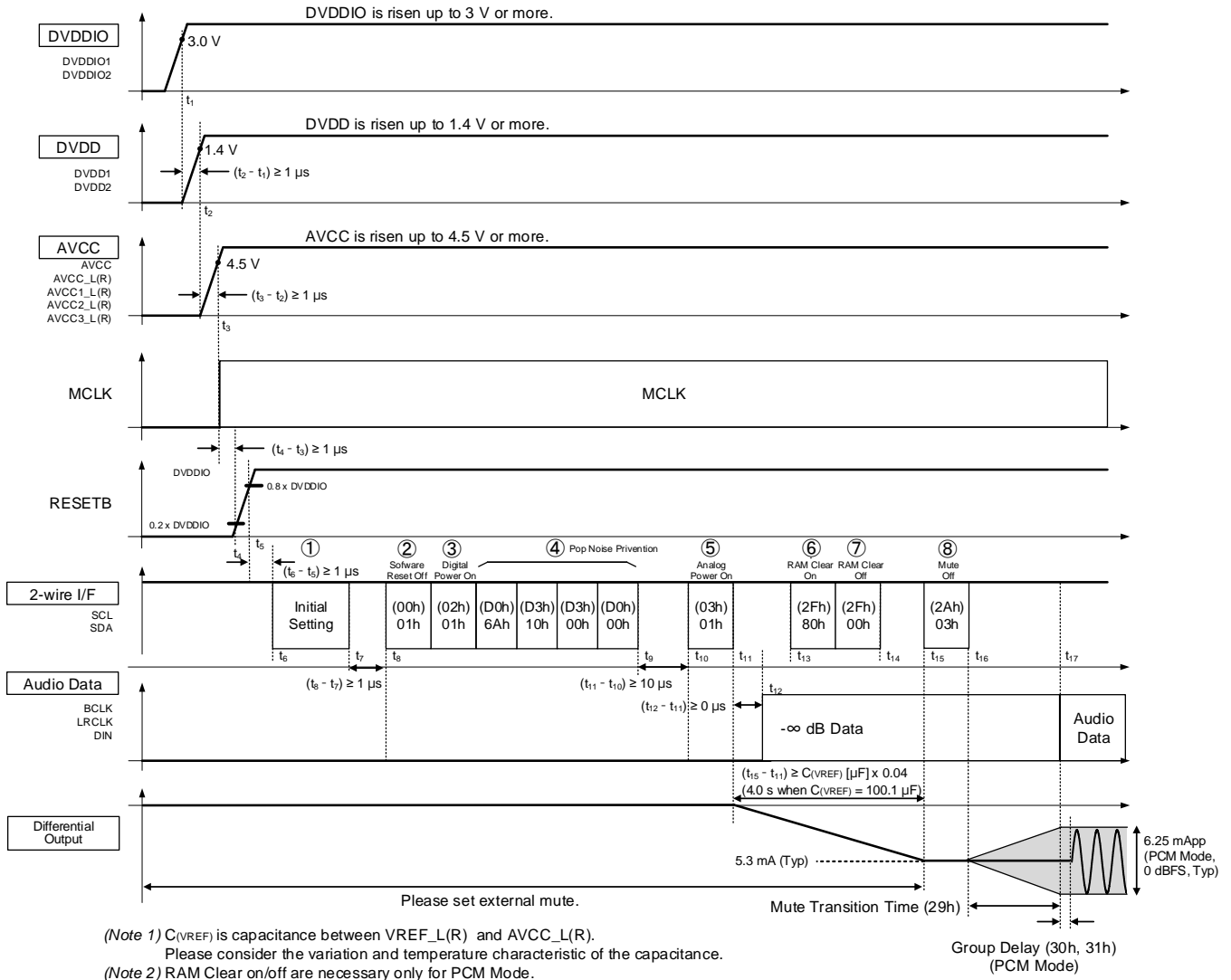


Figure 33. Power-On Sequence

Power-Off Sequence

In the power-off sequence, the power supply must be tuned off after register setting shown in the table below. The power supply should be turned off in the order of AVCC, DVDD, DVDDIO. Please execute the power-off sequence according to the following register settings and "Timing Chart". In case these sequences are not followed properly, normal operation cannot be guaranteed.

Table 18. Register Settings in Power-Off Sequence

Step	Operations	Register Address	Register Settings
1	Mute On	2Ah	= 00h
2	Analog Power Off	03h	= 00h
3	Digital Power Off	02h	= 00h

Timing Chart

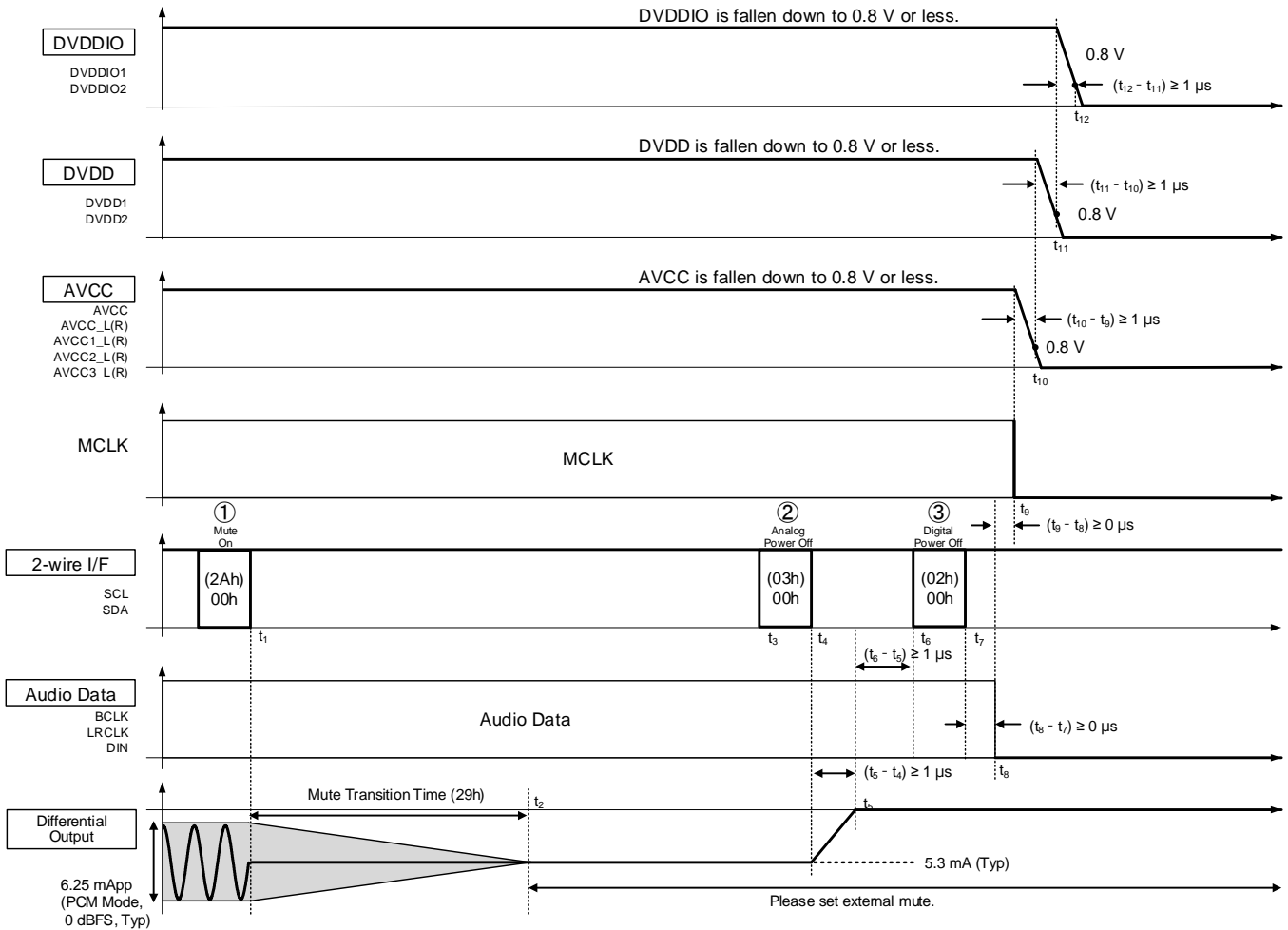


Figure 34. Power-Off Sequence

Mode Switching Sequence

Mode switching means switching from PCM mode to DSD mode, switching from DSD mode to PCM mode, and change of input signals (MCLK, BCLK / DSDCLK, LRCLK / DSD2, DSIN / DSD1) that accompany changes in sampling frequency in each mode. These input signals must be switched during software reset is on (SoftRst_X (00h[0]) = 0). Please execute the mode switching sequence according to the following register settings and timing charts. See the "Recommended Settings" section for more details on recommended register settings.

Table 19. Register Settings in Mode Switching Sequence

Step	Operations	Register Address	Register Settings	PCM Mode	DSD Mode
1	Mute On	2Ah	= 00h	○	○
2	Digital Power Off	02h	= 00h	○	○
3	Software Reset On	00h	= 00h	○	○
4	Mode Switching	04h	Clock 1	○	○
		06h	Clock 2	○	○
		10h	Audio I/F 1	○	○
		16h	DSD Filter	-	○
		30h	FIR Filter 1	○	-
		31h	FIR Filter 2	○	-
		40h	Delta Sigma	○	○
		60h	Setting 5 = 16h (PCM) / 9Eh (DSD)	○	○
		61h	Setting 6 = 16h (PCM) / 1Eh (DSD)	○	○
5	Software Reset Off	00h	= 01h	○	○
6	Digital Power On	02h	= 01h	○	○
7	RAM Clear On	2Fh	= 80h	○	-
8	RAM Clear Off	2Fh	= 00h	○	-
9	Mute Off	2Ah	= 03h	○	○

Caution: If mode switching sequence not be done according to the following timing charts, pop noise may occur. In such cases, please set external mute in parallel.

Timing Chart

PCM Mode to DSD Mode

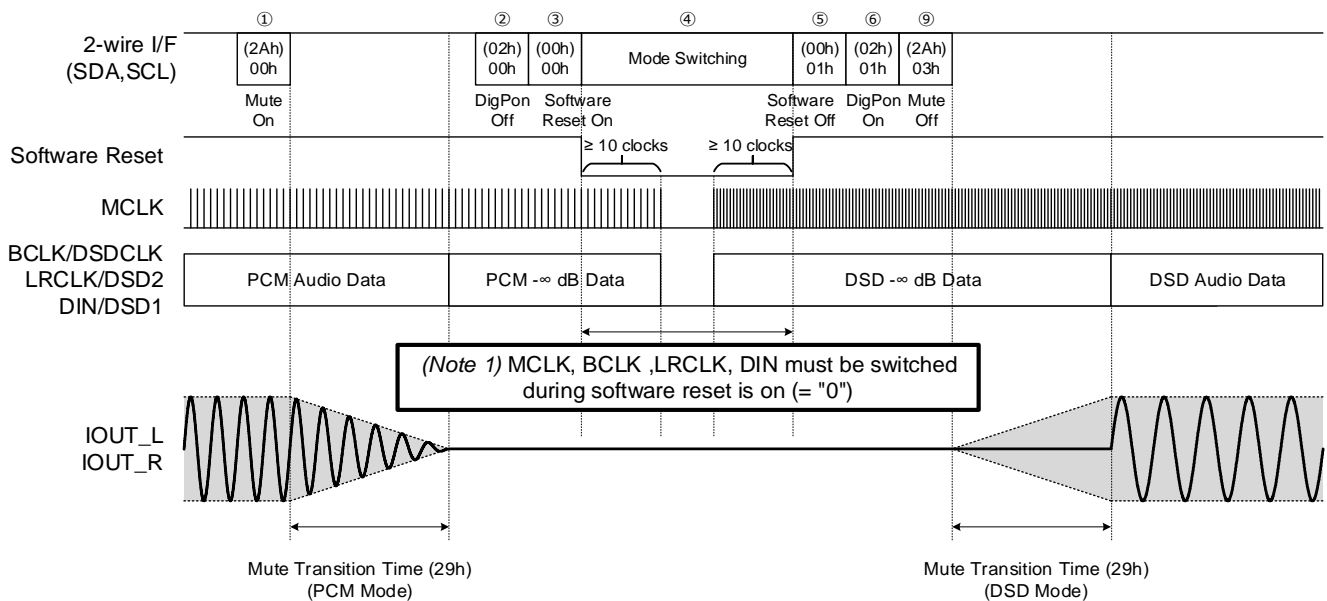


Figure 35. Mode Switching Sequence from PCM Mode to DSD Mode

Mode Switching Sequence - continued

DSD Mode to PCM Mode

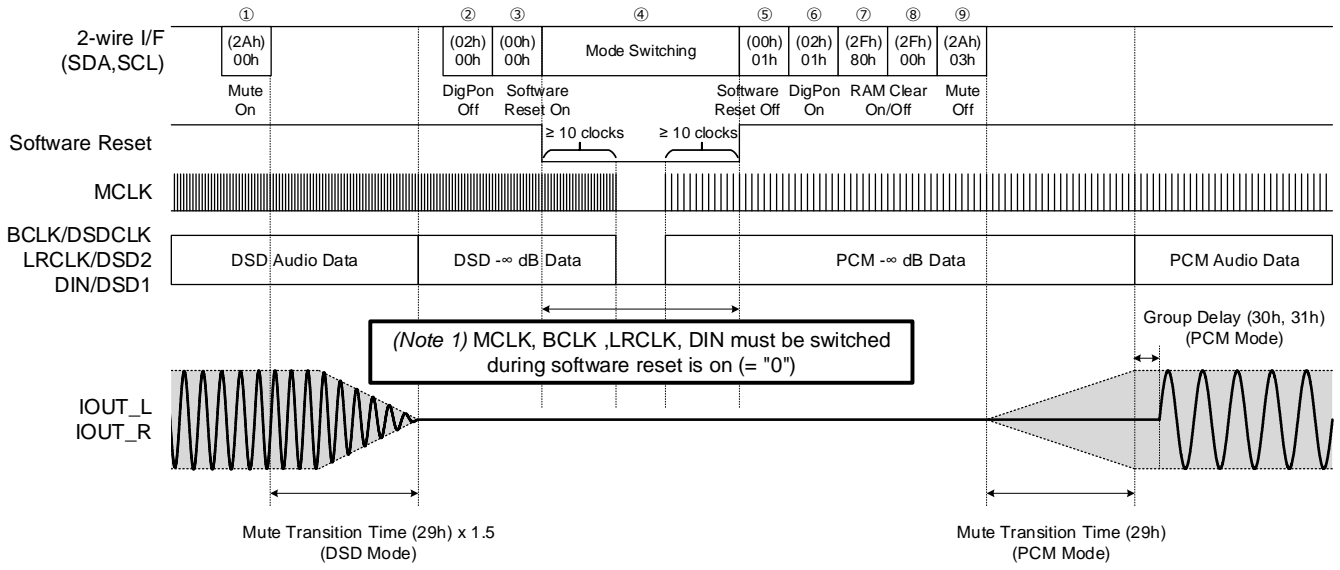


Figure 36. Mode Switching Sequence from DSD Mode to PCM Mode

Mode Switching between PCM Modes

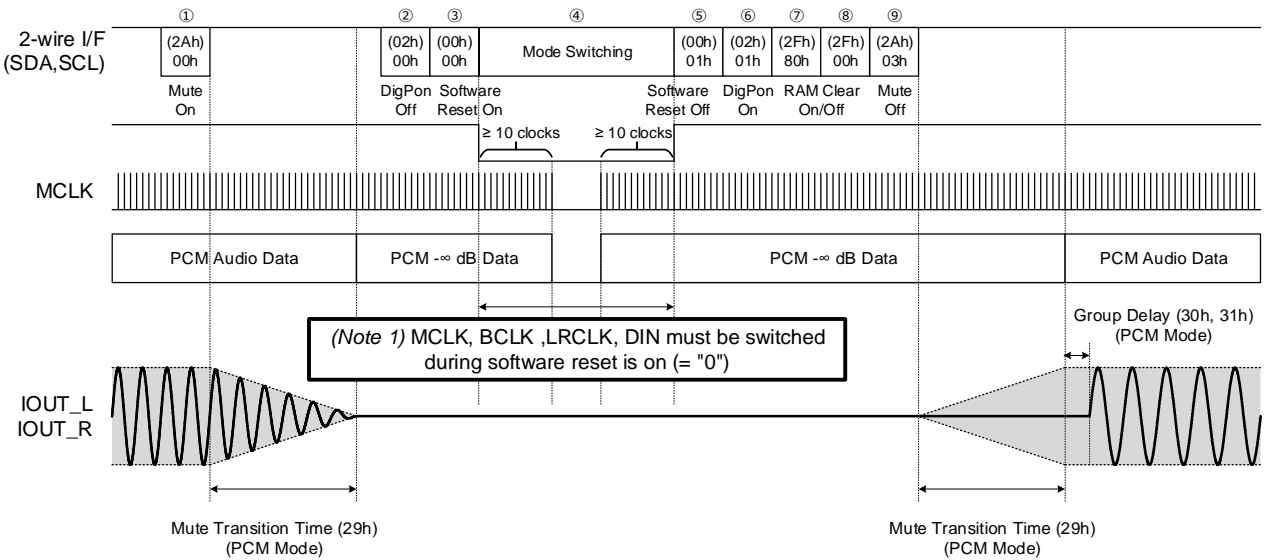


Figure 37. Mode Switching Sequence between PCM Modes

Recommended Settings

The recommended settings shown in the tables below get a good balance between electrical characteristics and sound quality for PCM mode and DSD mode.

Table 20. Recommended Settings in PCM Mode

fs (kHz)		32	44.1 48	88.2 96	176.4 192	352.8 384	705.6 768
MCLK (MHz)		24.5760	22.5792 24.5760	22.5792 24.5760	22.5792 24.5760	22.5792 24.5760	22.5792 24.5760
Address	Register	Recommended Setting					
04h	Clock 1	03h	02h	00h			
06h	Clock 2	00h					
10h	Audio I/F 1	0Bh					
30h	FIR Filter 1	01h		02h	04h	08h	
31h	FIR Filter 2	Sharp Roll-Off	80h	01h	02h	80h	
		Slow Roll-Off	83h	04h	05h		
40h	Delta Sigma	02h		11h			01h
60h	Setting 5	16h					
61h	Setting 6	16h					

Table 21. Recommended Settings in DSD Mode

DSDCLK (MHz)		2.8224	5.6448	11.2896	22.5792
MCLK (MHz)		= DSDCLK			
Address	Register	Recommended Setting			
04h	Clock 1	00h			
06h	Clock 2	00h			
10h	Audio I/F 1	8Bh			
16h	DSD Filter	06h	05h	04h	
40h	Delta Sigma	02h			
60h	Setting 5	9Eh			
61h	Setting 6	1Eh			

Sound Settings

In addition to selecting FIR filter (Sharp Roll-Off or Slow Roll-Off) or DSD filter, some register settings such that High Precision Calculation Mode, which is ROHM's original function, provide further adjustment of the sound quality. The registers are shown in the table below. Changing these register settings may affect audio characteristics such as THD+N. Please evaluate the register settings carefully before determining the setting value.

Table 22. Registers for Sound Setting

Register	Function
<u>PhaseAdj (06h[0])</u>	Phase adjustment for internal clock
<u>HpcMode (31h[7])</u>	High precision calculation for FIR filter
<u>DsSetting (40h[4]), DsOsr (40h[1:0])</u>	Over sampling rate of $\Delta\Sigma$ modulator

See the "Register Description" for more details on each register.

Application Examples

2ch Stereo

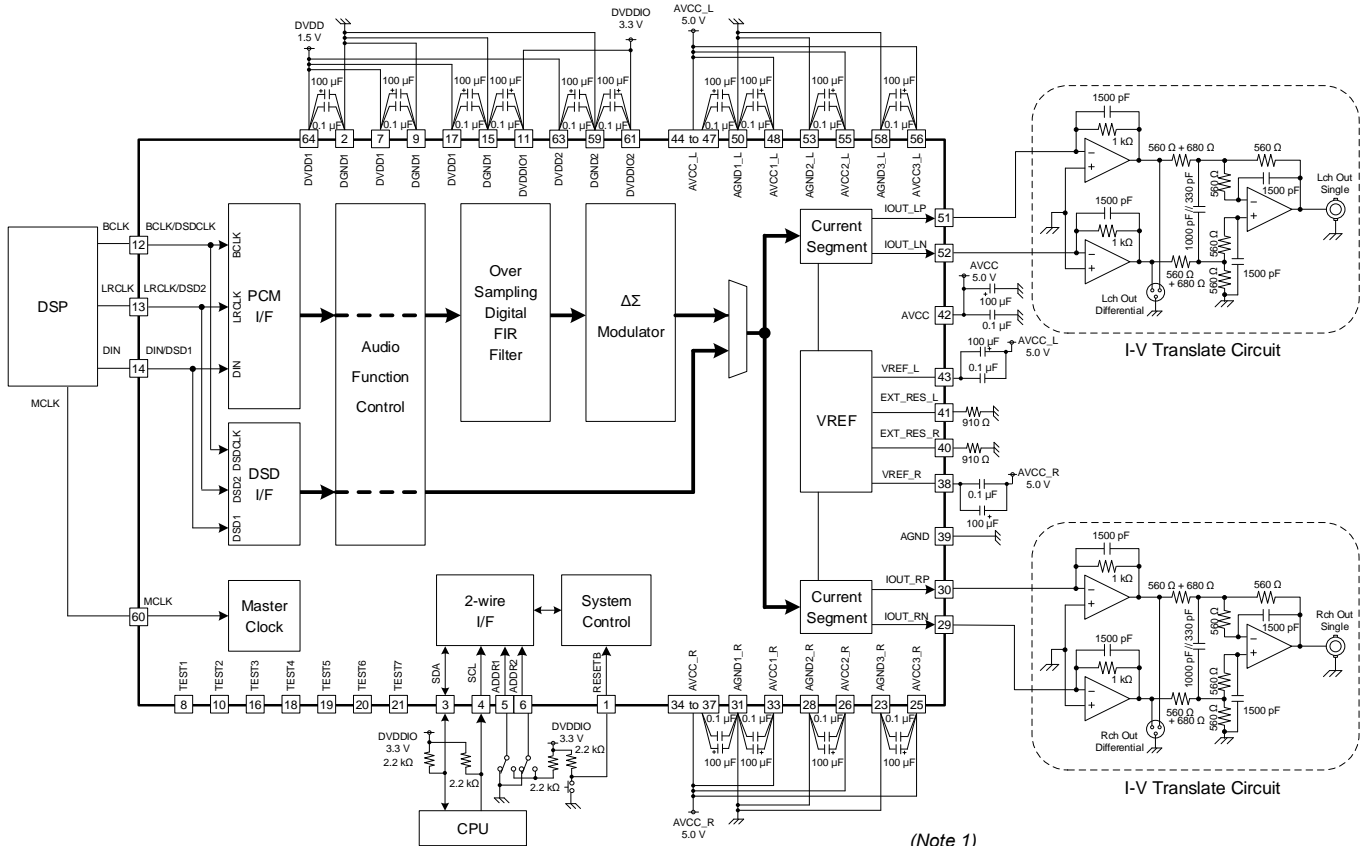


Figure 38. Application Circuit

(Note 1)
The written values of external parts are checked by sound test. Changing these values can affect the sound quality. Please check the sound when the values are changed.

I-V Translate Circuit (Enlarged)

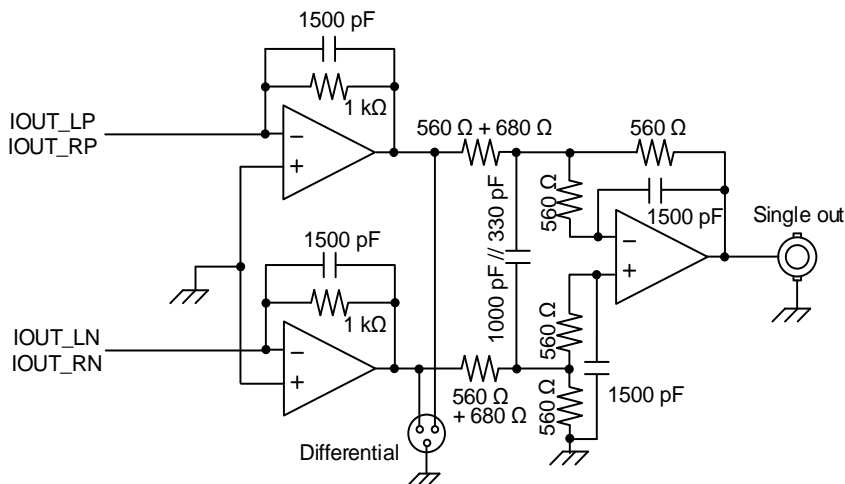


Figure 39. Application Circuit (I/V Translate Circuit)

Application Examples - continued

Mono Mode x2 - B

2ch stereo circuit can also configure Lch / Rch differential output in Mono Mode.

Table 23. Lch / Rch Differential Output Setting in Mono Mode

Setting	MonoSel (12h[1:0])		OutPol2 (14h[1])	
Lch output	10	Lch input	1	Rch polarity inverted
Rch output	11	Rch input	1	Rch polarity inverted

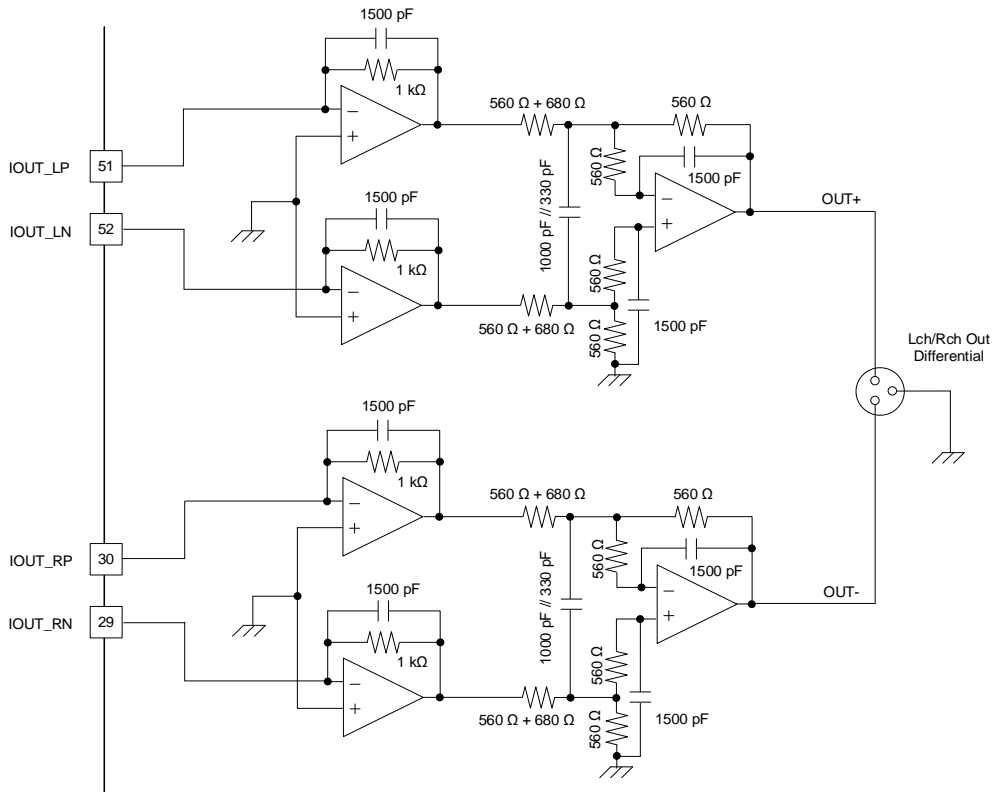


Figure 41. Application Circuit of Mono Mode x2 - B

Application Examples - continued

2ch x 2 = 4ch

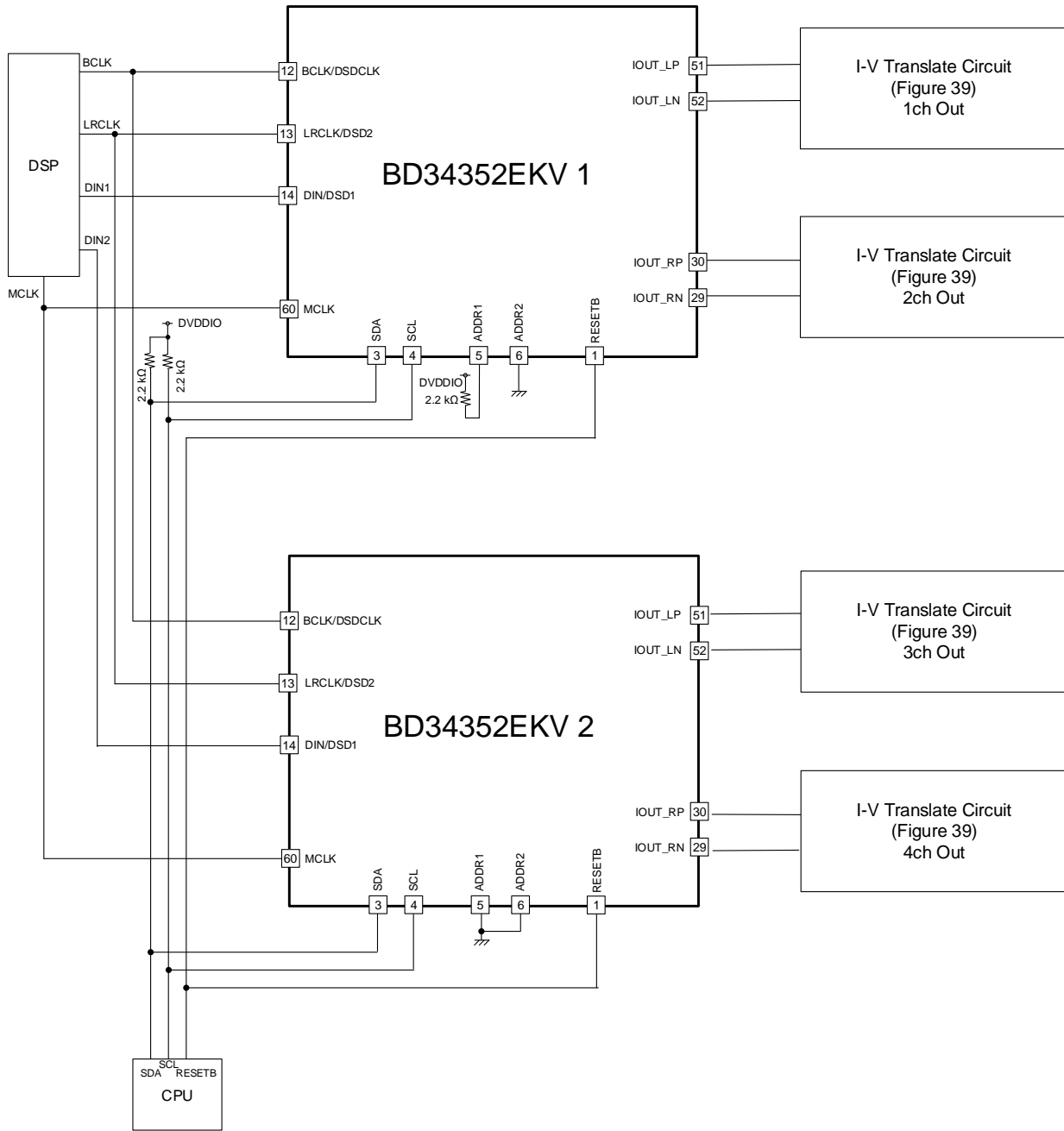


Figure 42. Application Circuit of 4ch Output

Application Examples - continued

2ch x 4 = 8ch

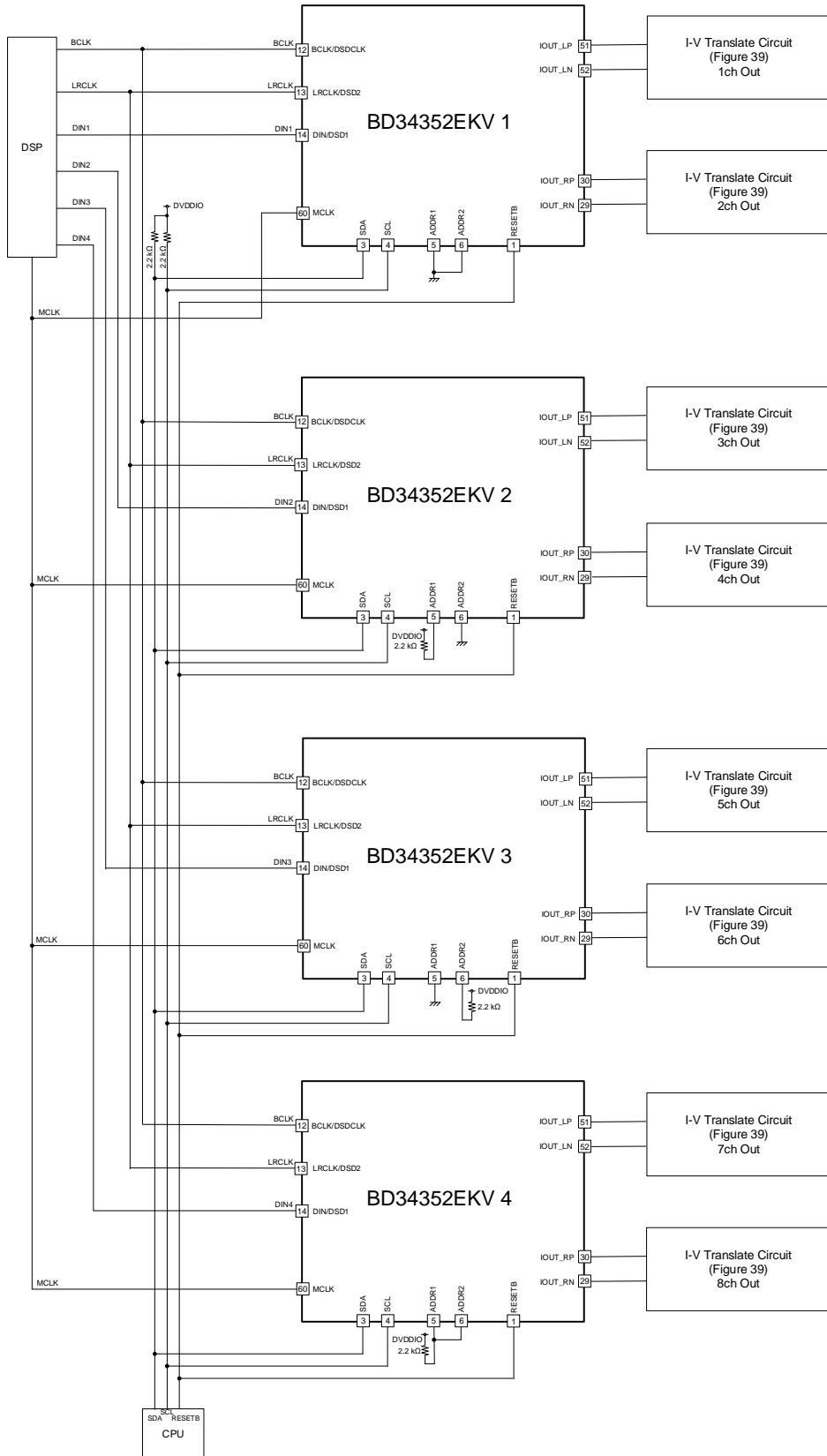


Figure 43. Application Circuit of 8ch Output

Operational Notes

1. Reverse Connection of Power Supply

Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. Power Supply Lines

Design the PCB layout pattern to provide low impedance supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. Ground Voltage

Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. Ground Wiring Pattern

When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. Recommended Operating Conditions

The function and operation of the IC are guaranteed within the range specified by the recommended operating conditions. The characteristic values are guaranteed only under the conditions of each item specified by the electrical characteristics.

6. Inrush Current

When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

7. Testing on Application Boards

When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

8. Inter-pin Short and Mounting Errors

Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

9. Unused Input Pins

Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

Operational Notes - continued

10. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When $GND > Pin A$ and $GND > Pin B$, the P-N junction operates as a parasitic diode.
 When $GND > Pin B$, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

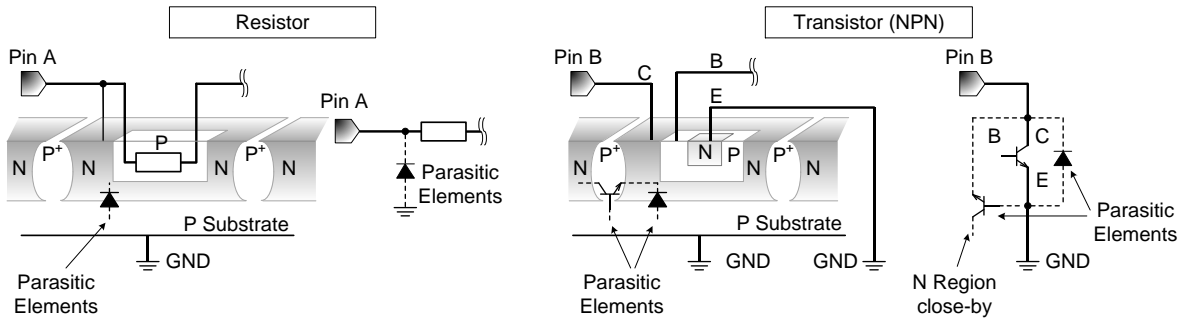
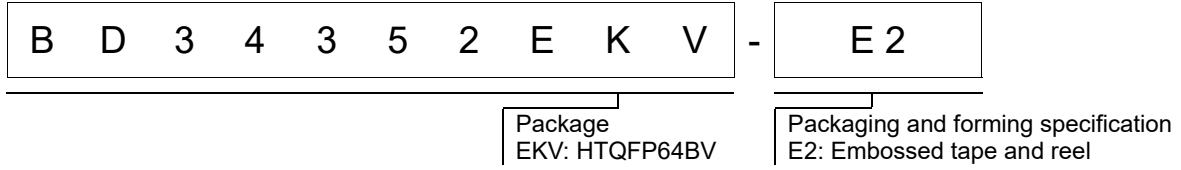


Figure 44. Example of Monolithic IC Structure

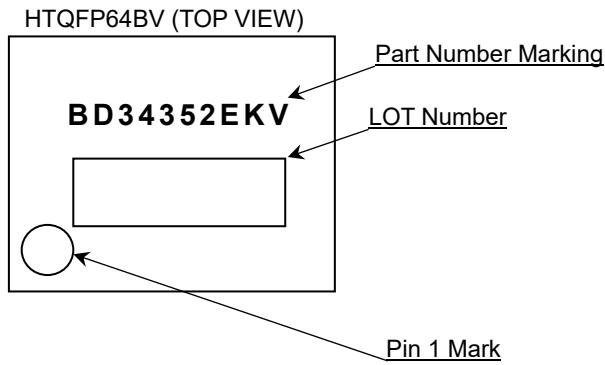
11. Ceramic Capacitor

When using a ceramic capacitor, determine a capacitance value considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

Ordering Information

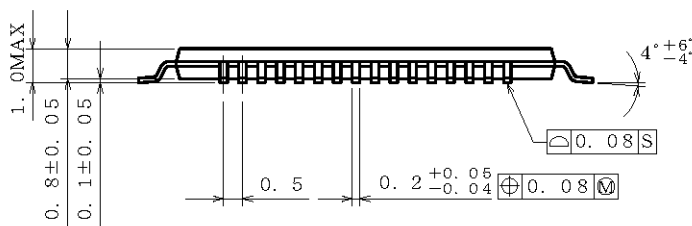
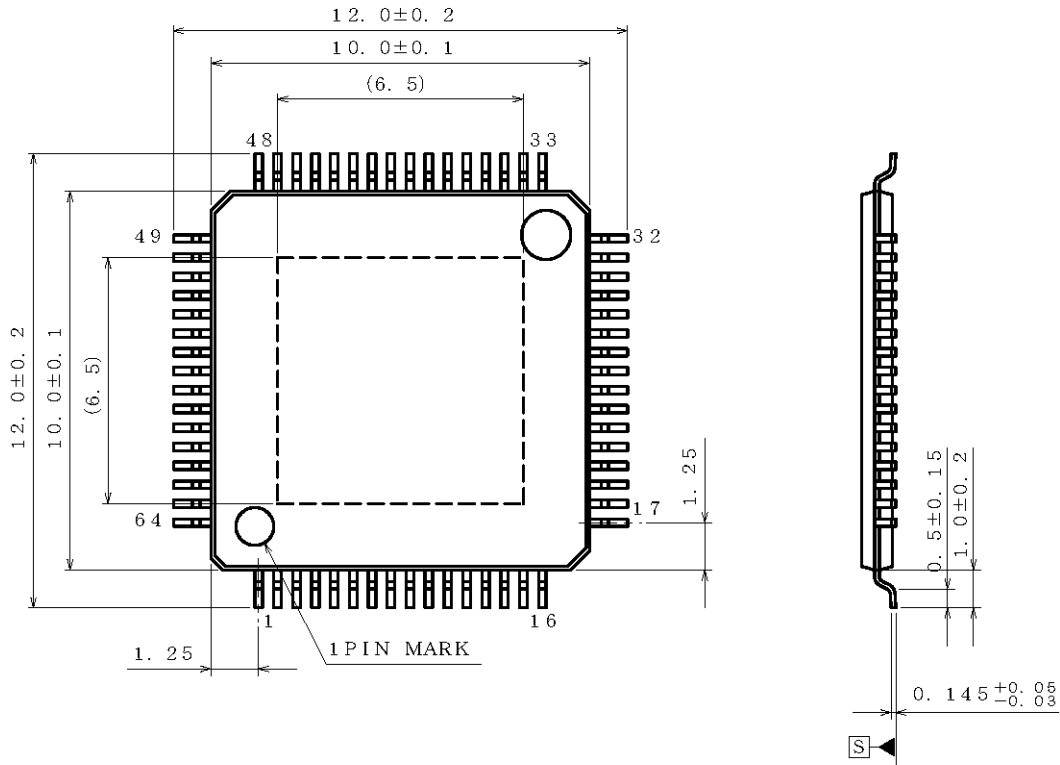


Marking Diagrams



Physical Dimension and Packing Information

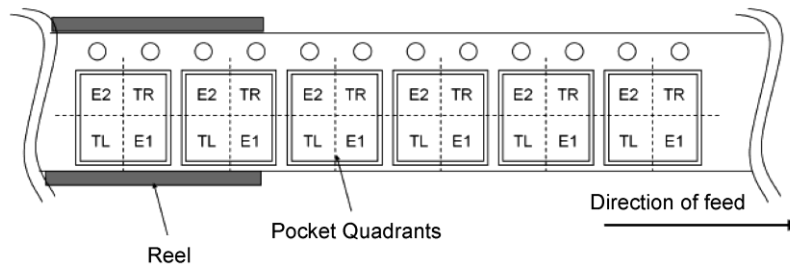
Package Name	HTQFP64BV
--------------	-----------



(UNIT : mm)
 PKG : HTQFP64BV
 Drawing No. EX282-5001-1

< Tape and Reel Information >

Tape	Embossed carrier tape
Quantity	1000pcs
Direction of feed	E2 The direction is the pin 1 of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand



Revision History

Date	Revision	Changes
05.Mar.2021	001	New Release

Notice

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- Our Products are designed and manufactured for application in ordinary electronic equipment (such as AV equipment, OA equipment, telecommunication equipment, home electronic appliances, amusement equipment, etc.). If you intend to use our Products in devices requiring extremely high reliability (such as medical equipment ^(Note 1), transport equipment, traffic equipment, aircraft/spacecraft, nuclear power controllers, fuel controllers, car equipment including car accessories, safety devices, etc.) and whose malfunction or failure may cause loss of human life, bodily injury or serious damage to property ("Specific Applications"), please consult with the ROHM sales representative in advance. Unless otherwise agreed in writing by ROHM in advance, ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of any ROHM's Products for Specific Applications.

(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASS III	CLASS III	CLASS II b	CLASS III
CLASS IV		CLASS III	

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 - Installation of redundant circuits to reduce the impact of single or multiple circuit failure
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 - Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
 - Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
 - Sealing or coating our Products with resin or other coating materials
 - Use of our Products without cleaning residue of flux (Exclude cases where no-clean type fluxes is used. However, recommend sufficiently about the residue.) ; or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
 - Use of the Products in places subject to dew condensation
- The Products are not subject to radiation-proof design.
- Please verify and confirm characteristics of the final or mounted products in using the Products.
- In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse, is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.
- De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.
- Confirm that operation temperature is within the specified range described in the product specification.
- ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

- When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.
- In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

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This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
 - [a] the Products are exposed to sea winds or corrosive gases, including Cl₂, H₂S, NH₃, SO₂, and NO₂
 - [b] the temperature or humidity exceeds those recommended by ROHM
 - [c] the Products are exposed to direct sunshine or condensation
 - [d] the Products are exposed to high Electrostatic
2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.
3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.
4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

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