

SIGMA2 & SIGMA LOGIC ANALYZERS



User's Guide

Features:

- Very large event memory (256 Mb)
- Up to 200 MHz sample speed
- Up to 16 inputs
- Flexible trigger options
- Controlled and powered by USB

SIGMA2/SIGMA: User's Guide v. 2.2, 2012-11-27

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TABLE OF CONTENTS

1. SIGMA2 AND SIGMA LOGIC ANALYZERS	3
2. INSTALLATION	3
3. TARGET CONNECTION	3
4. INDICATORS AND BUTTON	4
5 USING SIGMA & OMEGA LOGIC ANALYZERS SOFTWARE	5
5.1 Modes of operation	5
5.2 Input pins	6
5.3 Traces	7
5.4 Trigger settings	7
5.5 Quick start	8
5.6 Examination of measured data	8
6. PLUGINS	9
7. PROTOCOL DECODERS	12
7.1 UART Plugin (dll_uart.dll)	12
7.2 SPI Bus Analyzer Plugin (dll_spibus.dll)	12
7.3 I2C Bus Analyzer Plugin (dll_i2cbus.dll)	13
7.4 USB Analyzer Plugin	13
8. FREQUENCY MEASURING	
9. TECHNICAL SPECIFICATION	
9.1 Compresion specification	
9.2 Electrical specifications	19
10. PACKAGE CONTENTS	19
11 CONTACT INFORMATION	10

Note: This document contains hyperlinks pointing to web pages on the Internet. If the links happen to be broken (point to non existing page), please download recent version of this manual from www.asix.net.

1. SIGMA2 AND SIGMA LOGIC ANALYZERS

SIGMA2 and SIGMA are logic analyzers - development tools intended for tracing and debugging of TTL (and compatible) digital signals.

SIGMA is an original version of the logic analyzer, it was being delivered until November 2011. SIGMA2 is a new version which replaces original SIGMA; it has been available since December 2011. SIGMA2 is practically the same as SIGMA, it differs from its predecessor in following:

- new plastic enclosure
- different LED indication
- button added
- lower price

SIGMA2 name will be used in the following text for both logic analyzer versions if the features are the same. If there is a difference, SIGMA2 and SIGMA will be distinguished.

SIGMA2 is equipped with 256 Mb of memory and provides with up to 16 digital inputs and sampling rates up to 200 MHz. Built-in data compression allows for tracing of long running signals without exhausting logic analyzer memory. When using all 16 inputs, guaranteed minimum capacity is 14 million samples. SIGMA2 uses USB (Full-Speed, 12 Mbps) which ensures both data transfer and power delivery with a single cable. There is no additional power supply needed.

2. INSTALLATION

Install ASIX SIGMA&OMEGA APPLICATION PACKAGE to your computer. Connect SIGMA2 to a USB port or a USB hub using supplied cable. When a new device has been detected by operating system and it is asking for a driver, select option "install the driver from specific location" and navigate to the folder containing the driver (available on CD or for download at www.asix.net). The driver is not digitally signed thus you will be prompted to confirm installation of the driver.

Driver installation in Windows 7

For the driver instalation in Windows 7 use the latest driver downloaded from web or the driver included on SIGMA2 accessory CD-ROM. In Windows 7 the driver will not be installed automatically, it must be installed manually in a way described further: Open Device Manager and find connected SIGMA2 logic analyzer there. Open its properties window and select "Update driver". Select a location where the unpacked driver has been saved.

3. TARGET CONNECTION

The digital inputs are organized as two 8-pin ports (inputs 1 to 8 are merged into port 1, inputs 9 to 16 are merged into port 2). Pin-to-pin skew between inputs on a single port is rather low while it may be considerably higher between the ports. Trigger In (TI) may be used to initiate trigger by an external circuitry. Trigger Out (TO) indicates a trigger condition to an external

device (e.g. for measuring signal slope in particular conditions by an oscilloscope).



Fig. 1: Target connector

SIGMA2 is equipped by high impedance inputs with TTL logic levels (with 1 $\mbox{M}\Omega$ pull-down resistor).

Capacitance of probe cables should be taken into consideration when connecting to a debugged application, otherwise a cross-talks of fast signals may occur. The leads of the supplied cable with individual pins may be split to reduce capacitance between adjacent wires.

4. INDICATORS AND BUTTON SIGMA2 (new logic analyzer version only)

Main panel contains two bi-color LED indicators providing an operator with quick status information.

- • ONLINE / BUSY (green/yellow LED)
 - off: no USB power or USB is in Sleep mode or no USB driver has been installed
 - green: SIGMA2 was configured and it has been in idle state
 - *yellow:* SIGMA2 is acquiring data
- • TRIGGER STATUS (red/yellow LED)
 - *off:* trigger inactive no trigger condition has been detected
 - *red:* SIGMA2 is waiting for trigger condition
 - *yellow:* flashes when trigger condition or trigger pattern has been matched

The GO button helps to control the analyzer comfortably - it cyclically switches among essential operation states. When it is pressed in idle state the test is launched. When it is pressed in running state the trigger is initiated. And when it is pressed in triggered state the test is stopped, idle mode is launched and the data transfer from logic analyzer memory to PC begins.

SIGMA (old version of logic analyzer only)

Main panel contains seven LED indicators providing with overall status information at a glance.

- ON-LINE lights whenever SIGMA is connected with PC through USB
- **READY** lights when SIGMA has been configured and is in idle state
 USB BUSY indicates that data transfer is in progress
- TRIGGER WAIT SIGMA is waiting for trigger condition
- BUSY SIGMA is acquiring data
- **TRIGGER DETECT** flashes when trigger cond. or trigger pattern has been matched
- PIN CHANGE flashes upon change on an input pin

The button is not available at the old version of SIGMA.

5. USING SIGMA & OMEGA LOGIC ANALYZERS SOFTWARE

5.1 Modes of operation

SIGMA2 can operate in one of several modes possibly adapted to actual user needs or particular debugged application (all inputs with basic sampling rate or limited number of inputs at higher sampling rates). The mode of operation can be selected in *Settings/Clock source*.

Clocking Options
Clock Source Setup
 16 inputs, sampling rate 50MHz and lower Basic operation mode, sampling is derived from internal 50MHz oscillator. Sample rate can be divided by integer in range 1-256. 50 MHz
8 inputs, sampling rate 100MHz Sampling rate is fixed at 100MHz with reduced input pins to eight. Only pins Input1 to Input8 are used, only basic trigger options are available.
I inputs, sampling rate 200MHz Sampling rate is fixed at 200MHz with reduced input pins to four. Only pins Input1 to Input4 are used, only basic trigger options are available.
Async. clock source Data are sampled at fixed 50MHz, but stored only when selected pins toggles in the right way (DDR is also possible). In this mode, large setup and hold times are observed (1/50MHz=20ns). Clock-to-clock period can vary in full scale. Full trigger options are available. Maximum safe operating speed is approximately 20MHz. Input 1 Sample data on rising edge Sample data on falling edge
Sync. clock source In this mode, input holding Flip-Flops are sampled directly by edge of the selected clock. This mode profits in very small setup and hold times. Full trigger options are available. Maximum safe operating speed is 49MHz. PLL or DLL is not used, thus clock-to-clock period can vary, but clock must remain continuous. One or two successing clock-to-clock periods can be smaller than 10ns, but average clock period must be higher than 20ns. Clock must be applied before test starts. Input 1 Sec. Sample data on rising edge
Sample data on falling edge

Fig 2: Dialog možností režimu práce

- 16 inputs, 50 MHz (or slower, divided by 2 to 256)
- 8 inputs, 100 MHz, limited to port 1 only
- 4 inputs, 200 MHz, limited to first 4 inputs of port 1 only
- 16 inputs, 50 MHz, sampled only when selected pin has changed (asynchronous clock), rising, falling or both edges, max. clock speed ~ 40 MHz with 1:1 duty cycle, the asynchronous mode requires larger

amount of the analyzer memory space for saving of a sample, because the fact that the sample capture time must be saved as well.



Fig. 3: Sampling with asynchronous clock

 15 inputs, 1 synchronous clock input (only a first input on either port may be used as the clock signal), rising or falling edge, clock speed should be within the range of 1MHz to 99.9 MHz. The clock signal must be present before start of a test, several last samples are not contained in captured test because of pipelining.



Fig. 4: Sampling with synchronous clock

Data compression is used in any case, disregarding selected mode, giving possibility to capture long time running signals with precise timing. Actual compression ratio depends on characteristics of particular signal.

5.2 Input pins

Term **input pin** refers to physical input of SIGMA2. For user's convenience, aliases can be applied by *Settings/Inputs setup* or using I hotkey. The name may consist of letters, numbers and spaces and may be prefixed by hash (#), slash (/) or minus sign (-) to indicate negative polarity. Input names can also be indexed using a number in brackets which is typical for buses.

Bus copy function and keypresses Ctrl+1 or Ctrl+1 help to automate the naming process of bus signals. *Fill traces* function can be used to generate traces according to input signal names automatically.

5.3 Traces

Term **trace** refers to visualization of acquired data. A trace can be composed of several inputs as well, otherwise a single input may be used in multiple traces, e.g. it is possible to visualize several inputs as a bus while still having the possibility to display individual signals.

Traces are defined in *Settings/Traces setup* or using Ctrl+T hotkey. If a trace is defined as a bus, the value on the bus will be displayed according to configurable formatting. Radix from 2 to 36 can be used to format the value as a number using alphabetical characters for digits above 9. There are also special formatting options for displaying data as ASCII characters. Values which do not represent a printable character in selected set are shown as hexadecimal numbers. The output may be prefixed, suffixed, padded with zeros from the left to given particular width and likewise digit grouping can be used.

Traces can be also edited in main window by double clicking on a particular trace. Context menu in the main window can be used to add or remove traces.

5.4 Trigger settings

Trigger settings dialog can be invoked from menu by *Settings/Trigger Setup* or using a T hotkey.

Availability of certain trigger settings depends on clock settings. For sample rates of 100 and 200 MHz, only basic trigger on edge of selected input signal is available. In other modes either pin trigger or advanced trigger can be used. Advanced trigger allows user to precise specification of trigger condition likewise precondition which has to precede for the trigger to be activated.

Pin trigger settings define trigger event as combination of desired levels and edges on input pins. The trigger can occur immediately (occurs as soon as the defined combination turn up) or delayed by a counter.

Advanced trigger settings define trigger event by a boolean expression. A visual expression builder is used to create or edit the expression. There is a list of terms in expressions:

- simple input or trace a name: Input0, CLK, MISO
- a bus signal: BUS[0] or BUS(0)
- comparison with a constant: IN5=0, BUS=A6, BUS=h'a6', BUS=b'10100110', BUS=d'166'
- optionally prefixed with a negation operator: !TERM, -TERM, #TERM, /TERM

An optional precondition can be defined the same way. The trigger can be immediate, delayed by a counter or set to react on a certain event length, time distance of two events, or a gap length between events. Although this approach makes the describtion of very complex situations possible, accordingly it allows to define moment to be captured precisely, there are certain limitations determined by capabilities of the hardware. If the expression is too complex to be implemented in the hardware, exclamation icon appears to indicate this fact.

Other trigger settings include configurable post-trigger time, style of visual indication of the trigger using the LED, trigger out type (CMOS or open collector output) and Trigger In polarity and pull up/down resistor.

5.5 Quick start

- 1) Attach SIGMA2 to debugged application and launch ASIX SIGMA&OMEGA LOGIC ANALYZERS software.
- 2)Use *Settings/Clock source* dialog to select desired sampling rate and mode.
- 3)Open *Settings/Inputs setup* to rename input signals for your convenience (optional step).
- 4) Setup traces in *Settings/Traces setup* dialog to add traces.
- 5) Define trigger condition in *Settings/Trigger setup* dialog.
- 6) Finally run the test using *File/Test* command or simply hit **ENTER** in the main window.

This procedure can be followed automatically by selecting the menu item *Settings/Connection wizard*.

5.6 Examination of measured data

Navigation in the main window can be controlled by keyboard, mouse or by combination of both.

Sliding left/right along the time axis is controlled by left/right cursor arrows, <code>PgOp/PgDm</code> keys, mouse scrollwheel, mouse motion while holding down <code>Ctrl</code> key or by dragging the horizontal scrollbar.

Zooming is controlled by + and - keys, rotating scroolwheel while holding down Ctrl key. The * key zooms to 1:1 (every sample visible) while the / key zooms out to preview all available data at once. Highlighting part of the screen by dragging the mouse zooms to selected region.

6. PLUGINS

ASIX SIGMA&OMEGA LOGIC ANALYZERS software features modular design to add functionality according to users needs. This modularity is achieved by using **plugins**.

Plugins are dynamically loadable libraries (DLL files) located in the main program folder. Individual plugins can be enabled or disabled in *Settings/Plugins* dialog and configured in *Settings/Plugin Settings*

(if applicable). Several plugins are part of the ASIX SIGMA&OMEGA APPLICATION PACKAGE by default.

Some data decoded by some plugins (UART, SPI, I²C) can be inserted among captured signals as a virtual track. For that feature go to the *Settings/Traces Setup menu*. When the track is market by a click, the plugin can be chosen in the ComboBox on the right.

Bookmarks (dll_bookmarks.dll)

This plugin provides with possibility to define up to 10 bookmarks for convenient navigation in the data. Press Ctrl+shift+0 up to Ctrl+shift+9 to place or remove a bookmarks. To navigate to an existing bookmark, press Ctrl+0 up to Ctrl+9. To use the bookmarks cursor providing plugin (e.g. dll_mousecursor.dll) has to be enabled.

Edge search (dll_edgesearch.dll)

It enables easy motion over the signal edges. Press $Alt+ \leftarrow$ or $Alt+ \rightarrow$ to jump to nearest previous or next edge of the selected trace.

Show time at mouse pointer (dll_hinttime.dll)

It shows time position of the cursor location as a tooltip.

Other derived inputs (dll_inv.dll)

It adds virtual input signals which are inversions of real inputs.

Mouse Cursor (dll_mousecursor.dll)

It draws a vertical line under mouse cursor position. It also provides with magnetic edges and snapping to grid.

Disallow multiple instances (dll_mutex.dll)

This plugin simply assures that no more than a single instance of the SIGMA&OMEGA LOGIC ANALYZERS software is running at a time.

Show already downloaded from SIGMA2 (dll_sig0.dll)

SIGMA&OMEGA LOGIC ANALYZERS displays a raw preview of performed test as soon as data has been captured, there is no need to wait until complete test has been downloaded from SIGMA2. Then the detailed data is being downloaded with areas of user's interest first (i.e. when zooming in) in the background. Data which hasn't been downloaded yet are displayed as a gray background.

Simple marker (dll_simplemarker.dll)

Allows user to place a single mark at the cursor position by pressing spacebar. This is particularly useful for measuring time distance between two points (place the mark to one location, move the cursor to the other one and watch the tooltip).

<u>UART Plugin (dll_uart.dll)</u>

It decodes one or more captured UART signals and displays data in ASCII, decimal or hexadecimal value.

<u>SPI Bus Analyzer Plugin (dll_spibus.dll)</u>

It decodes captured signals such as SPI and displays data in hexadcimal value.

I2C Bus Analyzer Plugin (dll_i2cbus.dll)

It decodes captured signals such as I^2C and shows start bits, stop bits, addresses, acknowledges (ACK) and data in hexadecimal values.

USB 1.1 Plugin (dll_usb.dll)

Decodes captured signals as USB 1.1 signals. First a new decoder must be added in the *Settings/Plugin Settings/USB Plugin Configurations* menu using *Add New Decoder* button and the captured signals traces to be decoded must be chosen. After the OK button is pressed, a decoded data window is opened. The data decoding is started by menu *Other/Decode Now!* click or by the row key press. The communication can be decoded automatically after the data has been downloaded from the analyzer if there is *"Decode protocol automatically upon data download"* checked in the settings.

After decoding, the communication is displayed in a tree structure where all the packets are listed. The decoded packets can be itemized on the bits level. After clicking the decoded packet or some its part, the appropriate part of the captured tracks is highlighted. After right mouse button clicking a *Zoom* function from the local menu can be used, it shows the chosen section captured signals over all the width of the screen. The *Search/Find* function of the main menu provides various possibilities how to search in the decoded data.

It is required that a license is bought for the USB plugin functionality. The license is assigned to the logic analyzer hardware.

A dedicated hardware probe for easy connection of the USB signals to logic analyzer can be purchased optionally. It is equiped with two USB A connectors (plug and receptacle) and pins for the logic analyzer connection. The logic analyzer can be connected either directly to the USB signals or to the buffered USB signals. On the USB cable there must be found a suitable position for the probe, where the captured signals are the best quality. Additional plugins can be provided in the future.

Source codes of some plugins are released under GPL, thus users are free to modify or create plugins.

7. PROTOCOL DECODERS

Protocol decoders are drawn up as plugins.

7.1 UART Plugin (dll_uart.dll)

It decodes captured UART signal and displays that as ASCII characters, decimal or hexadecimal values.

UART Settings	
UART #1 UART #2	
UART #1	Add New Decoder
Source: RA4	Delete This Decoder
 Line is inverted (<0.8V = log.1; >2.0V = log.0) Start Bit is inverted (log.1) Stop Bit is inverted (log.0) Display Start Bits Display Stop Bits Display Parity Bit Display Bit Frames 	
Start bits: 1 💌 Data bits: 8 💌	
Stop bits: 1	
Parity: None 💌	
Speed: 2400 💌	
Display: hexadecimal 💌	
<u>Q</u> K <u>C</u> ancel]

Fig. 5: UART Plugin

There are several features available in UART plugin setting such as input selection, inversion of signal before decoding - which is an advantage for direct connection of **voltage level limited** RS-232 (user must be aware of minimal and maximal voltage level on Sigma2 inputs), start bit polarity thus selection of quiescent logic level, selection of visibility of start bits, stop bits, data bits and parity bits.

Furthermore it is possible to choose length of start and stop bits, type of parity

and word length. There are predefined UART baud rates or user defined baud rate (by bauds per second or by number of samples of logic analyzer per a bit)

7.2 SPI Bus Analyzer Plugin (dll_spibus.dll)

This plugin decodes captured SPI signal and displays that as hexadecimal values. For correct function it is necessary to set up appropriate data input, clock input and input that trigger counting out bits in a byte.

SPI Settings		
SPI #1		
SPI Bus #1		Add New Decoder
DATA Source:	Input1	Delete This Decoder
CLK Source:	Input2	🔽 🔽 DATA on rising edge
SYNC Source:	Input3	🔽 📃 Start on rising edge
📃 DATA are N	1SB	
	<u>0</u> K	Cancel

Fig. 6: SPI Plugin settings

It is possible to choose bit order (MSB first, LSB first), synchronising on rising or falling edge (signal chip select in positive or negative logic level) and data sampling on a rising or falling edge of clock signal.

7.3 I2C Bus Analyzer Plugin (dll_i2cbus.dll)

This plugin decodes captured I2C signal and displays start bits, stop bits, addresses, acknowledges and data in hexadecimal values.

I2C Bus Sett	tings	_	
I2C Bus #1			Add New Decoder
SCL Source::	Input1	~	Delete This Decoder
SDA Source:	Input2	~	
🔽 Display I2	C address byte 7bit long		
	<u>0</u> K		Cancel

Fig. 7: I2C Plugin settings

Each of input signals can be choosen as SDA or SCL signal. There are two possibilities how to display I2C address: with or without the LSB displayed (e.g. A0/A1 device address is displayed as A0W/A1R in first case or 50W/50R in the other).

7.4 USB Analyzer Plugin

Reading the USB specification is highly recommended before using USB Analyzer plugin.

Instalation

USB analyzer has been drawn up as one of the plugins and it is a part of the installation package and so there is no need to install that. For setting up the license hit License \rightarrow Install New License... in SIGMA2 main form.

Add New License
Add New License Licence:
123456789abcdef0123456789abcdeff
User Comment (for further identification):
<u>©</u> AC

Fig. 8: Adding a new license

What to measure

With USB analyzer plugin users can analyze USB 1,5 Mbps (Low-Speed) and 12 Mbps (full speed) data rate communication captured by *SIGMA2* analyzer.

Measure tool attachment

Although USB data comunication si partly differential, GND and both USB data signal (DATA+,DATA-) must be connected to *SIGMA2* analyzer. *SIGMA2* samples that signal with enough accuracy as a common TTL signal. Due to NRZI coding, which USB uses, analyzer does not distinguish between DATA+,DATA-, so they are interchangeable. But there are some line states on USB using single-ended signalling (e.g. Bus Reset a End-Of-Packet); that is the reason why connecting DATA+, DATA- only is not enough. Swapping the data lines the data rate is choosen. Behind the USB hub to Low-Speed (1.5 Mbps) device there is only Low-Speed communication, whereas to Full-Speed (12 Mpbs) device there are both Low-Speed and Full-Speed communication. 480 Mbps communication is called High-Speed and *SIGMA2* is not able to measure that.

USBprobe, which is attached, includes two 74AHCT125 TTL gates and USB connectors A and B wired so that it provides a USB extension. *SIGMA2* logic analyzer can be connected before or beyond the logic gates, it depends on an application – better to try. Generally, better results is reached with *USBprobe* connected directly to USB hub and the shorter USB cable, the better. Likewise it is important to shorten the way between *USBprobe* and *SIGMA2*.

On *USBprobe* there is 5V from PC directly accessible (through a 800mA irreversible fuse) – avoid a shortage! **It is highly inadvisable to join USBprobe directly to PC ports.** We suggest using USB hub with an external power source and joining *USBprobe* directly into that.

<u>Measuring</u>

Measuring is possible only with a purchased license.

USB data signals (DATA+, DATA-) can be connected to any two inputs, other inputs are allowed to be used for measuring of another signals or e.g. for measuring of another USB communications. Measuring of more than only one USB communication is possible.

Processing

When signals have been captured (= the test has been done) it is necessary to decode it. It can take tens of seconds depending on amount of the captured data. Decoding is proceed automatically, promptly when the data have been captured, if it is enabled in the USB analyzer settings dialog or it can be launch in the menu by choosing Decode \rightarrow Decode Now! or hitting **P**.

When decoding have finished there is a list of measured USB events in the events window (which is simultaneously the main window).

<u>Viewing</u>

Consider that decoding have finished and list of measured USB events is in the events window.

For decreasing number of events in the event window a configurable filter can be applied so that only requested events are displayed. For that option open the menu Settings \rightarrow Filter Settings. One or more USB addresses can be marked as requested such as 0,5..7 within range of 0 to 127 (USB uses 7bit wide address range). The same principle applies to endpoints within range of 0 to 15 (the endpoint direction – bit 7 - does not matter).

The zero address is dedicated for devices without address set. Likewise the zero endpoint is special control endpoint, which each device must include, the only one that support bidirectional transactions.

Due to the fact that the USB specification does not allow single devices to send data on they own the major part of the traffic is occupied by master (PC) asking slaves if data has got ready.

Therefore it can be useful to mask that frames without any data (terminated by NAK token), for doing that, as well as masking frames which is not destined for any particular device(e.g. Start-Of-Frame token, Bus Reset), visit the menu Settings \rightarrow Filter Settings.

On the highest level there is possibility to display or hide transactions ended by NAK token or ACK token, for that option use right mouse button and choose it from menu.

USB Filter Settings	8
C Shown packets	
Show packets for addresses	0127 ALL
and endpoints	015 ALL
Show addressless and end Hide NAKed transactions	lpointless packets
ОК	Cancel

Fig 9: USB Filter settings

Another way how to pop-up the Dialog Settings \rightarrow Filter Settings menu is to click on the title of Addr or on the Endpoint column.

5B SIGMA Plugin						×	USB SIGMA Plugin						
earch <u>D</u> ecode S	<u>e</u> ttings <u>H</u> e	lp .					Search Decode Sg	attings <u>H</u> ei	lp .				
Time	Length	Addr	Endp	Record	Notes		Time	Length	Addr	Endp	Record	Notes	
4 590 246 093ns	37.9µs	2	81	IN transaction	NAK	<u>^</u>	1 960 223 868ns	4.4ms	2	Control	Control transfer	Get unknown type (34) Descriptor 0	
4 594 245 903ns	37.8µs	2	82	IN transaction	NAK		2 990 783 858ns	337.9µs	2	Control	Control transfer	Class Specific Request 9	
4 598 245 713ns	37.8µs	2	81	IN transaction	NAK		4 014 274 803ns	106.8µs	2	81	IN transaction	ACK	
4 602 245 523ns	37.9µs	2	82	IN transaction	NAK		4 070 271 993ns	107.5µs	2	81	IN transaction	ACK	
4 606 245 298ns	107.5µs	2	81	IN transaction	ACK		4 222 264 438ns	106.8µs	2	81	IN transaction	ACK	
4 610 245 108ns	37.8µs	2	82	IN transaction	NAK		4 294 260 863ns	107.6µs	2	81	IN transaction	ACK	
4 614 244 883ns	37.9µs	2	81	IN transaction	NAK		4 542 248 523ns	107.6µs	2	81	IN transaction	ACK	
4 618 244 723ns	37.8µs	2	82	IN transaction	NAK		4 606 245 298ns	107.5µs	2	81	IN transaction	ACK	
4 622 244 533ns	37.9µs	2	81	IN transaction	NAK		4 678 241 723ns	107.5µs	2	81	IN transaction	ACK	
4 626 244 308ns	37.9µs	2	82	IN transaction	NAK		4 742 238 533ns	107.6µs	2	81	IN transaction	ACK	
4 630 244 118ns	37.8µs	2	81	IN transaction	NAK		4 854 232 953ns	106.8µs	2	81	IN transaction	ACK	
4 634 243 893ns	37.8µs	2	82	IN transaction	NAK		4 918 229 763ns	107.4µs	2	81	IN transaction	ACK	
4 638 243 738ns	37.8µs	2	81	IN transaction	NAK		4 982 226 573ns	106.9µs	2	81	IN transaction	ACK	
4 642 243 513ns	37.8µs	2	82	IN transaction	NAK	~	5 062 222 548ns	107.6µs	2	81	IN transaction	ACK	1

Fig 10: Window with hidden transactions which are ended with NAK

<u>Searching</u>

For searching for a specific type of packets or events (Bus Reset, Error, Stuffed Bit) open the Search \rightarrow Find... menu or hit Ctrl+F and then for another occurrence hit F3 key.

Find	X
Find IN token OUT token SETUP token SOF token ACK packet MAK packet ØDATA0 packet ØDATA1 packet Stuffed bit Bus Reset Error Origin © From Current Selection Entire Scope	Data Packet Contents Search string: • Data Packet Starting with • Data Packet Containing • Exact Data Packet Payload Match Scope IN transactions V OUT transactions SETUP transactions 0.127 Only transactions with address 0127 Only transactions with endpoint 015 V Unknown / no transactions
ОК	Cancel

Fig. 11: Finding window

	ogic Analyzer 1.12.						
ile View :	Settings Licence Help						
4	982 240 µs 4 982 250	µs 4.982	260 µs	4 982 2	70µs 4982280µs 4982	290 µs 4 982 300 µs 4 982 310 µ	ıs 4,982,320µs 4,982
Insut1			Hinr	INNNN			
inputi –		וח חחו	ם ח	ппппг			
Input2	זר הרות החר	וח חחו	1 00	ппппг	וחחחחחחחחח חחו		
Input3 –							
Input4							
-							
	USB SIGMA Plugin						×
	Search Decode S	ettings Hel	P				
	Time	Length	Addr	Endp	Record	Notes	
	4 970 227 178ns	37.9µs	2	82	IN transaction	NAK	^
	4 974 226 953ns	37.8µs	2	81	IN transaction	NAK	
	4 978 226 763ns	37.8µs	2	82	IN transaction	NAK	
				01	- mar	1 OK	
	4 982 226 573ns	106.9µs	2	81	IN transaction	ALK	
	4 982 226 573ns 4 982 226 573ns	106.9μs 22.7μs	2	81	in transaction ⊕ IN token	AUK	
	4 982 226 573ns 4 982 226 573ns 4 982 252 398ns	106.9µs 22.7µs 65.6µs	2	81	IN transaction IN token DATA0 packet	ALK 00 00 2C 00 00 00 00 00	
	4 982 226 573ns 4 982 226 573ns 4 982 252 398ns 4 982 321 433ns	106.9µs 22.7µs 65.6µs 12.0µs	2	81	IN transaction IN token DATA0 packet ACK packet	00 00 2C 00 00 00 00 00	
	4 982 226 573ns 4 982 226 573ns 4 982 225 398ns 4 982 321 433ns 4 986 226 348ns	106.9µs 22.7µs 65.6µs 12.0µs 37.8µs	2 2 2	81 81 82	IN transaction IN transaction DATA0 packet ACK packet IN transaction	ALK 00 00 2C 00 00 00 00 00 NAK	
	4 982 226 573ns 4 982 226 573ns 4 982 226 573ns 4 982 252 398ns 4 982 321 433ns 4 986 226 348ns 4 990 226 158ns	106.9µs 22.7µs 65.6µs 12.0µs 37.8µs 37.8µs	2 2 2 2 2	81 81 82 81	IN transaction IN transaction IN token DATA0 packet ACK packet IN transaction IN transaction IN transaction	ALK 00 00 2C 00 00 00 00 00 NAK NAK	

Fig. 12: DATA0 packet highlighted

If data packets (DATA0, DATA1) are being searched, searching can be limited to particular endpoint, device address or by hexadecimal string.

Linking the events window with the analyzer window

When a particular USB event has been choosen than real place of occurrence is highlighted. The place can be also zoom in by hitting the right mouse button and then choosing Zoom.

As well hitting the right mouse button in the analyzer window and then choosing Lookup in USB Communication highlights position in the events window.

Gathering of related communication into trees

In the basic USB plugin settings, related consecutive events are gathered into a tree (e.g. whole Control Transfer). This behavioral can leed to potential ambiguity in the order of USB events. In this cases Flat Decoding can be choosen in the Settings \rightarrow Settings... menu. It disables gathering of USB events so they are sorted top-down strictly by the particular time.

8. FREQUENCY MEASURING

A utility for measuring frequency on up to 4 inputs is provided as part of the ASIX SIGMA&OMEGA APPLICATION PACKAGE software package. Filtering and averaging can be selected for each measured input individually.

Please note, that the frequency measuring software and ASIX SIGMA&OMEGA LOGIC ANALYZERS software cannot be used simultaneously, an exclusive access to SIGMA2 is required.

9. TECHNICAL SPECIFICATION

9.1 Compresion specification

16 inputs, 50 MHz mode

Parametr	Hodnota	Jednotka
Memory size	256	Mbit
Maximum compressed data flow	915	Mbit/s
Worst conditions test lenght	0,29	S
Typical number of samples ¹⁾	2 milions	changes
Maximal test time ²⁾	45	min

- 1) Tested with I2C, SPI or UART serial protocols.
- 2) Test time with no signal changes on the inputs

9.2 Electrical specifications

	min.	typ.	max.	
V_{IL} input low voltage			0.8	V
V_{IH} input high voltage	2.0			V
V_{IN} absolute rating, inputs 116	-0.3		5.5	V
V_{IN} absolute rating, trigger I/O	-0.3		3.6	V
t _{sksp} single port 1)		1		ns
t _{skbp} between ports ²⁾		4.8		ns
$\Delta f/f_{typ}$ internal clock precision		50		ppm
T _A ambient temperature ³⁾	0		50	°C

- 1) $t_{\mbox{\tiny sksp}}$ is skew between pins belonging to the same port
- 2) t_{skbp} is skew between pins belonging to different ports
- 3) indoor use only

10. PACKAGE CONTENTS

- SIGMA2 logic analyzer
- Target cables: 20 individual pins (SIGMACAB) one-to-one 20 pins (SIGCAB20) one-to-one 10 pins (SIGCAB10)
- USB cable (A-B)
- CD-ROM (software, drivers)

11. CONTACT INFORMATION

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