

# HEF4047B

## Monostable/astable multivibrator

Rev. 5 — 16 December 2015

Product data sheet

## 1. General description

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The HEF4047B consists of a gatable astable multivibrator incorporating logic techniques to permit positive or negative edge-triggered monostable multivibrator action with retriggering and external counting options.

Inputs include +TRIGGER, -TRIGGER,  $\overline{\text{ASTABLE}}$ ,  $\overline{\text{ASTABLE}}$ , RETRIGGER and MR (master reset). Buffered outputs are O,  $\overline{\text{O}}$  and OSCILLATOR OUTPUT. In all modes of operation an external capacitor ( $C_T$ ) must be connected between CTC and RCTC, and an external resistor ( $R_T$ ) must be connected between RTC and RCTC.

A HIGH level on the  $\overline{\text{ASTABLE}}$  input enables astable operation. The period of the square wave at O and  $\overline{\text{O}}$  outputs is a function of the external components employed. 'True' input pulses on the  $\overline{\text{ASTABLE}}$  or 'complement' pulses on the  $\overline{\text{ASTABLE}}$  input, allow the circuit to be used as a gatable multivibrator. The OSCILLATOR OUTPUT period is half of the O output in the astable mode. However, a 50% duty factor is not guaranteed at this output.

In the monostable mode, positive edge-triggering is accomplished by applying a leading-edge pulse to the +TRIGGER input and a LOW level to the -TRIGGER input. For negative edge-triggering, a trailing-edge pulse is applied to the -TRIGGER and a HIGH level to the +TRIGGER. Input pulses may be of any duration relative to the output pulse. The multivibrator can be retriggered (on the leading-edge only) by applying a common pulse to both the RETRIGGER and +TRIGGER inputs. In this mode, the output pulse remains HIGH as long as the input pulse period is shorter than the period determined by the RC components.

An external count down option implements coupling O to an external 'N' counter and resetting the counter with the trigger pulse. The counter output pulse is fed back to the  $\overline{\text{ASTABLE}}$  input and has a duration equal to N times the period of the multivibrator. A HIGH level on the MR input assures no output pulse during an ON-power condition. This input can also be activated to terminate the output pulse at any time. In the monostable mode, a HIGH level or power-ON reset pulse must be applied to MR, whenever  $V_{DD}$  is applied.

## 2. Features and benefits

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### 2.1 General

- Monostable (one-shot) or astable (free-running) operation
- True and complemented buffered outputs
- Only one external resistor and capacitor required



2.2 Monostable multivibrator

- Positive- or negative-edge triggering
- Output pulse width independent of trigger pulse duration
- Retriggerable option for pulse-width expansion
- Long pulse width possible using small RC components with external counter provision
- Fast recovery time independent of pulse width
- Pulse-width accuracy maintained at duty cycles approaching 100%

2.3 Astable multivibrator

- Free-running or gatable operating modes
- 50% duty cycle
- Oscillator output available

3. Ordering information

Table 1. Ordering information

Type number	Package		Version
	Name	Description	
HEF4047BT	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1

4. Functional diagram

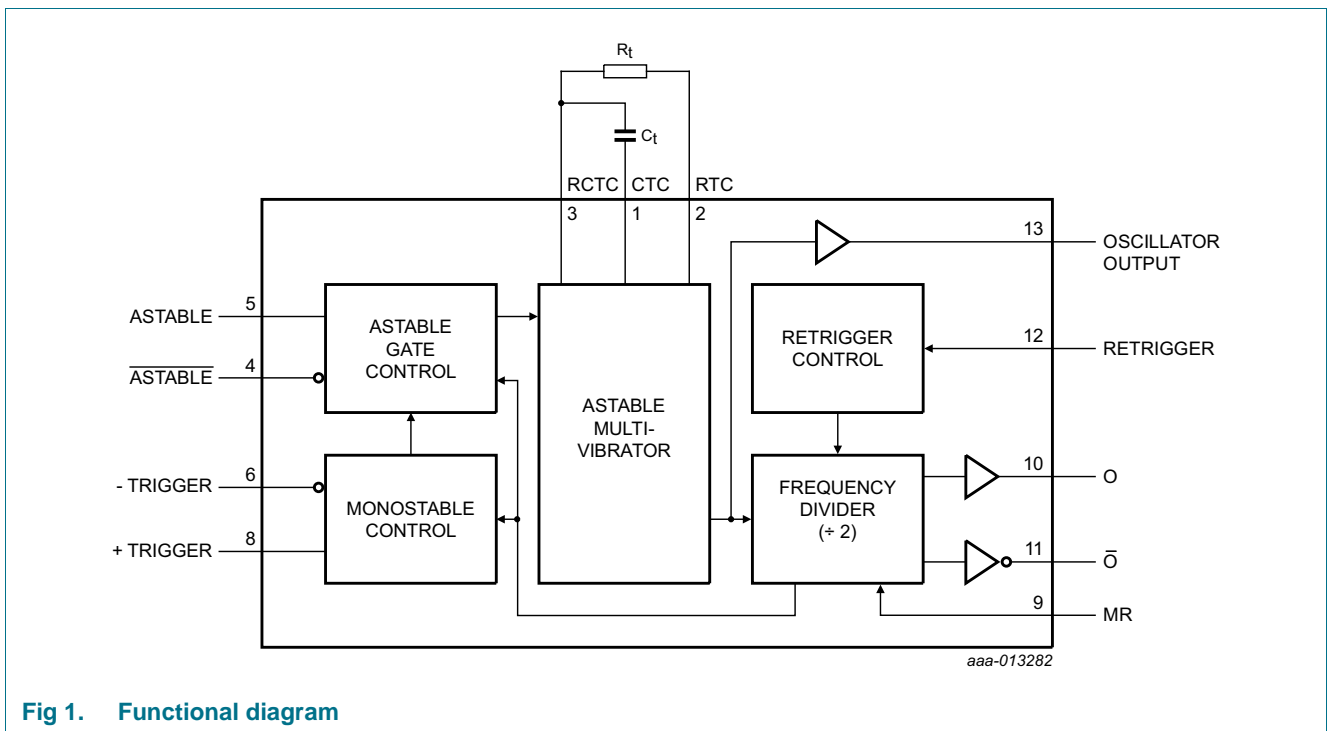
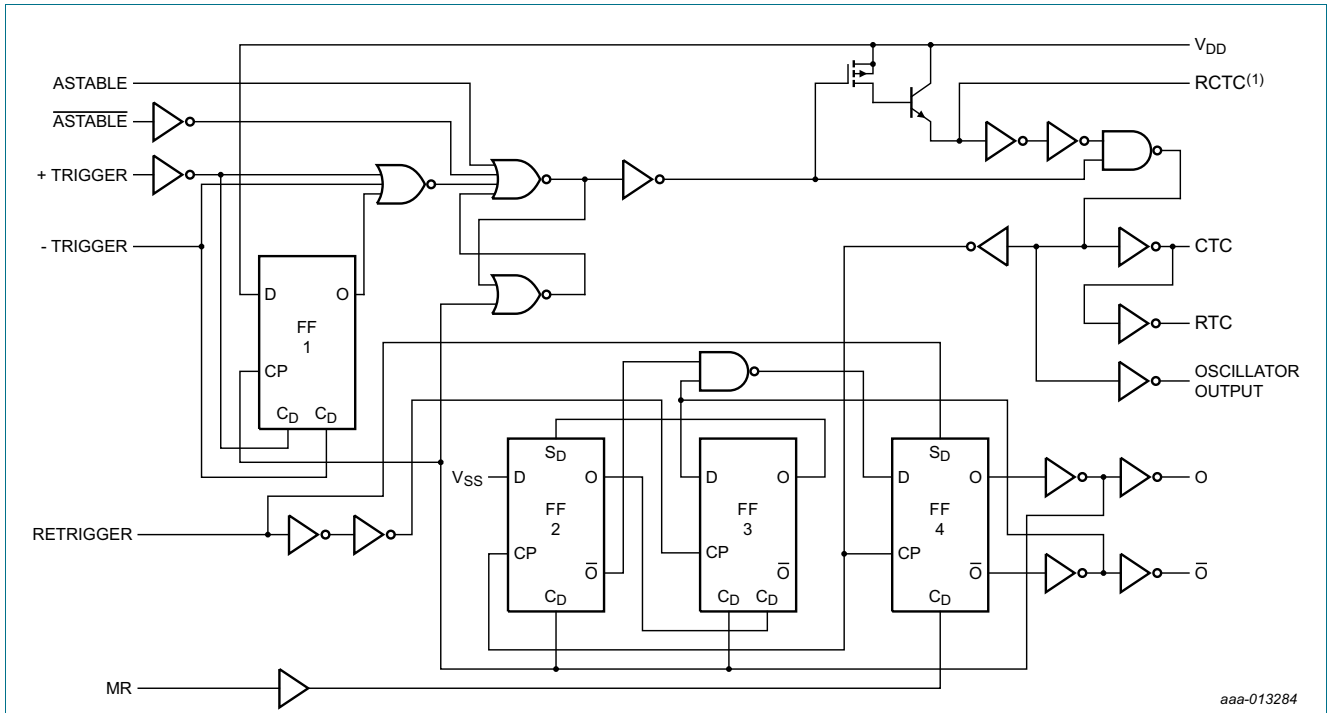


Fig 1. Functional diagram



(1) Special input protection that allows operating input voltages outside the supply voltage lines. Compared to the standard input protection pin 3 (RCTC) is more sensitive to static discharge; extra handling precautions are recommended.

Fig 2. Logic diagram

## 5. Pinning information

### 5.1 Pinning

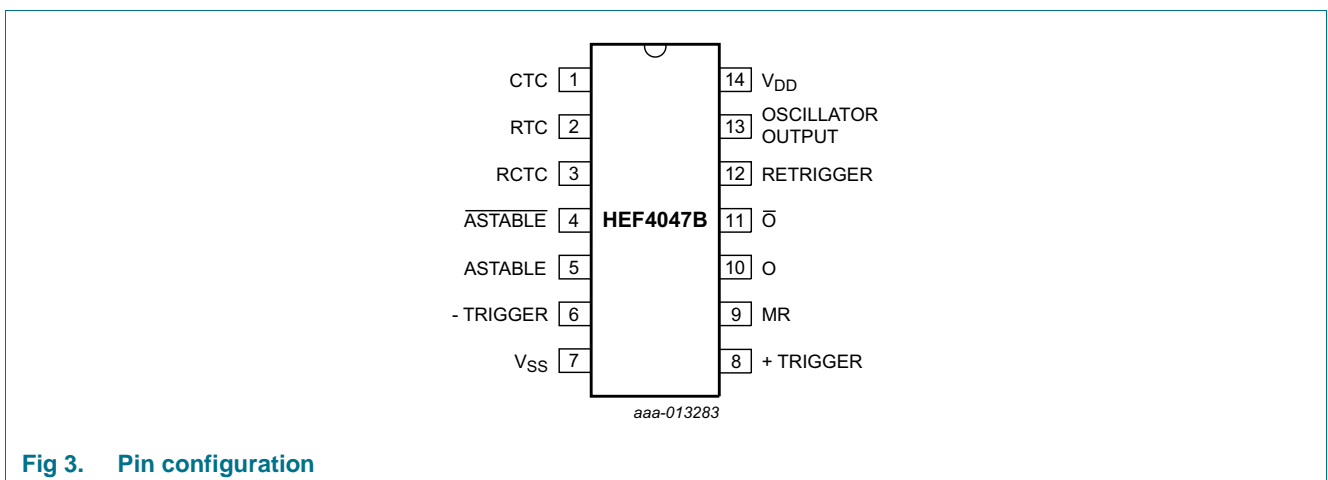


Fig 3. Pin configuration

## 5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
CTC	1	external capacitor connection
RTC	2	external resistor connection
RCTC	3	external capacitor/resistor connection
$\overline{\text{ASTABLE}}$	4	input
ASTABLE	5	input
-TRIGGER	6	input
V <sub>SS</sub>	7	ground supply voltage
+TRIGGER	8	input
MR	9	master reset input
O	10	output
$\overline{\text{O}}$	11	output
RETRIGGER	12	input
OSCILLATOR OUTPUT	13	oscillator output
V <sub>DD</sub>	14	supply voltage

## 6. Limiting values

Table 3. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>DD</sub>	supply voltage		-0.5	+18	V
I <sub>IK</sub>	input clamping current	V <sub>I</sub> < -0.5 V or V <sub>I</sub> > V <sub>DD</sub> + 0.5 V	-	±10	mA
V <sub>I</sub>	input voltage		-0.5	V <sub>DD</sub> + 0.5	V
I <sub>OK</sub>	output clamping current	V <sub>O</sub> < -0.5 V or V <sub>O</sub> > V <sub>DD</sub> + 0.5 V	-	±10	mA
I <sub>I/O</sub>	input/output current		-	±10	mA
I <sub>DD</sub>	supply current		-	50	mA
T <sub>stg</sub>	storage temperature		-65	+150	°C
T <sub>amb</sub>	ambient temperature		-40	+85	°C
P <sub>tot</sub>	total power dissipation	T <sub>amb</sub> = -40 °C to +85 °C			
		SO14 package <a href="#">[1]</a>	-	500	mW
P	power dissipation	per output	-	100	mW

[1] For SO14 package: P<sub>tot</sub> derates linearly with 8 mW/K above 70 °C.

## 7. Recommended operating conditions

Table 4. Operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DD}$	supply voltage		3	15	V
$V_I$	input voltage		0	$V_{DD}$	V
$T_{amb}$	ambient temperature	in free air	-40	+85	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{DD} = 5\text{ V}$	-	3.75	$\mu\text{s/V}$
		$V_{DD} = 10\text{ V}$	-	0.5	$\mu\text{s/V}$
		$V_{DD} = 15\text{ V}$	-	0.08	$\mu\text{s/V}$

## 8. Static characteristics

Table 5. Static characteristics

$V_{SS} = 0\text{ V}$ ;  $V_I = V_{SS}$  or  $V_{DD}$  unless otherwise specified.

Symbol	Parameter	Conditions	$V_{DD}$	$T_{amb} = -40\text{ °C}$		$T_{amb} = 25\text{ °C}$		$T_{amb} = 85\text{ °C}$		Unit
				Min	Max	Min	Max	Min	Max	
$V_{IH}$	HIGH-level input voltage	$ I_O  < 1\ \mu\text{A}$	5 V	3.5	-	3.5	-	3.5	-	V
			10 V	7.0	-	7.0	-	7.0	-	V
			15 V	11.0	-	11.0	-	11.0	-	V
$V_{IL}$	LOW-level input voltage	$ I_O  < 1\ \mu\text{A}$	5 V	-	1.5	-	1.5	-	1.5	V
			10 V	-	3.0	-	3.0	-	3.0	V
			15 V	-	4.0	-	4.0	-	4.0	V
$V_{OH}$	HIGH-level output voltage	$ I_O  < 1\ \mu\text{A}$	5 V	4.95	-	4.95	-	4.95	-	V
			10 V	9.95	-	9.95	-	9.95	-	V
			15 V	14.95	-	14.95	-	14.95	-	V
$V_{OL}$	LOW-level output voltage	$ I_O  < 1\ \mu\text{A}$	5 V	-	0.05	-	0.05	-	0.05	V
			10 V	-	0.05	-	0.05	-	0.05	V
			15 V	-	0.05	-	0.05	-	0.05	V
$I_{OH}$	HIGH-level output current	$V_O = 2.5\text{ V}$	5 V	-	-1.7	-	-1.4	-	-1.1	mA
		$V_O = 4.6\text{ V}$	5 V	-	-0.52	-	-0.44	-	-0.36	mA
		$V_O = 9.5\text{ V}$	10 V	-	-1.3	-	-1.1	-	-0.9	mA
		$V_O = 13.5\text{ V}$	15 V	-	-3.6	-	-3.0	-	-2.4	mA
$I_{OL}$	LOW-level output current	$V_O = 0.4\text{ V}$	5 V	0.52	-	0.44	-	0.36	-	mA
		$V_O = 0.5\text{ V}$	10 V	1.3	-	1.1	-	0.9	-	mA
		$V_O = 1.5\text{ V}$	15 V	3.6	-	3.0	-	2.4	-	mA
$I_I$	input leakage current		15 V	-	$\pm 0.3$	-	$\pm 0.3$	-	$\pm 1.0$	$\mu\text{A}$
		output transistor OFF; pin 3 at $V_{DD}$ or $V_{SS}$	15 V	-	$\pm 0.3$	-	$\pm 0.3$	-	$\pm 1.0$	$\mu\text{A}$
$I_{DD}$	supply current	$I_O = 0\text{ A}$	5 V	-	20	-	20	-	150	$\mu\text{A}$
			10 V	-	40	-	40	-	300	$\mu\text{A}$
			15 V	-	80	-	80	-	600	$\mu\text{A}$
$C_I$	input capacitance		-	-	-	7.5	-	-	pF	

## 9. Dynamic characteristics

**Table 6. Dynamic characteristics**

$V_{SS} = 0\text{ V}$ ;  $T_{amb} = 25\text{ °C}$ ; for test circuit and waveform, see [Figure 4](#) and [Figure 5](#); unless otherwise specified.

Symbol	Parameter	Conditions	V <sub>DD</sub>	Extrapolation formula	Min	Typ	Max	Unit
t <sub>PHL</sub>	HIGH to LOW propagation delay	ASTABLE, $\overline{\text{ASTABLE}}$ to OSCILLATOR OUTPUT	5 V <a href="#">[1]</a>	$68\text{ ns} + (0.55\text{ ns/pF})C_L$	-	95	190	ns
			10 V <a href="#">[1]</a>	$43\text{ ns} + (0.23\text{ ns/pF})C_L$	-	45	90	ns
			15 V <a href="#">[1]</a>	$22\text{ ns} + (0.16\text{ ns/pF})C_L$	-	30	60	ns
t <sub>PLH</sub>	LOW to HIGH propagation delay	$\overline{\text{ASTABLE}}$ , ASTABLE to OSCILLATOR OUTPUT	5 V <a href="#">[1]</a>	$58\text{ ns} + (0.55\text{ ns/pF})C_L$	-	85	170	ns
			10 V	$29\text{ ns} + (0.23\text{ ns/pF})C_L$	-	40	80	ns
			15 V	$22\text{ ns} + (0.16\text{ ns/pF})C_L$	-	30	60	ns
t <sub>PHL</sub>	HIGH to LOW propagation delay	ASTABLE, $\overline{\text{ASTABLE}}$ to O, $\overline{\text{O}}$	5 V <a href="#">[1]</a>	$123\text{ ns} + (0.55\text{ ns/pF})C_L$	-	150	300	ns
			10 V	$54\text{ ns} + (0.23\text{ ns/pF})C_L$	-	65	130	ns
			15 V	$42\text{ ns} + (0.16\text{ ns/pF})C_L$	-	50	100	ns
t <sub>PLH</sub>	LOW to HIGH propagation delay	$\overline{\text{ASTABLE}}$ , ASTABLE to O, $\overline{\text{O}}$	5 V <a href="#">[1]</a>	$103\text{ ns} + (0.55\text{ ns/pF})C_L$	-	130	260	ns
			10 V	$49\text{ ns} + (0.23\text{ ns/pF})C_L$	-	60	120	ns
			15 V	$37\text{ ns} + (0.16\text{ ns/pF})C_L$	-	45	90	ns
t <sub>PHL</sub>	HIGH to LOW propagation delay	+/-TRIGGER to O, $\overline{\text{O}}$	5 V <a href="#">[1]</a>	$133\text{ ns} + (0.55\text{ ns/pF})C_L$	-	160	320	ns
			10 V	$54\text{ ns} + (0.23\text{ ns/pF})C_L$	-	65	130	ns
			15 V	$42\text{ ns} + (0.16\text{ ns/pF})C_L$	-	50	100	ns
t <sub>PLH</sub>	LOW to HIGH propagation delay	+/-TRIGGER to O, $\overline{\text{O}}$	5 V <a href="#">[1]</a>	$128\text{ ns} + (0.55\text{ ns/pF})C_L$	-	155	310	ns
			10 V	$54\text{ ns} + (0.23\text{ ns/pF})C_L$	-	65	130	ns
			15 V	$42\text{ ns} + (0.16\text{ ns/pF})C_L$	-	50	100	ns
t <sub>PHL</sub>	HIGH to LOW propagation delay	+TRIGGER, RETRIGGER to $\overline{\text{O}}$	5 V <a href="#">[1]</a>	$38\text{ ns} + (0.55\text{ ns/pF})C_L$	-	65	130	ns
			10 V	$19\text{ ns} + (0.23\text{ ns/pF})C_L$	-	30	60	ns
			15 V	$17\text{ ns} + (0.16\text{ ns/pF})C_L$	-	25	50	ns
t <sub>PLH</sub>	LOW to HIGH propagation delay	+TRIGGER, RETRIGGER to O	5 V <a href="#">[1]</a>	$68\text{ ns} + (0.55\text{ ns/pF})C_L$	-	95	190	ns
			10 V	$29\text{ ns} + (0.23\text{ ns/pF})C_L$	-	40	80	ns
			15 V	$22\text{ ns} + (0.16\text{ ns/pF})C_L$	-	30	60	ns
t <sub>PHL</sub>	HIGH to LOW propagation delay	MR to O	5 V <a href="#">[1]</a>	$83\text{ ns} + (0.55\text{ ns/pF})C_L$	-	100	200	ns
			10 V	$34\text{ ns} + (0.23\text{ ns/pF})C_L$	-	45	90	ns
			15 V	$27\text{ ns} + (0.16\text{ ns/pF})C_L$	-	35	70	ns
t <sub>PLH</sub>	LOW to HIGH propagation delay	MR to $\overline{\text{O}}$	5 V <a href="#">[1]</a>	$83\text{ ns} + (0.55\text{ ns/pF})C_L$	-	100	200	ns
			10 V	$34\text{ ns} + (0.23\text{ ns/pF})C_L$	-	45	90	ns
			15 V	$27\text{ ns} + (0.16\text{ ns/pF})C_L$	-	35	70	ns
t <sub>THL</sub>	HIGH to LOW output transition time		5 V <a href="#">[1]</a>	$10\text{ ns} + (1.0\text{ ns/pF})C_L$	-	60	120	ns
			10 V	$9\text{ ns} + (0.42\text{ ns/pF})C_L$	-	30	60	ns
			15 V	$6\text{ ns} + (0.28\text{ ns/pF})C_L$	-	20	40	ns
t <sub>TLH</sub>	LOW to HIGH output transition time		5 V <a href="#">[1]</a>	$10\text{ ns} + (1.0\text{ ns/pF})C_L$	-	60	120	ns
			10 V	$9\text{ ns} + (0.42\text{ ns/pF})C_L$	-	30	60	ns
			15 V	$6\text{ ns} + (0.28\text{ ns/pF})C_L$	-	20	40	ns

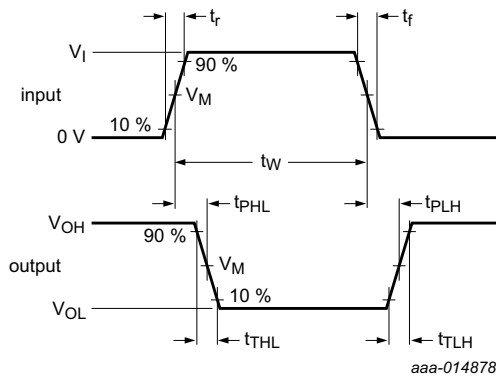
**Table 6. Dynamic characteristics ...continued**

$V_{SS} = 0\text{ V}$ ;  $T_{amb} = 25\text{ }^\circ\text{C}$ ; for test circuit and waveform, see [Figure 4](#) and [Figure 5](#); unless otherwise specified.

Symbol	Parameter	Conditions	V <sub>DD</sub>	Extrapolation formula	Min	Typ	Max	Unit
t <sub>w</sub>	pulse width	any input except MR	5 V	-	220	110	-	ns
			10 V	-	100	50	-	ns
			15 V	-	70	35	-	ns
		MR HIGH	5 V	-	60	30	-	ns
			10 V	-	30	15	-	ns
			15 V	-	20	10	-	ns

[1] The typical values of the propagation delay and transition times are calculated from the extrapolation formulas shown (C<sub>L</sub> in pF).

## 10. Waveforms



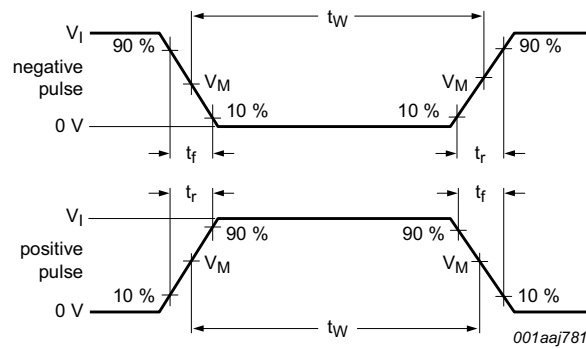
Measurement points are given in [Table 7](#).

Logic levels: V<sub>OL</sub> and V<sub>OH</sub> are typical output voltage levels that occur with the output load.

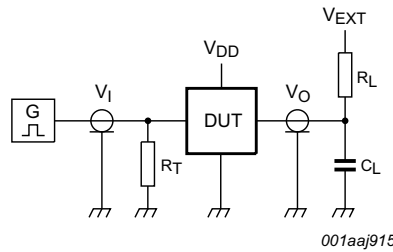
**Fig 4. input to output propagation delays, output transition time and pulse width**

**Table 7. Measurement points**

Supply voltage	Input	Output
V <sub>DD</sub>	V <sub>M</sub>	V <sub>M</sub>
5 V to 15 V	0.5V <sub>DD</sub>	0.5V <sub>DD</sub>



a. Input waveform



b. Test circuit

Test and measurement data is given in [Table 8](#).

Definitions test circuit:

DUT = Device Under Test.

$R_T$  = Termination resistance should be equal to output impedance  $Z_o$  of the pulse generator.

$C_L$  = Load capacitance including jig and probe capacitance.

Fig 5. Test circuit for measuring switching times

Table 8. Test data

Supply voltage	Input		Load		$V_{EXT}$
	$V_I$	$t_r, t_f$	$C_L$	$R_L$	$t_{PLH}, t_{PHL}$
5 V to 15 V	$V_{DD}$	$\leq 20$ ns	50 pF	1 k $\Omega$	open

## 11. Application information

Table 9. Functional connections [\[1\]](#)

Function	Pins connected to			Output pulse from pins	Output period or pulse width
	$V_{DD}$	$V_{SS}$	input pulse		
<b>Astable multivibrator</b>					
Free running	4, 5, 6, 14	7, 8, 9, 12	-	10, 11, 13	at pins 10, 11;
True gating	4, 6, 14	7, 8, 9, 12	5	10, 11, 13	$t_A = 4.40 R_t C_t$
Complement gating	6, 14	5, 7, 8, 9, 12	4	10, 11, 13	at pin 13: $t_A = 2.20 R_t C_t$



Table 9. Functional connections ...continued<sup>[1]</sup>

Function	Pins connected to			Output pulse from pins	Output period or pulse width
	V <sub>DD</sub>	V <sub>SS</sub>	input pulse		
<b>Monostable multivibrator</b>					
Positive edge-triggering	4, 14	5, 6, 7, 9, 12	8	10, 11	at pins 10, 11; t <sub>M</sub> = 2.48 R <sub>t</sub> C <sub>t</sub>
Negative edge-triggering	4, 8, 14	5, 7, 9, 12	6	10, 11	
Retriggerable	4, 14	5, 6, 7, 9	8, 12	10, 11	
External countdown <sup>[2]</sup>	14	5, 6, 7, 8, 9, 12	-	10, 11	

[1] In all cases, external resistor between pins 2 and 3, external capacitor between pins 1 and 3.

[2] Input pulse to RESET of external counting chip: external counting chip output to pin 4.

### 11.1 Astable mode design information

#### 11.1.1 Unit-to-unit transfer voltage variations

The following analysis presents worst case variations from unit-to-unit as a function of transfer voltage (V<sub>TR</sub>) shift for free running (astable) operation.

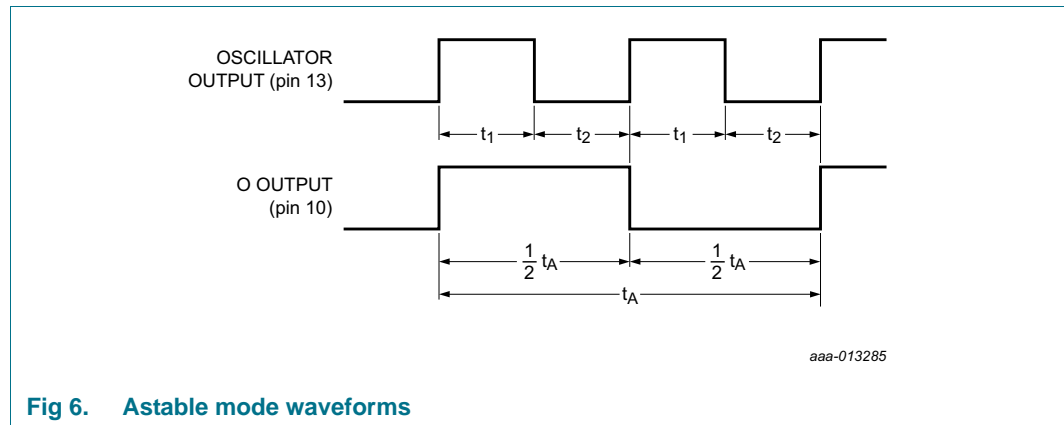


Fig 6. Astable mode waveforms

$$t_1 = -R_t C_t \ln \frac{V_{TR}}{V_{DD} + V_{TR}} \tag{1}$$

$$t_2 = -R_t C_t \ln \frac{V_{DD} - V_{TR}}{2V_{DD} - V_{TR}} \tag{2}$$

$$t_A = 2(t_1 + t_2) = -2R_t C_t \ln \frac{(V_{TR})(V_{DD} - V_{TR})}{(V_{DD} + V_{TR})(2V_{DD} - V_{TR})} \tag{3}$$

, where t<sub>A</sub> = astable mode pulse width; see [Table 10](#).

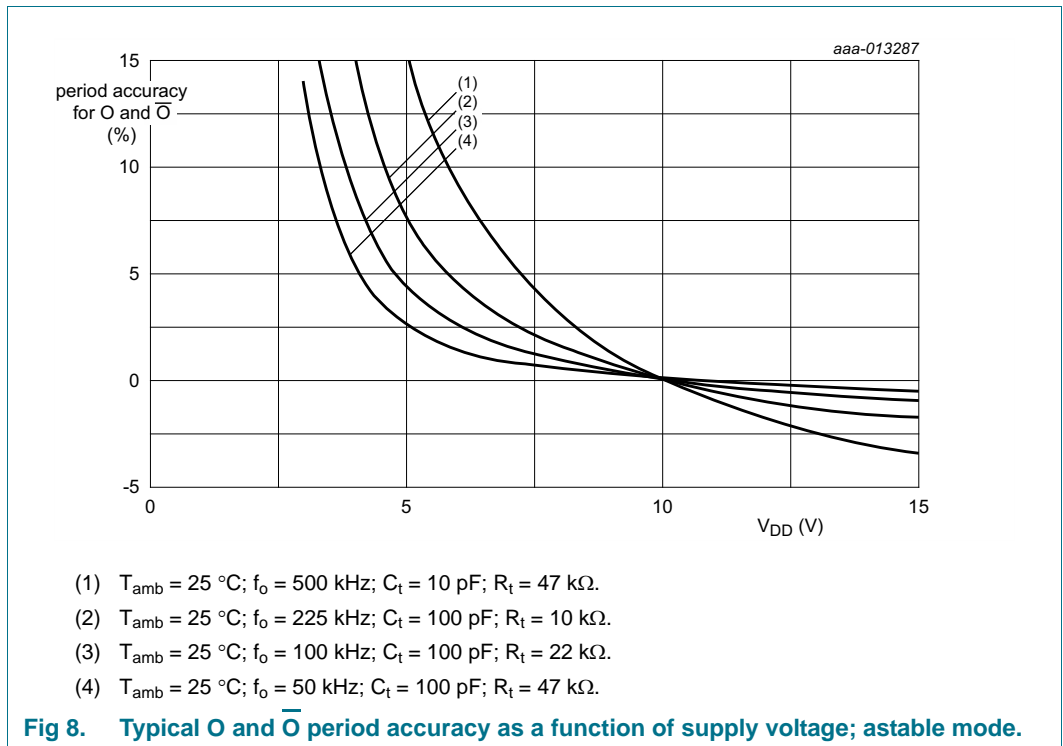
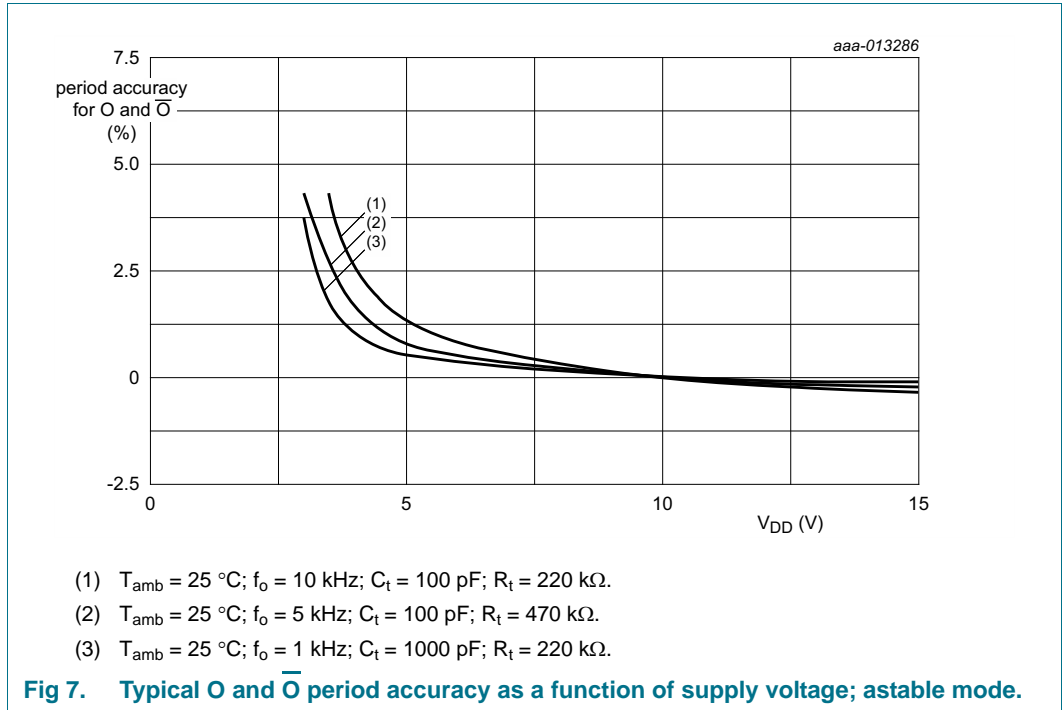
Table 10. Values for astable mode pulse width (t<sub>A</sub>)

	V <sub>TR</sub>			t <sub>A</sub>		
	Min	Typ	Max	Min	Typ <sup>[1]</sup>	Max
V <sub>DD</sub> = 5 V or 10 V	0.3 × V <sub>DD</sub>	0.5 × V <sub>DD</sub>	0.7 × V <sub>DD</sub>	4.71 R <sub>t</sub> C <sub>t</sub>	4.40 R <sub>t</sub> C <sub>t</sub>	4.71 R <sub>t</sub> C <sub>t</sub>
V <sub>DD</sub> = 15 V	4 V	0.5 × V <sub>DD</sub>	11 V	4.84 R <sub>t</sub> C <sub>t</sub>	4.40 R <sub>t</sub> C <sub>t</sub>	4.84 R <sub>t</sub> C <sub>t</sub>

[1] Therefore if t<sub>A</sub> = 4.40 R<sub>t</sub>C<sub>t</sub> is used, the maximum variation is (+7.0%; -0.0%) at 10 V.

11.1.2 Variations due to changes in  $V_{DD}$

In addition to variations from unit-to-unit, the astable period may vary as a function of frequency with respect to  $V_{DD}$ . Typical variations are presented graphically in [Figure 7](#) and [Figure 8](#) with 10 V as a reference.



11.2 Monostable mode design information

The following analysis presents worst case variations from unit-to-unit as a function of transfer voltage ( $V_{TR}$ ) shift for one-shot (monostable) operation.

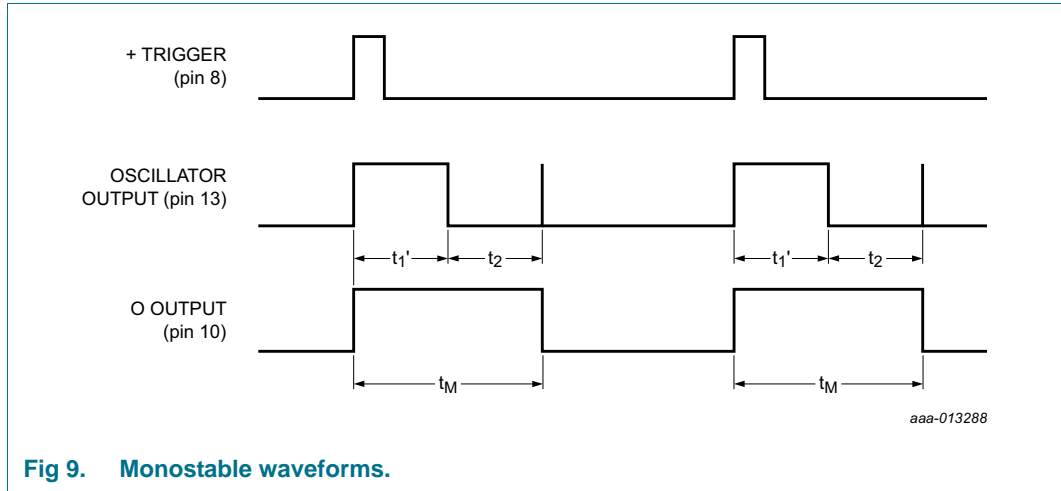


Fig 9. Monostable waveforms.

$$t_1' = -R_t C_t \ln \frac{V_{TR}}{2V_{DD}} \tag{4}$$

$$t_M = (t_1' + t_2) \tag{5}$$

$$t_M = -R_t C_t \ln \frac{(V_{TR})(V_{DD} - V_{TR})}{(2V_{DD} - V_{TR})(2V_{DD})} \tag{6}$$

, where  $t_M$  = monostable mode pulse width; see table [Table 11](#).

Table 11. Values for monostable mode pulse width ( $t_M$ )

	$V_{TR}$			$t_M$		
	Min	Typ	Max	Min	Typ <sup>[1]</sup>	Max
$V_{DD} = 5\text{ V or }10\text{ V}$	$0.3 \times V_{DD}$	$0.5 \times V_{DD}$	$0.7 \times V_{DD}$	$2.78 R_t C_t$	$2.48 R_t C_t$	$2.52 R_t C_t$
$V_{DD} = 15\text{ V}$	4 V	$0.5 \times V_{DD}$	11 V	$2.88 R_t C_t$	$2.48 R_t C_t$	$2.56 R_t C_t$

[1] In the astable mode, the first positive half cycle has a duration of  $t_M$ ; succeeding durations are  $\frac{1}{2} t_A$ . Therefore if  $t_M = 2.48 R_t C_t$  is used, the maximum variation is (+12%; -0.0%) at 10 V.

11.2.1 Retrigger mode operation

The HEF4047B can be used in the retrigger mode to extend the output pulse duration. It can also be used to compare the frequency of an input signal with the frequency of the internal oscillator. In the retrigger mode, the input pulse is applied to pins 8 and 12, and the output is taken from pin 10 or 11. Normal monostable action is obtained when one retrigger pulse is applied (see Figure 10). Extended pulse duration is obtained when more than one pulse is applied. For two input pulses,  $t_{RE} = t_1' + t_1 + 2t_2$ . For more than two pulses,  $t_{RE}$  (output O), terminates at some variable time,  $t_D$ , after the termination of the last retrigger pulse.  $t_D$  is variable because  $t_{RE}$  (output O) terminates after the second positive edge of the oscillator output appears at flip-flop 4.

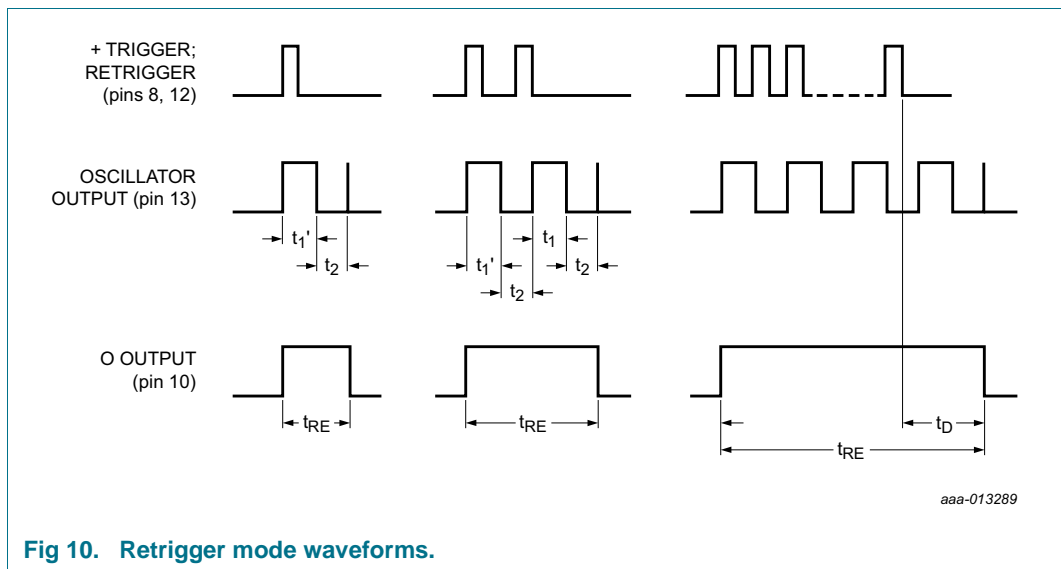


Fig 10. Retrigger mode waveforms.

11.2.2 External counter option

The use of external counting circuitry extends time  $t_M$  by any amount. Advantages include digitally controlled pulse duration, small timing capacitors for long time periods, and extremely fast recovery time. A typical implementation is shown in Figure 11.

The pulse duration at the output is:

$$t_{ext} = (N - 1)(t_A) + (t_M + 1/2 t_A) \tag{7}$$

Where  $t_{ext}$  = pulse duration of the circuitry, and N is the number of counts used.

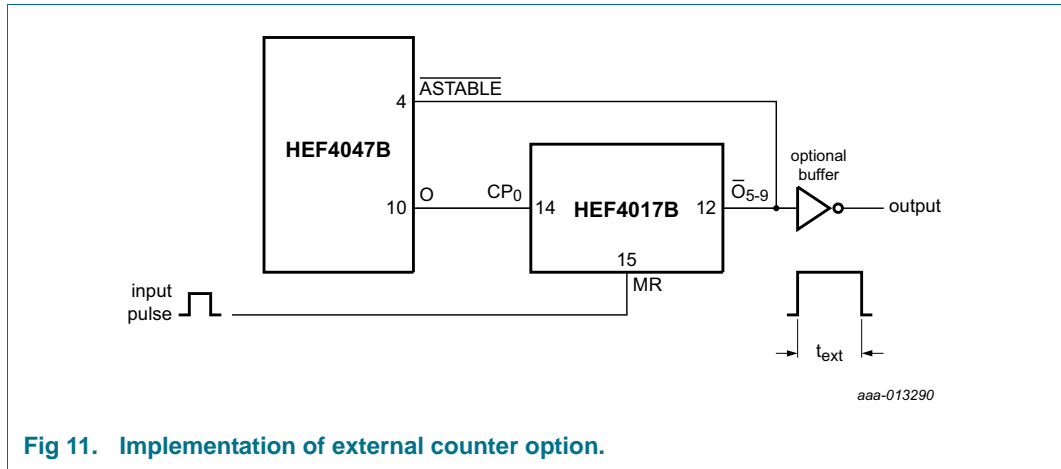


Fig 11. Implementation of external counter option.

### 11.2.3 Timing component limitations

The capacitor used in the circuit should be non-polarized and have low leakage (that is the parallel resistance of the capacitor should be an order of magnitude greater than the external resistor used). There is no upper or lower limit for either  $R_t$  or  $C_t$  value to maintain oscillation. However, for accuracy,  $C_t$  must be much larger than the inherent stray capacitance in the system (unless this capacitance can be measured and taken into account).  $R_t$  must be much larger than the LOCMOS 'ON' resistance in series with it, which typically is hundreds of ohms.

The recommended values for  $R_t$  and  $C_t$  to comply with previously calculated formulae without trimming should be:

- $C_t \geq 100 \text{ pF}$ , up to any practical value
- $10 \text{ k}\Omega \leq R_t \leq 1 \text{ M}\Omega$

### 11.2.4 Power consumption

In the standby mode (monostable or astable), power dissipation is a function of leakage current in the circuit. For dynamic operation, the power required to charge the external timing capacitor  $C_t$  is shown in the following formulae:

Astable mode:

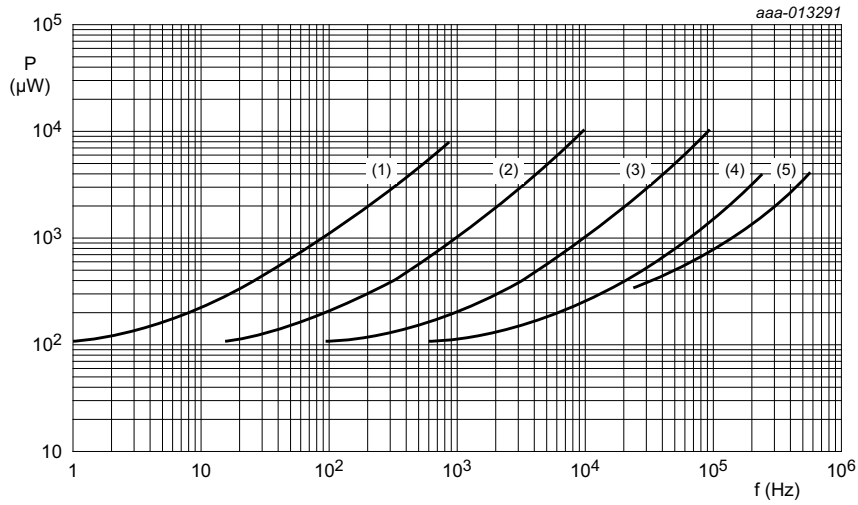
$$P = 2 C_t V^2 f \quad (f \text{ at output pin 13}) \tag{8}$$

$$P = 4 C_t V^2 f \quad (f \text{ at output pins 10 and 11}) \tag{9}$$

Monostable mode:

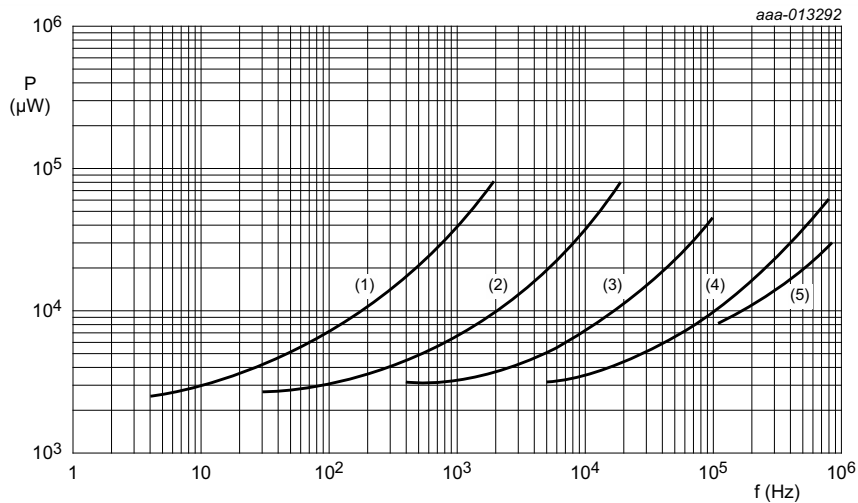
$$P = \frac{(2.9 C_t V^2)(\text{duty cycle})}{T} \quad (f \text{ at output pins 10 and 11}) \tag{10}$$

Because the power dissipation does not depend on  $R_t$ , a design for minimum power dissipation would be a small value of  $C_t$ . The value of  $R$  would depend on the desired period (within the limitations discussed previously). Typical power consumption in astable mode is shown in [Figure 12](#), [Figure 13](#) and [Figure 14](#).



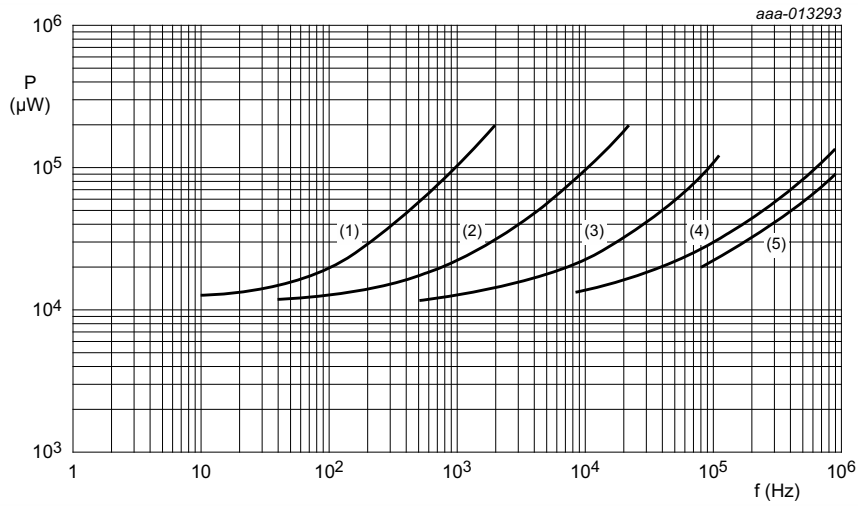
- $V_{DD} = 5\text{ V.}$
- (1)  $C_t = 100\text{ nF.}$
  - (2)  $C_t = 10\text{ nF.}$
  - (3)  $C_t = 1\text{ nF.}$
  - (4)  $C_t = 100\text{ pF.}$
  - (5)  $C_t = 10\text{ pF.}$

Fig 12. Power consumption as a function of the output frequency at O or  $\bar{O}$ ; astable mode.



- $V_{DD} = 10\text{ V.}$
- (1)  $C_t = 100\text{ nF.}$
  - (2)  $C_t = 10\text{ nF.}$
  - (3)  $C_t = 1\text{ nF.}$
  - (4)  $C_t = 100\text{ pF.}$
  - (5)  $C_t = 10\text{ pF.}$

Fig 13. Power consumption as a function of the output frequency at O or  $\bar{O}$ ; astable mode.



- $V_{DD} = 15\text{ V.}$
- (1)  $C_t = 100\text{ nF.}$
  - (2)  $C_t = 10\text{ nF.}$
  - (3)  $C_t = 1\text{ nF.}$
  - (4)  $C_t = 100\text{ pF.}$
  - (5)  $C_t = 10\text{ pF.}$

**Fig 14. Power consumption as a function of the output frequency at O or  $\bar{O}$ ; astable mode.**

12. Package outline

SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1



Fig 15. Package outline SOT108-1 (SO14)



## 13. Abbreviations

Table 12. Abbreviations

Acronym	Description
DUT	Device Under Test

## 14. Revision history

Table 13. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
HEF4047B v.5	20151216	Product data sheet	-	HEF4047B v.4
Modifications:	<ul style="list-style-type: none"> <li>Type number HEF4047BP (SOT27-1) removed.</li> </ul>			
HEF4047B v.4	20140915	Product data sheet	-	HEF4047B_CVN_3
Modifications:	<ul style="list-style-type: none"> <li>The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.</li> <li>Legal texts have been adapted to the new company name where appropriate.</li> </ul>			
HEF4047B_CVN_3	19950101	Product specification	-	-

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Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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