A71CH

Plug & Trust Secure Element

Rev. 1.0 — 21 February 2018
449310

Objective short data sheet
COMPANY PUBLIC

1. Introduction

The A71CH is a ready-to-use solution providing a root of trust at the IC level and proven, chip-to-cloud security right out of the box. It is a platform capable of securely storing and provisioning credentials, securely connecting IoT devices to cloud services and performing cryptographic node authentication.

The A71CH solution provides basic security measures protecting the IC against many physical and logical attacks. It can be used with various host platforms and host operating systems to secure a broad range of applications. It is complemented by a comprehensive product support package, offering easy design-in with plug & play host application code, easy to use development kits, reference designs, and extensive documentation for product evaluation.

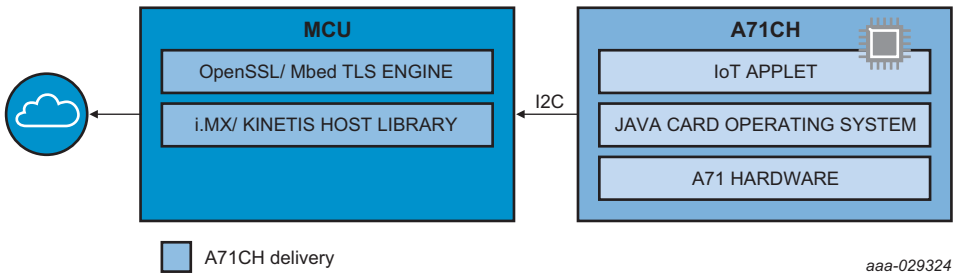


Fig 1. A71CH block diagram

2. General description

2.1 A71CH naming conventions

The following table explains the naming conventions of the commercial product name of the A71CH products. Every A71CH product gets assigned such a commercial name, which includes also customer and application specific data.

The A71CH commercial names have the following format.

A71CHxagpp(p)/mvsrrff

The 'A71CH' is a constant, all other letters are variables, which are explained in Table 1.

Table 1. A71CH commercial name format

Variable	Meaning	Values	Description
x	IC hardware specification code	1	standard operational ambient temperature: –25 °C to +90 °C I^2C interface supported
		2	standard operational ambient temperature: –40 °C to +90 °C I^2C interface supported
a	embedded operating system code	C	Java card operating system
g	embedded application firmware (applet) code	H	H is a fixed value = IoT security applet pre installed
pp(p)	package type code dd(d)= Delivery Type, TK2= HVSON8 (4x4), UK= WLCSP12		
m	Manufacturing Site Code	T	
v	Silicon Version Code	0	
s	Silicon Version Subcode	B	
rr	ROM Code ID		
ff	FabKey ID		

2.2 I^2C interface

The A71CH has an I^2C interface in slave mode, supporting data rates up to 400 kbit/s operating in Fast-Mode (FM). The I^2C interface is using the Smartcard I^2C protocol as defined in Ref. 3 which is based on SMBus.

More information about I^2C address used during A71CH implementation can be found in Ref. 4; the default I^2C address after power-on-reset is 0x90 for Write, and 0x91 for Read.

2.3 Security licensing

NXP Semiconductors has obtained a patent license for SPA and DPA countermeasures from Cryptography Research Incorporated (CRI). This license covers both hardware and software countermeasures. It is important to customers that countermeasures within the operation system are covered under this license agreement with CRI. Further details can be obtained on request.

3. Features and benefits

3.1 Key benefits

- Secure, zero-touch connectivity
- End-to-end security, from chip to edge to cloud
- Secure credential injection for IC-level root of trust
- Fast design-in with complete product support package
- Easy to integrate with different MCU platforms

3.2 Security features

The A71CH security concepts includes many security measures to protect the chip.

The A71CH operates fully autonomously based on an integrated Javacard operating system and applet. Direct memory access is possible by the fixed functionalities of the applet only. With that, the content from the memory is fully isolated from the host system.

Attack protection by integrated design measures in the chip layout, the logic and the functional blocks.

3.3 Cryptography features

The A71CH Secure Element provides the following functionality:

- Protected Access storage, generation, insertion or deletion of 4 key pairs (ECC NIST P-256)
- Systematic enforced authentication
- Secure key management
- Protected Access storage, insertion or deletion of 3 public keys
- Signature generation and verification (ECDSA)
- Shared secret calculation for Key Agreement (ECDH or ECDH-E)
- Protected Access storage and use of 2 monotonic counters (32 bits each)
- Protected Access storage, insertion or deletion of symmetric secrets (8x 128 bits); longer keys can be used by using a ConstructedSecret type
- Content protected access to keys
- A unique chip ID (18 bytes)
- HKDF key derivation using the symmetric secrets as key, Extract & Expand or Expand only modes
- HMAC SHA256 calculation in one shot or sequential
- Freezing of credentials (= OTP behavior)
- Secure channel SCPO3 GP support
- (Optional) trust provisioning of key pairs, public keys, symmetric secrets, etc.
- Possibility to lock the A71CH module as transport lock mechanism

ECC keys and operations support the following ECC curve:

- NIST P-256

3.4 Functional features

- Dedicated MX51 security CPU
- 400 kbit/s I^2C Fast-mode interface
- –40 °C to +90 °C operational ambient temperature (A7102)
- On-chip Javacard operating system
- 40 µA typical sleep mode current with I^2C pads in tristate mode
- 10 µA max deep sleep mode current with I^2C pads in tristate mode
- High-performance Public Key Infrastructure (PKI)
- EEPROM with min 500,000 cycles endurance and min 25 years retention time
- HVSON8 package

4. Applications

4.1 Use Cases and target applications

- A710xCH EXAMPLE USE CASES
  - Secure connection to public/private clouds, edge computing platforms, infrastructure
  - Secure Amazon Web Services-compliant connectivity
  - Secure commissioning
  - Device-to-device authentication
  - Proof of origin / anti-counterfeiting
  - Key storage and data protection
  - Secure provisioning of credentials
  - Ecosystem protection
- A710xCH TARGET APPLICATIONS
  - Connected industrial devices
  - Sensor networks
  - IP cameras
  - Home gateways
  - Home appliances

5. Ordering information

5.1 Ordering options

Table 2. Ordering information

Type number[1]	Package		
	Name	Description	Version
A7101agTK2/...	HVSON-8	plastic thermal enhanced very thin small outline package; no leads; 8 terminals; body 4 × 4 × 0.85 mm	SOT909-1
A7102agTK2/...			

[1] a = A or C, g = G, C or A, according to the A71CH type classification see Section 2.1 “A71CH naming conventions”

Table 3. A71CH type table

12NC	Type number	Product	Package
9353 68 097118	A7101CHTK2/T0BC2V6	A71(01)CH	HVSON8
9353 635 15118	A7102CHTK2/T0BC2A5	A71(02)CH	HVSON8

Table 4. A71CH type table

12NC	Type number	Development kit	Description
935368997598	OM3710/A71CHARD	OM3710/A71CHARD	Arduino compatible development kit
935369302598	OM3710/A71CHPCB	OM3710/A71CHPCB	Mini PCP
		OM3710/B001	I^2C Bird

Table 5 gives an overview of available A71CH product types.

Table 5. A71CH feature table

Product type[1]	Operational ambient temperature	Interface option
A7101Cgpp(p)	–25 °C to +90 °C	I^2C
A7102Cgpp(p)	–40 °C to +90 °C	

[1] g = G, C, or A; pp(p) = UA or HN1, according the A71CH type classification see Section 2.1 “A71CH naming conventions”

5.1.1 Samples and final products

Section 5.1.2, gives details of how to order samples and final products.

5.1.2 Ordering A71CH samples

Samples can be ordered from NXP Semiconductors via nxp.com using the "Buy Direct" button.

Note that NXP Semiconductors can provide up to 5 pieces free of charge. Larger quantities have to be ordered separately.

6. Functional description

6.1 Functional diagram

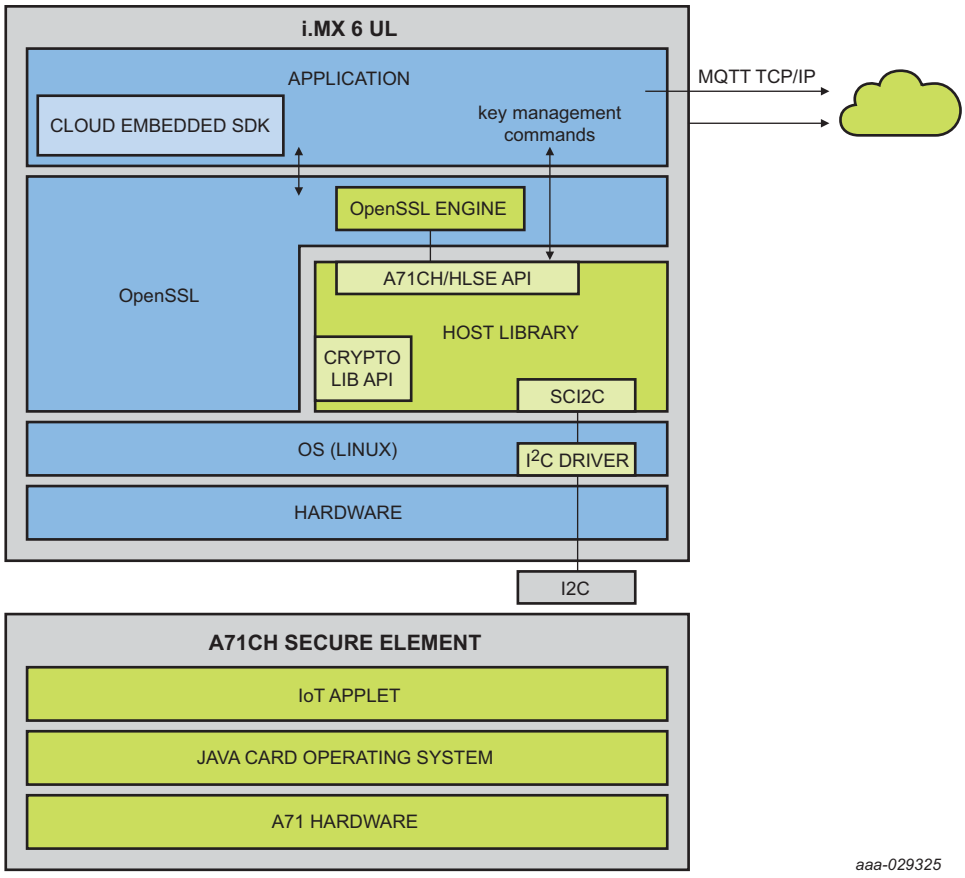


Fig 2. A71CH functional diagram - example Open SSL

The A71CH uses I²C as communication interface as described in the following section. The A71CH commands are wrapped using the Smartcard I² protocol (SCI2C). The detailed documentation for the A71CH commands [ref to APDU Spec] and SCI2C encapsulation (Ref. 3) is available in NXP docstore."

In order to simplify the product usage a host library was created which takes care for the A71CH commands and SCI2C protocol encapsulation. The host library for various platforms is available for download with complete sources on the A71CH website.

6.2 I²C Interface

The A71CH has an I²C interface in slave mode, supporting data rates up to 400 kbit/s operating in Fast-Mode (FM). The I²C interface is using the Smartcard I²C protocol as defined in Ref. 3 which is based on SMBus. More information about I²C address used during A71CH implementation can be found in Ref. 4. The default I²C address after power-on-reset depends on the bootup condition as shown in Table 6.

6.3 Automatic Communication Mode detection at Power on

The IC configures its interface according to the pin state as shown in the table below. The host system must keep the voltage levels stable at these pins for at least 500 µs after power-on-reset.

Table 6. I²C address

Value at startup				I²C address	
IF0	IF1	I2C_SCL	I2C_SDA	Write	Read
0	x	0	0	n.a.	n.a.
1	0	1	1	0x90	0x91
1	1	1	1	0x92	0x93

6.4 Power-saving modes

The device provides two power-saving operation modes, the SLEEP mode and the DEEP SLEEP mode. These modes are activated via pad RST_N (DEEP SLEEP mode) or by the device.

6.4.1 SLEEP mode

The SLEEP mode has the following properties:

- all internal clocks are frozen,
- CPU enters power saving mode with program execution being stopped,
- CPU registers keep their contents,
- RAM keeps its contents,

The A71CH enters automatically into SLEEP mode and also wakes up automatically from SLEEP mode. In SLEEP mode, all internal clocks are stopped. The IOs hold the logical states they had at the time IDLE was activated. During SLEEP mode security sensors HVS, LVS, LTS, HTS, Light Sensors, Glitch Sensors and Active Shielding are disabled.

There are two ways to exit from the SLEEP mode:

- A reset signal on RST_N
- An External Interrupt edge triggered by a falling edge on I2C_SDA

6.4.2 DEEP SLEEP mode

The A71CHx provides a special sleep mode offering maximum power saving. It is reached by pulling RST_N to a logic zero level for more than 500 µs.

While in deep sleep mode the internal power is completely switched off and only the IO pads stay supplied. All digital pads will stay in high-Z mode.

To leave the DEEP SLEEP mode RST_N has to be released and set to a logic „1“ level.

7. Pinning information

7.1 Pinning

7.1.1 Pinning HVSON8

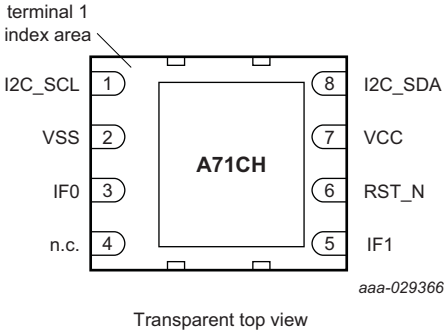


Fig 3. Pin configuration for HVSON-8 (SOT909-1)

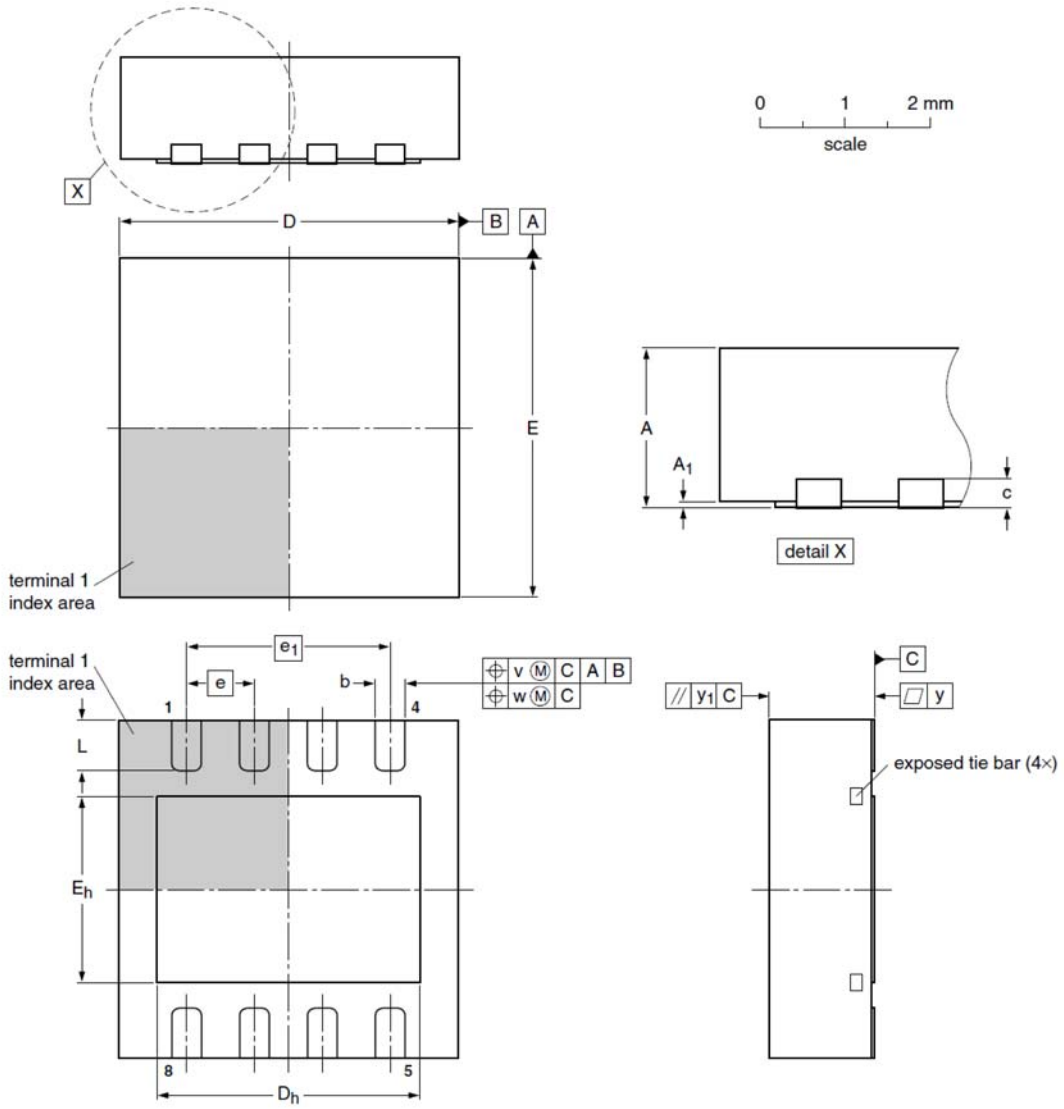
Table 7. Pin description HVSON8

Symbol	Pin	Description
I2C_SCL	1	I^2C clock
VSS	2	ground
IF0	3	interface activation, apply high on startup
n.c.	4	not connected
IF1	5	I^2C address selection
RST_N	6	reset input, active LOW
VCC	7	power supply voltage input
I2C_SDA	8	I^2C data

8. Package outline

HVSON8: plastic thermal enhanced very thin small outline package; no leads;
8 terminals; body 4 x 4 x 0.85 mm

SOT909-1



DIMENSIONS (mm are the original dimensions)

UNIT	A(1) max.	A1	b	c	D(1)	Dh	E(1)	Eh	e	e1	L	v	w	y	y1
mm	1	0.05 0.00	0.4 0.3	0.2	4.1 3.9	3.25 2.95	4.1 3.9	2.35 2.05	0.8	2.4	0.65 0.40	0.1	0.05	0.05	0.1

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT909-1		MO-229				~~05-09-26~~ 05-09-28

Fig 4. Package outline SOT909-1

9. Packing information

9.1 Reel packing

The A71CH product is available on 7” tape on reel and 13” tape on reel. Details are provided in Table 8.

Table 8. Reel packing options

Package type	Reel type	Minimum packing quantity
HVSON8	7” tape on reel	1500
HVSON8	13” tape on reel[1]	6000

[1] For details about packing method, product orientation, tape dimensions and labeling for A71 parts in HVSON8 package having an ordering code (12NC) ending 118 refer to Ref. 2.

10. Electrical and timing characteristics

The electrical interface characteristics of static (DC) and dynamic (AC) parameters for pads and functions used for I^2C are in accordance with the NXP I^2C specification (see Ref. 1).

11. Limiting values

Table 9. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to VSS (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DD}	supply voltage			-0.3	+4.6	V
V_I	input voltage	any signal pad		-0.3	+4.6	V
I_I	input current	pad I2C_SDA, I2C_SCL		-	10	mA
I_O	output current	pad I2C_SDA, I2C_SCL		-	10	mA
I_{lu}	latch-up current	$V_I < 0$ V or $V_I > V_{DD}$		-	100	mA
V_{esd_hbm}	electrostatic discharge voltage (Human Body Model)	pads VCC, VSS, RST_N, I2C_SDA, I2C_SCL	[1]		± 2.0	kV
V_{esd_cdm}	electrostatic discharge voltage (Charge Device Model)	pads VCC, VSS, RST_N, I2C_SDA, I2C_SCL	[3]		± 500	V
P_{tot}	Total power dissipation		[2]	-	1	W
T_{stg}	Storage temperature			-55	+125	°C

[1] MIL Standard 883-D method 3015; human body model; C = 100 pF, R = 1.5 kΩ; T_{amb} = –25 °C to +85 °C.

[2] Depending on appropriate thermal resistance of the package.

[3] JESD22-C101, JEDEC Standard Field induced charge device model test method.

12. Recommended operating conditions

The A71CH offers two operation modes, the so-called 1V8 mode and the 3V3 mode targeted for battery supplied applications.

Table 10. Recommended operating conditions

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DD}	supply voltage range	3V3 mode range CPU in free runing mode		2.50	3.3	3.6	V
		1V8 mode		1.62	1.8	1.98	V
V_I	DC input voltage on digital I/O pads I2C_SCL, I2C_SDA	3V3 mode		0		3.6	V
		1V8 mode		0		3.6	V
V_I	DC input voltage on digital input pad RST_N	3V3 mode		0		3.6	V
		1V8 mode		0		3.6	V
T_{amb}	Operating ambient temperature	A7101		-25		+90	°C
		A7102		-40		+90	°C

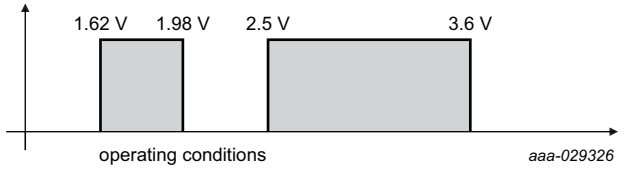


Fig 5. Recommended operating conditions over voltage range

13. Characteristics

13.1 DC characteristics

Measurement conventions

Testing measurements are performed at the contact pads of the device under test. All voltages are defined with respect to the ground contact pad VSS. All currents flowing into the device are considered positive.

13.1.1 General and I²C I/O interface

Table 11. Electrical DC characteristics of I2C_SCL, I2C_SDA and RST_N

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Input/Output: I2C_SCL, I2C_SDA in push-pull mode							
V_{IH}	HIGH level input voltage			0.7 V_{DD}		V_{Imax}[1]	V
V_{IL}	LOW level input voltage			-0.5		0.3 V_{DD}	V
I_{IH}	HIGH level input current in input mode	$V_{IHmin} < V_I < V_{IHmax}$				± 10	µA
I_{IL}	LOW level input current	$V_{ILmin} < V_I < V_{ILmax}$				± 10	µA
V_{OH}	HIGH level output voltage	I_{OH} = –3.0 mA; 3V3 mode	[2]	0.7 V_{DD}			V
		I_{OH} = –3.0 mA; 1V8 mode	[2]	0.7 V_{DD}			V
V_{OL}	LOW level output voltage	I_{OL} = 3.0 mA 3V3 mode				0.4	V
		I_{OL} = 2.0 mA 1V8 mode				0.2 V_{DD}	V
Input/Output: I2C_SCL, I2C_SDA in open-drain mode							
V_{IH}	HIGH level input voltage			0.7 V_{DD}		V_{Imax}[1]	V
V_{IL}	LOW level input voltage			-0.5		0.3 V_{DD}	V
I_{IH}	HIGH level input current in input mode	$V_{IHmin} < V_I < V_{IHmax}$				± 10	µA
I_{IL}	LOW level input current	$V_{ILmin} < V_I < V_{ILmax}$				± 10	µA
V_{OL}	LOW level output voltage	I_{OL} = 3.0 mA 3V3 mode				0.4	V
		I_{OL} = 2.0 mA 1V8 mode				0.2 V_{DD}	V
Input: RST_N							
V_{IH1}	HIGH level input voltage			0.7 V_{DD}		V_{Imax}[1]	V
V_{IL1}	LOW level input voltage			-0.3		0.3 V_{DD}	V
I_{IH1}	HIGH level RST_N input current	$V_{IH1min} \leq V_I \leq V_{DD}$	[3]			± 20	µA
I_{IL1}	LOW level RST_N input current	$0 V \leq V_I \leq V_{IL1max}$;	[3]			± 20	µA

[1] Maximum value according to Table 10 “Recommended operating conditions”

[2] : External pull-up resistor 20 kΩ to VDD. The worst case test condition for parameter V_{OH} is present at minimum V_{DD}. For class A supply voltage conditions V_{DD} = 4.5 V is the worst case with respect to the fix specification limit V_{OHmin} = 3.8 V (0.844 V_{DD}). The supply voltage related limit “0.7 V_{DD}“is a stricter requirement than the fix value 3.8 V at high V_{DD} (0.7 V_{DD} = 3.85 V at V_{DD} = 5.5 V). So, in the V_{DD} range 4.5 V to 5.5 V, V_{OHmin} is specified as “the larger value of 0.7 V_{DD} and 3.8 V, respectively”.

[3] The active low RST_N input internally has a resistive pull-down device to VSS. Accordingly a current is flowing into the pad voltages above 0 V. Figure 6 shows the RST_N input characteristic.

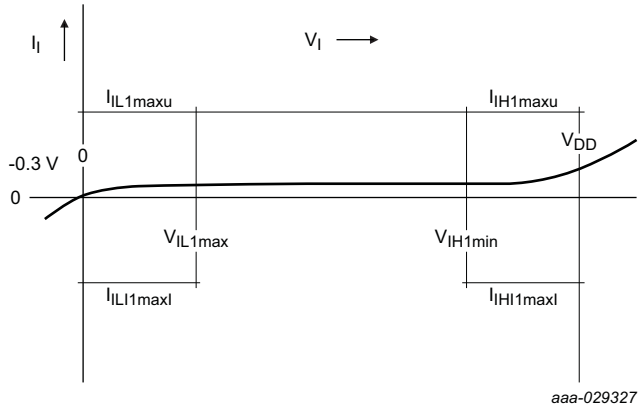


Fig 6. Input characteristic of RST_N

13.1.2 I²C interface at 3V3 mode operation[1]

Table 12. Electrical characteristics of IC supply voltage V_{DD}; V_{SS} = 0 V; T_{amb} = -40 to +90 °C

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Supply							
V_{DD}	supply voltage range	3V3 mode range CPU in free running mode		2.50	3.3	3.6	V
I_{DD}	operating mode: typical CPU						
	no coprocessor active	CPU at 4 MHz			1.45	1.6	mA
	no coprocessor active	CPU at 12 MHz			2.3	2.5	mA
	no coprocessor active	CPU at 24 MHz			2.85	3.1	mA
	no coprocessor active	CPU at 31 MHz			3.4	3.7	mA
	DES coprocessor active (4 MHz)	CPU at 31 MHz			4.0	4.6	mA
	AES coprocessor active (4 MHz)	CPU at 31 MHz			4.3	4.9	mA
	FameXE coprocessor active (FameXE clock = 18 MHz)	CPU at 31 MHz			5.4	5.9	mA
	no coprocessor active	CPU in free running mode			6.3	7.0	mA
	EPROM programming in progress	CPU in free running mode			7.3	8.0	mA
	DES coprocessor active (36 MHz)	CPU in free running mode			8.2	9.2	mA
	AES coprocessor active (36 MHz)	CPU in free running mode			9.3	10.3	mA
	FameXE coprocessor active (FameXE clock = 4 MHz)	CPU in free running mode			6.6	7.3	mA
	FameXE coprocessor active (FameXE clock = 18 MHz)	CPU in free running mode			8.3	9.2	mA
	FameXE coprocessor active (FameXE clock = 48 MHz)	CPU in free running mode			11.5	12.5	mA
	FameXE coprocessor active (FameXE clock = 72 MHz)	CPU in free running mode			13.7	15.1	mA
$I_{DD(ID)}$	supply current CPU IDLE mode	T_{amb} = 25 °C			1.15	1.3	mA
$I_{DD(SLP)}$	supply current SLEEP mode	T_{amb} = 25 °C			45	150	µA
$I_{DD(DSLP)}$	supply current deep sleep mode	RST_N at 0V, T_{amb} = 25 °C				10	µA
		RST_N at 0V, T_{amb} = 90 °C				10	µA

[1] All appropriately marked values are typical values and only referenced for information. They are subject to change without notice.

13.1.3 I²C interface at 1V8 mode operation[1]

Table 13. Electrical characteristics of IC supply voltage V_{DD}; V_{SS} = 0 V; T_{amb} = -40 to +90 °C

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Supply							
V_{DD}	supply voltage range	1V8 mode range		1.62	1.8	1.98	V
I_{DD}	operating mode: typical CPU						
	no coprocessor active	CPU at 4 MHz			1.0		mA
	no coprocessor active	CPU at 12 MHz			1.35		mA
	no coprocessor active	CPU at 24 MHz			2.0		mA
	no coprocessor active	CPU at 31 MHz			2.3		mA
	no coprocessor active	CPU in free running mode			2.45		mA
	DES coprocessor active (36MHz)	CPU in free running mode			2.1		mA
	AES coprocessor active (36MHz)	CPU in free running mode			2.7		mA
	FameXE coprocessor active (FameXE clock = 4 MHz)	CPU in free running mode			2.4		mA
	FameXE coprocessor active (FameXE clock = 18 MHz)	CPU in free running mode			3.45		mA
	FameXE coprocessor active (FameXE clock = 48 MHz)	CPU in free running mode			5.7		mA
	FameXE coprocessor active (FameXE clock = 72 MHz)	CPU in free running mode			7.5		mA
$I_{DD(ID)}$	supply current CPU IDLE mode	T_{amb} = 25 °C			0.76	0.9	mA
$I_{DD(SLP)}$	supply current SLEEP mode	T_{amb} = 25 °C			40	80	µA
$I_{DD(DSLP)}$	supply current deep sleep mode	RST_N at 0V, T_{amb} = 25 °C				10	µA
		RST_N at 0V, T_{amb} = 90 °C				10	µA

[1] All appropriately marked values are typical values and only referenced for information. They are subject to change without notice.

13.2 AC characteristics

Table 14. Non-volatile memory timing characteristics; V_{DD} = 1.8 V ± 10% or 3 V ± 10% V; V_{SS} = 0 V; T_{amb} = -40 to 90 °C

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_{EEP}	EEPROM erase + program time				2.7		ms
t_{EEE}	EEPROM erase time				1.7		ms
t_{EEW}	EEPROM program time				1.0		ms
t_{EER}	EEPROM data retention time	T_{amb} = +55 °C		25			years
N_{EEC}	EEPROM endurance (number of programming cycles)			5×10^5			cycles

13.3 EMC/EMI

EMC and EMI resistance according to IEC 61967-4.

14. Abbreviations

Table 15. Abbreviations

Acronym	Description
AES	Advanced Encryption Standard
CRC	Cyclic Redundancy Check
DES	Digital Encryption Standard
DPA	Differential Power Analysis
DSS	Digital Signature Standard
ECC	Elliptic Curve Cryptography
EEPROM	Electrically Erasable Programmable Read-Only Memory
I/O	Input/Output
MAC	Message Authentication Code
OS	Operating System
PKI	Public Key Infrastructure
SFI	Single Fault Injection
SHA	Secure Hash Algorithm

15. References

[1] I^2C-bus specification and user manual, Rev. 3.0 — June-19-2007, NXP Semiconductors

[2] SOT909-1; HVSON8; Reel pack; Ordering code (12NC) ending 118; Packing Information; Rev. 2 — 19 April 2013

[3] Application note SCIIC Protocol Specification, Application note, Rev 1.5, an195015 — 31 January 2017

[4] Datasheet A710x family with JCOP 2.4.2. R1 – Secure authentication microcontroller, Rev 3.5, ds236635 — 17 November 2017

16. Revision history

Table 16. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
449310	20180221	Objective short data sheet		
Modifications:	• Initial version			

17. Legal information

17.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

17.2 Definitions

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ICs with DPA Countermeasures functionality

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