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Ultra-Low-Power Real Time Clock with Integrated Power Switch

MAX31334

Product Highlights

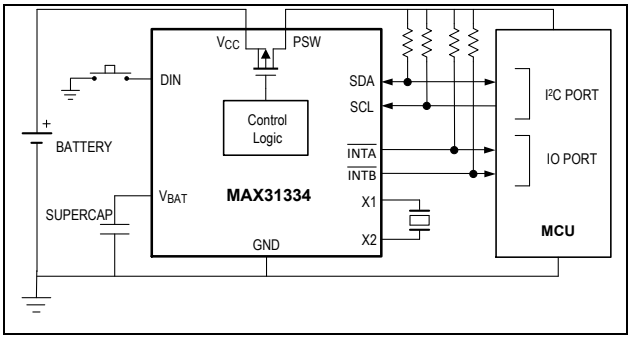
- Ultra-Low-Power Real Time Clock
  - 70nA Timekeeping Current
  - 1.1V to 5.5V Timekeeping Voltage Range
  - Automatic Switchover to Backup Supply on Power Failure
  - Trickle Charger for External Supercapacitor
- Integrated Power Switch with State Machine Increases System Battery Life
  - Up to 500mA Continuous Current
  - Ultra-Low 57mΩ On-Resistance
  - Wakeup on Periodic Interrupt—Countdown Timer (100ms to 1hr) and Alarms (1s Resolution)
  - Wakeup on External Interrupt, Like Pushbutton
- Saves Board Space
  - No External Capacitors Required for Crystal
  - 1.5mm x 2mm 12-WLP
  - 3mm x 3mm 12-TDFN
- Value-Add Features for Ease of Use
  - Works with Many 32.768kHz Crystals (no C_L limitation)
  - Two Time-of-Day Alarms
  - Event Detection and Timestamps
  - 1/128 Second Register
  - 32 bytes of User RAM

See more *Product Highlights*

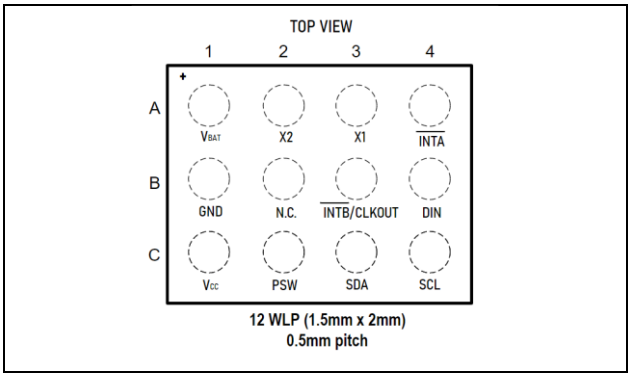
Key Applications

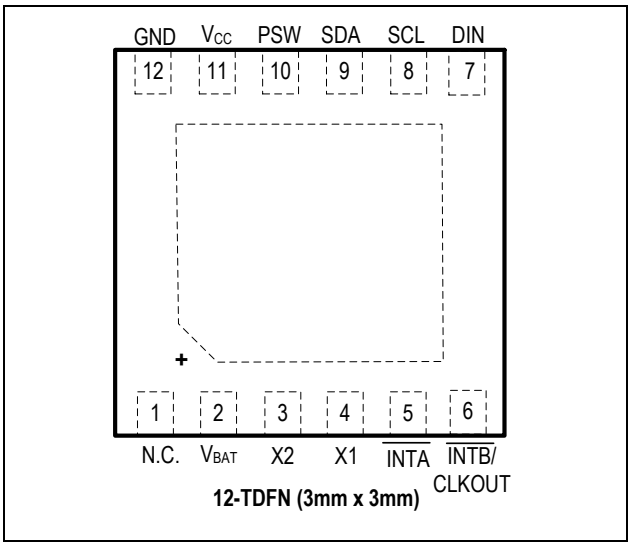
- Electronic Shelf Label
- Ultra-low-power IoT Modules
- Medical Wearables
- Temperature Loggers
- Asset Tracking
- Battery-Powered Devices

Simplified Application Diagram



Pin Description





See more *Who should use this part.*

***Ordering Information* appears at end of data sheet**

19-101569; Rev 0; 8/22

Absolute Maximum Ratings

Voltage Range on Any Pin Relative to Ground..... -0.3V to +6V

PSW Output Continuous Current..... 500mA

Operating Temperature Range..... -40°C to +85°C

Junction Temperature.....+125°C

Storage Temperature Range..... -55°C to +125°C

Soldering Temperature (Reflow) .....260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

12-WLP

Package Code	W121L1+2
Outline Number	*21-100630*
Land Pattern Number	Refer to *Application Note 1891*
Four Layer Board:	
Junction-to-Ambient Thermal Resistance (θ_{JA})	61.89°C/W
Junction-to-Case Thermal Resistance (θ_{JC})	N/A

12-TDFN

Package Code	TD1233+1C
Outline Number	*21-0664*
Land Pattern Number	*90-0397*
Single Layer Board:	
Junction-to-Ambient Thermal Resistance (θ_{JA})	63°C/W
Junction-to-Case Thermal Resistance (θ_{JC})	8.5°C/W
Four Layer Board:	
Junction-to-Ambient Thermal Resistance (θ_{JA})	41°C/W
Junction-to-Case Thermal Resistance (θ_{JC})	8.5°C/W

Electrical Characteristics

(V_{CC} = +1.1V to +5.5V, V_{ACT} = Active Supply Rail (V_{CC} or V_{BAT}), T_A = -40°C to +85°C, unless otherwise noted. Typical values at V_{CC} = +3.0V, T_A = +25°C, WLP package, unless otherwise noted. Limits are 100% tested at T_A = +25°C. *Note 1*.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DC CHARACTERISTICS							
Timekeeping Supply Voltage Range	V_{CC}	(*Note 3*)		1.1		5.5	V
Interface Supply Voltage Range	V_{CCIO}	Full Operation		1.62		5.5	V
Initial Power-On Voltage	$V_{CC(POR)}$			1.7			V
Timekeeping Current	I_{CCT}	(*Note 4*) PSW = OFF	V_{ACT} = +1.8V		70	750	nA
			V_{ACT} = +3.0V		70	750	
			V_{ACT} = +4.2V		75	800	

(V_{CC} = +1.1V to +5.5V, V_{ACT} = Active Supply Rail (V_{CC} or V_{BAT}), T_A = -40°C to +85°C, unless otherwise noted. Typical values at V_{CC} = +3.0V, T_A = +25°C, WLP package, unless otherwise noted. Limits are 100% tested at T_A = +25°C. *Note 1*.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Maximum Supply Power-Up Slew Rate	T_{VCCR}				5		V/ms
Maximum Supply Switchover Slew Rate	T_{VCCF}				0.5		V/ms
POWER SWITCH (PSW) CHARACTERISTICS							
PSW Supply Range	$V_{CC(PSW)}$			1.62		5.5	V
PSW Output On-Resistance	R_{PSW}	PSW = ON	V_{CC} = +1.8V		95	165	mΩ
			V_{CC} = +3.0V		57	90	
			V_{CC} = +4.2V		47	75	
PSW Output Voltage	$V_{OL(PSW)}$	PSW = OFF	V_{CC} = +1.8V, I_{SINK} = 200µA			0.1	V
			V_{CC} = +3.0V, I_{SINK} = 1.6mA			0.2	
BATTERY BACKUP AND THRESHOLD							
Timekeeping Backup Voltage Range	V_{BAT}			1.1		5.5	V
Power Fail Threshold Voltage	V_{PF}	V_{TH1}			1.55		V
		V_{TH2}			2.0		
Trickle-Charge Current-Limiting Resistance	R1				3.3		kΩ
	R2				6.4		
	R3				11.3		
Minimum Battery Voltage for V_{CC} to V_{BAT} switch (Auto Mode)	V_{BAT_SW}	$V_{CC} < V_{TH1}$ and $V_{CC} < V_{BAT\_SW}$			1.5		V
SCHMITT TRIGGER INPUT (DIN)							
Logic 1 Input	V_{IH}	V_{ACT} = 1.8 to 5.5V		0.7 x V_{ACT}		V_{ACT} + 0.3	V
		V_{ACT} = 1.62V		0.75 x V_{ACT}		V_{ACT} + 0.3	
Logic 0 Input	V_{IL}	V_{ACT} = 1.8 to 5.5V		-0.3		0.3 x V_{ACT}	V
		V_{ACT} = 1.62V		-0.3		0.25 x V_{ACT}	
Input Leakage	I_{LI}			-0.1		+0.1	µA
LOGIC INPUTS AND OUTPUTS							
Logic 1 Input (SDA, SCL)	V_{IH}	V_{CC} = 1.62V		0.75 x V_{CC}		V_{CC} + 0.3	V
		V_{CC} = 1.8V to 5.5V		0.7 x V_{CC}		V_{CC} + 0.3	

(V_{CC} = +1.1V to +5.5V, V_{ACT} = Active Supply Rail (V_{CC} or V_{BAT}), T_A = -40°C to +85°C, unless otherwise noted. Typical values at V_{CC} = +3.0V, T_A = +25°C, WLP package, unless otherwise noted. Limits are 100% tested at T_A = +25°C. *Note 1*.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Logic 0 Input (SDA, SCL)	V_{IL}	V_{CC} = 1.62V	-0.3		0.25 x V_{CC}	V
		V_{CC} = 1.8V to 5.5V	-0.3		0.3 x V_{CC}	
Input Leakage (SCL)	I_{IL}	V_{CC} ≥ 1.62V	-0.1		+0.1	µA
Output Leakage (SDA, $\overline{INTA}$, $\overline{INTB}$/CLKOUT)	I_O	V_{CC} ≥ 1.62V	-1		+1	µA
Output Logic 0 (SDA, $\overline{INTA}$, $\overline{INTB}$/CLKOUT)	I_{OL}	V_{OL} = +0.4V, V_{CC} ≥ 1.62V	2			mA
AC CHARACTERISTICS (V_{CC} = +1.62V to +5.5V)						
SCL Clock Frequency	f_{SCL}	(*Note 5*)	10		400	kHz
Bus Free Time Between a STOP and START Condition	t_{BUF}		1.3			µs
Hold Time (Repeated) START Condition	$t_{HD:STA}$	(*Note 6*)	0.6			µs
Low Period of SCL Clock	t_{LOW}		1.3			µs
High Period of SCL Clock	t_{HIGH}		0.6			µs
Data Hold Time	$t_{HD:DAT}$	(*Note 7*, *Note 8*)	0		0.9	µs
Data Setup Time	$t_{SU:DAT}$	V_{CC} = 3.0V (*Note 9*)	100			ns
Setup Time for a Repeated START Condition	$t_{SU:STA}$		0.6			µs
Minimum Rise Time of Both SDA and SCL Signals	t_{RMIN}	(*Note 10*)		20 + 0.1C_B		ns
Maximum Rise Time of Both SDA and SCL Signals	t_{RMAX}			300		ns
Minimum Fall Time for Both SDA and SCL Signals	t_{FMIN}	(*Note 10*)		20 + 0.1C_B		ns
Maximum Fall Time for Both SDA and SCL Signals	t_{FMAX}			300		ns
Setup Time for STOP Condition	$t_{SU:STO}$		0.6			µs
Maximum Capacitive Load for Each Bus Line	C_B	(*Note 10*)		400		pF

(V_{CC} = +1.1V to +5.5V, V_{ACT} = Active Supply Rail (V_{CC} or V_{BAT}), T_A = -40°C to +85°C, unless otherwise noted. Typical values at V_{CC} = +3.0V, T_A = +25°C, WLP package, unless otherwise noted. Limits are 100% tested at T_A = +25°C. *Note 1*.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
I/O Capacitance	$C_{I/O}$	(*Note 11*)		10		pF
SCL Spike Suppression	t_{SP}	(*Note 11*)		37		ns
Oscillator Stop Flag (OSF) Delay	t_{OSF}	(*Note 12*)		30	100	ms
Timeout Interval	$t_{TIMEOUT}$	(*Note 13*)	25		35	ms

Note 1: Limits at -40°C and +85°C are guaranteed by design; not production tested.

Note 2: Voltage referenced to ground.

Note 3: Timekeeping function is active through this range. I^2C operation is not guaranteed below $V_{CCIO(min)}$.

Note 4: Specified with I^2C bus inactive. Oscillator (timekeeping function) operational. (ENCLKO = 0).

Note 5: The minimum SCL clock frequency is limited by the bus timeout feature, which resets the serial bus interface if SCL is held low for $t_{TIMEOUT}$.

Note 6: After this period, the first clock pulse is generated.

Note 7: A device must internally provide a hold time of at least 300ns for the SDA signal (referred to the V_{IHMIN} of the SCL signal) to bridge the undefined region of the falling edge of SCL.

Note 8: The maximum $t_{HD:DAT}$ need only be met if the device does not stretch the low period (t_{LOW}) of the SCL signal.

Note 9: A fast-mode device can be used in a standard-mode system, but the requirement $t_{SU:DAT} \geq 250ns$ must then be met.

This is automatically the case if the device does not stretch the low period of the SCL signal. If such a device does stretch the low period of the SCL signal, it must output the next data bit to the SDA line $t_{RMAX} + t_{SU:DAT} = 1000 + 250 = 1250ns$ before the SCL line is released.

Note 10: C_B is the total capacitance of one bus line, including all connected devices, in pF.

Note 11: Guaranteed by design; not 100% production tested.

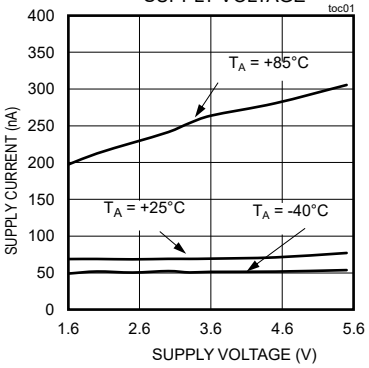
Note 12: The parameter t_{OSF} is the period of time the oscillator must be stopped for the OSF flag to be set over V_{CC} range.

Note 13: The device I^2C interface is in reset state and can receive a new START condition when SCL is held low for at least $t_{TIMEOUTMAX}$. Once the device detects this condition, the SDA output is released. The oscillator must be running for this function to work.

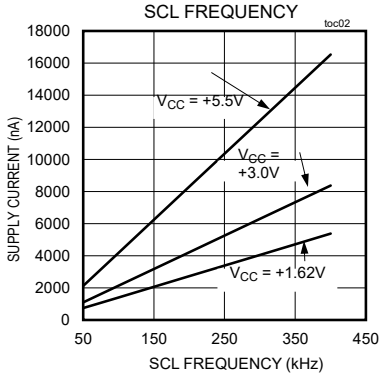
Typical Operating Characteristics

V_{CC} = 3V; T_A = +25°C, unless noted otherwise (T_A = +25°C, unless otherwise noted.)

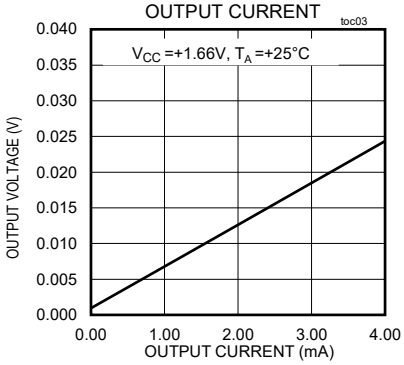
POWER SUPPLY CURRENT vs. SUPPLY VOLTAGE



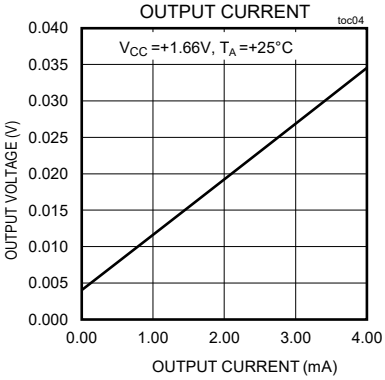
POWER SUPPLY CURRENT vs. SCL FREQUENCY



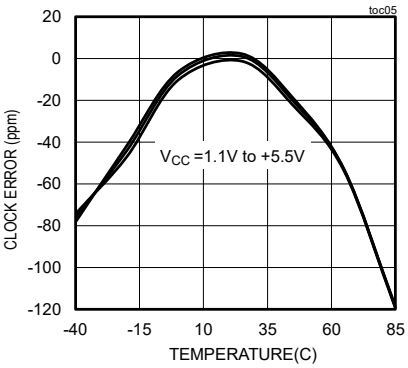
$\overline{INTA}$ OUTPUT VOLTAGE LOW vs. OUTPUT CURRENT



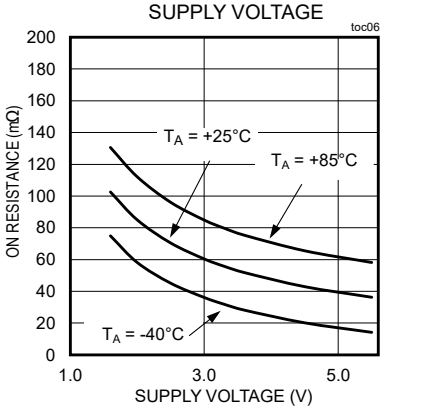
CLKOUT/INTBb OUTPUT VOLTAGE LOW vs. OUTPUT CURRENT



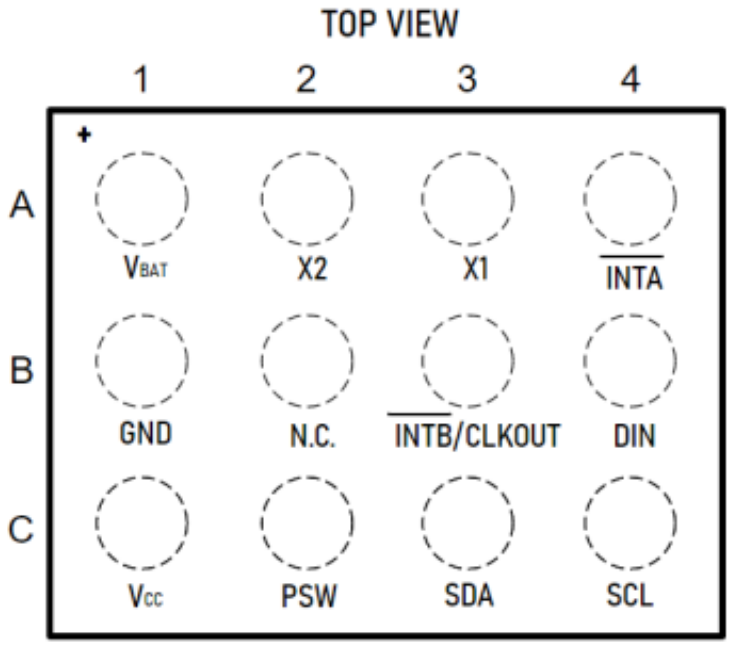
CLOCK ERROR vs. TEMPERATURE



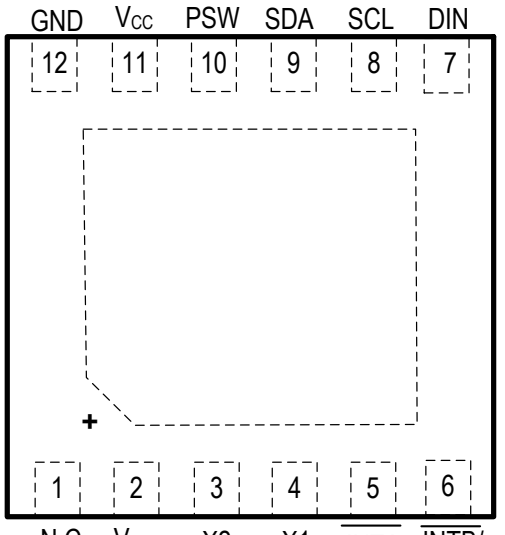
POWER SWITCH ON RESISTANCE vs. SUPPLY VOLTAGE



Pin Configurations



12 WLP (1.5mm x 2mm)
0.5mm pitch

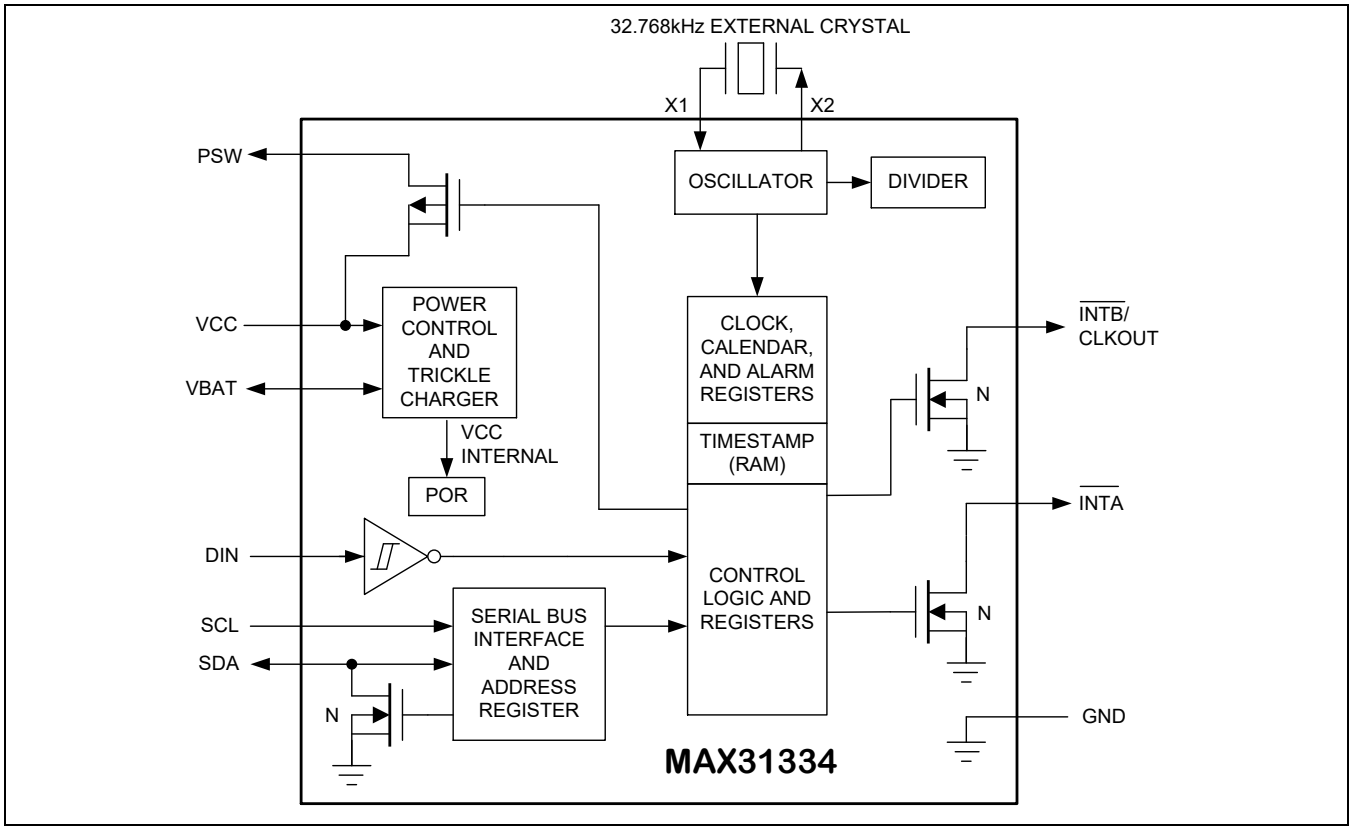


12-TDFN (3mm x 3mm)

Pin Descriptions

PIN		NAME	FUNCTION
WLP	TDFN		
A1	2	VBAT	Backup Battery Input and Trickle Charger Output. Connect to GND when backup battery is not used.
A2	3	X2	Second Crystal Input for an External 32.768kHz Crystal. See the *Oscillator Circuit and Clock Accuracy* section for recommended external crystal parameters.
A3	4	X1	First Crystal Input for an External 32.768kHz Crystal. See the *Oscillator Circuit and Clock Accuracy* section for recommended external crystal parameters.
A4	5	$\overline{\text{INTA}}$	Active-Low Interrupt Output. This pin is used to output an alarm interrupt. It is an open-drain pin and requires an external pullup resistor. If not used, connect this pin to ground. See *Table 2*.
B1	12	GND	Ground
B2	1	N.C.	Not connected
B3	6	$\overline{\text{INTB}}$/CLK OUT	Square-Wave Clock or Active-Low Interrupt Output. This pin is used to output a programmable square wave or an alarm interrupt signal. This is an open-drain output and requires an external pullup resistor. If not used, connect this pin to ground. See *Table 2*.
B4	7	DIN	Digital SCHMITT TRIGGER Input. Connect to ground if not used.
C1	11	VCC	Supply Voltage
C2	10	PSW	Power switch output. VCC is output through a 57mΩ switch when turned on. This pin is pulled down to 0V when the switch is turned off.
C3	9	SDA	Serial-data input/output. SDA is the input/output pin for the I^2C serial interface. The SDA pin is open-drain and requires an external pullup resistor.
C4	8	SCL	Serial-clock input. SCL is used to synchronize data movement on the serial interface.

Functional Diagrams



Detailed Description

The MAX31334 ultra-low-power, real-time clock (RTC) is a time-keeping device that consumes only 70nA timekeeping current. It features an integrated high-side power pass switch that enables ultra-low-power idle modes on duty-cycled applications by disconnecting power to other devices on the system. The power switch on/off durations can be controlled by periodic interrupt sources such as countdown timer (programmable from 100ms to 1hr) and alarms (1s resolution). The power switch can also be controlled by an external interrupt (from a pushbutton, for example) on the DIN pin. The MAX31334 supports a wide range of crystals with any loading (C_L) spec which broadens the pool of usable crystals for this device. This device is accessed through an I^2C serial interface. An integrated power-on reset function ensures deterministic default register status upon power-up.

The device also features a backup supply pin (V_{BAT}) and automatically switches over to this supply when the main supply (V_{CC}) drops below the programmed threshold voltage. Other features include two time-of-day alarms, interrupt outputs, a programmable square-wave output, event detection input with timestamping (32-byte timestamp registers double as RAM storage), a serial bus timeout mechanism.

The digital Schmitt trigger input (DIN) can also be used to record timestamps and/or assert an interrupt on a falling/rising edge of the DIN signal. The clock/calendar provides seconds, minutes, hours, day, date, month, and year information. A 1/128 seconds register is available for a sub-second timestamp resolution. The date at the end of the month is automatically adjusted for months with fewer than 31 days, including corrections for leap year. The clock operates in 24-hour/12-hour format.

The MAX31334 is available in lead (Pb)-free/RoHS compliant, 12-bump, 1.5mm x 2mm WLP with 0.5mm pitch, as well as a 12-pin 3mm x 3mm TDFN package.

The device supports the -40°C to +85°C extended temperature range.

Clock/Calendar

The time and calendar information are obtained by reading the appropriate I^2C registers. The time and calendar data are set or initialized by writing to the appropriate time/date registers. The contents of the time and calendar registers are in the binary-coded decimal (BCD) format. The century bit (bit 7 of the Month register) is toggled when the Years register overflows from 99 to 00. The day-of-week register increments at midnight. Values that correspond to the day of week are user-defined but must be sequential (i.e., if 1 equals Sunday, then 2 equals Monday, and so on). Illogical time and date entries result in undefined operation. A write to any of clock/calendar registers updates the clock/calendar after a 3ms window.

I^2C Interface

The I^2C interface is guaranteed to operate when V_{CC} is between 1.62V and 5.5V. The I^2C interface is accessible whenever V_{CC} is at a valid level. To prevent invalid device operation, the I^2C interface should not be accessed when VCC is below +1.62V. The peripheral address is defined as the seven most significant bits (MSBs) sent by the controller after a START condition. The address is 1101000 (or 0xD0, left justified with LSB set to 0). The eighth bit is used to define a write or read operation. If a microcontroller connected to the MAX31334 resets during I^2C communication, it is possible that the microcontroller and the MAX31334 could become unsynchronized. In such scenarios, the timeout feature in the MAX31334 can be used to reset the I^2C peripheral controller if the SCL is held low for $>t_{TIMEOUT}$. After a loss of communication, if the microcontroller initiates a new I^2C transaction, the MAX31334's I^2C state machine is reset.

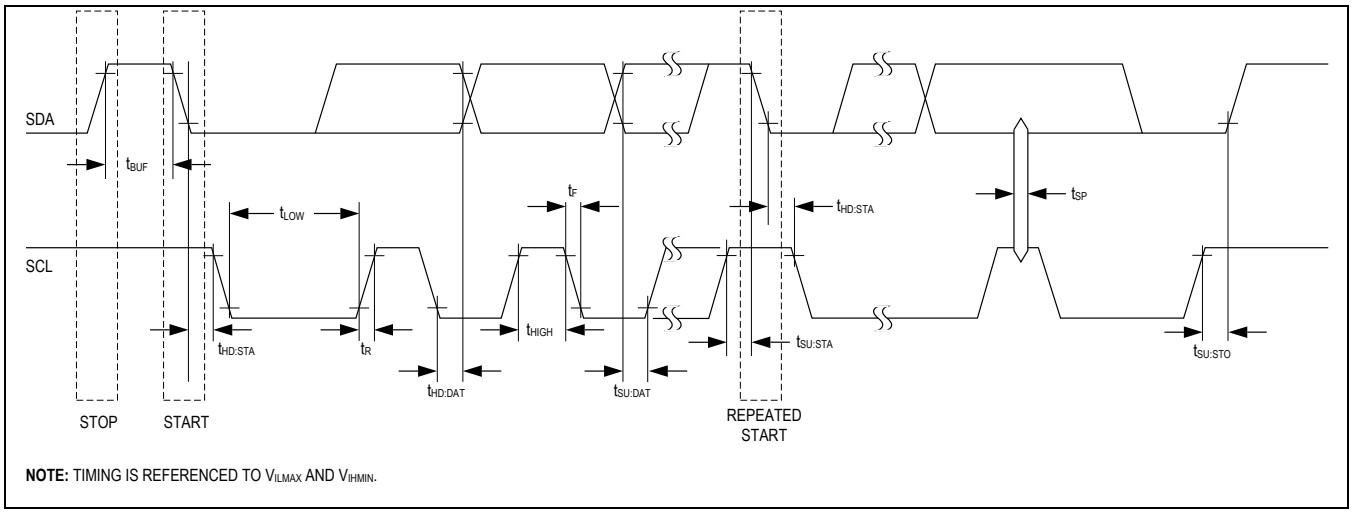


Figure 1. I^2C Timing Diagram

Oscillator Circuit and Clock Accuracy

The MAX31334 uses an external 32.768kHz crystal. The oscillator circuit does not require any external components to operate. This also enables the use of many 32.768kHz crystals regardless of the loading (C_L) spec. A crystal with a minimum Quality Factor of 9000 must be used for sustaining oscillations. After the oscillator is enabled, the startup time of the oscillator circuit is usually less than one second.

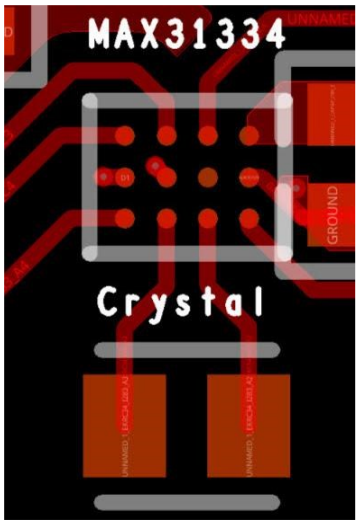


Figure 2. PCB Layout Example

It is recommended to minimize the trace lengths from the crystal to the X1/X2 pins of the MAX31334 and avoid placing them close to any nearby ground plane to minimize the parasitic capacitance. Also, keep any other high-speed clock routings including signal from INTB/CLKO pin far away from these X1/X2 pins to reduce coupling effect which can degrade the oscillator signal integrity. *Figure 2* shows the recommended PCB layout for the crystal and oscillator.

The accuracy of the MAX31334 depends on the parallel resonant frequency of the crystal used, which is typically above the nominal 32.768kHz. The device includes a fractional divider circuit that can correct the typical accuracy close to 0ppm. The MAX31334 is factory-trimmed to ensure a typical accuracy of ±20ppm with the NDK NX2012SA 6pF crystal, which is also used on the MAX31334SHLD evaluation board. As stated previously, any other suitable crystal can be used instead. Due to the nature of the oscillator and the nature of quartz blanks inside different crystals, the accuracy observed with other crystals can be off by 10 to 100's of ppm. The MAX31334 provides an option to digitally correct the clock accuracy using the OFFSET_HIGH (20h) and OFFSET_LOW (21h) registers. These registers enable the user to measure and enter the absolute error. The digital logic then calculates the required compensation and corrects the accuracy with a resolution of 0.477ppm. Follow the steps to measure and correct the clock accuracy on your board.

1. Power on the MAX31334 and write 0x07 to the RTC_CONFIG2 (04h) register to enable the uncorrected 32kHz output clock.
2. Measure the clock frequency on INTB/CLKO pin using a frequency counter and record it as MEAS.
3. Calculate uncorrected crystal accuracy in ppm as: ACC = ((MEAS – 32768) x 10^6)/32768
4. Calculate the offset value as: OFFSET = int{ACC/0.477}.
5. Split the final 16-bit OFFSET value and enter the upper eight bits into the OFFSET_HIGH register, then the lower eight bits into the OFFSET_LOW register.
6. The new offset correction starts taking effect after the OFFSET_LOW byte is written.

The new offset correction remains valid as long as there is power source (VCC or VBAT) provided. The offset registers default to a factory-trimmed value at every power-on-reset (POR) event.

Power Management

The MAX31334 features a backup battery voltage pin (VBAT) in addition to the primary supply voltage pin (VCC). Initial power-up should always be performed on the VCC domain, and this rail is expected to be equal to or higher than VCC(POR) = 1.7V; this ensures a successful POR function. If the VCC rail stays below 1.7V (but above 1.62V) during the initial power-up, an external I^2C controller can communicate with the MAX31334, but successful operation is not guaranteed because POR was not achieved.

The MAX31334 has a power management function which monitors supply voltage on V_{CC} and backup battery voltage on V_{BAT}, and then determines which source to use as an internal supply. There is a PFAIL interrupt flag status bit in the register map to indicate the power fail condition. The V_{BAT} pin should be connected to the backup battery. If there is no backup battery, V_{BAT} should be tied to ground. Power management control bits Pwr_mgmt[1:0] (register 1Dh) are used as follows: for the Power Management Auto and Trickle Charger mode, a "power fail voltage" can be programmed to 1.55V (default) or 2V. MAX31334 switches from the backup battery to the internal power supply if and only if the main supply VCC is lower than both the power fail voltage and the backup battery voltage (and the backup battery voltage is higher than VBAT_SW = 1.5V). Otherwise, VCC remains as the main supply. There is an PFAIL interrupt flag status bit in the STATUS (00h) register that can be used as a power fail flag. The PFAIL interrupt flag monitors the VCC supply and is set when VCC falls below the power fail threshold voltage.

Table 1. Power Management

EN_TRICKLE	VBACK_SEL	MANUAL_SEL	MODE OF OPERATION	
1	x	0	**POWER MANAGEMENT AUTO AND TRICKLE CHARGER ON**	
			Supply Condition	Active Supply
			VCC < VPF, VCC < VBAT	VBAT
			VCC < VPF, VCC > VBAT	VCC
			VCC > VPF, VCC < VBAT	VCC
			VCC > VPF, VCC > VBAT	VCC
1	0	1	Power Management Manual and Trickle Charger On Active Supply = VCC	
1	1	1	Power Management Manual and Trickle Charger On Active Supply = VBAT for VBAT > VCC	
0	x	0	**Power Management Auto and Trickle Charger Off**	
			Supply Condition	Active Supply
			VCC < VPF, VCC < VBAT	VBAT
			VCC < VPF, VCC > VBAT	VCC
			VCC > VPF, VCC < VBAT	VCC
			VCC > VPF, VCC > VBAT	VCC
0	0	1	Power Management Manual and Trickle Charger Off Active Supply = VCC	
0	1	1	Power Management Manual and Trickle Charger Off Active Supply = VBAT for VBAT > VCC	

Trickle Charger

The trickle charger is for charging an external super capacitor or a rechargeable battery. The maximum charging current can be calculated as follows:

$I_{MAX} = (V_{CC} - V_D - V_{BAT}) / R$

where V_D is the diode voltage drop, V_{BAT} is the voltage of the battery being charged, and R is the resistance selected in the charging path. As the battery charges, the battery voltage increases and the voltage across the charging path decreases. Therefore, the charging current also decreases.

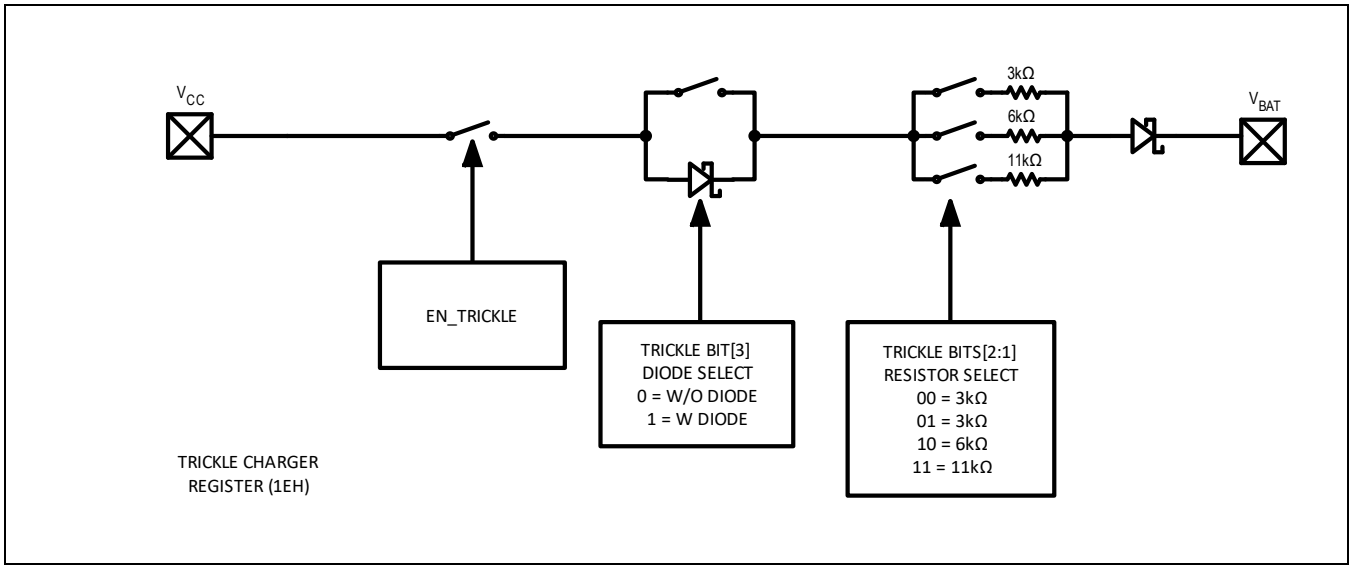


Figure 3. Trickle Charger

Power Switch (PSW) State Machine

The MAX31334 includes a power switch state machine (PSW SM) that controls the operation of the switch, thereby controlling the on/off durations of all downstream devices powered through the PSW pin.

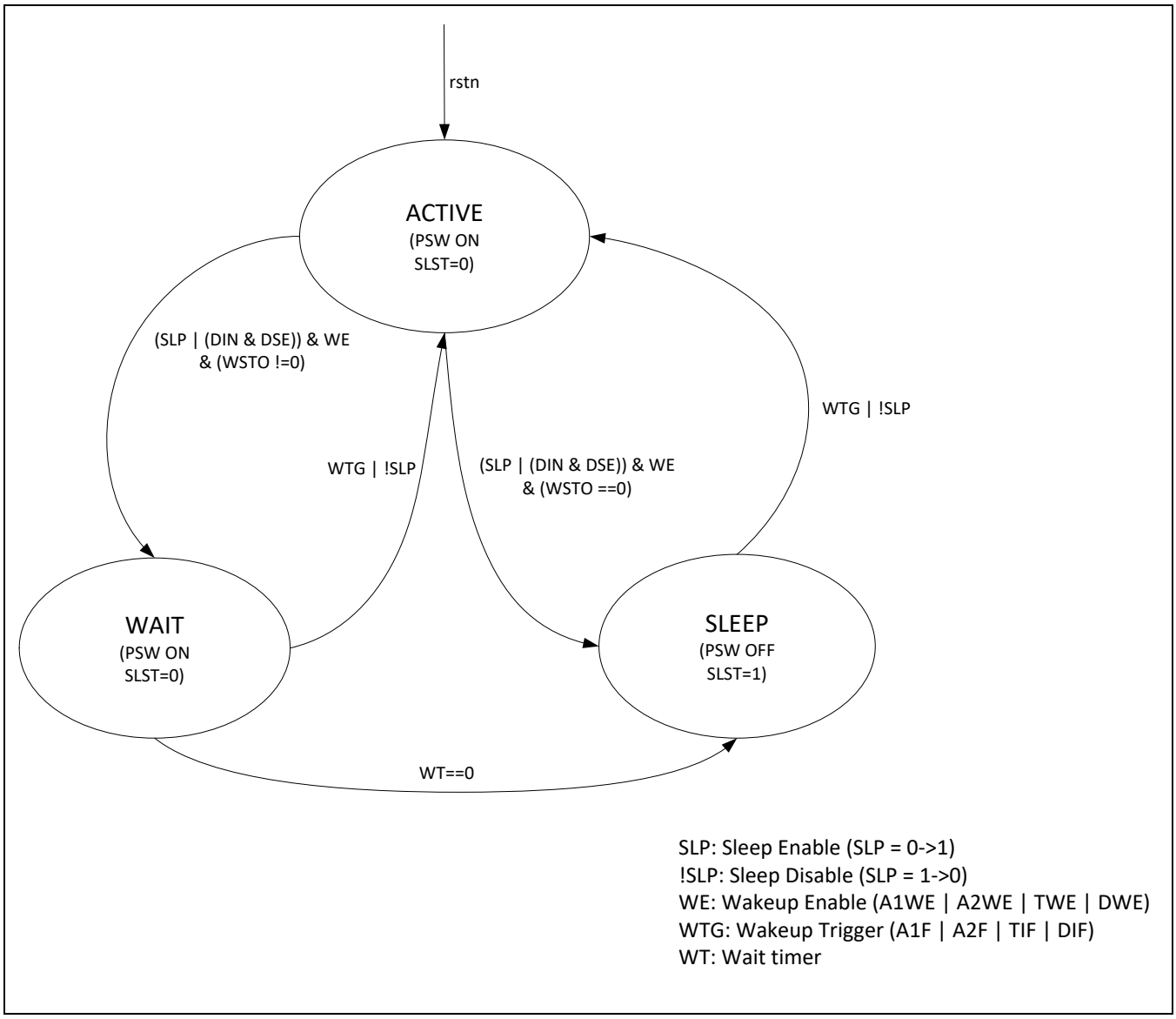


Figure 4. PSW State Machine

ACTIVE

This is the default operating state of the MAX31334 PSW SM, where PSW = ON and SLST = 0.
The MAX31334 enters ACTIVE each time a POR event is detected on the VCC pin.
All the configuration related to the switch (wait/sleep duration and wakeup sources) must be done in this state.

Four possible wakeup sources can be configured:

1. The Countdown Timer can be enabled as a wakeup source by setting TWE = 1. Before exiting the Active state, the countdown timer needs to be configured through registers Timer_Init (1Bh, 1Ch) and Timer_Config (06h), and then enabled (TE = 1) to begin the count.

2. Alarm1 can be enabled as a wakeup source by setting A1WE = 1 and configuring the match condition using the Alarm1 registers (10h to 15h).

3. Alarm2 can be enabled as a wakeup source by setting A2WE = 1 and configuring the match condition using the Alarm2 registers (16h to 18h).

4. An external trigger on the DIN pin can be enabled as a wakeup source by setting DWE = 1 and configuring the trigger polarity (DIP) and debounce (DDB).

Additionally, The DIN pin can also be enabled as a sleep entry trigger by setting DSE = 1.
The transition to the next state (WAIT or SLEEP) is achieved through one of two ways:
1. Write SLP = 1 through I^2C
2. Valid transition on DIN pin && DSE == 1

Transition to the next state does not occur if the oscillator is disabled or OSF = 1.

WAIT

This is the intermediate WAIT state of the MAX31334 PSW SM, where PSW = ON and SLST = 0. This state provides additional time for the microcontroller to perform any critical tasks before it loses power in SLEEP.
The duration of WAIT depends on the value of the WSTO bitfield and can last up to ~55ms. The WSTO bitfield needs to be programmed to the desired value before exiting ACTIVE.

Exit from WAIT to SLEEP occurs when the WSTO timeout duration elapses.

Exit from WAIT back to ACTIVE can occur through one of four events:

1. Countdown timer elapses && TWE==1
2. Valid DIN transition detected && DWE==1
3. Alarm1 match condition occurs && A1WE==1
4. Alarm2 match condition occurs && A2WE==1

If more than one wakeup source is enabled, the first event among the four listed triggers a transition to ACTIVE.

If WSTO = 0, this state is bypassed and the PSW SM directly enters SLEEP.

SLEEP

This is the SLEEP state of the PSW SM, where PSW = OFF and SLST = 1.
The PSW pin is pulled down to GND, thereby cutting power to all the downstream devices on this rail.
Exit from SLEEP back to ACTIVE can occur through one of 4 events:
1. Countdown timer elapses && TWE==1
2. Valid DIN transition detected && DWE==1
3. Alarm1 match condition occurs && A1WE==1
4. Alarm2 match condition occurs && A2WE==1

If more than one wakeup source is enabled, the first event among the four listed triggers a transition to ACTIVE.
During normal operation, this does not transition from SLEEP to WAIT.

Special Conditions

Some special conditions can also trigger a transition from SLEEP (or WAIT) to ACTIVE:
1. Oscillator is disabled (EN_OSC = 0) or stops abruptly (OSF = 1).
2. Write SLP = 0 through I^2C.

Note: When DSE = 1, writing SLP = 0 through I^2C does not bring the SM back to ACTIVE. This is a special condition, and the user needs to write DSE = 0 to bring the SM back to ACTIVE.

Interrupt Status and Outputs

When an interrupt is asserted, a corresponding status bit in STATUS (00h) register becomes “1”, and an interrupt output transitions from High to Low. The interrupt status bit and output can be cleared by reading the STATUS (00h) register. See *Table 2* for interrupt configurations.

Table 2. Interrupt Modes

ENCLKO	$\overline{INTA}$	CLKOUT/$\overline{INTB}$
0	$\overline{INTA}$: Alarm2, Timer, Power Fail (PFAIL), Digital interrupt (DIN)	$\overline{INTB}$: Alarm1
1	$\overline{INTA}$: Alarm1, Alarm2 Timer, Power Fail (PFAIL), Digital interrupt (DIN)	CLKOUT

Alarms

The MAX31334 contains two time-of-day/date alarms. Alarm 1 can be set by writing to registers 10h–15h. Alarm 2 can be set by writing to registers 16h to 18h. The alarms can be programmed by the A1IE and A2IE bits in Int_en register to activate the INT output on an alarm match condition. Bit 7 of each of the time-of-day/date alarm registers and bit 6 of Alm1_mon register are mask bits (*Table 3*). When all the mask bits for each alarm are logic 0, an alarm only occurs when the values in the timekeeping registers match the corresponding values stored in the time-of-day, date, month, and year alarm registers. The alarms can also be programmed to repeat every second, minute, hour, day, or date. *Table 3* and *Table 4* shows the possible settings. Configurations not listed in the table result in illogical operation. The DY_DT_MATCH bit (bit 6 of the alarm day/date registers) controls whether the alarm value stored in bits 0 to 5 of that register represents the day of the week or the date of the month. If DY_DT_MATCH is written to logic 0, the alarm is the result of a match with date of the month. If DY_DT_MATCH is written to logic 1, the alarm is the result of a match with day of the week.

Table 3. Alarm 1 Settings

DY/DT	ALARM 1 REGISTER MASK BITS (BIT 7)						ALARM RATE
	A1M6	A1M5	A1M4	A1M3	A1M2	A1M1	
X	1	1	1	1	1	1	Alarm once a second
X	1	1	1	1	1	0	Alarm when seconds match
X	1	1	1	1	0	0	Alarm when minutes and seconds match
X	1	1	1	0	0	0	Alarm when hours, minutes, and seconds match
0	1	1	0	0	0	0	Alarm when dates, hours, minutes, and seconds match
0	1	0	0	0	0	0	Alarm when months, dates, hours, minutes, and seconds match
0	0	0	0	0	0	0	Alarm when years, months, dates, hours, minutes, and seconds match
1	1	1	0	0	0	0	Alarm when days, hours, minutes, and seconds match

Table 4. Alarm 2 Settings

DY/DT	ALARM 2 REGISTER MASK BITS (BIT 7)			ALARM RATE
	A2M4	A2M3	A2M2	Alarm once per minute (00 seconds of every minute)
X	1	1	1	Alarm when minutes match
X	1	1	0	Alarm when hours and minutes match
X	1	0	0	Alarm when dates, hours, and minutes match
0	0	0	0	Alarm when days, hours, and minutes match
1	0	0	0	Alarm when days, hours, and minutes match

Countdown Timer

The MAX31334 features a countdown timer with a pause function. The timer can be configured by writing to registers Timer_config (06h) and Timer_init (1Bh, 1Ch). The Timer_init register should be loaded with the initial value from which the timer would start counting down. The Timer_config register allows these configuration options:

- Select the frequency of the timer using the TFS[1:0] field.
- Start/stop the timer using the TE (Timer Enable) bit.
- Enable/disable the timer repeat function using the TRPT bit. This function reloads and restarts the timer with the same init value once it counts down to zero.
- Pause/resume the countdown at any time when the timer is enabled using the TPAUSE bit (explained as follows).

The timer can be programmed to assert the INT output whenever it counts down to zero. This can be enabled/disabled using the TIE bit in register Int_en register (01h).

The TPAUSE bit is only valid when TE = 1. This bit must be reset to 0 whenever TE is reset to 0.

Table 5 highlights the steps to be used for various use cases involving TE and TPAUSE.

Typical use cases:

- Countdown timer without pause: Step 1 → Step 2 → Step 1 and so on
- Countdown timer with pause: Step 1 → Step 2 → Step 3a → Step 3b → Step 1 and so on

Table 5. Countdown Timer Sequence

SEQUENCE	TE	TPAUSE	ACTION
Step 1	0	0	Countdown timer is reset, and ready for next countdown operation. Timer_init can be programmed in this state.
Step 2	1	0	Countdown timer starts counting down from the value programmed in Timer_init
Step 3a (Optional)	1	1	Countdown timer is paused and is ready to start counting down when TPAUSE is programmed back to '0'. Contents of the countdown timer are preserved in this state.
Step 3b If 3a is true	1	0	Countdown timer is brought out of pause state and starts counting down from the paused value.
	0	1	Not allowed

Timestamps

The MAX31334 can record and store timestamps when triggered by specific events. Up to four timestamps can be stored in the four banks of timestamp registers (TS0, TS1, TS2, and TS3). Each TS bank contains seven registers for date/time information and one TSx_Flags register to indicate which event triggered this timestamp.

The MAX31334 can be configured to record timestamps on these events:

- Rising/falling edge (configurable) on DIN pin
- Supply switch from VCC to VBAT
- Supply switch from VBAT to VCC
- VBAT voltage drops below VBATLOW level (2V)

The part can either be configured to record only the first four timestamps and not record any subsequent events (TSOW = 0, *Figure 4*) or to keep recording every configured event and only keep the four latest events by overwriting the oldest event each time (TSOW = 1, *Figure 5*).

All the configuration related to timestamps can be found in the Timestamp_Config (05h) register. To start recording timestamps, the TSVLOW, TSPWM, TSDIN, TSOW bits need to be configured as desired and the TSE (timestamp enable) bit should be set to 1. The timestamp banks can be read through I^2C by accessing the corresponding register address. The TSR bit can be used to reset all the timestamp banks to 0 and start recording new timestamps again (if TSE = 1).

When the timestamp functionality is not used (TSE = 0), all 32 bytes of timestamp registers can be used as user RAM. After setting TSE = 0, write TSR = 1 to ensure RAM functionality.

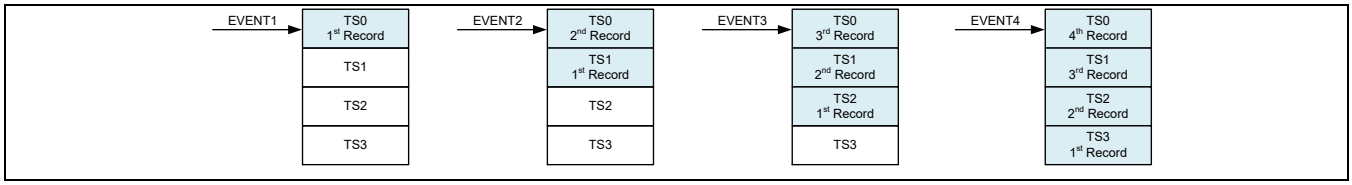


Figure 5. Timestamps with TSOW = 0

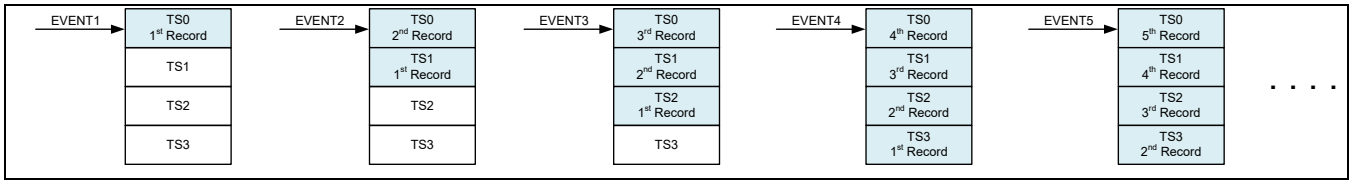


Figure 6. Timestamps with TSOW = 1

Applications Information

Power Supply Decoupling

To achieve the best results when using the device, decouple the V_{CC} and/or V_{BAT} power supplies with 0.1µF and/or 1.0µF capacitors. Use a high-quality ceramic surface-mount capacitor if possible. Surface-mount components minimize lead inductance which improves performance and ceramic capacitors tend to have adequate high-frequency response for decoupling applications.

Using Open-Drain Outputs

The $\overline{INTA}$ and $\overline{INTB}$/CLKO outputs are open-drain and therefore require an external pullup resistor to realize logic-high output levels. Pullup resistor values around 10kΩ are typical.

Battery Leakage Current

When the MAX31334 switches from V_{CC} to V_{BAT} supply, the DIN pin buffer internally operates on the V_{BAT} supply rail. If this pin is externally connected to an intermediate voltage level (between 0.7V and V_{BAT} - 0.7V), then there is a high leakage current (tens of microamperes) on the V_{BAT} supply. This scenario can occur when the system V_{CC} rail is discharging and the MAX31334 has switched to V_{BAT} supply, but the DIN pin is pulled up to the V_{CC} rail. The DIN pin can be pulled up to V_{BAT} instead of V_{CC} to ensure minimal negligible leakage when the MAX31334 is running on V_{BAT}.

SDA and SCL Pullup Resistors

SDA is an open-drain output and requires an external pullup resistor to realize a logic-high level. Because the device does not use clock cycle stretching, a controller using either an open-drain output with a pullup resistor or CMOS output driver (push-pull) could be used for SCL.

Register Map

RC34_REGS

ADDRESS	NAME	MSB							LSB
RTC_REG									
0x00	STATUS[7:0]	PSDECT	OSF	PFAIL	VBATLOW	DIF	TIF	A2F	A1F
0x01	INT_EN[7:0]	–	DOSF	PFAILE	VBATLOWIE	DIE	TIE	A2IE	A1IE
0x02	RTC_RESET[7:0]	–	–	–	–	–	–	–	SWRST
0x03	RTC_CONFIG1[7:0]	–	–	A1AC[1:0]		DIP	–	I2C_TIMEOUT	EN_OSC
0x04	RTC_CONFIG2[7:0]	SLST	–	–	DSE	DDB	ENCLKO	CLKO_HZ[1:0]	
0x05	TIMESTAMP_CONFIG[7:0]	–	–	TSVLOW	TSPWM	TSDIN	TSOW	TSR	TSE
0x06	TIMER_CONFIG[7:0]	–	–	–	TE	TPAUSE	TRPT	TFS[1:0]	
0x07	SLEEP_CONFIG[7:0]	SLP	WSTO[2:0]			DWE	TWE	A2WE	A1WE

ADDRESS	NAME	MSB							LSB
0x08	SECONDS_1_128[7:0]	–	_1_2s	_1_4s	_1_8s	_1_16s	_1_32s	_1_64s	_1_128s
0x09	SECONDS[7:0]	–	SEC_10[2:0]			SECONDS[3:0]			
0x0A	MINUTES[7:0]	–	MIN_10[2:0]			MINUTES[3:0]			
0x0B	HOURS[7:0]	–	F_24_12	HR_20_AM_PM	HR_10	HOUR[3:0]			
0x0C	DAY[7:0]	–	–	–	–	–	DAY[2:0]		
0x0D	DATE[7:0]	–	–	DATE_10[1:0]		DATE[3:0]			
0x0E	MONTH[7:0]	CENTURY	–	–	MONTH_10	MONTH[3:0]			
0x0F	YEAR[7:0]	YEAR_10[3:0]				YEAR[3:0]			
0x10	ALM1_SEC[7:0]	A1M1	A1_SEC_10[2:0]			A1_SECONDS[3:0]			
0x11	ALM1_MIN[7:0]	A1M2	A1_MIN_10[2:0]			A1_MINUTES[3:0]			
0x12	ALM1_HRS[7:0]	A1M3	–	A1_HR_20_AM_PM	A1_HR_10	A1_HOUR[3:0]			
0x13	ALM1_DAY_DATE[7:0]	A1M4	A1_DY_DT_MATCH	A1_DATE_10[1:0]		A1_DAY_DATE[3:0]			
0x14	ALM1_MON[7:0]	A1M5	A1M6	–	A1_MONTH_10	A1_MONTH[3:0]			
0x15	ALM1_YEAR[7:0]	A1_YEAR_10[3:0]				A1_YEAR[3:0]			
0x16	ALM2_MIN[7:0]	A2M2	A2_MIN_10[2:0]			A2_MINUTES[3:0]			
0x17	ALM2_HRS[7:0]	A2M3	–	A2_HR_20_AM_PM	A2_HR_10	A2_HOUR[3:0]			
0x18	ALM2_DAY_DATE[7:0]	A2M4	A2_DY_DT_MATCH	A2_DATE_10[1:0]		A2_DAY_DATE[3:0]			
0x19	TIMER_COUNT2[7:0]	TIMER_COUNT[15:8]							
0x1A	TIMER_COUNT1[7:0]	TIMER_COUNT[7:0]							
0x1B	TIMER_INIT2[7:0]	TIMER_INIT[15:8]							
0x1C	TIMER_INIT1[7:0]	TIMER_INIT[7:0]							

ADDRESS	NAME	MSB							LSB
0x1D	PWR_MGMT[7:0]	–	–	–	–	EN_VBAT_DETECT	PFVT	VBACK_SEL	MANUAL_SEL
0x1E	TRICKLE_REG[7:0]	–	–	–	–	TRICKLE[2:0]			EN_TRICKLE
0x20	OFFSET_HIGH[7:0]	COMPWORD[15:8]							
0x21	OFFSET_LOW[7:0]	COMPWORD[7:0]							
TS_RAM_REG									
0x30	TS0_SEC_1_128[7:0]	–	_1_2s	_1_4s	_1_8s	_1_16s	_1_32s	_1_64s	_1_128s
0x31	TS0_SEC[7:0]	–	SEC_10[2:0]			SEC[3:0]			
0x32	TS0_MIN[7:0]	–	MIN_10[2:0]			MIN[3:0]			
0x33	TS0_HOUR[7:0]	–	F_24_12	HR_20_AM_PM	HR_10	HOUR[3:0]			
0x34	TS0_DATE[7:0]	–	–	DATE_10[1:0]		DATE[3:0]			
0x35	TS0_MONTH[7:0]	CENTURY	–	–	MONTH_10	MONTH[3:0]			
0x36	TS0_YEAR[7:0]	YEAR_10[3:0]				YEAR[3:0]			
0x37	TS0_FLAGS[7:0]	–	–	–	–	VLOWF	VBATF	VCCF	DINF
0x38	TS1_SEC_1_128[7:0]	–	_1_2s	_1_4s	_1_8s	_1_16s	_1_32s	_1_64s	_1_128s
0x39	TS1_SEC[7:0]	–	SEC_10[2:0]			SEC[3:0]			
0x3A	TS1_MIN[7:0]	–	MIN_10[2:0]			MIN[3:0]			
0x3B	TS1_HOUR[7:0]	–	F_24_12	HR_20_AM_PM	HR_10	HOUR[3:0]			
0x3C	TS1_DATE[7:0]	–	–	DATE_10[1:0]		DATE[3:0]			
0x3D	TS1_MONTH[7:0]	CENTURY	–	–	MONTH_10	MONTH[3:0]			
0x3E	TS1_YEAR[7:0]	YEAR_10[3:0]				YEAR[3:0]			
0x3F	TS1_FLAGS[7:0]	–	–	–	–	VLOWF	VBATF	VCCF	DINF

ADDRESS	NAME	MSB							LSB
0x40	TS2_SEC_1_128[7:0]	–	_1_2s	_1_4s	_1_8s	_1_16s	_1_32s	_1_64s	_1_128s
0x41	TS2_SEC[7:0]	–	SEC_10[2:0]			SEC[3:0]			
0x42	TS2_MIN[7:0]	–	MIN_10[2:0]			MIN[3:0]			
0x43	TS2_HOUR[7:0]	–	F_24_12	HR_20_AM_PM	HR_10	HOUR[3:0]			
0x44	TS2_DATE[7:0]	–	–	DATE_10[1:0]		DATE[3:0]			
0x45	TS2_MONTH[7:0]	CENTURY	–	–	MONTH_10	MONTH[3:0]			
0x46	TS2_YEAR[7:0]	YEAR_10[3:0]				YEAR[3:0]			
0x47	TS2_FLAGS[7:0]	–	–	–	–	VLOWF	VBATF	VCCF	DINF
0x48	TS3_SEC_1_128[7:0]	–	_1_2s	_1_4s	_1_8s	_1_16s	_1_32s	_1_64s	_1_128s
0x49	TS3_SEC[7:0]	–	SEC_10[2:0]			SEC[3:0]			
0x4A	TS3_MIN[7:0]	–	MIN_10[2:0]			MIN[3:0]			
0x4B	TS3_HOUR[7:0]	–	F_24_12	HR_20_AM_PM	HR_10	HOUR[3:0]			
0x4C	TS3_DATE[7:0]	–	–	DATE_10[1:0]		DATE[3:0]			
0x4D	TS3_MONTH[7:0]	CENTURY	–	–	MONTH_10	MONTH[3:0]			
0x4E	TS3_YEAR[7:0]	YEAR_10[3:0]				YEAR[3:0]			
0x4F	TS3_FLAGS[7:0]	–	–	–	–	VLOWF	VBATF	VCCF	DINF

Register Details

STATUS (0x0)

Interrupt Status Register

BIT	7	6	5	4	3	2	1	0
Field	PSDECT	OSF	PFAIL	VBATLOW	DIF	TIF	A2F	A1F

Reset	0b0	0b1	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	Read, Ext	Read, Ext	Read, Ext	Read, Ext	Read, Ext	Read, Ext	Read, Ext	Read, Ext

BITFIELD	BITS	DESCRIPTION	DECODE
PSDECT	7	Main supply source indication. This bit is not cleared after a successful I²C read.	0x0: Device is running on VCC 0x1: Device is running on VBAT
OSF	6	Oscillator stop flag. This bit is not cleared after a successful I²C read.	0x0: Oscillator is running (or DOSF = 1) 0x1: Oscillator has stopped
PFAIL	5	Power Fail flag. This bit is cleared automatically after a successful I²C read.	0x0: No power fail condition on V_{CC} 0x1: There is a power fail condition on V_{CC}. After an initial power fail condition occurs, if the condition does not persist, this bit can only be cleared by reading the Status register.
VBATLOW	4	VBAT Low Flag. This bit is cleared automatically after a successful I²C read.	
DIF	3	Digital (DIN) interrupt flag. This bit is cleared automatically after a successful I²C read.	
TIF	2	Timer interrupt flag. This bit is cleared automatically after a successful I²C read.	
A2F	1	Alarm2 interrupt flag. This bit is cleared automatically after a successful I²C read.	
A1F	0	Alarm1 Interrupt flag. This bit is cleared automatically after a successful I²C read.	0x0: Set to zero when RTC time doesn't match to alarm1 register. 0x1: Set to 1 when RTC time matches the alarm1 register. When this is set to 1, and A1IE = 1, an interrupt is generated on pin INTAb/INTBb.

INT_EN (0x1)

Interrupt Enable Register

BIT	7	6	5	4	3	2	1	0
Field	–	DOSF	PFAILE	VBATLOWIE	DIE	TIE	A2IE	A1IE
Reset	–	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	–	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
DOSF	6	Disable oscillator flag	0x0: Allow the OSF to indicate the oscillator status. 0x1: Disable the oscillator flag, irrespective of the oscillator status.
PFAILE	5	Power fail Interrupt enable	0x0: Disable PFAIL flag and interrupt 0x1: Enable PFAIL flag and interrupt
VBATLOWIE	4	VBAT Low Interrupt Enable	0x0: Disable VBAT Low flag and interrupt 0x1: Enable VBAT Low flag and interrupt

BITFIELD	BITS	DESCRIPTION	DECODE
DIE	3	Digital (DIN) interrupt enable	0x0: Disable DIN flag and interrupt 0x1: Enable DIN flag and interrupt
TIE	2	Timer interrupt enable	0x0: Disable Timer flag and interrupt 0x1: Enable Timer flag and interrupt
A2IE	1	Alarm2 interrupt enable	0x0: Disable Alarm2 flag and interrupt 0x1: Enable Alarm2 flag and interrupt
A1IE	0	Alarm1 interrupt enable	0x0: Disable Alarm1 flag and interrupt 0x1: Enable Alarm1 flag and interrupt

RTC_RESET (0x2)

RTC Software Reset Register

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	SWRST
Reset	–	–	–	–	–	–	–	0b0
Access Type	–	–	–	–	–	–	–	Write, Read, Ext

BITFIELD	BITS	DESCRIPTION	DECODE
SWRST	0	Active high software reset bit	0x0: Device is in normal mode. 0x1: Resets the digital block and the I²C programmable registers except for RAM registers and RTC_reset.SWRST. Oscillator is disabled

RTC_CONFIG1 (0x3)

RTC Configuration Register 1

BIT	7	6	5	4	3	2	1	0
Field	–	–	A1AC[1:0]		DIP	–	I2C_TIMEOUT	EN_OSC
Reset	–	–	0b00		0b0	–	0b1	0b1
Access Type	–	–	Write, Read		Write, Read	–	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
A1AC	5:4	Alarm1 Auto Clear	0x0: Alarm1 flag and interrupt can only be cleared by reading Status register through I²C 0x1: Alarm1 flag and interrupt are cleared ~10ms after assertion 0x2: Alarm1 flag and interrupt are cleared ~500ms after assertion 0x3: Alarm1 flag and interrupt are cleared ~5s after assertion. This option should not be used when Alarm1 is set to OncePerSec.
DIP	3	Digital (DIN) interrupt polarity	0x0: Interrupt triggers on falling edge of DIN input. 0x1: Interrupt triggers on rising edge of DIN input.

BITFIELD	BITS	DESCRIPTION	DECODE
I2C_TIMEOUT	1	I²C timeout enable	0x0: Disables I²C timeout 0x1: Enables I²C timeout
EN_OSC	0	Active-high enable for the crystal oscillator	0x0: Disable oscillator 0x1: Enable oscillator

RTC_CONFIG2 (0x4)

RTC Configuration Register 2

BIT	7	6	5	4	3	2	1	0
Field	SLST	–	–	DSE	DDB	ENCLKO	CLKO_HZ[1:0]	
Reset	0b0	–	–	0b0	0b0	0b0	0b11	
Access Type	Read, Ext	–	–	Write, Read	Write, Read	Write, Read	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
SLST	7	Sleep State	0x0: SLST = 0 indicates the PSW SM is not in SLEEP. 0x1: SLST = 1 indicates the PSW SM is in SLEEP.
DSE	4	Digital (DIN) pin Sleep Entry Enable	0x0: DIN pin cannot be used to enter SLEEP (SLEEP entry is only possible by writing SLP = 1 through I²C). 0x1: DIN pin can be used to enter SLEEP.
DDB	3	Digital (DIN) pin Debounce Enable	0x0: No debounce on DIN pin. 0x1: 50ms debounce on DIN pin enabled.
ENCLKO	2	CLKOUT enable	0x0: Sets INTBb/CLKOUT pin as INTBb (interrupt). Alarm1 interrupt occurs on INTBb pin. 0x1: Sets INTBb/CLKOUT pin as CLKO (clock output). Alarm1 interrupt occurs on INTAb pin.
CLKO_HZ	1:0	Set output clock frequency on INTBb/CLKOUT pin	0x0: 1Hz 0x1: 64Hz 0x2: 1.024kHz 0x3: 32kHz (uncompensated)

TIMESTAMP_CONFIG (0x5)

Timestamp Configuration Register

BIT	7	6	5	4	3	2	1	0
Field	–	–	TSVLOW	TSPWM	TSDIN	TSOW	TSR	TSE
Reset	–	–	0b0	0b0	0b0	0b1	0b0	0b0
Access Type	–	–	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read, Pulse	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
TSVLOW	5	Record Timestamp on VBATLOW detection	0x0: Disable 0x1: Enable

BITFIELD	BITS	DESCRIPTION	DECODE
TSPWM	4	Record Timestamp on power supply switch (VCC ⇔ VBAT)	0x0: Disable 0x1: Enable
TSDIN	3	Record Timestamp on DIN transition. Polarity controlled by DIP bitfield in RTC_Config1 register.	0x0: Disable 0x1: Enable
TSOW	2	Timestamp Overwrite	0x0: Four timestamps are recorded (TS0 → ... → TS3). Latest timestamp is always stored in the TS0 bank. Further TS trigger events do not record timestamps. Reset TS block using TSR bit to clear all timestamps and start recording new TS again. 0x1: More than four timestamps are recorded by overwriting oldest timestamp. Latest timestamp is always stored in the TS0 bank and the earliest timestamp is stored in the TS3 bank. Reset using the TSR bit to clear all timestamps and start recording again.
TSR	1	Timestamp Registers Reset	0x0: No effect 0x1: All Timestamp registers are reset to 0x00. If TSE = 1, timestamp recording starts again.
TSE	0	Timestamp Enable	0x0: Timestamp function disabled. All Timestamp registers can be used as user RAM. Timestamp block needs to be reset using TSR bit before these registers are used as user RAM. 0x1: Timestamp function enabled.

TIMER_CONFIG (0x6)

Countdown Timer Configuration Register

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	TE	TPAUSE	TRPT	TFS[1:0]	
Reset	–	–	–	0b0	0b0	0b1	0b00	
Access Type	–	–	–	Write, Read	Write, Read	Write, Read	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
TE	4	Timer enable. Also see TPAUSE field for additional information.	0x0: Timer is reset. New timer countdown value (Timer_Init) can be programmed in this state. Note: In this state, ensure TPAUSE is also programmed to 0, if TPAUSE was set to 1 earlier 0x1: Timer starts counting down from the value programmed in Timer_Init.
TPAUSE	3	Timer Pause. This field is valid only when TE = 1. When TE is programmed to 0, this field must also be reset to 0. Details about Timer Pause are explained in detail in the *Countdown Timer* section.	0x0: Timer continues to count down from the paused count value as per programming. 0x1: Timer is paused, however the count value is retained. When this bit is reset back to 0, count down continues from the paused value.
TRPT	2	Timer repeat mode. Controls the timer interrupt function.	0x0: Countdown timer halts once it reaches zero. 0x1: Countdown timer reloads the value from the timer initial register upon reaching zero and restarts counting.
TFS	1:0	Timer frequency selection	0x0: 1024Hz 0x1: 256Hz

BITFIELD	BITS	DESCRIPTION	DECODE
			0x2: 64Hz 0x3: 16Hz

SLEEP_CONFIG (0x7)

Timestamp Configuration Register

BIT	7	6	5	4	3	2	1	0
Field	SLP	WSTO[2:0]			DWE	TWE	A2WE	A1WE
Reset	0b0	0x0			0b0	0b0	0b0	0b0
Access Type	Write, Read, Dual	Write, Read			Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
SLP	7	Sleep Enable	0x0: Write SLP = 0 to bring the SM back to ACTIVE. 0x1: Write SLP = 1 to initiate entry into SLEEP (through WAIT). This transition to the next state only happens when at least one wakeup source (DWE, TWE, A1WE, A2WE) is enabled.
WSTO	6:4	Wait State Timeout This bitfield must be set before writing SLP = 1 if a finite WAIT duration is desired before entering SLEEP.	0x0: 0ms 0x1: 7.8ms 0x2: 15.6ms 0x3: 23.4ms 0x4: 31.2ms 0x5: 39.0ms 0x6: 46.8ms 0x7: 54.6ms
DWE	3	DIN Wakeup Enable	0x0: DIN Wakeup disabled. 0x1: DIN Wakeup enabled. When a transition on DIN pin is detected (polarity based on DIP), the PSW SM transitions from SLEEP to ACTIVE (PSW = ON).
TWE	2	Timer Wakeup Enable	0x0: Timer Wakeup disabled. 0x1: Timer Wakeup enabled. When Countdown Timer elapses (Timer Count = 0), the PSW SM transitions from SLEEP to ACTIVE (PSW = ON).
A2WE	1	Alarm2 Wakeup Enable	0x0: Alarm2 Wakeup disabled. 0x1: Alarm2 Wakeup enabled. When Alarm2 match condition occurs, the PSW SM transitions from SLEEP to ACTIVE (PSW = ON).
A1WE	0	Alarm1 Wakeup Enable	0x0: Alarm1 Wakeup disabled. 0x1: Alarm1 Wakeup enabled. When Alarm1 match condition occurs, the PSW SM transitions from SLEEP to ACTIVE (PSW = ON).

SECONDS_1_128 (0x8)

1/128 Seconds Register

BIT	7	6	5	4	3	2	1	0
Field	–	_1_2s	_1_4s	_1_8s	_1_16s	_1_32s	_1_64s	_1_128s

Reset	–	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	–	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION
_1_2s	6	
_1_4s	5	
_1_8s	4	
_1_16s	3	
_1_32s	2	
_1_64s	1	
_1_128s	0	

SECONDS (0x9)

Seconds Configuration Register

BIT	7	6	5	4	3	2	1	0
Field	–	SEC_10[2:0]			SECONDS[3:0]			
Reset	–	0b000			0x0			
Access Type	–	Write, Read, Dual			Write, Read, Dual			

BITFIELD	BITS	DESCRIPTION
SEC_10	6:4	RTC seconds in multiples of 10
SECONDS	3:0	RTC seconds value.

MINUTES (0xA)

Minutes Configuration Register

BIT	7	6	5	4	3	2	1	0
Field	–	MIN_10[2:0]			MINUTES[3:0]			
Reset	–	0b000			0x0			
Access Type	–	Write, Read, Dual			Write, Read, Dual			

BITFIELD	BITS	DESCRIPTION
MIN_10	6:4	RTC minutes in multiples of 10
MINUTES	3:0	RTC minutes value

HOURS (0xB)

Hours Configuration Register

BIT	7	6	5	4	3	2	1	0
Field	–	F_24_12	HR_20_AM_PM	HR_10	HOUR[3:0]			
Reset	–	0b0	0b0	0b0	0x0			
Access Type	–	Write, Read	Write, Read, Dual	Write, Read, Dual	Write, Read, Dual			

BITFIELD	BITS	DESCRIPTION	DECODE
F_24_12	6	Sets RTC in 12-hr or 24-hr format	0x0: 24 hour format (Hours counts from 0 to 23) 0x1: 12 hour format (Hours counts from 1 to 12)
HR_20_AM_PM	5	In 12 hr format, this works as the AM/PM indicator. In 24 hr format, it is the RTC hours in multiples of 20 (BCD).	0x0: Indicates AM in 12-hr format. 0x1: Indicates PM in 12-hr format.
HR_10	4	RTC hours in multiples of 10 (BCD)	
HOUR	3:0	RTC hours value (BCD)	

DAY (0xC)

Day Configuration Register

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	DAY[2:0]		
Reset	–	–	–	–	–	0b001		
Access Type	–	–	–	–	–	Write, Read, Dual		

BITFIELD	BITS	DESCRIPTION
DAY	2:0	RTC days

DATE (0xD)

Date Configuration Register

BIT	7	6	5	4	3	2	1	0
Field	–	–	DATE_10[1:0]		DATE[3:0]			
Reset	–	–	0b00		0x1			
Access Type	–	–	Write, Read, Dual		Write, Read, Dual			

BITFIELD	BITS	DESCRIPTION
DATE_10	5:4	RTC date in multiples of 10 (BCD)
DATE	3:0	RTC date (BCD)

MONTH (0xE)

Month Configuration Register

BIT	7	6	5	4	3	2	1	0
Field	CENTURY	–	–	MONTH_10	MONTH[3:0]			
Reset	0b0	–	–	0b0	0x1			
Access Type	Write, Read, Dual	–	–	Write, Read, Dual	Write, Read, Dual			

BITFIELD	BITS	DESCRIPTION	DECODE
CENTURY	7	Century bit	0x0: Year is in 21st century 0x1: Year is in 22nd century
MONTH_10	4	RTC month in multiples of 10 (BCD)	
MONTH	3:0	RTC months (BCD)	

YEAR (0xF)

Year Configuration Register

BIT	7	6	5	4	3	2	1	0
Field	YEAR_10[3:0]				YEAR[3:0]			
Reset	0x0				0x0			
Access Type	Write, Read, Dual				Write, Read, Dual			

BITFIELD	BITS	DESCRIPTION
YEAR_10	7:4	RTC year multiples of 10 (BCD)

BITFIELD	BITS	DESCRIPTION
YEAR	3:0	RTC years (BCD)

ALM1_SEC (0x10)

Alarm1 Seconds Configuration Register

BIT	7	6	5	4	3	2	1	0
Field	A1M1	A1_SEC_10[2:0]			A1_SECONDS[3:0]			
Reset	0b0	0b000			0x0			
Access Type	Write, Read	Write, Read			Write, Read			

BITFIELD	BITS	DESCRIPTION
A1M1	7	Alarm1 mask bit for seconds
A1_SEC_10	6:4	Alarm1 seconds in multiples of 10
A1_SECONDS	3:0	Alarm1 seconds

ALM1_MIN (0x11)

Alarm1 Minutes Configuration Register

BIT	7	6	5	4	3	2	1	0
Field	A1M2	A1_MIN_10[2:0]			A1_MINUTES[3:0]			
Reset	0b0	0b000			0x0			
Access Type	Write, Read	Write, Read			Write, Read			

BITFIELD	BITS	DESCRIPTION
A1M2	7	Alarm1 mask bit for minutes
A1_MIN_10	6:4	Alarm1 minutes in multiples of 10
A1_MINUTES	3:0	Alarm1 minutes

ALM1_HRS (0x12)

Alarm1 Hours Configuration Register

BIT	7	6	5	4	3	2	1	0

Field	A1M3	–	A1_HR_20_AM_PM	A1_HR_10	A1_HOUR[3:0]
Reset	0b0	–	0b0	0b0	0x0
Access Type	Write, Read	–	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
A1M3	7	Alarm1 mask bit for hours	
A1_HR_20_AM_PM	5	In 12 hr format, this works as the AM/PM indicator. In 24 hr format, it is the Alarm1 hours in multiples of 20 (BCD).	0x0: Indicates AM in 12-hr format. 0x1: Indicates PM in 12-hr format.
A1_HR_10	4	Alarm1 hours in multiples of 10	
A1_HOUR	3:0	Alarm1 hours	

ALM1_DAY_DATE (0x13)

Alarm1 Day/Date Configuration Register

BIT	7	6	5	4	3	2	1	0
Field	A1M4	A1_DY_DT_MATCH	A1_DATE_10[1:0]		A1_DAY_DATE[3:0]			
Reset	0b0	0b0	0b00		0x0			
Access Type	Write, Read	Write, Read	Write, Read		Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
A1M4	7	Alarm1 mask bit for day/date	
A1_DY_DT_MATCH	6		0x0: Alarm when date match 0x1: Alarm when day match
A1_DATE_10	5:4	Alarm1 date in multiples of 10	
A1_DAY_DATE	3:0	Alarm1 day/date	

ALM1_MON (0x14)

Alarm1 Month Configuration Register

BIT	7	6	5	4	3	2	1	0
Field	A1M5	A1M6	–	A1_MONTH_10	A1_MONTH[3:0]			
Reset	0b0	0b0	–	0b0	0x0			
Access Type	Write, Read	Write, Read	–	Write, Read	Write, Read			

BITFIELD	BITS	DESCRIPTION
A1M5	7	Alarm1 mask bit for month
A1M6	6	Alarm1 mask bit for year
A1_MONTH_10	4	Alarm1 months in multiples of 10
A1_MONTH	3:0	Alarm1 months

ALM1_YEAR (0x15)

Alarm1 Year Configuration Register

BIT	7	6	5	4	3	2	1	0
Field	A1_YEAR_10[3:0]				A1_YEAR[3:0]			
Reset	0x0				0x0			
Access Type	Write, Read				Write, Read			

BITFIELD	BITS	DESCRIPTION
A1_YEAR_10	7:4	Alarm1 year in multiples of 10
A1_YEAR	3:0	Alarm1 years

ALM2_MIN (0x16)

Alarm2 Minutes Configuration Register

BIT	7	6	5	4	3	2	1	0
Field	A2M2	A2_MIN_10[2:0]			A2_MINUTES[3:0]			
Reset	0b0	0b000			0x0			
Access Type	Write, Read	Write, Read			Write, Read			

BITFIELD	BITS	DESCRIPTION
A2M2	7	Alarm2 mask bit for minutes **DY/DT** | **ALARM 2 MASK BITS (BIT 7)** | **ALARM RATE** **A2M4** | **A2M3** | **A2M2**

BITFIELD	BITS	DESCRIPTION
		X 1 1 1 Once per Minute X 1 1 0 Minute Match. X 1 0 0 H&M Match 0 0 0 0 Date&H&M Match 1 0 0 0 Day&H&M Match
A2_MIN_10	6:4	Alarm2 minutes in multiples of 10
A2_MINUTES	3:0	Alarm2 minutes

ALM2_HRS (0x17)

Alarm2 Hours Configuration Register

BIT	7	6	5	4	3	2	1	0
Field	A2M3	–	A2_HR_20_AM_PM	A2_HR_10	A2_HOUR[3:0]			
Reset	0b0	–	0b0	0b0	0x0			
Access Type	Write, Read	–	Write, Read	Write, Read	Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
A2M3	7	Alarm2 mask bit for hours	
A2_HR_20_AM_PM	5	In 12 hr format, this works as the AM/PM indicator. In 24 hr format, it is the Alarm2 hours in multiples of 20 (BCD).	0x0: Indicates AM in 12-hr format. 0x1: Indicates PM in 12-hr format.
A2_HR_10	4	Alarm2 hours in multiples of 10	
A2_HOUR	3:0	Alarm2 hours	

ALM2_DAY_DATE (0x18)

Alarm2 Day/Date Configuration Register

BIT	7	6	5	4	3	2	1	0
Field	A2M4	A2_DY_DT_MATCH	A2_DATE_10[1:0]		A2_DAY_DATE[3:0]			
Reset	0b0	0b0	0b00		0x0			
Access Type	Write, Read	Write, Read	Write, Read		Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
A2M4	7	Alarm2 mask bit for day/date	
A2_DY_DT_MATCH	6	This bit selects alarm when day match or date match.	0x0: Alarm when date match 0x1: Alarm when day match
A2_DATE_10	5:4	Alarm2 date in multiples of 10	
A2_DAY_DATE	3:0	Alarm2 day/date	

TIMER_COUNT2 (0x19)

Countdown Timer Value Register

BIT	7	6	5	4	3	2	1	0
Field	TIMER_COUNT[15:8]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
TIMER_COUNT	7:0	Count down timer current count value. The current timer value can be read by reading this register.

TIMER_COUNT1 (0x1A)

Countdown Timer Value Register

BIT	7	6	5	4	3	2	1	0
Field	TIMER_COUNT[7:0]							
Reset	0x00							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
TIMER_COUNT	7:0	Count down timer current count value. The current timer value can be read by reading this register.

TIMER_INIT2 (0x1B)

Countdown Timer Initialization Register

BIT	7	6	5	4	3	2	1	0

Field	TIMER_INIT[15:8]
Reset	0x00
Access Type	Write, Read

BITFIELD	BITS	DESCRIPTION
TIMER_INIT	7:0	Count down timer initial value. The timer is loaded with the contents of this register when it reaches to zero in repeat mode.

TIMER_INIT1 (0x1C)

Countdown Timer Initialization Register

BIT	7	6	5	4	3	2	1	0
Field	TIMER_INIT[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
TIMER_INIT	7:0	Count down timer initial value. The timer is loaded with the contents of this register when it reaches to zero in repeat mode.

PWR_MGMT (0x1D)

Power Management Configuration Register

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	EN_VBAT_DETECT	PFVT	VBACK_SEL	MANUAL_SEL
Reset	–	–	–	–	0b0	0b0	0b0	0b0
Access Type	–	–	–	–	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
EN_VBAT_DETECT	3	Enable for Battery Voltage Detector	0x0: Turn-off Battery Voltage Detector 0x1: Turn-on Battery Voltage Detector
PFVT	2	Power fail threshold voltage. Sets analog comparator threshold voltage. Require D_MAN_SEL = 0 for this setting to have effect.	0x0: 1.5V 0x1: 2.0V
VBACK_SEL	1	Backup battery select. Require D_MANUAL_SEL = 1 for this bit to have effect. **Can only select**	0x0: Use V_{CC} as supply. 0x1: Use V_{BAT} as supply.

BITFIELD	BITS	DESCRIPTION	DECODE
		backup battery (0x1), when VCC < VBAT. **In Test Mode, if "D_VBAT_TEST = 1", VBAT can be selected even VCC > VBAT.**	
MANUAL_SEL	0	When this bit is low, input control block decides which supply to use. When this bit is high, user can manually select V_{BACKUP} as supply only when V_{CC} is lower than V_{BACKUP}.	0x0: Circuit decides whether to use V_{CC} or V_{BAT} as supply. 0x1: User decides whether to use V_{CC} or V_{BAT} as supply by setting D_VBAT_SEL bit.

TRICKLE_REG (0x1E)

Trickle Charger Configuration Register

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	TRICKLE[2:0]			EN_TRICKLE
Reset	–	–	–	–	0b000			0b0
Access Type	–	–	–	–	Write, Read			Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
TRICKLE	3:1	Sets the charging path for trickle charger.	0x0: 3kΩ in series with a Schottky diode 0x1: 3kΩ in series with a Schottky diode 0x2: 6kΩ in series with a Schottky diode 0x3: 11kΩ in series with a Schottky diode 0x4: 3kΩ in series with a diode + Schottky diode 0x5: 3kΩ in series with a diode + Schottky diode 0x6: 6kΩ in series with a diode + Schottky diode 0x7: 11kΩ in series with a diode + Schottky diode
EN_TRICKLE	0	Trickle charger enable.	0x0: Trickle charger disabled 0x1: Trickle charger enabled

OFFSET_HIGH (0x20)

Offset Configuration Register High

BIT	7	6	5	4	3	2	1	0
Field	COMPWORD[15:8]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COMPWORD	7:0	Compensation Words (2's complement) provides the option to digitally tune the oscillator output frequency by applying correction pulses. It can be used for accuracy tuning, aging

BITFIELD	BITS	DESCRIPTION
		offset, or temperature compensation. Resolution = 0.477ppm If there are no writes to these bits, the factory trim values are used instead.

OFFSET_LOW (0x21)

Offset Configuration Register Low

BIT	7	6	5	4	3	2	1	0
Field	COMPWORD[7:0]							
Reset	0x00							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
COMPWORD	7:0	Compensation Words (2's complement) provides the option to digitally tune the oscillator output frequency by applying correction pulses. It can be used for accuracy tuning, aging offset, or temperature compensation. Resolution = 0.477ppm If there are no writes to these bits, the factory trim values are used instead.

TS0_SEC_1_128 (0x30)

BIT	7	6	5	4	3	2	1	0
Field	–	_1_2s	_1_4s	_1_8s	_1_16s	_1_32s	_1_64s	_1_128s
Reset	–	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	–	Write, Read	Write, Read	Write, Read, Dual	Write, Read	Write, Read	Write, Read	Write, Read, Dual

BITFIELD	BITS	DESCRIPTION
_1_2s	6	
_1_4s	5	
_1_8s	4	
_1_16s	3	
_1_32s	2	
_1_64s	1	

BITFIELD	BITS	DESCRIPTION
_1_128s	0	

TS0_SEC (0x31)

BIT	7	6	5	4	3	2	1	0
Field	–	SEC_10[2:0]			SEC[3:0]			
Reset	–	0b000			0x0			
Access Type	–	Write, Read, Dual			Write, Read, Dual			

BITFIELD	BITS	DESCRIPTION
SEC_10	6:4	
SEC	3:0	

TS0_MIN (0x32)

BIT	7	6	5	4	3	2	1	0
Field	–	MIN_10[2:0]			MIN[3:0]			
Reset	–	0b000			0x0			
Access Type	–	Write, Read			Write, Read, Dual			

BITFIELD	BITS	DESCRIPTION
MIN_10	6:4	
MIN	3:0	

TS0_HOUR (0x33)

BIT	7	6	5	4	3	2	1	0
Field	–	F_24_12	HR_20_AM_PM	HR_10	HOUR[3:0]			
Reset	–	0b0	0b0	0b0	0x0			
Access Type	–	Write, Read	Write, Read, Dual	Write, Read, Dual	Write, Read, Dual			

BITFIELD	BITS	DESCRIPTION
F_24_12	6	
HR_20_AM_PM	5	
HR_10	4	
HOUR	3:0	

TS0_DATE (0x34)

BIT	7	6	5	4	3	2	1	0
Field	–	–	DATE_10[1:0]		DATE[3:0]			
Reset	–	–	0b00		0x0			
Access Type	–	–	Write, Read		Write, Read, Dual			

BITFIELD	BITS	DESCRIPTION
DATE_10	5:4	
DATE	3:0	

TS0_MONTH (0x35)

BIT	7	6	5	4	3	2	1	0
Field	CENTURY	–	–	MONTH_10	MONTH[3:0]			
Reset	0b0	–	–	0b0	0x0			
Access Type	Write, Read	–	–	Write, Read	Write, Read, Dual			

BITFIELD	BITS	DESCRIPTION
CENTURY	7	
MONTH_10	4	
MONTH	3:0	

TS0_YEAR (0x36)

BIT	7	6	5	4	3	2	1	0

Field	YEAR_10[3:0]	YEAR[3:0]
Reset	0x0	0x0
Access Type	Write, Read	Write, Read, Dual

BITFIELD	BITS	DESCRIPTION
YEAR_10	7:4	
YEAR	3:0	

TS0_FLAGS (0x37)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	VLOWF	VBATF	VCCF	DINF
Reset	–	–	–	–	0b0	0b0	0b0	0b0
Access Type	–	–	–	–	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
VLOWF	3	Indicates if this Timestamp was triggered by VLOW detection	0x0: Not triggered by VLOW detection 0x1: Triggered by VLOW detection
VBATF	2	Indicates if this Timestamp was triggered by VCC -> VBAT switch	0x0: Not triggered by VCC -> VBAT switch 0x1: Triggered by VCC -> VBAT switch
VCCF	1	Indicates if this Timestamp was triggered by VBAT -> VCC switch	0x0: Not triggered by VBAT -> VCC switch 0x1: Triggered by VBAT -> VCC switch
DINF	0	Indicates if this Timestamp was triggered by DIN transition	0x0: Not triggered by DIN 0x1: Triggered by DIN

TS1_SEC_1_128 (0x38)

BIT	7	6	5	4	3	2	1	0
Field	–	_1_2s	_1_4s	_1_8s	_1_16s	_1_32s	_1_64s	_1_128s
Reset	–	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	–	Write, Read	Write, Read	Write, Read, Dual	Write, Read	Write, Read	Write, Read	Write, Read, Dual

BITFIELD	BITS	DESCRIPTION
_1_2s	6	
_1_4s	5	
_1_8s	4	
_1_16s	3	
_1_32s	2	
_1_64s	1	
_1_128s	0	

TS1_SEC (0x39)

BIT	7	6	5	4	3	2	1	0
Field	–	SEC_10[2:0]			SEC[3:0]			
Reset	–	0b000			0x0			
Access Type	–	Write, Read, Dual			Write, Read, Dual			

BITFIELD	BITS	DESCRIPTION
SEC_10	6:4	
SEC	3:0	

TS1_MIN (0x3A)

BIT	7	6	5	4	3	2	1	0
Field	–	MIN_10[2:0]			MIN[3:0]			
Reset	–	0b000			0x0			
Access Type	–	Write, Read			Write, Read, Dual			

BITFIELD	BITS	DESCRIPTION
MIN_10	6:4	
MIN	3:0	

TS1_HOUR (0x3B)

BIT	7	6	5	4	3	2	1	0
Field	–	F_24_12	HR_20_AM_PM	HR_10	HOUR[3:0]			
Reset	–	0b0	0b0	0b0	0x0			
Access Type	–	Write, Read	Write, Read, Dual	Write, Read, Dual	Write, Read, Dual			

BITFIELD	BITS	DESCRIPTION
F_24_12	6	
HR_20_AM_PM	5	
HR_10	4	
HOUR	3:0	

TS1_DATE (0x3C)

BIT	7	6	5	4	3	2	1	0
Field	–	–	DATE_10[1:0]		DATE[3:0]			
Reset	–	–	0b00		0x0			
Access Type	–	–	Write, Read		Write, Read, Dual			

BITFIELD	BITS	DESCRIPTION
DATE_10	5:4	
DATE	3:0	

TS1_MONTH (0x3D)

BIT	7	6	5	4	3	2	1	0
Field	CENTURY	–	–	MONTH_10	MONTH[3:0]			
Reset	0b0	–	–	0b0	0x0			
Access Type	Write, Read	–	–	Write, Read	Write, Read, Dual			

BITFIELD	BITS	DESCRIPTION
CENTURY	7	
MONTH_10	4	
MONTH	3:0	

TS1_YEAR (0x3E)

BIT	7	6	5	4	3	2	1	0
Field	YEAR_10[3:0]				YEAR[3:0]			
Reset	0x0				0x0			
Access Type	Write, Read				Write, Read, Dual			

BITFIELD	BITS	DESCRIPTION
YEAR_10	7:4	
YEAR	3:0	

TS1_FLAGS (0x3F)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	VLOWF	VBATF	VCCF	DINF
Reset	–	–	–	–	0b0	0b0	0b0	0b0
Access Type	–	–	–	–	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
VLOWF	3	Indicates if this Timestamp was triggered by VLOW detection	0x0: Not triggered by VLOW detection 0x1: Triggered by VLOW detection
VBATF	2	Indicates if this Timestamp was triggered by VCC → VBAT switch	0x0: Not triggered by VCC → VBAT switch 0x1: Triggered by VCC → VBAT switch
VCCF	1	Indicates if this Timestamp was triggered by VBAT → VCC switch	0x0: Not triggered by VBAT → VCC switch 0x1: Triggered by VBAT → VCC switch
DINF	0	Indicates if this Timestamp was triggered by DIN transition	0x0: Not triggered by DIN 0x1: Triggered by DIN

TS2_SEC_1_128 (0x40)

BIT	7	6	5	4	3	2	1	0
Field	–	_1_2s	_1_4s	_1_8s	_1_16s	_1_32s	_1_64s	_1_128s
Reset	–	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	–	Write, Read	Write, Read	Write, Read, Dual	Write, Read	Write, Read	Write, Read	Write, Read, Dual

BITFIELD	BITS	DESCRIPTION
_1_2s	6	
_1_4s	5	
_1_8s	4	
_1_16s	3	
_1_32s	2	
_1_64s	1	
_1_128s	0	

TS2_SEC (0x41)

BIT	7	6	5	4	3	2	1	0
Field	–	SEC_10[2:0]			SEC[3:0]			
Reset	–	0b000			0x0			
Access Type	–	Write, Read, Dual			Write, Read, Dual			

BITFIELD	BITS	DESCRIPTION
SEC_10	6:4	
SEC	3:0	

TS2_MIN (0x42)

BIT	7	6	5	4	3	2	1	0
Field	–	MIN_10[2:0]			MIN[3:0]			

Reset	–	0b000	0x0
Access Type	–	Write, Read	Write, Read, Dual

BITFIELD	BITS	DESCRIPTION
MIN_10	6:4	
MIN	3:0	

TS2_HOUR (0x43)

BIT	7	6	5	4	3	2	1	0
Field	–	F_24_12	HR_20_AM_PM	HR_10	HOUR[3:0]			
Reset	–	0b0	0b0	0b0	0x0			
Access Type	–	Write, Read	Write, Read, Dual	Write, Read, Dual	Write, Read, Dual			

BITFIELD	BITS	DESCRIPTION
F_24_12	6	
HR_20_AM_PM	5	
HR_10	4	
HOUR	3:0	

TS2_DATE (0x44)

BIT	7	6	5	4	3	2	1	0
Field	–	–	DATE_10[1:0]		DATE[3:0]			
Reset	–	–	0b00		0x0			
Access Type	–	–	Write, Read		Write, Read, Dual			

BITFIELD	BITS	DESCRIPTION
DATE_10	5:4	
DATE	3:0	

TS2_MONTH (0x45)

BIT	7	6	5	4	3	2	1	0
Field	CENTURY	–	–	MONTH_10	MONTH[3:0]			
Reset	0b0	–	–	0b0	0x0			
Access Type	Write, Read	–	–	Write, Read	Write, Read, Dual			

BITFIELD	BITS	DESCRIPTION
CENTURY	7	
MONTH_10	4	
MONTH	3:0	

TS2_YEAR (0x46)

BIT	7	6	5	4	3	2	1	0
Field	YEAR_10[3:0]				YEAR[3:0]			
Reset	0x0				0x0			
Access Type	Write, Read				Write, Read, Dual			

BITFIELD	BITS	DESCRIPTION
YEAR_10	7:4	
YEAR	3:0	

TS2_FLAGS (0x47)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	VLOWF	VBATF	VCCF	DINF
Reset	–	–	–	–	0b0	0b0	0b0	0b0
Access Type	–	–	–	–	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
VLOWF	3	Indicates if this Timestamp was triggered by VLOW detection	0x0: Not triggered by VLOW detection 0x1: Triggered by VLOW detection

BITFIELD	BITS	DESCRIPTION	DECODE
VBATF	2	Indicates if this Timestamp was triggered by VCC → VBAT switch	0x0: Not triggered by VCC → VBAT switch 0x1: Triggered by VCC → VBAT switch
VCCF	1	Indicates if this Timestamp was triggered by VBAT → VCC switch	0x0: Not triggered by VBAT → VCC switch 0x1: Triggered by VBAT → VCC switch
DINF	0	Indicates if this Timestamp was triggered by DIN transition	0x0: Not triggered by DIN 0x1: Triggered by DIN

TS3_SEC_1_128 (0x48)

BIT	7	6	5	4	3	2	1	0
Field	–	_1_2s	_1_4s	_1_8s	_1_16s	_1_32s	_1_64s	_1_128s
Reset	–	0b0	0b0	0b0	0b0	0b0	0b0	0b0
Access Type	–	Write, Read	Write, Read	Write, Read, Dual	Write, Read	Write, Read	Write, Read	Write, Read, Dual

BITFIELD	BITS	DESCRIPTION
_1_2s	6	
_1_4s	5	
_1_8s	4	
_1_16s	3	
_1_32s	2	
_1_64s	1	
_1_128s	0	

TS3_SEC (0x49)

BIT	7	6	5	4	3	2	1	0
Field	–	SEC_10[2:0]			SEC[3:0]			
Reset	–	0b000			0x0			
Access Type	–	Write, Read, Dual			Write, Read, Dual			

BITFIELD	BITS	DESCRIPTION
SEC_10	6:4	
SEC	3:0	

TS3_MIN (0x4A)

BIT	7	6	5	4	3	2	1	0
Field	–	MIN_10[2:0]			MIN[3:0]			
Reset	–	0b000			0x0			
Access Type	–	Write, Read			Write, Read, Dual			

BITFIELD	BITS	DESCRIPTION
MIN_10	6:4	
MIN	3:0	

TS3_HOUR (0x4B)

BIT	7	6	5	4	3	2	1	0
Field	–	F_24_12	HR_20_AM_PM	HR_10	HOUR[3:0]			
Reset	–	0b0	0b0	0b0	0x0			
Access Type	–	Write, Read	Write, Read, Dual	Write, Read, Dual	Write, Read, Dual			

BITFIELD	BITS	DESCRIPTION
F_24_12	6	
HR_20_AM_PM	5	
HR_10	4	
HOUR	3:0	

TS3_DATE (0x4C)

BIT	7	6	5	4	3	2	1	0

Field	–	–	DATE_10[1:0]	DATE[3:0]
Reset	–	–	0b00	0x0
Access Type	–	–	Write, Read	Write, Read, Dual

BITFIELD	BITS	DESCRIPTION
DATE_10	5:4	
DATE	3:0	

TS3_MONTH (0x4D)

BIT	7	6	5	4	3	2	1	0
Field	CENTURY	–	–	MONTH_10	MONTH[3:0]			
Reset	0b0	–	–	0b0	0x0			
Access Type	Write, Read	–	–	Write, Read	Write, Read, Dual			

BITFIELD	BITS	DESCRIPTION
CENTURY	7	
MONTH_10	4	
MONTH	3:0	

TS3_YEAR (0x4E)

BIT	7	6	5	4	3	2	1	0
Field	YEAR_10[3:0]				YEAR[3:0]			
Reset	0x0				0x0			
Access Type	Write, Read				Write, Read, Dual			

BITFIELD	BITS	DESCRIPTION
YEAR_10	7:4	
YEAR	3:0	

TS3_FLAGS (0x4F)

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	VLOWF	VBATF	VCCF	DINF
Reset	–	–	–	–	0b0	0b0	0b0	0b0
Access Type	–	–	–	–	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
VLOWF	3	Indicates if this Timestamp was triggered by VLOW detection	0x0: Not triggered by VLOW detection 0x1: Triggered by VLOW detection
VBATF	2	Indicates if this Timestamp was triggered by VCC → VBAT switch	0x0: Not triggered by VCC → VBAT switch 0x1: Triggered by VCC → VBAT switch
VCCF	1	Indicates if this Timestamp was triggered by VBAT → VCC switch	0x0: Not triggered by VBAT → VCC switch 0x1: Triggered by VBAT → VCC switch
DINF	0	Indicates if this Timestamp was triggered by DIN transition	0x0: Not triggered by DIN 0x1: Triggered by DIN

Ordering Information

PART NUMBER	TEMP RANGE	PIN-PACKAGE
MAX31334EWC+	-40°C to +85°C	12-WLP
MAX31334EWC+T	-40°C to +85°C	12-WLP
MAX31334ETC+*	-40°C to +85°C	12-TDFN
MAX31334ETC+T*	-40°C to +85°C	12-TDFN

**Future product—contact factory for availability*

+Denotes a lead(Pb)-free/ROHS-compliant package

T = Tape and reel.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	8/22	Release for Market Intro	—