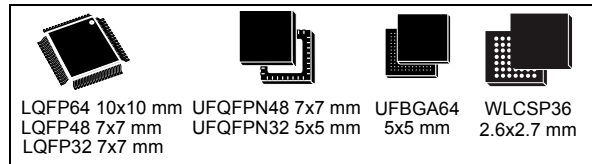


ARM[®]-based 32-bit MCU, 16 to 64-KB Flash, timers, ADC, DAC and communication interfaces, 2.0-3.6 V

Datasheet - production data

Features

- Core: ARM[®] 32-bit Cortex[®]-M0 CPU, frequency up to 48 MHz
- Memories
 - 16 to 64 Kbytes of Flash memory
 - 8 Kbytes of SRAM with HW parity checking
- CRC calculation unit
- Reset and power management
 - Digital and I/O supply: $V_{DD} = 2.0\text{ V to }3.6\text{ V}$
 - Analog supply: $V_{DDA} = \text{from } V_{DD} \text{ to } 3.6\text{ V}$
 - Power-on/Power down reset (POR/PDR)
 - Programmable voltage detector (PVD)
 - Low power modes: Sleep, Stop, Standby
 - V_{BAT} supply for RTC and backup registers
- Clock management
 - 4 to 32 MHz crystal oscillator
 - 32 kHz oscillator for RTC with calibration
 - Internal 8 MHz RC with x6 PLL option
 - Internal 40 kHz RC oscillator
- Up to 55 fast I/Os
 - All mappable on external interrupt vectors
 - Up to 36 I/Os with 5 V tolerant capability
- 5-channel DMA controller
- One 12-bit, 1.0 μs ADC (up to 16 channels)
 - Conversion range: 0 to 3.6 V
 - Separate analog supply from 2.4 up to 3.6
- One 12-bit DAC channel
- Two fast low-power analog comparators with programmable input and output
- Up to 18 capacitive sensing channels supporting touchkey, linear and rotary touch sensors
- Up to 11 timers
 - One 16-bit 7-channel advanced-control timer for 6 channels PWM output, with deadtime generation and emergency stop
 - One 32-bit and one 16-bit timer, with up to 4 IC/OC, usable for IR control decoding



- One 16-bit timer, with 2 IC/OC, 1 OCN, deadtime generation and emergency stop
- Two 16-bit timers, each with IC/OC and OCN, deadtime generation, emergency stop and modulator gate for IR control
- One 16-bit timer with 1 IC/OC
- Independent and system watchdog timers
- SysTick timer: 24-bit downcounter
- One 16-bit basic timer to drive the DAC
- Calendar RTC with alarm and periodic wakeup from Stop/Standby
- Communication interfaces
 - Up to two I²C interfaces; one supporting Fast Mode Plus (1 Mbit/s) with 20 mA current sink, SMBus/PMBus and wakeup from Stop mode
 - Up to two USARTs supporting master synchronous SPI and modem control; one with ISO7816 interface, LIN, IrDA capability, auto baud rate detection and wakeup feature
 - Up to two SPIs (18 Mbit/s) with 4 to 16 programmable bit frame, one with I²S interface multiplexed
- HDMI CEC interface, wakeup on header reception
- Serial wire debug (SWD)
- 96-bit unique ID
- All packages ECOPACK[®]2

Table 1. Device summary

| Reference | Part number |
|-------------|---|
| STM32F051xx | STM32F051C4, STM32F051K4, STM32F051R4 STM32F051C6, STM32F051K6, STM32F051R6 STM32F051C8, STM32F051K8, STM32F051R8, STM32F051T8 |

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1 Introduction

This datasheet provides the ordering information and mechanical device characteristics of the STM32F051xx microcontrollers.

This document should be read in conjunction with the STM32F0xxxx reference manual (RM0091). The reference manual is available from the STMicroelectronics website www.st.com.

For information on the ARM[®] Cortex[®]-M0 core, please refer to the Cortex[®]-M0 Technical Reference Manual, available from the www.arm.com website.



2 Description

The STM32F051xx microcontrollers incorporate the high-performance ARM[®] Cortex[®]-M0 32-bit RISC core operating at a 48 MHz frequency, high-speed embedded memories (up to 64 Kbytes of Flash memory and 8 Kbytes of SRAM), and an extensive range of enhanced peripherals and I/Os. All devices offer standard communication interfaces (up to two I²Cs, up to two SPIs, one I2S, one HDMI CEC and up to two USARTs), one 12-bit ADC, one 12-bit DAC, six 16-bit timers, one 32-bit timer and an advanced-control PWM timer.

The STM32F051xx microcontrollers operate in the -40 to +85 °C and -40 to +105 °C temperature ranges, from a 2.0 to 3.6 V power supply. A comprehensive set of power-saving modes allows the design of low-power applications.

The STM32F051xx microcontrollers include devices in seven different packages ranging from 32 pins to 64 pins with a die form also available upon request. Depending on the device chosen, different sets of peripherals are included. The description below provides an overview of the complete range of STM32F051xx peripherals proposed.

These features make the STM32F051xx microcontrollers suitable for a wide range of applications such as application control and user interfaces, hand-held equipment, A/V receivers and digital TV, PC peripherals, gaming and GPS platforms, industrial applications, PLCs, inverters, printers, scanners, alarm systems, video intercoms, and HVACs.

Table 2. STM32F051xx family device features and peripheral count

| Peripheral | | STM32F051Kx | | | STM32F051T8 | STM32F051Cx | | | STM32F051Rx | | | |
|---------------------------------|--------------------------|--|----|----|----------------------|----------------------|----|-------|-------------------------|----|----|--|
| Flash (Kbyte) | | 16 | 32 | 64 | 64 | 16 | 32 | 64 | 16 | 32 | 64 | |
| SRAM (Kbyte) | | 8 | | | | | | | | | | |
| Timers | Advanced control | 1 (16-bit) | | | | | | | | | | |
| | General purpose | 5 (16-bit) 1 (32-bit) | | | | | | | | | | |
| | Basic | 1 (16-bit) | | | | | | | | | | |
| Comm. interfaces | SPI [I2S] ⁽¹⁾ | 1 [1] ⁽²⁾ | | | 1 [1] ⁽²⁾ | 1 [1] ⁽²⁾ | | 2 [1] | 1 [1] ⁽²⁾ | | | |
| | I ² C | 1 ⁽³⁾ | | | 1 ⁽³⁾ | 1 ⁽³⁾ | | 2 | 1 ⁽³⁾ | | 2 | |
| | USART | 1 ⁽⁴⁾ | 2 | | 2 | 1 ⁽⁴⁾ | 2 | | 1 ⁽⁴⁾ | 2 | | |
| | CEC | 1 | | | | | | | | | | |
| 12-bit ADC (number of channels) | | 1 (10 ext. + 3 int.) | | | | | | | 1 (16 ext. + 3 int.) | | | |
| 12-bit DAC (number of channels) | | 1 (1) | | | | | | | | | | |
| Analog comparator | | 2 | | | | | | | | | | |
| GPIOs | | 25 (on LQFP32) 27 (on UFQFPN32) | | | 29 | 39 | | | 55 | | | |
| Capacitive sensing channels | | 13 (on LQFP32) 14 (on UFQFPN32) | | | 14 | 17 | | | 18 | | | |
| Max. CPU frequency | | 48 MHz | | | | | | | | | | |
| Operating voltage | | 2.0 to 3.6 V | | | | | | | | | | |
| Operating temperature | | Ambient operating temperature: -40°C to 85°C / -40°C to 105°C Junction temperature: -40°C to 105°C / -40°C to 125°C | | | | | | | | | | |
| Packages | | LQFP32 UFQFPN32 | | | WLCSP36 | LQFP48 UFQFPN48 | | | LQFP64 UFBGA64 | | | |

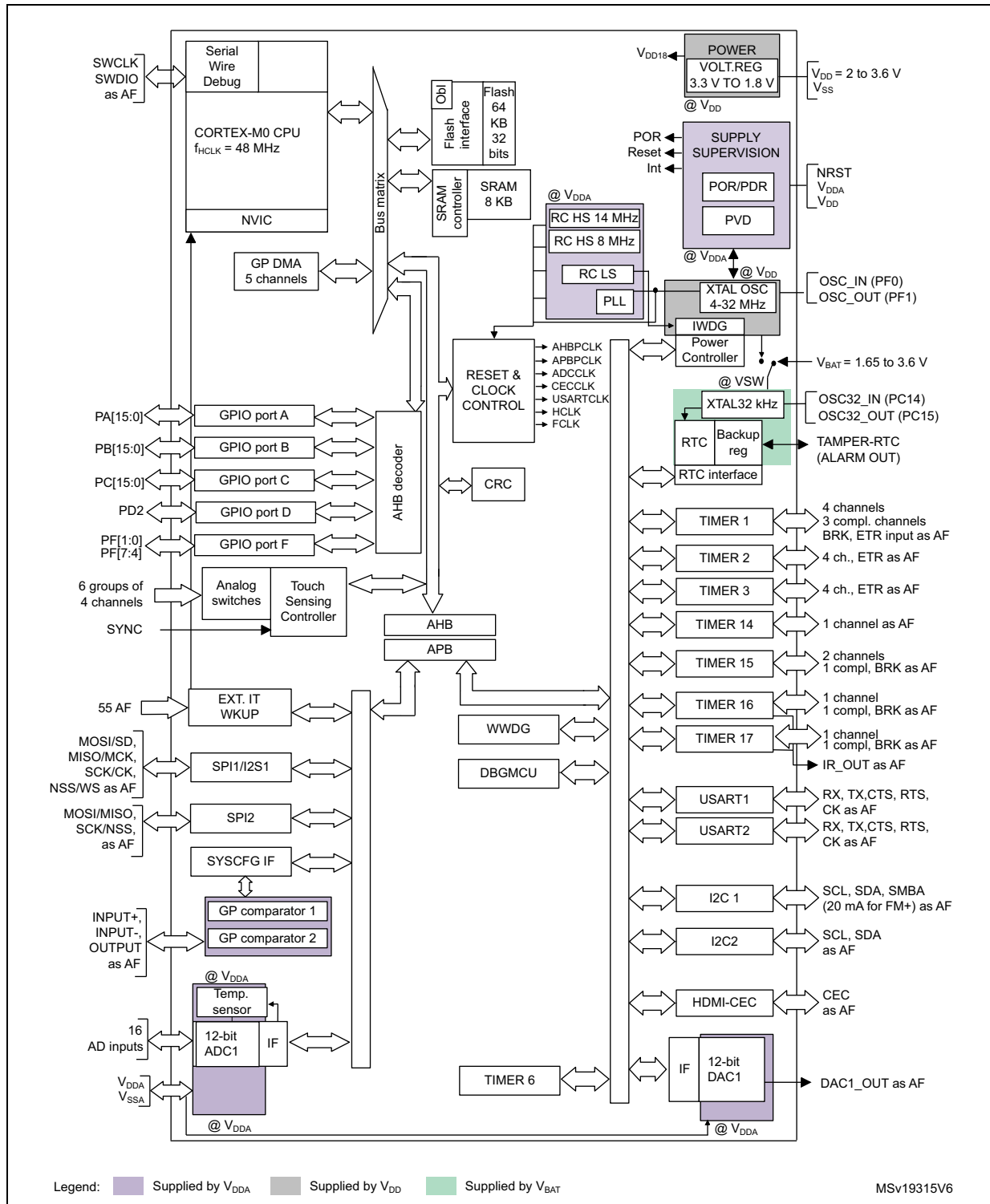
1. The SPI1 interface can be used either in SPI mode or in I2S audio mode.

2. SPI2 is not present.

3. I2C2 is not present.

4. USART2 is not present.

Figure 1. Block diagram



3 Functional overview

3.1 ARM[®]-Cortex[®]-M0 core with embedded Flash and SRAM

The ARM[®] Cortex[®]-M0 processor is the latest generation of ARM processors for embedded systems. It has been developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced system response to interrupts.

The ARM[®] Cortex[®]-M0 32-bit RISC processor features exceptional code-efficiency, delivering the high-performance expected from an ARM core in the memory size usually associated with 8- and 16-bit devices.

The STM32F0xx family has an embedded ARM core and is therefore compatible with all ARM tools and software.

Figure 1 shows the general block diagram of the device family.

3.2 Memories

The device has the following features:

- 8 Kbytes of embedded SRAM accessed (read/write) at CPU clock speed with 0 wait states and featuring embedded parity checking with exception generation for fail-critical applications.
- The non-volatile memory is divided into two arrays:
 - 16 to 64 Kbytes of embedded Flash memory for programs and data
 - Option bytes

The option bytes are used to write-protect the memory (with 4 KB granularity) and/or readout-protect the whole memory with the following options:

- Level 0: no readout protection
- Level 1: memory readout protection, the Flash memory cannot be read from or written to if either debug features are connected or boot in RAM is selected
- Level 2: chip readout protection, debug features (Cortex[®]-M0 serial wire) and boot in RAM selection disabled

3.3 Boot modes

At startup, the boot pin and boot selector option bit are used to select one of the three boot options:

- Boot from User Flash
- Boot from System Memory
- Boot from embedded SRAM

The boot loader is located in System Memory. It is used to reprogram the Flash memory by using USART on pins PA14/PA15 or PA9/PA10.

3.4 Cyclic redundancy check calculation unit (CRC)

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code from a 32-bit data word and a CRC-32 (Ethernet) polynomial.

Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a means of verifying the Flash memory integrity. The CRC calculation unit helps compute a signature of the software during runtime, to be compared with a reference signature generated at link-time and stored at a given memory location.

3.5 Power management

3.5.1 Power supply schemes

- $V_{DD} = V_{DDIO1} = 2.0$ to 3.6 V: external power supply for I/Os (V_{DDIO1}) and the internal regulator. It is provided externally through VDD pins.
- V_{DDA} = from V_{DD} to 3.6 V: external analog power supply for ADC, DAC, Reset blocks, RCs and PLL (minimum voltage to be applied to V_{DDA} is 2.4 V when the ADC or DAC are used). It is provided externally through VDDA pin. The V_{DDA} voltage level must be always greater or equal to the V_{DD} voltage level and must be established first.
- $V_{BAT} = 1.65$ to 3.6 V: power supply for RTC, external clock 32 kHz oscillator and backup registers (through power switch) when V_{DD} is not present.

For more details on how to connect power pins, refer to [Figure 13: Power supply scheme](#).

3.5.2 Power supply supervisors

The device has integrated power-on reset (POR) and power-down reset (PDR) circuits. They are always active, and ensure proper operation above a threshold of 2 V. The device remains in reset mode when the monitored supply voltage is below a specified threshold, $V_{POR/PDR}$, without the need for an external reset circuit.

- The POR monitors only the V_{DD} supply voltage. During the startup phase it is required that V_{DDA} should arrive first and be greater than or equal to V_{DD} .
- The PDR monitors both the V_{DD} and V_{DDA} supply voltages, however the V_{DDA} power supply supervisor can be disabled (by programming a dedicated Option bit) to reduce the power consumption if the application design ensures that V_{DDA} is higher than or equal to V_{DD} .

The device features an embedded programmable voltage detector (PVD) that monitors the V_{DD} power supply and compares it to the V_{PVD} threshold. An interrupt can be generated when V_{DD} drops below the V_{PVD} threshold and/or when V_{DD} is higher than the V_{PVD} threshold. The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software.

3.5.3 Voltage regulator

The regulator has two operating modes and it is always enabled after reset.

- Main (MR) is used in normal operating mode (Run).
- Low power (LPR) can be used in Stop mode where the power demand is reduced.

In Standby mode, it is put in power down mode. In this mode, the regulator output is in high impedance and the kernel circuitry is powered down, inducing zero consumption (but the contents of the registers and SRAM are lost).

3.5.4 Low-power modes

The STM32F051xx microcontrollers support three low-power modes to achieve the best compromise between low power consumption, short startup time and available wakeup sources:

- **Sleep mode**

In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs.

- **Stop mode**

Stop mode achieves very low power consumption while retaining the content of SRAM and registers. All clocks in the 1.8 V domain are stopped, the PLL, the HSI RC and the HSE crystal oscillators are disabled. The voltage regulator can also be put either in normal or in low power mode.

The device can be woken up from Stop mode by any of the EXTI lines. The EXTI line source can be one of the 16 external lines, the PVD output, RTC, I2C1, USART1,, COMPx or the CEC.

The peripherals listed above can be configured to enable the HSI RC oscillator for processing incoming data. If this is used when the voltage regulator is put in low power mode, the regulator is first switched to normal mode before the clock is provided to the given peripheral.

- **Standby mode**

The Standby mode is used to achieve the lowest power consumption. The internal voltage regulator is switched off so that the entire 1.8 V domain is powered off. The PLL, the HSI RC and the HSE crystal oscillators are also switched off. After entering Standby mode, SRAM and register contents are lost except for registers in the RTC domain and Standby circuitry.

The device exits Standby mode when an external reset (NRST pin), an IWDG reset, a rising edge on the WKUP pins, or an RTC event occurs.

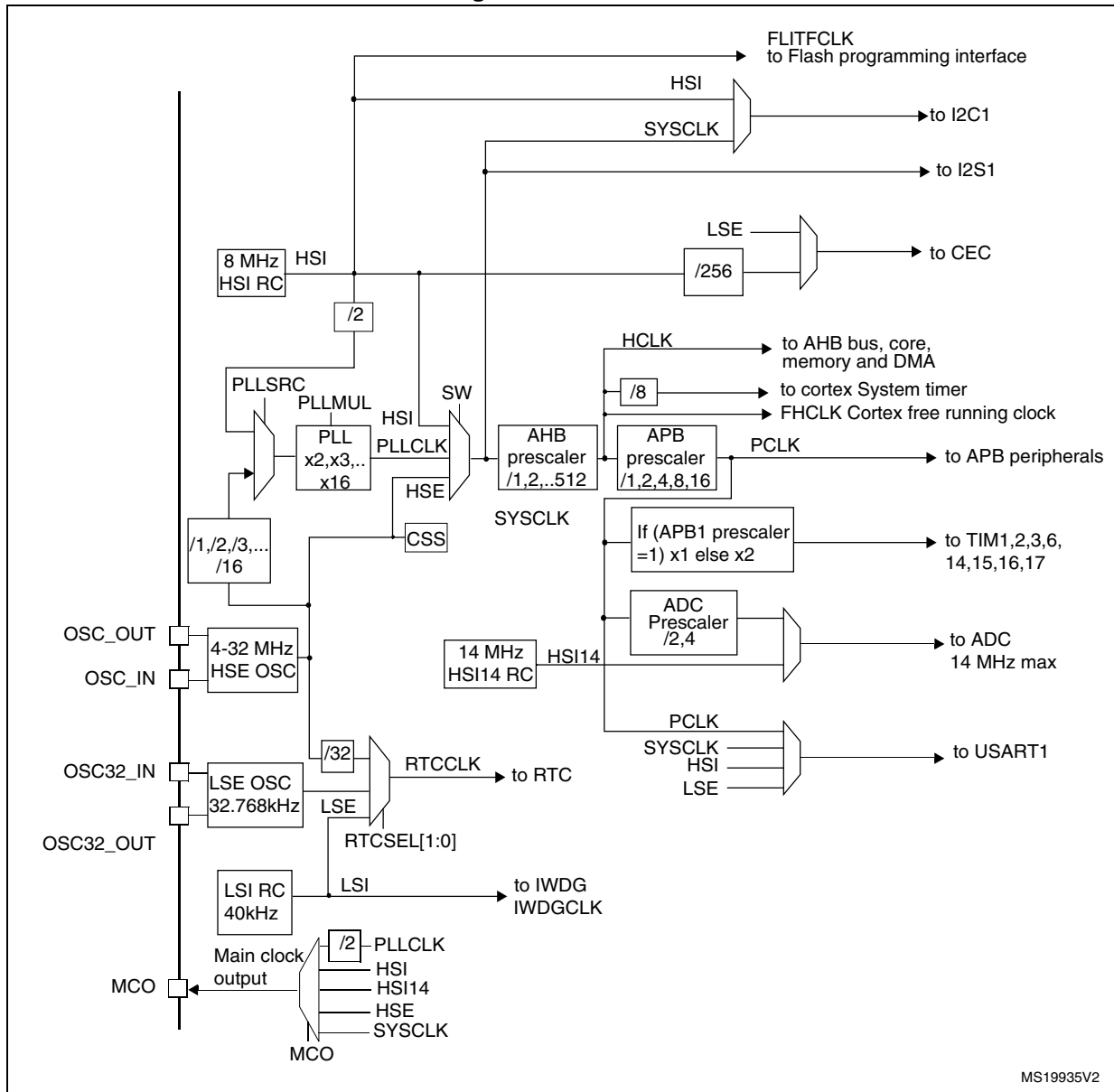
Note: The RTC, the IWDG, and the corresponding clock sources are not stopped by entering Stop or Standby mode.

3.6 Clocks and startup

System clock selection is performed on startup, however the internal RC 8 MHz oscillator is selected as default CPU clock on reset. An external 4-32 MHz clock can be selected, in which case it is monitored for failure. If failure is detected, the system automatically switches back to the internal RC oscillator. A software interrupt is generated if enabled. Similarly, full interrupt management of the PLL clock entry is available when necessary (for example on failure of an indirectly used external crystal, resonator or oscillator).

Several prescalers allow the application to configure the frequency of the AHB and the APB domains. The maximum frequency of the AHB and the APB domains is 48 MHz.

Figure 2. Clock tree



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3.7 General-purpose inputs/outputs (GPIOs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions.

The I/O configuration can be locked if needed following a specific sequence in order to avoid spurious writing to the I/Os registers.

3.8 Direct memory access controller (DMA)

The 5-channel general-purpose DMAs manage memory-to-memory, peripheral-to-memory and memory-to-peripheral transfers.

The DMA supports circular buffer management, removing the need for user code intervention when the controller reaches the end of the buffer.

Each channel is connected to dedicated hardware DMA requests, with support for software trigger on each channel. Configuration is made by software and transfer sizes between source and destination are independent.

DMA can be used with the main peripherals: SPI, I2S, I2C, USART, all TIMx timers (except TIM14), DAC and ADC.

3.9 Interrupts and events

3.9.1 Nested vectored interrupt controller (NVIC)

The STM32F0xx family embeds a nested vectored interrupt controller able to handle up to 32 maskable interrupt channels (not including the 16 interrupt lines of Cortex[®]-M0) and 4 priority levels.

- Closely coupled NVIC gives low latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Closely coupled NVIC core interface
- Allows early processing of interrupts
- Processing of late arriving higher priority interrupts
- Support for tail-chaining
- Processor state automatically saved
- Interrupt entry restored on interrupt exit with no instruction overhead

This hardware block provides flexible interrupt management features with minimal interrupt latency.

3.9.2 Extended interrupt/event controller (EXTI)

The extended interrupt/event controller consists of 24 edge detector lines used to generate interrupt/event requests and wake-up the system. Each line can be independently configured to select the trigger event (rising edge, falling edge, both) and can be masked independently. A pending register maintains the status of the interrupt requests. The EXTI can detect an external line with a pulse width shorter than the internal clock period. Up to 55 GPIOs can be connected to the 16 external interrupt lines.

3.10 Analog to digital converter (ADC)

The 12-bit analog to digital converter has up to 16 external and 3 internal (temperature sensor, voltage reference, VBAT voltage measurement) channels and performs conversions in single-shot or scan modes. In scan mode, automatic conversion is performed on a selected group of analog inputs.

The ADC can be served by the DMA controller.

An analog watchdog feature allows very precise monitoring of the converted voltage of one, some or all selected channels. An interrupt is generated when the converted voltage is outside the programmed thresholds.

3.10.1 Temperature sensor

The temperature sensor (TS) generates a voltage V_{SENSE} that varies linearly with temperature.

The temperature sensor is internally connected to the ADC_IN16 input channel which is used to convert the sensor output voltage into a digital value.

The sensor provides good linearity but it has to be calibrated to obtain good overall accuracy of the temperature measurement. As the offset of the temperature sensor varies from chip to chip due to process variation, the uncalibrated internal temperature sensor is suitable for applications that detect temperature changes only.

To improve the accuracy of the temperature sensor measurement, each device is individually factory-calibrated by ST. The temperature sensor factory calibration data are stored by ST in the system memory area, accessible in read-only mode.

Table 3. Temperature sensor calibration values

| Calibration value name | Description | Memory address |
|------------------------|---|---------------------------|
| TS_CAL1 | TS ADC raw data acquired at a temperature of 30 °C (± 5 °C), $V_{DDA} = 3.3$ V (± 10 mV) | 0x1FFF F7B8 - 0x1FFF F7B9 |
| TS_CAL2 | TS ADC raw data acquired at a temperature of 110 °C (± 5 °C), $V_{DDA} = 3.3$ V (± 10 mV) | 0x1FFF F7C2 - 0x1FFF F7C3 |

3.10.2 Internal voltage reference (V_{REFINT})

The internal voltage reference (V_{REFINT}) provides a stable (bandgap) voltage output for the ADC and comparators. V_{REFINT} is internally connected to the ADC_IN17 input channel. The precise voltage of V_{REFINT} is individually measured for each part by ST during production test and stored in the system memory area. It is accessible in read-only mode.

Table 4. Internal voltage reference calibration values

| Calibration value name | Description | Memory address |
|------------------------|---|---------------------------|
| VREFINT_CAL | Raw data acquired at a temperature of 30 °C (± 5 °C), $V_{DDA} = 3.3$ V (± 10 mV) | 0x1FFF F7BA - 0x1FFF F7BB |

3.10.3 V_{BAT} battery voltage monitoring

This embedded hardware feature allows the application to measure the V_{BAT} battery voltage using the internal ADC channel ADC_IN18. As the V_{BAT} voltage may be higher than V_{DDA} , and thus outside the ADC input range, the V_{BAT} pin is internally connected to a bridge divider by 2. As a consequence, the converted digital value is half the V_{BAT} voltage.

3.11 Digital-to-analog converter (DAC)

The 12-bit buffered DAC channels can be used to convert digital signals into analog voltage signal outputs. The chosen design structure is composed of integrated resistor strings and an amplifier in non-inverting configuration.

This digital Interface supports the following features:

- Left or right data alignment in 12-bit mode
- Synchronized update capability
- DMA capability
- External triggers for conversion

Five DAC trigger inputs are used in the device. The DAC is triggered through the timer trigger outputs and the DAC interface is generating its own DMA requests.

3.12 Comparators (COMP)

The device embeds two fast rail-to-rail low-power comparators with programmable reference voltage (internal or external), hysteresis and speed (low speed for low power) and with selectable output polarity.

The reference voltage can be one of the following:

- External I/O
- DAC output pins
- Internal reference voltage or submultiple (1/4, 1/2, 3/4). Refer to [Table 24: Embedded internal reference voltage](#) for the value and precision of the internal reference voltage.

Both comparators can wake up from STOP mode, generate interrupts and breaks for the timers and can be also combined into a window comparator.

3.13 Touch sensing controller (TSC)

The STM32F051xx devices provide a simple solution for adding capacitive sensing functionality to any application. These devices offer up to 18 capacitive sensing channels distributed over 6 analog I/O groups.

Capacitive sensing technology is able to detect the presence of a finger near a sensor which is protected from direct touch by a dielectric (glass, plastic...). The capacitive variation introduced by the finger (or any conductive object) is measured using a proven implementation based on a surface charge transfer acquisition principle. It consists of charging the sensor capacitance and then transferring a part of the accumulated charges into a sampling capacitor until the voltage across this capacitor has reached a specific threshold. To limit the CPU bandwidth usage, this acquisition is directly managed by the hardware touch sensing controller and only requires few external components to operate.

The touch sensing controller is fully supported by the STMTouch touch sensing firmware library, which is free to use and allows touch sensing functionality to be implemented reliably in the end application.

Table 5. Capacitive sensing GPIOs available on STM32F051xx devices

| Group | Capacitive sensing signal name | Pin name | Group | Capacitive sensing signal name | Pin name |
|-------|--------------------------------|----------|-------|--------------------------------|----------|
| 1 | TSC_G1_IO1 | PA0 | 4 | TSC_G4_IO1 | PA9 |
| | TSC_G1_IO2 | PA1 | | TSC_G4_IO2 | PA10 |
| | TSC_G1_IO3 | PA2 | | TSC_G4_IO3 | PA11 |
| | TSC_G1_IO4 | PA3 | | TSC_G4_IO4 | PA12 |
| 2 | TSC_G2_IO1 | PA4 | 5 | TSC_G5_IO1 | PB3 |
| | TSC_G2_IO2 | PA5 | | TSC_G5_IO2 | PB4 |
| | TSC_G2_IO3 | PA6 | | TSC_G5_IO3 | PB6 |
| | TSC_G2_IO4 | PA7 | | TSC_G5_IO4 | PB7 |
| 3 | TSC_G3_IO1 | PC5 | 6 | TSC_G6_IO1 | PB11 |
| | TSC_G3_IO2 | PB0 | | TSC_G6_IO2 | PB12 |
| | TSC_G3_IO3 | PB1 | | TSC_G6_IO3 | PB13 |
| | TSC_G3_IO4 | PB2 | | TSC_G6_IO4 | PB14 |

Table 6. No. of capacitive sensing channels available on STM32F051x devices

| Analog I/O group | Number of capacitive sensing channels | | | | |
|---------------------------------------|---------------------------------------|-------------|-------------|-------------------------|-----------------------|
| | STM32F051Rx | STM32F051Cx | STM32F051Tx | STM32F051KxU (UFQFPN32) | STM32F051KxT (LQFP32) |
| G1 | 3 | 3 | 3 | 3 | 3 |
| G2 | 3 | 3 | 3 | 3 | 3 |
| G3 | 3 | 2 | 2 | 2 | 1 |
| G4 | 3 | 3 | 3 | 3 | 3 |
| G5 | 3 | 3 | 3 | 3 | 3 |
| G6 | 3 | 3 | 0 | 0 | 0 |
| Number of capacitive sensing channels | 18 | 17 | 14 | 14 | 13 |

3.14 Timers and watchdogs

The STM32F051xx devices include up to six general-purpose timers, one basic timer and an advanced control timer.

[Table 7](#) compares the features of the different timers.

Table 7. Timer feature comparison

| Timer type | Timer | Counter resolution | Counter type | Prescaler factor | DMA request generation | Capture/compare channels | Complementary outputs |
|------------------|--------------|--------------------|-------------------|---------------------------------|------------------------|--------------------------|-----------------------|
| Advanced control | TIM1 | 16-bit | Up, down, up/down | Any integer between 1 and 65536 | Yes | 4 | 3 |
| General purpose | TIM2 | 32-bit | Up, down, up/down | Any integer between 1 and 65536 | Yes | 4 | No |
| | TIM3 | 16-bit | Up, down, up/down | Any integer between 1 and 65536 | Yes | 4 | No |
| | TIM14 | 16-bit | Up | Any integer between 1 and 65536 | No | 1 | No |
| | TIM15 | 16-bit | Up | Any integer between 1 and 65536 | Yes | 2 | 1 |
| | TIM16, TIM17 | 16-bit | Up | Any integer between 1 and 65536 | Yes | 1 | 1 |
| Basic | TIM6 | 16-bit | Up | Any integer between 1 and 65536 | Yes | No | No |

3.14.1 Advanced-control timer (TIM1)

The advanced-control timer (TIM1) can be seen as a three-phase PWM multiplexed on six channels. It has complementary PWM outputs with programmable inserted dead times. It can also be seen as a complete general-purpose timer. The four independent channels can be used for:

- Input capture
- Output compare
- PWM generation (edge or center-aligned modes)
- One-pulse mode output

If configured as a standard 16-bit timer, it has the same features as the TIMx timer. If configured as the 16-bit PWM generator, it has full modulation capability (0-100%).

The counter can be frozen in debug mode.

Many features are shared with those of the standard timers which have the same architecture. The advanced control timer can therefore work together with the other timers via the Timer Link feature for synchronization or event chaining.

3.14.2 General-purpose timers (TIM2..3, TIM14..17)

There are six synchronizable general-purpose timers embedded in the STM32F051xx devices (see [Table 7](#) for differences). Each general-purpose timer can be used to generate PWM outputs, or as simple time base.

TIM2, TIM3

STM32F051xx devices feature two synchronizable 4-channel general-purpose timers. TIM2 is based on a 32-bit auto-reload up/downcounter and a 16-bit prescaler. TIM3 is based on a 16-bit auto-reload up/downcounter and a 16-bit prescaler. They feature 4 independent channels each for input capture/output compare, PWM or one-pulse mode output. This gives up to 12 input captures/output compares/PWMs on the largest packages.

The TIM2 and TIM3 general-purpose timers can work together or with the TIM1 advanced-control timer via the Timer Link feature for synchronization or event chaining.

TIM2 and TIM3 both have independent DMA request generation.

These timers are capable of handling quadrature (incremental) encoder signals and the digital outputs from 1 to 3 hall-effect sensors.

Their counters can be frozen in debug mode.

TIM14

This timer is based on a 16-bit auto-reload upcounter and a 16-bit prescaler.

TIM14 features one single channel for input capture/output compare, PWM or one-pulse mode output.

Its counter can be frozen in debug mode.

TIM15, TIM16 and TIM17

These timers are based on a 16-bit auto-reload upcounter and a 16-bit prescaler.

TIM15 has two independent channels, whereas TIM16 and TIM17 feature one single channel for input capture/output compare, PWM or one-pulse mode output.

The TIM15, TIM16 and TIM17 timers can work together, and TIM15 can also operate with TIM1 via the Timer Link feature for synchronization or event chaining.

TIM15 can be synchronized with TIM16 and TIM17.

TIM15, TIM16 and TIM17 have a complementary output with dead-time generation and independent DMA request generation.

Their counters can be frozen in debug mode.

3.14.3 Basic timer TIM6

This timer is mainly used for DAC trigger generation. It can also be used as a generic 16-bit time base.

3.14.4 Independent watchdog (IWDG)

The independent watchdog is based on an 8-bit prescaler and 12-bit downcounter with user-defined refresh window. It is clocked from an independent 40 kHz internal RC and as it operates independently from the main clock, it can operate in Stop and Standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free running timer for application timeout management. It is hardware or software configurable through the option bytes. The counter can be frozen in debug mode.

3.14.5 System window watchdog (WWDG)

The system window watchdog is based on a 7-bit downcounter that can be set as free running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the APB clock (PCLK). It has an early warning interrupt capability and the counter can be frozen in debug mode.

3.14.6 SysTick timer

This timer is dedicated to real-time operating systems, but could also be used as a standard down counter. It features:

- A 24-bit down counter
- Autoreload capability
- Maskable system interrupt generation when the counter reaches 0
- Programmable clock source (HCLK or HCLK/8)

3.15 Real-time clock (RTC) and backup registers

The RTC and the five backup registers are supplied through a switch that takes power either on V_{DD} supply when present or through the V_{BAT} pin. The backup registers are five 32-bit registers used to store 20 bytes of user application data when V_{DD} power is not present. They are not reset by a system or power reset, or when the device wakes up from Standby mode.

The RTC is an independent BCD timer/counter. Its main features are the following:

- Calendar with subseconds, seconds, minutes, hours (12 or 24 format), week day, date, month, year, in BCD (binary-coded decimal) format.
- Automatic correction for 28, 29 (leap year), 30, and 31 day of the month.
- Programmable alarm with wake up from Stop and Standby mode capability.
- On-the-fly correction from 1 to 32767 RTC clock pulses. This can be used to synchronize the RTC with a master clock.
- Digital calibration circuit with 1 ppm resolution, to compensate for quartz crystal inaccuracy.
- Two anti-tamper detection pins with programmable filter. The MCU can be woken up from Stop and Standby modes on tamper event detection.
- Timestamp feature which can be used to save the calendar content. This function can be triggered by an event on the timestamp pin, or by a tamper event. The MCU can be woken up from Stop and Standby modes on timestamp event detection.
- Reference clock detection: a more precise second source clock (50 or 60 Hz) can be used to enhance the calendar precision.

The RTC clock sources can be:

- A 32.768 kHz external crystal
- A resonator or oscillator
- The internal low-power RC oscillator (typical frequency of 40 kHz)
- The high-speed external clock divided by 32

3.16 Inter-integrated circuit interfaces (I²C)

Up to two I²C interfaces (I2C1 and I2C2) can operate in multimaster or slave modes. Both can support Standard mode (up to 100 kbit/s), or Fast mode (up to 400 kbit/s) and I2C1 supports also Fast Mode Plus (up to 1 Mbit/s) with 20 mA output drive.

Both support 7-bit and 10-bit addressing modes, multiple 7-bit slave addresses (two addresses, one with configurable mask). They also include programmable analog and digital noise filters.

Table 8. Comparison of I2C analog and digital filters

| | Analog filter | Digital filter |
|----------------------------------|---|--|
| Pulse width of suppressed spikes | ≥ 50 ns | Programmable length from 1 to 15 I2C peripheral clocks |
| Benefits | Available in Stop mode | 1. Extra filtering capability vs. standard requirements. 2. Stable length |
| Drawbacks | Variations depending on temperature, voltage, process | Wakeup from Stop on address match is not available when digital filter is enabled. |

In addition, I2C1 provides hardware support for SMBUS 2.0 and PMBUS 1.1: ARP capability, Host notify protocol, hardware CRC (PEC) generation/verification, timeouts verifications and ALERT protocol management. I2C1 also has a clock domain independent from the CPU clock, allowing the I2C1 to wake up the MCU from Stop mode on address match.

The I2C interfaces can be served by the DMA controller.

Refer to [Table 9](#) for the differences between I2C1 and I2C2.

Table 9. STM32F051xx I²C implementation

| I2C features ⁽¹⁾ | I2C1 | I2C2 |
|--|------|------|
| 7-bit addressing mode | X | X |
| 10-bit addressing mode | X | X |
| Standard mode (up to 100 kbit/s) | X | X |
| Fast mode (up to 400 kbit/s) | X | X |
| Fast Mode Plus (up to 1 Mbit/s) with output drive I/Os | X | - |
| Independent clock | X | - |

Table 9. STM32F051xx I²C implementation (continued)

| I ² C features ⁽¹⁾ | I2C1 | I2C2 |
|--|------|------|
| SMBus | X | - |
| Wakeup from STOP | X | - |

1. X = supported.

3.17 Universal synchronous/asynchronous receiver transmitters (USART)

The device embeds up to two universal synchronous/asynchronous receiver transmitters (USART1, USART2), which communicate at speeds of up to 6 Mbit/s.

They provide hardware management of the CTS, RTS and RS485 DE signals, multiprocessor communication mode, master synchronous communication and single-wire half-duplex communication mode. USART1 supports also SmartCard communication (ISO 7816), IrDA SIR ENDEC, LIN Master/Slave capability and auto baud rate feature, and has a clock domain independent from the CPU clock, allowing to wake up the MCU from Stop mode.

The USART interfaces can be served by the DMA controller.

Table 10. STM32F051xx USART implementation

| USART modes/features ⁽¹⁾ | USART1 | USART2 |
|---|--------|--------|
| Hardware flow control for modem | X | X |
| Continuous communication using DMA | X | X |
| Multiprocessor communication | X | X |
| Synchronous mode | X | X |
| Smartcard mode | X | - |
| Single-wire half-duplex communication | X | X |
| IrDA SIR ENDEC block | X | - |
| LIN mode | X | - |
| Dual clock domain and wakeup from Stop mode | X | - |
| Receiver timeout interrupt | X | - |
| Modbus communication | X | - |
| Auto baud rate detection | X | - |
| Driver Enable | X | X |

1. X = supported.

3.18 Serial peripheral interface (SPI)/Inter-integrated sound interfaces (I²S)

Up to two SPIs are able to communicate up to 18 Mbit/s in slave and master modes in full-duplex and half-duplex communication modes. The 3-bit prescaler gives 8 master mode frequencies and the frame size is configurable from 4 bits to 16 bits.

One standard I²S interface (multiplexed with SPI1) supporting four different audio standards can operate as master or slave at half-duplex communication mode. It can be configured to transfer 16 and 24 or 32 bits with 16-bit or 32-bit data resolution and synchronized by a specific signal. Audio sampling frequency from 8 kHz up to 192 kHz can be set by an 8-bit programmable linear prescaler. When operating in master mode, it can output a clock for an external audio component at 256 times the sampling frequency.

Table 11. STM32F051xx SPI/I2S implementation

| SPI features ⁽¹⁾ | SPI1 | SPI2 |
|-----------------------------|------|------|
| Hardware CRC calculation | X | X |
| Rx/Tx FIFO | X | X |
| NSS pulse mode | X | X |
| I2S mode | X | - |
| TI mode | X | X |

1. X = supported.

3.19 High-definition multimedia interface (HDMI) - consumer electronics control (CEC)

The device embeds a HDMI-CEC controller that provides hardware support for the Consumer Electronics Control (CEC) protocol (Supplement 1 to the HDMI standard).

This protocol provides high-level control functions between all audiovisual products in an environment. It is specified to operate at low speeds with minimum processing and memory overhead. It has a clock domain independent from the CPU clock, allowing the HDMI_CEC controller to wakeup the MCU from Stop mode on data reception.

3.20 Serial wire debug port (SW-DP)

An ARM SW-DP interface is provided to allow a serial wire debugging tool to be connected to the MCU.

4 Pinouts and pin descriptions

Figure 3. LQFP64 64-pin package pinout (top view)

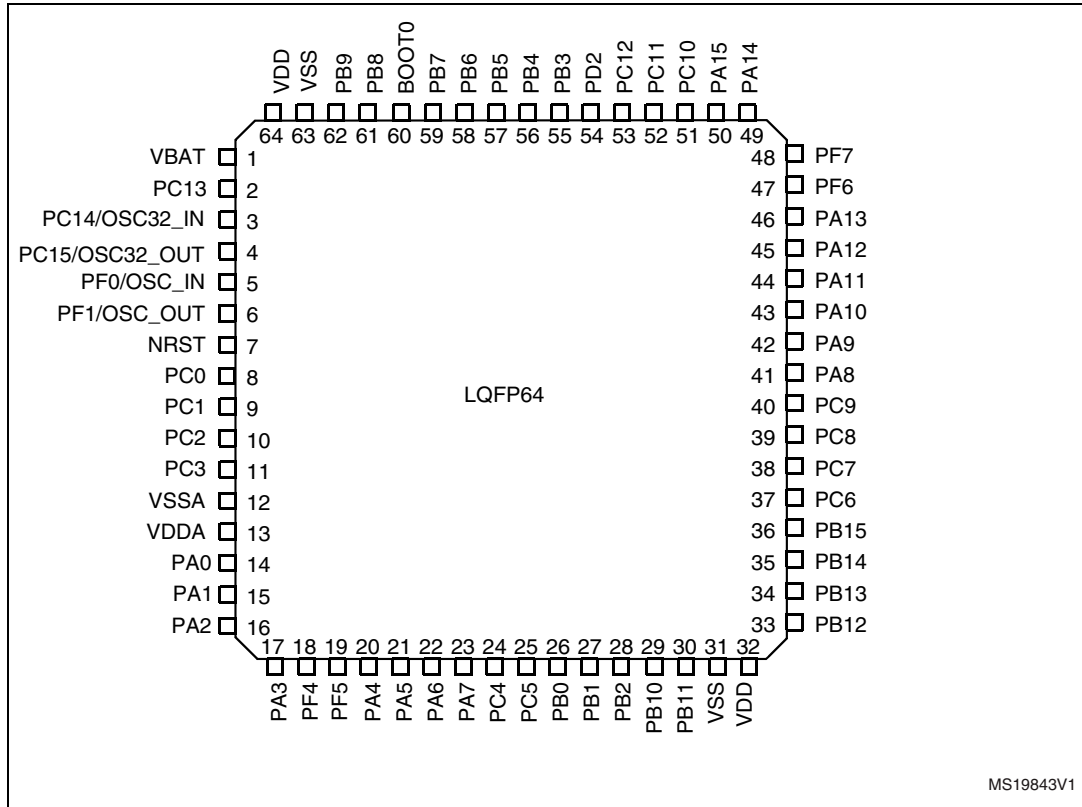


Figure 4. UFBGA64 64-pin package ball-out (top view)

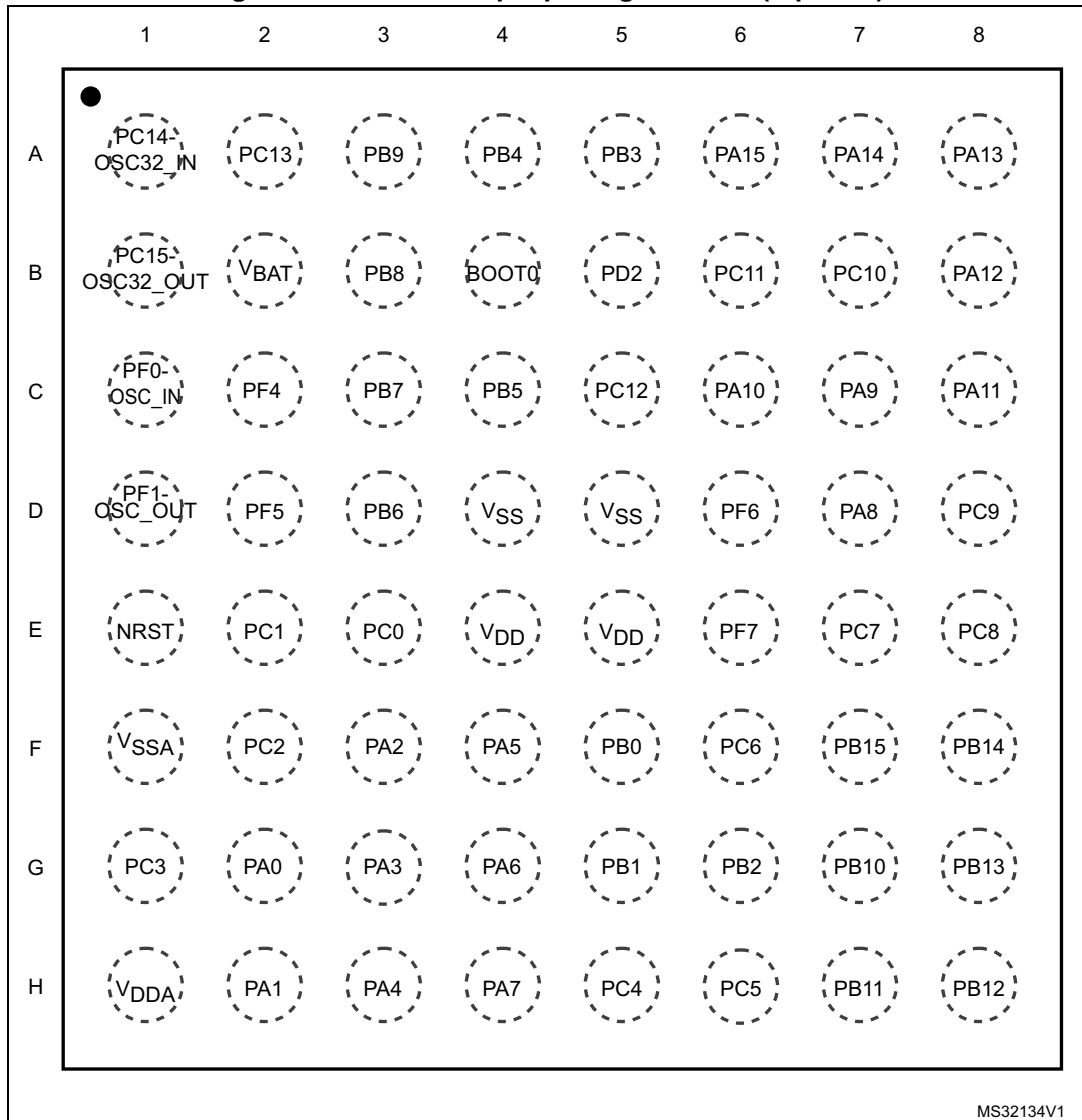


Figure 5. LQFP48 48-pin package pinout (top view)

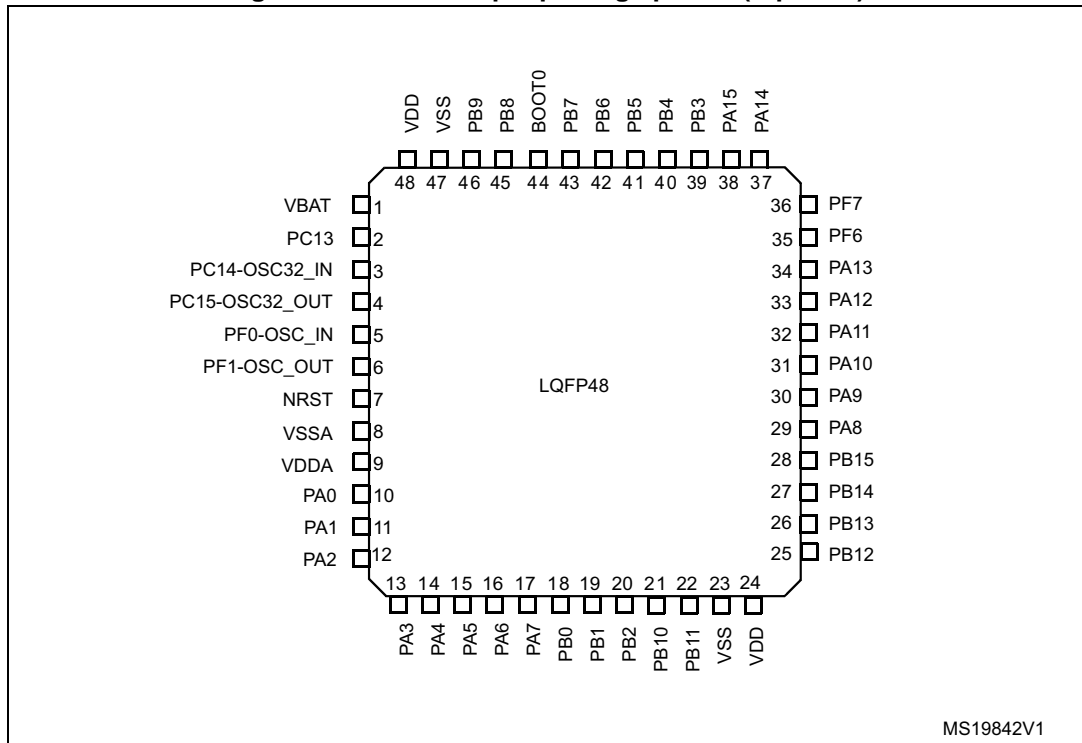


Figure 6. UFQFPN48 48-pin package pinout (top view)

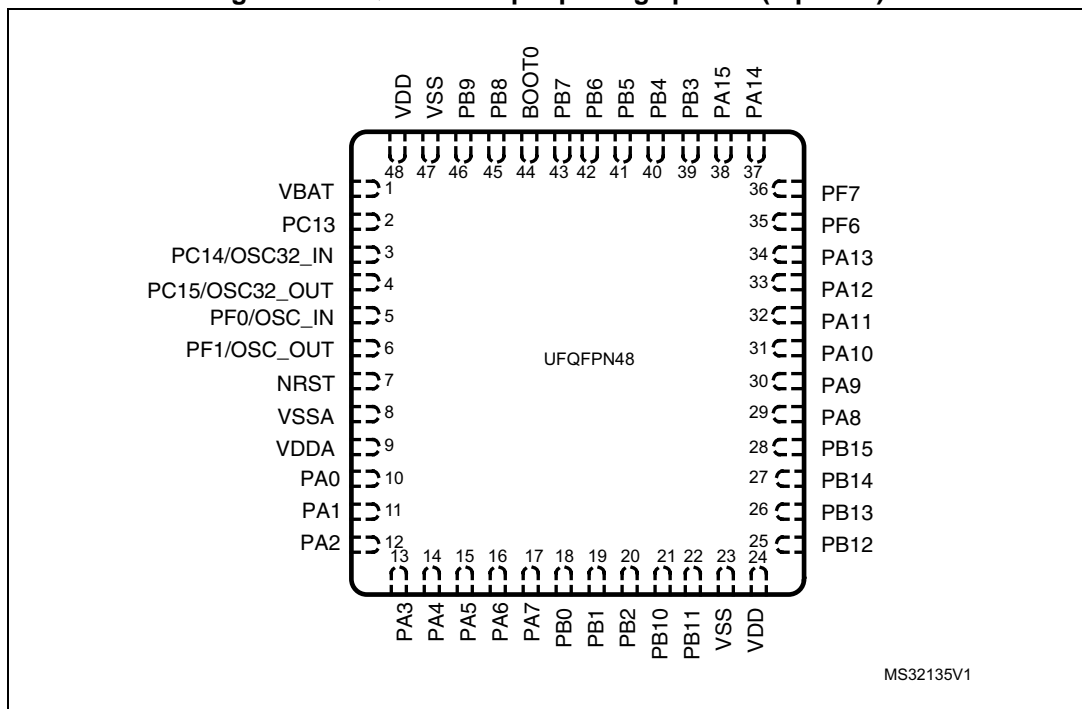
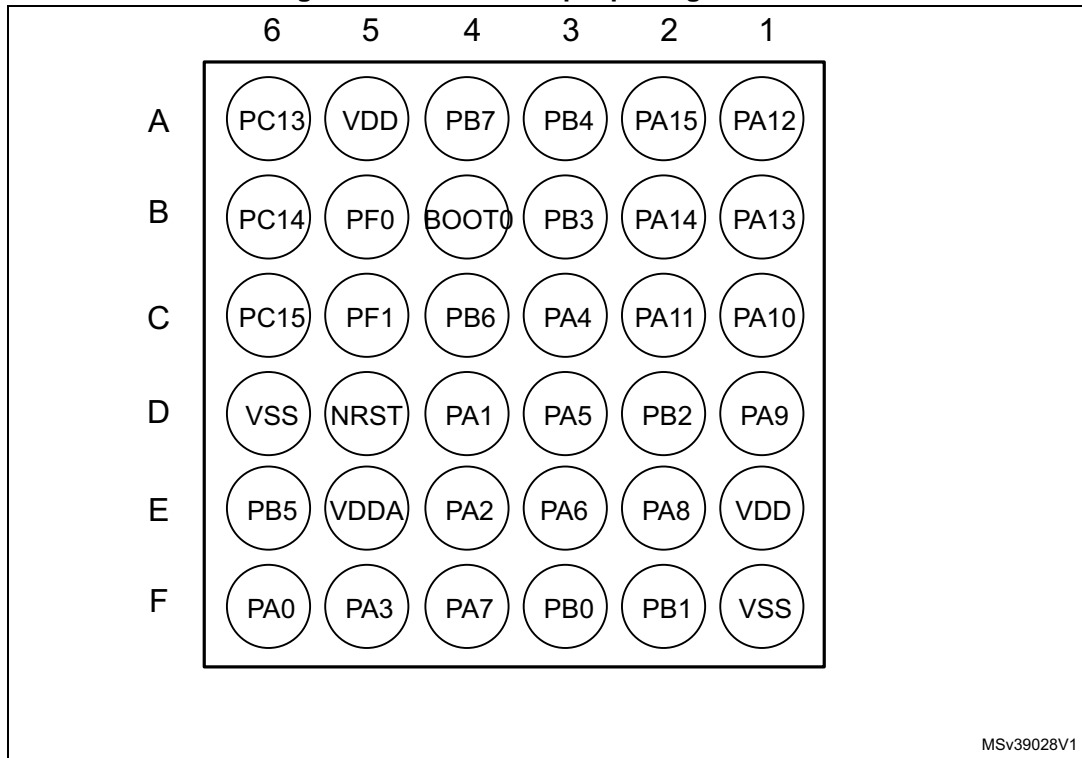


Figure 7. WLCSP36 36-pin package ball-out



1. The above figure shows the package bottom view.

Figure 8. LQFP32 32-pin package pinout (top view)

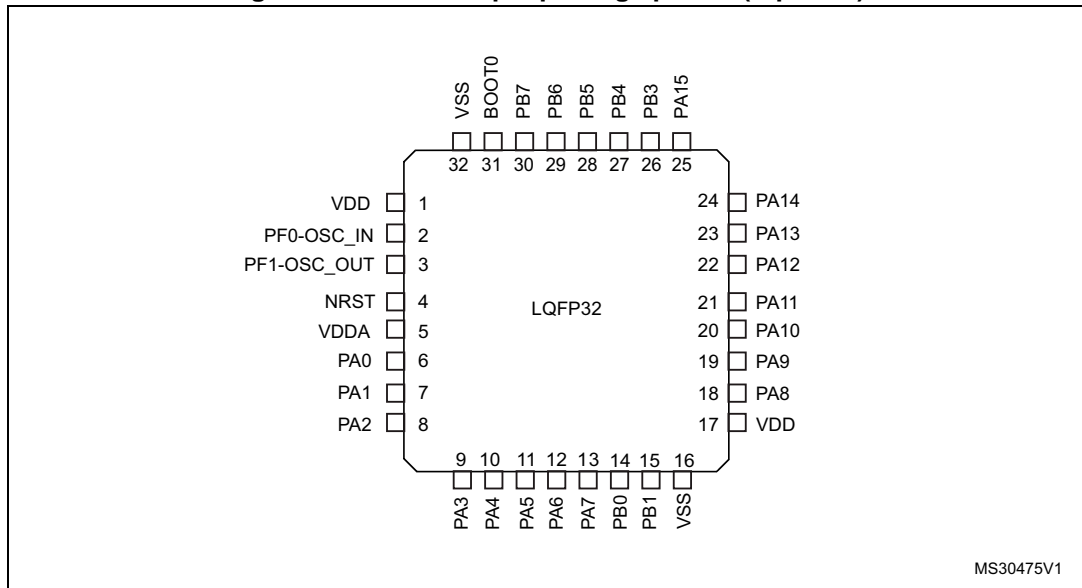
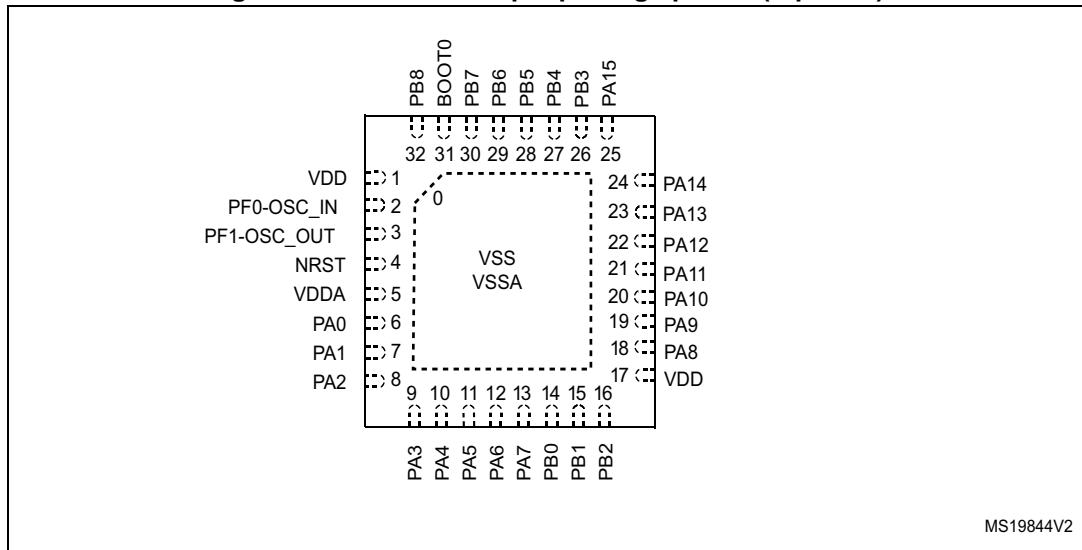


Figure 9. UFQFPN32 32-pin package pinout (top view)



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Table 12. Legend/abbreviations used in the pinout table

| Name | Abbreviation | Definition |
|---------------|---|--|
| Pin name | Unless otherwise specified in brackets below the pin name, the pin function during and after reset is the same as the actual pin name | |
| Pin type | S | Supply pin |
| | I | Input only pin |
| | I/O | Input / output pin |
| I/O structure | FT | 5 V tolerant I/O |
| | FTf | 5 V tolerant I/O, FM+ capable |
| | TTa | 3.3 V tolerant I/O directly connected to ADC |
| | TC | Standard 3.3 V I/O |
| | B | Dedicated BOOT0 pin |
| | RST | Bidirectional reset pin with embedded weak pull-up resistor |
| Notes | Unless otherwise specified by a note, all I/Os are set as floating inputs during and after reset. | |
| Pin functions | Alternate functions | Functions selected through GPIOx_AFR registers |
| | Additional functions | Functions directly selected/enabled through peripheral registers |

Table 13. Pin definitions

| Pin number | | | | | | Pin name (function after reset) | Pin type | I/O structure | Notes | Pin functions | |
|------------|---------|----------------|---------|--------|---------|---------------------------------------|----------|---------------|--------|---|--|
| LQFP64 | UFBGA64 | LQFP48/UQFPN48 | WLCSP36 | LQFP32 | UQFPN32 | | | | | Alternate functions | Additional functions |
| 1 | B2 | 1 | - | - | - | VBAT | S | - | - | Backup power supply | |
| 2 | A2 | 2 | A6 | - | - | PC13 | I/O | TC | (1)(2) | - | RTC_TAMP1, RTC_TS, RTC_OUT, WKUP2 |
| 3 | A1 | 3 | B6 | - | - | PC14-OSC32_IN (PC14) | I/O | TC | (1)(2) | - | OSC32_IN |
| 4 | B1 | 4 | C6 | - | - | PC15-OSC32_OUT (PC15) | I/O | TC | (1)(2) | - | OSC32_OUT |
| 5 | C1 | 5 | B5 | 2 | 2 | PF0-OSC_IN (PF0) | I/O | FT | - | - | OSC_IN |
| 6 | D1 | 6 | C5 | 3 | 3 | PF1-OSC_OUT (PF1) | I/O | FT | - | - | OSC_OUT |
| 7 | E1 | 7 | D5 | 4 | 4 | NRST | I/O | RST | - | Device reset input / internal reset output (active low) | |
| 8 | E3 | - | - | - | - | PC0 | I/O | TTa | - | EVENTOUT | ADC_IN10 |
| 9 | E2 | - | - | - | - | PC1 | I/O | TTa | - | EVENTOUT | ADC_IN11 |
| 10 | F2 | - | - | - | - | PC2 | I/O | TTa | - | EVENTOUT | ADC_IN12 |
| 11 | G1 | - | - | - | - | PC3 | I/O | TTa | - | EVENTOUT | ADC_IN13 |
| 12 | F1 | 8 | D6 | - | 0 | VSSA | S | - | - | Analog ground | |
| 13 | H1 | 9 | E5 | 5 | 5 | VDDA | S | - | - | Analog power supply | |
| 14 | G2 | 10 | F6 | 6 | 6 | PA0 | I/O | TTa | - | USART2_CTS, TIM2_CH1_ETR, COMP1_OUT, TSC_G1_IO1 | ADC_IN0, COMP1_INM6, RTC_TAMP2, WKUP1 |
| 15 | H2 | 11 | D4 | 7 | 7 | PA1 | I/O | TTa | - | USART2_RTS, TIM2_CH2, TSC_G1_IO2, EVENTOUT | ADC_IN1, COMP1_INP |
| 16 | F3 | 12 | E4 | 8 | 8 | PA2 | I/O | TTa | - | USART2_TX, TIM2_CH3, TIM15_CH1, COMP2_OUT, TSC_G1_IO3 | ADC_IN2, COMP2_INM6 |

Table 13. Pin definitions (continued)

| Pin number | | | | | | Pin name (function after reset) | Pin type | I/O structure | Notes | Pin functions | |
|------------|---------|-----------------|---------|--------|----------|---------------------------------------|----------|---------------|-------|--|--|
| LQFP64 | UFPGA64 | LQFP48/UFQFPN48 | WLCSP36 | LQFP32 | UFQFPN32 | | | | | Alternate functions | Additional functions |
| 17 | G3 | 13 | F5 | 9 | 9 | PA3 | I/O | TTa | - | USART2_RX, TIM2_CH4, TIM15_CH2, TSC_G1_IO4 | ADC_IN3, COMP2_INP |
| 18 | C2 | - | - | - | - | PF4 | I/O | FT | - | EVENTOUT | - |
| 19 | D2 | - | - | - | - | PF5 | I/O | FT | - | EVENTOUT | - |
| 20 | H3 | 14 | C3 | 10 | 10 | PA4 | I/O | TTa | - | SPI1_NSS, I2S1_WS, USART2_CK, TIM14_CH1, TSC_G2_IO1 | ADC_IN4, COMP1_INM4, COMP2_INM4, DAC_OUT1 |
| 21 | F4 | 15 | D3 | 11 | 11 | PA5 | I/O | TTa | - | SPI1_SCK, I2S1_CK, CEC, TIM2_CH1_ETR, TSC_G2_IO2 | ADC_IN5, COMP1_INM5, COMP2_INM5 |
| 22 | G4 | 16 | E3 | 12 | 12 | PA6 | I/O | TTa | - | SPI1_MISO, I2S1_MCK, TIM3_CH1, TIM1_BKIN, TIM16_CH1, COMP1_OUT, TSC_G2_IO3, EVENTOUT | ADC_IN6 |
| 23 | H4 | 17 | F4 | 13 | 13 | PA7 | I/O | TTa | - | SPI1_MOSI, I2S1_SD, TIM3_CH2, TIM14_CH1, TIM1_CH1N, TIM17_CH1, COMP2_OUT, TSC_G2_IO4, EVENTOUT | ADC_IN7 |
| 24 | H5 | - | - | - | - | PC4 | I/O | TTa | - | EVENTOUT | ADC_IN14 |
| 25 | H6 | - | - | - | - | PC5 | I/O | TTa | - | TSC_G3_IO1 | ADC_IN15 |
| 26 | F5 | 18 | F3 | 14 | 14 | PB0 | I/O | TTa | - | TIM3_CH3, TIM1_CH2N, TSC_G3_IO2, EVENTOUT | ADC_IN8 |

Table 13. Pin definitions (continued)

| Pin number | | | | | | Pin name (function after reset) | Pin type | I/O structure | Notes | Pin functions | |
|------------|---------|-----------------|---------|--------|----------|---------------------------------------|----------|---------------|-------|--|----------------------|
| LQFP64 | UFPGA64 | LQFP48/UFQFPN48 | WLCSP36 | LQFP32 | UFQFPN32 | | | | | Alternate functions | Additional functions |
| 27 | G5 | 19 | F2 | 15 | 15 | PB1 | I/O | TTa | - | TIM3_CH4, TIM14_CH1, TIM1_CH3N, TSC_G3_IO3 | ADC_IN9 |
| 28 | G6 | 20 | D2 | - | 16 | PB2 | I/O | FT | (3) | TSC_G3_IO4 | - |
| 29 | G7 | 21 | - | - | - | PB10 | I/O | FT | - | I2C2_SCL, CEC, TIM2_CH3, TSC_SYNC | - |
| 30 | H7 | 22 | - | - | - | PB11 | I/O | FT | - | I2C2_SDA, TIM2_CH4, TSC_G6_IO1, EVENTOUT | - |
| 31 | D4 | 23 | F1 | 16 | 0 | VSS | S | | - | Ground | |
| 32 | E4 | 24 | E1 | 17 | 17 | VDD | S | | - | Digital power supply | |
| 33 | H8 | 25 | - | - | - | PB12 | I/O | FT | - | SPI2_NSS, TIM1_BKIN, TSC_G6_IO2, EVENTOUT | - |
| 34 | G8 | 26 | - | - | - | PB13 | I/O | FT | - | SPI2_SCK, TIM1_CH1N, TSC_G6_IO3 | - |
| 35 | F8 | 27 | - | - | - | PB14 | I/O | FT | - | SPI2_MISO, TIM1_CH2N, TIM15_CH1, TSC_G6_IO4 | - |
| 36 | F7 | 28 | - | - | - | PB15 | I/O | FT | - | SPI2_MOSI, TIM1_CH3N, TIM15_CH1N, TIM15_CH2 | RTC_REFIN |
| 37 | F6 | - | - | - | - | PC6 | I/O | FT | - | TIM3_CH1 | - |
| 38 | E7 | - | - | - | - | PC7 | I/O | FT | - | TIM3_CH2 | - |
| 39 | E8 | - | - | - | - | PC8 | I/O | FT | - | TIM3_CH3 | - |
| 40 | D8 | - | - | - | - | PC9 | I/O | FT | - | TIM3_CH4 | - |

Table 13. Pin definitions (continued)

| Pin number | | | | | | Pin name (function after reset) | Pin type | I/O structure | Notes | Pin functions | |
|------------|---------|-----------------|---------|--------|----------|---------------------------------------|----------|---------------|-------|---|----------------------|
| LQFP64 | UFPGA64 | LQFP48/UFQFPN48 | WLCSP36 | LQFP32 | UFQFPN32 | | | | | Alternate functions | Additional functions |
| 41 | D7 | 29 | E2 | 18 | 18 | PA8 | I/O | FT | - | USART1_CK, TIM1_CH1, EVENTOUT, MCO | - |
| 42 | C7 | 30 | D1 | 19 | 19 | PA9 | I/O | FT | - | USART1_TX, TIM1_CH2, TIM15_BKIN, TSC_G4_IO1 | - |
| 43 | C6 | 31 | C1 | 20 | 20 | PA10 | I/O | FT | - | USART1_RX, TIM1_CH3, TIM17_BKIN, TSC_G4_IO2 | - |
| 44 | C8 | 32 | C2 | 21 | 21 | PA11 | I/O | FT | - | USART1_CTS, TIM1_CH4, COMP1_OUT, TSC_G4_IO3, EVENTOUT | - |
| 45 | B8 | 33 | A1 | 22 | 22 | PA12 | I/O | FT | - | USART1_RTS, TIM1_ETR, COMP2_OUT, TSC_G4_IO4, EVENTOUT | - |
| 46 | A8 | 34 | B1 | 23 | 23 | PA13 (SWDIO) | I/O | FT | (4) | IR_OUT, SWDIO | - |
| 47 | D6 | 35 | - | - | - | PF6 | I/O | FT | | I2C2_SCL | - |
| 48 | E6 | 36 | - | - | - | PF7 | I/O | FT | | I2C2_SDA | - |
| 49 | A7 | 37 | B2 | 24 | 24 | PA14 (SWCLK) | I/O | FT | (4) | USART2_TX, SWCLK | - |
| 50 | A6 | 38 | A2 | 25 | 25 | PA15 | I/O | FT | - | SPI1_NSS, I2S1_WS, USART2_RX, TIM2_CH1_ETR, EVENTOUT | - |
| 51 | B7 | - | - | - | - | PC10 | I/O | FT | - | | - |
| 52 | B6 | - | - | - | - | PC11 | I/O | FT | - | | - |
| 53 | C5 | - | - | - | - | PC12 | I/O | FT | - | | - |
| 54 | B5 | - | - | - | - | PD2 | I/O | FT | - | TIM3_ETR | - |

Table 13. Pin definitions (continued)

| Pin number | | | | | | Pin name (function after reset) | Pin type | I/O structure | Notes | Pin functions | |
|------------|---------|-----------------|---------|--------|----------|---------------------------------------|----------|---------------|-------|---|----------------------|
| LQFP64 | UFPGA64 | LQFP48/UFQFPN48 | WLCSP36 | LQFP32 | UFQFPN32 | | | | | Alternate functions | Additional functions |
| 55 | A5 | 39 | B3 | 26 | 26 | PB3 | I/O | FT | - | SPI1_SCK, I2S1_CK, TIM2_CH2, TSC_G5_IO1, EVENTOUT | - |
| 56 | A4 | 40 | A3 | 27 | 27 | PB4 | I/O | FT | - | SPI1_MISO, I2S1_MCK, TIM3_CH1, TSC_G5_IO2, EVENTOUT | - |
| 57 | C4 | 41 | E6 | 28 | 28 | PB5 | I/O | FT | - | SPI1_MOSI, I2S1_SD, I2C1_SMBA, TIM16_BKIN, TIM3_CH2 | - |
| 58 | D3 | 42 | C4 | 29 | 29 | PB6 | I/O | FTf | - | I2C1_SCL, USART1_TX, TIM16_CH1N, TSC_G5_IO3 | - |
| 59 | C3 | 43 | A4 | 30 | 30 | PB7 | I/O | FTf | - | I2C1_SDA, USART1_RX, TIM17_CH1N, TSC_G5_IO4 | - |
| 60 | B4 | 44 | B4 | 31 | 31 | BOOT0 | I | B | - | Boot memory selection | |
| 61 | B3 | 45 | - | - | 32 | PB8 | I/O | FTf | (3) | I2C1_SCL, CEC, TIM16_CH1, TSC_SYNC | - |
| 62 | A3 | 46 | - | - | - | PB9 | I/O | FTf | - | I2C1_SDA, IR_OUT, TIM17_CH1, EVENTOUT | - |
| 63 | D5 | 47 | D6 | 32 | 0 | VSS | S | | - | Ground | |
| 64 | E5 | 48 | A5 | 1 | 1 | VDD | S | | - | Digital power supply | |

1. PC13, PC14 and PC15 are supplied through the power switch. Since the switch only sinks a limited amount of current (3 mA), the use of GPIOs PC13 to PC15 in output mode is limited:
 - The speed should not exceed 2 MHz with a maximum load of 30 pF.
 - These GPIOs must not be used as current sources (e.g. to drive an LED).

2. After the first RTC domain power-up, PC13, PC14 and PC15 operate as GPIOs. Their function then depends on the content of the RTC registers which are not reset by the main reset. For details on how to manage these GPIOs, refer to the RTC domain and RTC register descriptions in the reference manual.



3. On the LQFP32 package, PB2 and PB8 should be treated as unconnected pins (even when they are not available on the package, they are not forced to a defined level by hardware).
4. After reset, these pins are configured as SWDIO and SWCLK alternate functions, and the internal pull-up on the SWDIO pin and the internal pull-down on the SWCLK pin are activated.



Table 14. Alternate functions selected through GPIOA_AFR registers for port A

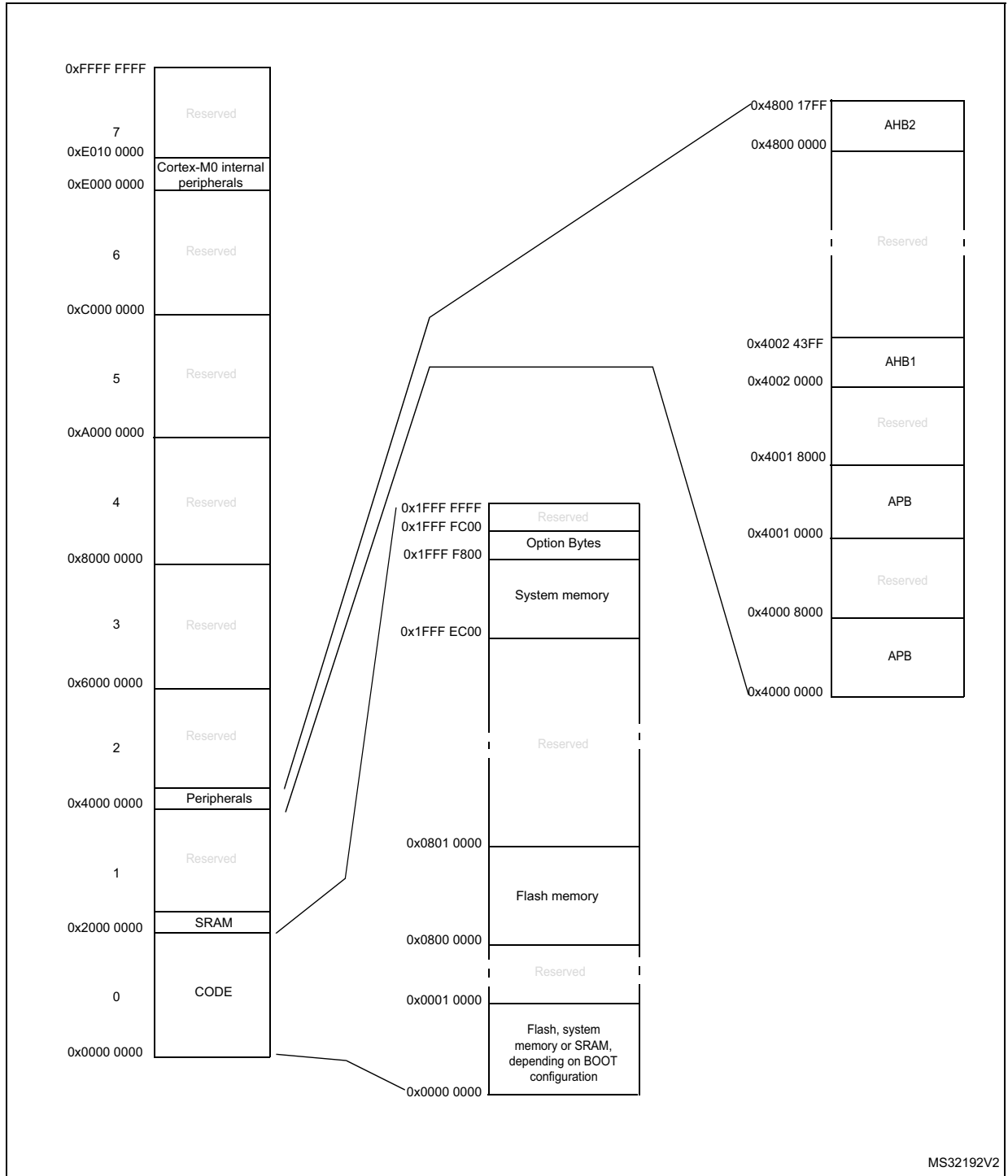
| Pin name | AF0 | AF1 | AF2 | AF3 | AF4 | AF5 | AF6 | AF7 |
|----------|---------------------|------------|--------------|------------|-----------|-----------|----------|-----------|
| PA0 | - | USART2_CTS | TIM2_CH1_ETR | TSC_G1_IO1 | | - | - | COMP1_OUT |
| PA1 | EVENTOUT | USART2_RTS | TIM2_CH2 | TSC_G1_IO2 | | | - | - |
| PA2 | TIM15_CH1 | USART2_TX | TIM2_CH3 | TSC_G1_IO3 | - | - | - | COMP2_OUT |
| PA3 | TIM15_CH2 | USART2_RX | TIM2_CH4 | TSC_G1_IO4 | - | - | - | - |
| PA4 | SPI1_NSS, I2S1_WS | USART2_CK | - | TSC_G2_IO1 | TIM14_CH1 | - | - | - |
| PA5 | SPI1_SCK, I2S1_CK | CEC | TIM2_CH1_ETR | TSC_G2_IO2 | - | - | - | - |
| PA6 | SPI1_MISO, I2S1_MCK | TIM3_CH1 | TIM1_BKIN | TSC_G2_IO3 | | TIM16_CH1 | EVENTOUT | COMP1_OUT |
| PA7 | SPI1_MOSI, I2S1_SD | TIM3_CH2 | TIM1_CH1N | TSC_G2_IO4 | TIM14_CH1 | TIM17_CH1 | EVENTOUT | COMP2_OUT |
| PA8 | MCO | USART1_CK | TIM1_CH1 | EVENTOUT | | - | - | - |
| PA9 | TIM15_BKIN | USART1_TX | TIM1_CH2 | TSC_G4_IO1 | - | - | - | - |
| PA10 | TIM17_BKIN | USART1_RX | TIM1_CH3 | TSC_G4_IO2 | - | - | - | - |
| PA11 | EVENTOUT | USART1_CTS | TIM1_CH4 | TSC_G4_IO3 | - | - | - | COMP1_OUT |
| PA12 | EVENTOUT | USART1_RTS | TIM1_ETR | TSC_G4_IO4 | - | - | - | COMP2_OUT |
| PA13 | SWDIO | IR_OUT | | - | - | - | - | - |
| PA14 | SWCLK | USART2_TX | - | - | - | - | - | - |
| PA15 | SPI1_NSS, I2S1_WS | USART2_RX | TIM2_CH1_ETR | EVENTOUT | | - | - | - |

Table 15. Alternate functions selected through GPIOB_AFR registers for port B

| Pin name | AF0 | AF1 | AF2 | AF3 |
|----------|---------------------|-----------|------------|------------|
| PB0 | EVENTOUT | TIM3_CH3 | TIM1_CH2N | TSC_G3_IO2 |
| PB1 | TIM14_CH1 | TIM3_CH4 | TIM1_CH3N | TSC_G3_IO3 |
| PB2 | | | | TSC_G3_IO4 |
| PB3 | SPI1_SCK, I2S1_CK | EVENTOUT | TIM2_CH2 | TSC_G5_IO1 |
| PB4 | SPI1_MISO, I2S1_MCK | TIM3_CH1 | EVENTOUT | TSC_G5_IO2 |
| PB5 | SPI1_MOSI, I2S1_SD | TIM3_CH2 | TIM16_BKIN | I2C1_SMBA |
| PB6 | USART1_TX | I2C1_SCL | TIM16_CH1N | TSC_G5_IO3 |
| PB7 | USART1_RX | I2C1_SDA | TIM17_CH1N | TSC_G5_IO4 |
| PB8 | CEC | I2C1_SCL | TIM16_CH1 | TSC_SYNC |
| PB9 | IR_OUT | I2C1_SDA | TIM17_CH1 | EVENTOUT |
| PB10 | CEC | I2C2_SCL | TIM2_CH3 | TSC_SYNC |
| PB11 | EVENTOUT | I2C2_SDA | TIM2_CH4 | TSC_G6_IO1 |
| PB12 | SPI2_NSS | EVENTOUT | TIM1_BKIN | TSC_G6_IO2 |
| PB13 | SPI2_SCK | | TIM1_CH1N | TSC_G6_IO3 |
| PB14 | SPI2_MISO | TIM15_CH1 | TIM1_CH2N | TSC_G6_IO4 |
| PB15 | SPI2_MOSI | TIM15_CH2 | TIM1_CH3N | TIM15_CH1N |

5 Memory mapping

Figure 10. STM32F051xx memory map



MS32192V2

Table 16. STM32F051xx peripheral register boundary addresses

| Bus | Boundary address | Size | Peripheral |
|------|---------------------------|---------|-----------------|
| | 0x4800 1800 - 0x5FFF FFFF | ~384 MB | Reserved |
| AHB2 | 0x4800 1400 - 0x4800 17FF | 1 KB | GPIOF |
| | 0x4800 1000 - 0x4800 13FF | 1 KB | Reserved |
| | 0x4800 0C00 - 0x4800 0FFF | 1 KB | GPIOD |
| | 0x4800 0800 - 0x4800 0BFF | 1 KB | GPIOC |
| | 0x4800 0400 - 0x4800 07FF | 1 KB | GPIOB |
| | 0x4800 0000 - 0x4800 03FF | 1 KB | GPIOA |
| | 0x4002 4400 - 0x47FF FFFF | ~128 MB | Reserved |
| AHB1 | 0x4002 4000 - 0x4002 43FF | 1 KB | TSC |
| | 0x4002 3400 - 0x4002 3FFF | 3 KB | Reserved |
| | 0x4002 3000 - 0x4002 33FF | 1 KB | CRC |
| | 0x4002 2400 - 0x4002 2FFF | 3 KB | Reserved |
| | 0x4002 2000 - 0x4002 23FF | 1 KB | FLASH Interface |
| | 0x4002 1400 - 0x4002 1FFF | 3 KB | Reserved |
| | 0x4002 1000 - 0x4002 13FF | 1 KB | RCC |
| | 0x4002 0400 - 0x4002 0FFF | 3 KB | Reserved |
| | 0x4002 0000 - 0x4002 03FF | 1 KB | DMA |
| | 0x4001 8000 - 0x4001 FFFF | 32 KB | Reserved |
| APB | 0x4001 5C00 - 0x4001 7FFF | 9 KB | Reserved |
| | 0x4001 5800 - 0x4001 5BFF | 1 KB | DBGMCU |
| | 0x4001 4C00 - 0x4001 57FF | 3 KB | Reserved |
| | 0x4001 4800 - 0x4001 4BFF | 1 KB | TIM17 |
| | 0x4001 4400 - 0x4001 47FF | 1 KB | TIM16 |
| | 0x4001 4000 - 0x4001 43FF | 1 KB | TIM15 |
| | 0x4001 3C00 - 0x4001 3FFF | 1 KB | Reserved |
| | 0x4001 3800 - 0x4001 3BFF | 1 KB | USART1 |
| | 0x4001 3400 - 0x4001 37FF | 1 KB | Reserved |
| | 0x4001 3000 - 0x4001 33FF | 1 KB | SPI1/I2S1 |
| | 0x4001 2C00 - 0x4001 2FFF | 1 KB | TIM1 |
| | 0x4001 2800 - 0x4001 2BFF | 1 KB | Reserved |
| | 0x4001 2400 - 0x4001 27FF | 1 KB | ADC |
| | 0x4001 0800 - 0x4001 23FF | 7 KB | Reserved |
| | 0x4001 0400 - 0x4001 07FF | 1 KB | EXTI |
| | 0x4001 0000 - 0x4001 03FF | 1 KB | SYSCFG + COMP |

Table 16. STM32F051xx peripheral register boundary addresses (continued)

| Bus | Boundary address | Size | Peripheral |
|---------------------------|---------------------------|-------|------------|
| | 0x4000 8000 - 0x4000 FFFF | 32 KB | Reserved |
| APB | 0x4000 7C00 - 0x4000 7FFF | 1 KB | Reserved |
| | 0x4000 7800 - 0x4000 7BFF | 1 KB | CEC |
| | 0x4000 7400 - 0x4000 77FF | 1 KB | DAC |
| | 0x4000 7000 - 0x4000 73FF | 1 KB | PWR |
| | 0x4000 5C00 - 0x4000 6FFF | 5 KB | Reserved |
| | 0x4000 5800 - 0x4000 5BFF | 1 KB | I2C2 |
| | 0x4000 5400 - 0x4000 57FF | 1 KB | I2C1 |
| | 0x4000 4800 - 0x4000 53FF | 3 KB | Reserved |
| | 0x4000 4400 - 0x4000 47FF | 1 KB | USART2 |
| | 0x4000 3C00 - 0x4000 43FF | 2 KB | Reserved |
| | 0x4000 3800 - 0x4000 3BFF | 1 KB | SPI2 |
| | 0x4000 3400 - 0x4000 37FF | 1 KB | Reserved |
| | 0x4000 3000 - 0x4000 33FF | 1 KB | IWDG |
| | 0x4000 2C00 - 0x4000 2FFF | 1 KB | WWDG |
| | 0x4000 2800 - 0x4000 2BFF | 1 KB | RTC |
| | 0x4000 2400 - 0x4000 27FF | 1 KB | Reserved |
| | 0x4000 2000 - 0x4000 23FF | 1 KB | TIM14 |
| | 0x4000 1400 - 0x4000 1FFF | 3 KB | Reserved |
| | 0x4000 1000 - 0x4000 13FF | 1 KB | TIM6 |
| | 0x4000 0800 - 0x4000 0FFF | 2 KB | Reserved |
| 0x4000 0400 - 0x4000 07FF | 1 KB | TIM3 | |
| 0x4000 0000 - 0x4000 03FF | 1 KB | TIM2 | |

6 Electrical characteristics

6.1 Parameter conditions

Unless otherwise specified, all voltages are referenced to V_{SS} .

6.1.1 Minimum and maximum values

Unless otherwise specified, the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at $T_A = 25\text{ }^\circ\text{C}$ and $T_A = T_{A\text{max}}$ (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean $\pm 3\sigma$).

6.1.2 Typical values

Unless otherwise specified, typical data are based on $T_A = 25\text{ }^\circ\text{C}$, $V_{DD} = V_{DDA} = 3.3\text{ V}$. They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated (mean $\pm 2\sigma$).

6.1.3 Typical curves

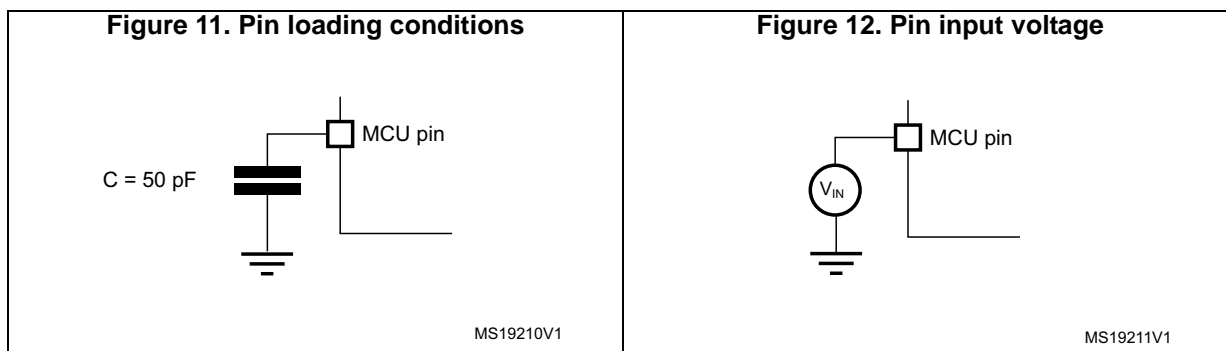
Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

6.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in [Figure 11](#).

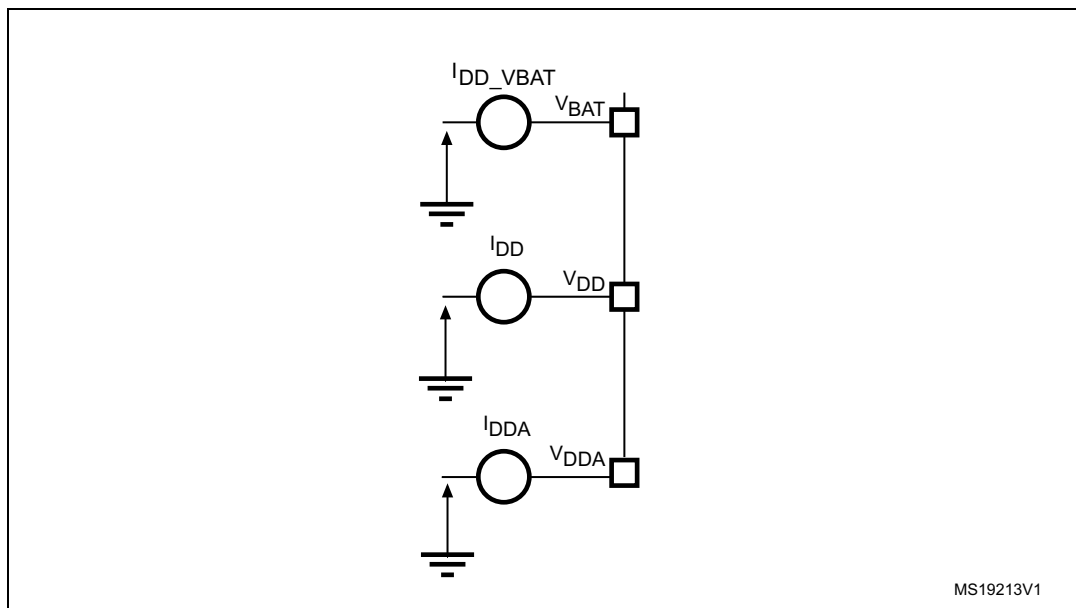
6.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in [Figure 12](#).



6.1.7 Current consumption measurement

Figure 14. Current consumption measurement scheme



6.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in [Table 17: Voltage characteristics](#), [Table 18: Current characteristics](#) and [Table 19: Thermal characteristics](#) may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 17. Voltage characteristics⁽¹⁾

| Symbol | Ratings | Min | Max | Unit |
|----------------------|--|--|-------------------------|------|
| $V_{DD}-V_{SS}$ | External main supply voltage | -0.3 | 4.0 | V |
| $V_{DDA}-V_{SS}$ | External analog supply voltage | -0.3 | 4.0 | V |
| $V_{DD}-V_{DDA}$ | Allowed voltage difference for $V_{DD} > V_{DDA}$ | - | 0.4 | V |
| $V_{BAT}-V_{SS}$ | External backup supply voltage | -0.3 | 4.0 | V |
| $V_{IN}^{(2)}$ | Input voltage on FT and FTf pins | $V_{SS} - 0.3$ | $V_{DDIOx} + 4.0^{(3)}$ | V |
| | Input voltage on TTa pins | $V_{SS} - 0.3$ | 4.0 | V |
| | BOOT0 | 0 | 9.0 | V |
| | Input voltage on any other pin | $V_{SS} - 0.3$ | 4.0 | V |
| $ \Delta V_{DDx} $ | Variations between different V_{DD} power pins | - | 50 | mV |
| $ V_{SSx} - V_{SS} $ | Variations between all the different ground pins | - | 50 | mV |
| $V_{ESD(HBM)}$ | Electrostatic discharge voltage (human body model) | see Section 6.3.12: Electrical sensitivity characteristics | | |

1. All main power (V_{DD} , V_{DDA}) and ground (V_{SS} , V_{SSA}) pins must always be connected to the external power supply, in the permitted range.
2. V_{IN} maximum must always be respected. Refer to [Table 18: Current characteristics](#) for the maximum allowed injected current values.
3. Valid only if the internal pull-up/pull-down resistors are disabled. If internal pull-up or pull-down resistor is enabled, the maximum limit is 4 V.

Table 18. Current characteristics

| Symbol | Ratings | Max. | Unit |
|-----------------------|---|----------------------|------|
| ΣI_{VDD} | Total current into sum of all VDD power lines (source) ⁽¹⁾ | 120 | mA |
| ΣI_{VSS} | Total current out of sum of all VSS ground lines (sink) ⁽¹⁾ | -120 | |
| $I_{VDD(PIN)}$ | Maximum current into each VDD power pin (source) ⁽¹⁾ | 100 | |
| $I_{VSS(PIN)}$ | Maximum current out of each VSS ground pin (sink) ⁽¹⁾ | -100 | |
| $I_{IO(PIN)}$ | Output current sunk by any I/O and control pin | 25 | |
| | Output current source by any I/O and control pin | -25 | |
| $\Sigma I_{IO(PIN)}$ | Total output current sunk by sum of all I/Os and control pins ⁽²⁾ | 80 | |
| | Total output current sourced by sum of all I/Os and control pins ⁽²⁾ | -80 | |
| $I_{INJ(PIN)}^{(3)}$ | Injected current on B, FT and FTf pins | -5/+0 ⁽⁴⁾ | |
| | Injected current on TC and RST pin | ± 5 | |
| | Injected current on TTa pins ⁽⁵⁾ | ± 5 | |
| $\Sigma I_{INJ(PIN)}$ | Total injected current (sum of all I/O and control pins) ⁽⁶⁾ | ± 25 | |

1. All main power (VDD, VDDA) and ground (VSS, VSSA) pins must always be connected to the external power supply, in the permitted range.
2. This current consumption must be correctly distributed over all I/Os and control pins. The total output current must not be sunk/sourced between two consecutive power supply pins referring to high pin count QFP packages.
3. A positive injection is induced by $V_{IN} > V_{DDIOx}$ while a negative injection is induced by $V_{IN} < V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. Refer to [Table 17: Voltage characteristics](#) for the maximum allowed input voltage values.
4. Positive injection is not possible on these I/Os and does not occur for input voltages lower than the specified maximum value.
5. On these I/Os, a positive injection is induced by $V_{IN} > V_{DDA}$. Negative injection disturbs the analog performance of the device. See note ⁽²⁾ below [Table 54: ADC accuracy](#).
6. When several inputs are submitted to a current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values).

Table 19. Thermal characteristics

| Symbol | Ratings | Value | Unit |
|-----------|------------------------------|-------------|------|
| T_{STG} | Storage temperature range | -65 to +150 | °C |
| T_J | Maximum junction temperature | 150 | °C |

6.3 Operating conditions

6.3.1 General operating conditions

Table 20. General operating conditions

| Symbol | Parameter | Conditions | Min | Max | Unit |
|------------|---|--|----------|---------------------|------|
| f_{HCLK} | Internal AHB clock frequency | - | 0 | 48 | MHz |
| f_{PCLK} | Internal APB clock frequency | - | 0 | 48 | |
| V_{DD} | Standard operating voltage | - | 2.0 | 3.6 | V |
| V_{DDA} | Analog operating voltage (ADC and DAC not used) | Must have a potential equal to or higher than V_{DD} | V_{DD} | 3.6 | V |
| | Analog operating voltage (ADC and DAC used) | | 2.4 | 3.6 | |
| V_{BAT} | Backup operating voltage | - | 1.65 | 3.6 | V |
| V_{IN} | I/O input voltage | TC and RST I/O | -0.3 | $V_{DDIOx}+0.3$ | V |
| | | TTa I/O | -0.3 | $V_{DDA}+0.3^{(1)}$ | |
| | | FT and FTf I/O | -0.3 | $5.5^{(1)}$ | |
| | | BOOT0 | 0 | 5.5 | |
| P_D | Power dissipation at $T_A = 85\text{ °C}$ for suffix 6 or $T_A = 105\text{ °C}$ for suffix 7 ⁽²⁾ | LQFP64 | - | 444 | mW |
| | | LQFP48 | - | 364 | |
| | | LQFP32 | - | 357 | |
| | | UFQFPN32 | - | 526 | |
| | | UFQFPN48 | - | 625 | |
| | | UFBGA64 | - | 308 | |
| | | WLCSP36 | - | 333 | |
| T_A | Ambient temperature for the suffix 6 version | Maximum power dissipation | -40 | 85 | °C |
| | | Low power dissipation ⁽³⁾ | -40 | 105 | |
| | Ambient temperature for the suffix 7 version | Maximum power dissipation | -40 | 105 | °C |
| | | Low power dissipation ⁽³⁾ | -40 | 125 | |
| T_J | Junction temperature range | Suffix 6 version | -40 | 105 | °C |
| | | Suffix 7 version | -40 | 125 | |

1. For operation with a voltage higher than $V_{DDIOx} + 0.3\text{ V}$, the internal pull-up resistor must be disabled.
2. If T_A is lower, higher P_D values are allowed as long as T_J does not exceed T_{Jmax} . See [Section 7.8: Thermal characteristics](#).
3. In low power dissipation state, T_A can be extended to this range as long as T_J does not exceed T_{Jmax} (see [Section 7.8: Thermal characteristics](#)).

6.3.2 Operating conditions at power-up / power-down

The parameters given in [Table 21](#) are derived from tests performed under the ambient temperature condition summarized in [Table 20](#).

Table 21. Operating conditions at power-up / power-down

| Symbol | Parameter | Conditions | Min | Max | Unit |
|------------|--------------------------|------------|-----|----------|-----------------|
| t_{VDD} | V_{DD} rise time rate | - | 0 | ∞ | $\mu\text{s/V}$ |
| | V_{DD} fall time rate | | 20 | ∞ | |
| t_{VDDA} | V_{DDA} rise time rate | - | 0 | ∞ | |
| | V_{DDA} fall time rate | | 20 | ∞ | |

6.3.3 Embedded reset and power control block characteristics

The parameters given in [Table 22](#) are derived from tests performed under the ambient temperature and supply voltage conditions summarized in [Table 20: General operating conditions](#).

Table 22. Embedded reset and power control block characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|----------------------|-------------------------------------|-----------------------------|---------------------|------|---------------------|------|
| $V_{POR/PDR}^{(1)}$ | Power on/power down reset threshold | Falling edge ⁽²⁾ | 1.80 | 1.88 | 1.96 ⁽³⁾ | V |
| | | Rising edge | 1.84 ⁽³⁾ | 1.92 | 2.00 | V |
| $V_{PDRhyst}$ | PDR hysteresis | | - | 40 | - | mV |
| $t_{RSTTEMPO}^{(4)}$ | Reset temporization | | 1.50 | 2.50 | 4.50 | ms |

1. The PDR detector monitors V_{DD} and also V_{DDA} (if kept enabled in the option bytes). The POR detector monitors only V_{DD} .
2. The product behavior is guaranteed by design down to the minimum $V_{POR/PDR}$ value.
3. Data based on characterization results, not tested in production.
4. Guaranteed by design, not tested in production.

Table 23. Programmable voltage detector characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|------------|-----------------|--------------|------|------|------|------|
| V_{PVD0} | PVD threshold 0 | Rising edge | 2.1 | 2.18 | 2.26 | V |
| | | Falling edge | 2 | 2.08 | 2.16 | V |
| V_{PVD1} | PVD threshold 1 | Rising edge | 2.19 | 2.28 | 2.37 | V |
| | | Falling edge | 2.09 | 2.18 | 2.27 | V |
| V_{PVD2} | PVD threshold 2 | Rising edge | 2.28 | 2.38 | 2.48 | V |
| | | Falling edge | 2.18 | 2.28 | 2.38 | V |
| V_{PVD3} | PVD threshold 3 | Rising edge | 2.38 | 2.48 | 2.58 | V |
| | | Falling edge | 2.28 | 2.38 | 2.48 | V |

Table 23. Programmable voltage detector characteristics (continued)

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-------------------------------------|-------------------------|--------------|------|------|---------------------|------|
| V _{PVD4} | PVD threshold 4 | Rising edge | 2.47 | 2.58 | 2.69 | V |
| | | Falling edge | 2.37 | 2.48 | 2.59 | V |
| V _{PVD5} | PVD threshold 5 | Rising edge | 2.57 | 2.68 | 2.79 | V |
| | | Falling edge | 2.47 | 2.58 | 2.69 | V |
| V _{PVD6} | PVD threshold 6 | Rising edge | 2.66 | 2.78 | 2.9 | V |
| | | Falling edge | 2.56 | 2.68 | 2.8 | V |
| V _{PVD7} | PVD threshold 7 | Rising edge | 2.76 | 2.88 | 3 | V |
| | | Falling edge | 2.66 | 2.78 | 2.9 | V |
| V _{PVDhyst} ⁽¹⁾ | PVD hysteresis | | - | 100 | - | mV |
| I _{DD(PVD)} | PVD current consumption | | - | 0.15 | 0.26 ⁽¹⁾ | μA |

1. Guaranteed by design, not tested in production.

6.3.4 Embedded reference voltage

The parameters given in [Table 24](#) are derived from tests performed under the ambient temperature and supply voltage conditions summarized in [Table 20: General operating conditions](#).

Table 24. Embedded internal reference voltage

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|------------------------|---|-----------------------------------|----------------------|-----|---------------------|--------|
| V _{REFINT} | Internal reference voltage | -40 °C < T _A < +105 °C | 1.16 | 1.2 | 1.25 | V |
| | | -40 °C < T _A < +85 °C | 1.16 | 1.2 | 1.24 ⁽¹⁾ | V |
| t _{START} | ADC_IN17 buffer startup time | - | - | - | 10 ⁽²⁾ | μs |
| t _{S_vrefint} | ADC sampling time when reading the internal reference voltage | - | 4 ⁽²⁾ | - | - | μs |
| ΔV _{REFINT} | Internal reference voltage spread over the temperature range | V _{DDA} = 3 V | - | - | 10 ⁽²⁾ | mV |
| T _{Coeff} | Temperature coefficient | - | - 100 ⁽²⁾ | - | 100 ⁽²⁾ | ppm/°C |

1. Data based on characterization results, not tested in production.

2. Guaranteed by design, not tested in production.

6.3.5 Supply current characteristics

The current consumption is a function of several parameters and factors such as the operating voltage, ambient temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed binary code.

The current consumption is measured as described in [Figure 14: Current consumption measurement scheme](#).

All Run-mode current consumption measurements given in this section are performed with a reduced code that gives a consumption equivalent to CoreMark code.

Typical and maximum current consumption

The MCU is placed under the following conditions:

- All I/O pins are in analog input mode
- All peripherals are disabled except when explicitly mentioned
- The Flash memory access time is adjusted to the f_{HCLK} frequency:
 - 0 wait state and Prefetch OFF from 0 to 24 MHz
 - 1 wait state and Prefetch ON above 24 MHz
- When the peripherals are enabled $f_{PCLK} = f_{HCLK}$

The parameters given in [Table 25](#) to [Table 31](#) are derived from tests performed under ambient temperature and supply voltage conditions summarized in [Table 20: General operating conditions](#).

Table 25. Typical and maximum current consumption from the V_{DD} supply at V_{DD} = 3.6 V

| Symbol | Parameter | Conditions | f _{HCLK} | All peripherals enabled | | | | All peripherals disabled | | | | Unit | |
|-----------------|--|---|--------------------|-------------------------|-------------------------------------|---------------------|--------|--------------------------|-------------------------------------|---------------------|--------|--------------------|---------------------|
| | | | | Typ | Max @ T _A ⁽¹⁾ | | | Typ | Max @ T _A ⁽¹⁾ | | | | |
| | | | | | 25 °C | 85 °C | 105 °C | | 25 °C | 85 °C | 105 °C | | |
| I _{DD} | Supply current in Run mode, code executing from Flash | HSE bypass, PLL on | 48 MHz | 22.0 | 22.8 | 22.8 | 23.8 | 11.8 | 12.7 | 12.7 | 13.3 | mA | |
| | | | 32 MHz | 15.0 | 15.5 | 15.5 | 16.0 | 7.6 | 8.7 | 8.7 | 9.0 | | |
| | | | 24 MHz | 12.2 | 13.2 | 13.2 | 13.6 | 7.2 | 7.9 | 7.9 | 8.1 | | |
| | | HSE bypass, PLL off | 8 MHz | 4.4 | 5.2 | 5.2 | 5.4 | 2.7 | 2.9 | 2.9 | 3.0 | | |
| | | | 1 MHz | 1.0 | 1.3 | 1.3 | 1.4 | 0.7 | 0.9 | 0.9 | 0.9 | | |
| | | HSI clock, PLL on | 48 MHz | 22.0 | 22.8 | 22.8 | 23.8 | 11.8 | 12.7 | 12.7 | 13.3 | | |
| | | | 32 MHz | 15.0 | 15.5 | 15.5 | 16.0 | 7.6 | 8.7 | 8.7 | 9.0 | | |
| | | | 24 MHz | 12.2 | 13.2 | 13.2 | 13.6 | 7.2 | 7.9 | 7.9 | 8.1 | | |
| | | HSI clock, PLL off | 8 MHz | 4.4 | 5.2 | 5.2 | 5.4 | 2.7 | 2.9 | 2.9 | 3.0 | | |
| | | Supply current in Run mode, code executing from RAM | HSE bypass, PLL on | 48 MHz | 22.2 | 23.2 ⁽²⁾ | 23.2 | 24.4 ⁽²⁾ | 12.0 | 12.7 ⁽²⁾ | 12.7 | | 13.3 ⁽²⁾ |
| | | | | 32 MHz | 15.4 | 16.3 | 16.3 | 16.8 | 7.8 | 8.7 | 8.7 | | 9.0 |
| | | | | 24 MHz | 11.2 | 12.2 | 12.2 | 12.8 | 6.2 | 7.9 | 7.9 | | 8.1 |
| | HSE bypass, PLL off | | 8 MHz | 4.0 | 4.5 | 4.5 | 4.7 | 1.9 | 2.9 | 2.9 | 3.0 | | |
| | | | 1 MHz | 0.6 | 0.8 | 0.8 | 0.9 | 0.3 | 0.6 | 0.6 | 0.7 | | |
| | HSI clock, PLL on | | 48 MHz | 22.2 | 23.2 | 23.2 | 24.4 | 12.0 | 12.7 | 12.7 | 13.3 | | |
| | | | 32 MHz | 15.4 | 16.3 | 16.3 | 16.8 | 7.8 | 8.7 | 8.7 | 9.0 | | |
| | | | 24 MHz | 11.2 | 12.2 | 12.2 | 12.8 | 6.2 | 7.9 | 7.9 | 8.1 | | |
| | HSI clock, PLL off | | 8 MHz | 4.0 | 4.5 | 4.5 | 4.7 | 1.9 | 2.9 | 2.9 | 3.0 | | |
| I _{DD} | Supply current in Sleep mode, code executing from Flash or RAM | | HSE bypass, PLL on | 48 MHz | 14.0 | 15.3 ⁽²⁾ | 15.3 | 16.0 ⁽²⁾ | 2.8 | 3.0 ⁽²⁾ | 3.0 | 3.2 ⁽²⁾ | mA |
| | | | | 32 MHz | 9.5 | 10.2 | 10.2 | 10.7 | 2.0 | 2.1 | 2.1 | 2.3 | |
| | | | | 24 MHz | 7.3 | 7.8 | 7.8 | 8.3 | 1.5 | 1.7 | 1.7 | 1.9 | |
| | | HSE bypass, PLL off | 8 MHz | 2.6 | 2.9 | 2.9 | 3.0 | 0.6 | 0.8 | 0.8 | 0.8 | | |
| | | | 1 MHz | 0.4 | 0.6 | 0.6 | 0.6 | 0.2 | 0.4 | 0.4 | 0.4 | | |
| | | HSI clock, PLL on | 48 MHz | 14.0 | 15.3 | 15.3 | 16.0 | 3.8 | 4.0 | 4.1 | 4.2 | | |
| | | | 32 MHz | 9.5 | 10.2 | 10.2 | 10.7 | 2.6 | 2.7 | 2.8 | 2.8 | | |
| | | | 24 MHz | 7.3 | 7.8 | 7.8 | 8.3 | 2.0 | 2.1 | 2.1 | 2.1 | | |
| | | HSI clock, PLL off | 8 MHz | 2.6 | 2.9 | 2.9 | 3.0 | 0.6 | 0.8 | 0.8 | 0.8 | | |

1. Data based on characterization results, not tested in production unless otherwise specified.
2. Data based on characterization results and tested in production (using one common test limit for sum of I_{DD} and I_{DDA}).



Table 26. Typical and maximum current consumption from the V_{DDA} supply

| Symbol | Parameter | Conditions (1) | f _{HCLK} | V _{DDA} = 2.4 V | | | | V _{DDA} = 3.6 V | | | | Unit |
|------------------|---|---------------------|-------------------|--------------------------|-------------------------------------|-------|--------------------|--------------------------|-------------------------------------|-------|--------------------|------|
| | | | | Typ | Max @ T _A ⁽²⁾ | | | Typ | Max @ T _A ⁽²⁾ | | | |
| | | | | | 25 °C | 85 °C | 105 °C | | 25 °C | 85 °C | 105 °C | |
| I _{DDA} | Supply current in Run or Sleep mode, code executing from Flash or RAM | HSE bypass, PLL on | 48 MHz | 150 | 170 ⁽³⁾ | 178 | 182 ⁽³⁾ | 164 | 183 ⁽³⁾ | 195 | 198 ⁽³⁾ | μA |
| | | | 32 MHz | 104 | 121 | 126 | 128 | 113 | 129 | 135 | 138 | |
| | | | 24 MHz | 82 | 96 | 100 | 103 | 88 | 102 | 106 | 108 | |
| | | HSE bypass, PLL off | 8 MHz | 2.0 | 2.7 | 3.1 | 3.3 | 3.5 | 3.8 | 4.1 | 4.4 | |
| | | | 1 MHz | 2.0 | 2.7 | 3.1 | 3.3 | 3.5 | 3.8 | 4.1 | 4.4 | |
| | | HSI clock, PLL on | 48 MHz | 220 | 240 | 248 | 252 | 244 | 263 | 275 | 278 | |
| | | | 32 MHz | 174 | 191 | 196 | 198 | 193 | 209 | 215 | 218 | |
| | | | 24 MHz | 152 | 167 | 173 | 174 | 168 | 183 | 190 | 192 | |
| | | HSI clock, PLL off | 8 MHz | 72 | 79 | 82 | 83 | 83.5 | 91 | 94 | 95 | |

1. Current consumption from the V_{DDA} supply is independent of whether the digital peripherals are enabled or disabled, being in Run or Sleep mode or executing from Flash or RAM. Furthermore, when the PLL is off, I_{DDA} is independent from the frequency.
2. Data based on characterization results, not tested in production unless otherwise specified.
3. Data based on characterization results and tested in production (using one common test limit for sum of I_{DD} and I_{DDA}).

Table 27. Typical and maximum current consumption in Stop and Standby modes

| Symbol | Parameter | Conditions | Typ @V _{DD} (V _{DD} = V _{DDA}) | | | | | | Max ⁽¹⁾ | | | Unit | |
|------------------|--------------------------------|--|--|----------------------|-------|-------|-------|-------|------------------------|------------------------|-------------------------|--------------------|---|
| | | | 2.0 V | 2.4 V | 2.7 V | 3.0 V | 3.3 V | 3.6 V | T _A = 25 °C | T _A = 85 °C | T _A = 105 °C | | |
| I _{DD} | Supply current in Stop mode | Regulator in run mode, all oscillators OFF | 15 | 15.1 | 15.25 | 15.45 | 15.7 | 16 | (2) | | (2) | μA | |
| | | Regulator in low-power mode, all oscillators OFF | 3.15 | 3.25 | 3.35 | 3.45 | 3.7 | 4 | (2) | | (2) | | |
| | Supply current in Standby mode | LSI ON and IWDG ON | 0.8 | 0.95 | 1.05 | 1.2 | 1.35 | 1.5 | - | - | - | | |
| | | LSI OFF and IWDG OFF | 0.65 | 0.75 | 0.85 | 0.95 | 1.1 | 1.3 | 2 ⁽²⁾ | 2.5 | 3 ⁽²⁾ | | |
| I _{DDA} | Supply current in Stop mode | V _{DDA} monitoring ON | Regulator in run mode, all oscillators OFF | 1.85 | 2 | 2.15 | 2.3 | 2.45 | 2.6 | 3.5 ⁽²⁾ | 3.5 | 4.5 ⁽²⁾ | |
| | | | Regulator in low-power mode, all oscillators OFF | 1.85 | 2 | 2.15 | 2.3 | 2.45 | 2.6 | 3.5 ⁽²⁾ | 3.5 | 4.5 ⁽²⁾ | |
| | Supply current in Standby mode | V _{DDA} monitoring ON | LSI ON and IWDG ON | 2.25 | 2.5 | 2.65 | 2.85 | 3.05 | 3.3 | - | - | - | |
| | | | LSI OFF and IWDG OFF | 1.75 | 1.9 | 2 | 2.15 | 2.3 | 2.5 | 3.5 ⁽²⁾ | 3.5 | 4.5 ⁽²⁾ | |
| | Supply current in Stop mode | V _{DDA} monitoring OFF | Regulator in run mode, all oscillators OFF | 1.11 | 1.15 | 1.18 | 1.22 | 1.27 | 1.35 | - | - | - | |
| | | | Regulator in low-power mode, all oscillators OFF | 1.11 | 1.15 | 1.18 | 1.22 | 1.27 | 1.35 | - | - | - | |
| | | Supply current in Standby mode | V _{DDA} monitoring OFF | LSI ON and IWDG ON | 1.5 | 1.58 | 1.65 | 1.78 | 1.91 | 2.04 | - | - | - |
| | | | | LSI OFF and IWDG OFF | 1 | 1.02 | 1.05 | 1.05 | 1.15 | 1.22 | - | - | - |

1. Data based on characterization results, not tested in production unless otherwise specified.
2. Data based on characterization results and tested in production (using one common test limit for sum of I_{DD} and I_{DDA}).

Table 28. Typical and maximum current consumption from the V_{BAT} supply

| Symbol | Parameter | Conditions | Typ @ V _{BAT} | | | | | | Max ⁽¹⁾ | | | Unit |
|----------------------|---------------------------|---|------------------------|---------|---------|---------|---------|---------|------------------------|------------------------|-------------------------|------|
| | | | = 1.65 V | = 1.8 V | = 2.4 V | = 2.7 V | = 3.3 V | = 3.6 V | T _A = 25 °C | T _A = 85 °C | T _A = 105 °C | |
| I _{DD_VBAT} | RTC domain supply current | LSE & RTC ON; “Xtal mode”: lower driving capability; LSEDRV[1:0] = '00' | 0.47 | 0.49 | 0.59 | 0.65 | 0.80 | 0.91 | 1.0 | 1.3 | 1.7 | µA |
| | | LSE & RTC ON; “Xtal mode” higher driving capability; LSEDRV[1:0] = '11' | 0.76 | 0.79 | 0.88 | 0.98 | 1.13 | 1.21 | 1.3 | 1.6 | 2.1 | |

1. Data based on characterization results, not tested in production.

Typical current consumption

The MCU is placed under the following conditions:

- $V_{DD} = V_{DDA} = 3.3\text{ V}$
- All I/O pins are in analog input configuration
- The Flash access time is adjusted to f_{HCLK} frequency:
 - 0 wait state and Prefetch OFF from 0 to 24 MHz
 - 1 wait state and Prefetch ON above 24 MHz
- When the peripherals are enabled, $f_{PCLK} = f_{HCLK}$
- PLL is used for frequencies greater than 8 MHz
- AHB prescaler of 2, 4, 8 and 16 is used for the frequencies 4 MHz, 2 MHz, 1 MHz and 500 kHz respectively

Table 29. Typical current consumption, code executing from Flash, running from HSE 8 MHz crystal

| Symbol | Parameter | f_{HCLK} | Typical consumption in Run mode | | Typical consumption in Sleep mode | | Unit |
|-----------|---|------------|---------------------------------|----------------------|-----------------------------------|----------------------|---------------|
| | | | Peripherals enabled | Peripherals disabled | Peripherals enabled | Peripherals disabled | |
| I_{DD} | Current consumption from V_{DD} supply | 48 MHz | 23.2 | 13.3 | 13.2 | 3.1 | mA |
| | | 36 MHz | 17.6 | 10.3 | 10.1 | 2.6 | |
| | | 32 MHz | 15.6 | 9.3 | 9.0 | 2.4 | |
| | | 24 MHz | 12.1 | 7.4 | 7.0 | 2.0 | |
| | | 16 MHz | 8.4 | 5.1 | 5.0 | 1.6 | |
| | | 8 MHz | 4.5 | 3.0 | 2.8 | 1.1 | |
| | | 4 MHz | 2.8 | 2.0 | 2.0 | 1.1 | |
| | | 2 MHz | 1.9 | 1.5 | 1.5 | 1.0 | |
| | | 1 MHz | 1.5 | 1.3 | 1.3 | 1.0 | |
| | | 500 kHz | 1.2 | 1.2 | 1.1 | 1.0 | |
| I_{DDA} | Current consumption from V_{DDA} supply | 48 MHz | 151 | | | | μA |
| | | 36 MHz | 113 | | | | |
| | | 32 MHz | 101 | | | | |
| | | 24 MHz | 79 | | | | |
| | | 16 MHz | 57 | | | | |
| | | 8 MHz | 2.2 | | | | |
| | | 4 MHz | 2.2 | | | | |
| | | 2 MHz | 2.2 | | | | |
| | | 1 MHz | 2.2 | | | | |
| | | 500 kHz | 2.2 | | | | |

I/O system current consumption

The current consumption of the I/O system has two components: static and dynamic.

I/O static current consumption

All the I/Os used as inputs with pull-up generate current consumption when the pin is externally held low. The value of this current consumption can be simply computed by using the pull-up/pull-down resistors values given in [Table 48: I/O static characteristics](#).

For the output pins, any external pull-down or external load must also be considered to estimate the current consumption.

Additional I/O current consumption is due to I/Os configured as inputs if an intermediate voltage level is externally applied. This current consumption is caused by the input Schmitt trigger circuits used to discriminate the input value. Unless this specific configuration is required by the application, this supply current consumption can be avoided by configuring these I/Os in analog mode. This is notably the case of ADC input pins which should be configured as analog inputs.

Caution: Any floating input pin can also settle to an intermediate voltage level or switch inadvertently, as a result of external electromagnetic noise. To avoid current consumption related to floating pins, they must either be configured in analog mode, or forced internally to a definite digital value. This can be done either by using pull-up/down resistors or by configuring the pins in output mode.

I/O dynamic current consumption

In addition to the internal peripheral current consumption measured previously (see [Table 31: Peripheral current consumption](#)), the I/Os used by an application also contribute to the current consumption. When an I/O pin switches, it uses the current from the I/O supply voltage to supply the I/O pin circuitry and to charge/discharge the capacitive load (internal or external) connected to the pin:

$$I_{SW} = V_{DDIOx} \times f_{SW} \times C$$

where

I_{SW} is the current sunk by a switching I/O to charge/discharge the capacitive load

V_{DDIOx} is the I/O supply voltage

f_{SW} is the I/O switching frequency

C is the total capacitance seen by the I/O pin: $C = C_{INT} + C_{EXT} + C_S$

C_S is the PCB board capacitance including the pad pin.

The test pin is configured in push-pull output mode and is toggled by software at a fixed frequency.

Table 30. Switching output I/O current consumption

| Symbol | Parameter | Conditions ⁽¹⁾ | I/O toggling frequency (f _{SW}) | Typ | Unit |
|--|-------------------------|--|---|-------|------|
| I _{sw} | I/O current consumption | V _{DDIOx} = 3.3 V C = C _{INT} | 4 MHz | 0.07 | mA |
| | | | 8 MHz | 0.15 | |
| | | | 16 MHz | 0.31 | |
| | | | 24 MHz | 0.53 | |
| | | | 48 MHz | 0.92 | |
| | | V _{DDIOx} = 3.3 V C _{EXT} = 0 pF C = C _{INT} + C _{EXT} + C _S | 4 MHz | 0.18 | |
| | | | 8 MHz | 0.37 | |
| | | | 16 MHz | 0.76 | |
| | | | 24 MHz | 1.39 | |
| | | | 48 MHz | 2.188 | |
| | | V _{DDIOx} = 3.3 V C _{EXT} = 10 pF C = C _{INT} + C _{EXT} + C _S | 4 MHz | 0.32 | |
| | | | 8 MHz | 0.64 | |
| | | | 16 MHz | 1.25 | |
| | | | 24 MHz | 2.23 | |
| | | | 48 MHz | 4.442 | |
| | | V _{DDIOx} = 3.3 V C _{EXT} = 22 pF C = C _{INT} + C _{EXT} + C _S | 4 MHz | 0.49 | |
| | | | 8 MHz | 0.94 | |
| | | | 16 MHz | 2.38 | |
| | | | 24 MHz | 3.99 | |
| | | | | | |
| | | V _{DDIOx} = 3.3 V C _{EXT} = 33 pF C = C _{INT} + C _{EXT} + C _S | 4 MHz | 0.64 | |
| | | | 8 MHz | 1.25 | |
| | | | 16 MHz | 3.24 | |
| | | | 24 MHz | 5.02 | |
| | | | | | |
| | | V _{DDIOx} = 3.3 V C _{EXT} = 47 pF C = C _{INT} + C _{EXT} + C _S C = C _{int} | 4 MHz | 0.81 | |
| | | | 8 MHz | 1.7 | |
| | | | 16 MHz | 3.67 | |
| V _{DDIOx} = 2.4 V C _{EXT} = 47 pF C = C _{INT} + C _{EXT} + C _S C = C _{int} | 4 MHz | 0.66 | | | |
| | 8 MHz | 1.43 | | | |
| | 16 MHz | 2.45 | | | |
| | 24 MHz | 4.97 | | | |

1. C_S = 7 pF (estimated value).

On-chip peripheral current consumption

The current consumption of the on-chip peripherals is given in [Table 31](#). The MCU is placed under the following conditions:

- All I/O pins are in analog mode
- All peripherals are disabled unless otherwise mentioned
- The given value is calculated by measuring the current consumption
 - with all peripherals clocked off
 - with only one peripheral clocked on
- Ambient operating temperature and supply voltage conditions summarized in [Table 17: Voltage characteristics](#)

Table 31. Peripheral current consumption

| Peripheral | | Typical consumption at 25 °C | Unit |
|------------|----------------------------|------------------------------|--------|
| AHB | BusMatrix ⁽¹⁾ | 5 | µA/MHz |
| | DMA1 | 7 | |
| | SRAM | 1 | |
| | Flash interface | 14 | |
| | CRC | 2 | |
| | GPIOA | 9 | |
| | GPIOB | 12 | |
| | GPIOC | 2 | |
| | GIOD | 1 | |
| | GPIOF | 1 | |
| | TSC | 6 | |
| | All AHB peripherals | 55 | |

Table 31. Peripheral current consumption (continued)

| | Peripheral | Typical consumption at 25 °C | Unit |
|-----|----------------------------|------------------------------|--------|
| APB | APB-Bridge ⁽²⁾ | 3 | µA/MHz |
| | SYSCFG | 3 | |
| | ADC ⁽³⁾ | 5 | |
| | TIM1 | 17 | |
| | SPI1 | 10 | |
| | USART1 | 19 | |
| | TIM15 | 11 | |
| | TIM16 | 8 | |
| | TIM17 | 8 | |
| | DBG (MCU Debug Support) | 0.5 | |
| | TIM2 | 17 | |
| | TIM3 | 13 | |
| | TIM6 | 3 | |
| | TIM14 | 6 | |
| | WWDG | 1 | |
| | SPI2 | 7 | |
| | USART2 | 7 | |
| | I2C1 | 4 | |
| | I2C2 | 5 | |
| | DAC | 2 | |
| PWR | 1 | | |
| CEC | 2 | | |
| | All APB peripherals | 149 | |

1. The BusMatrix automatically is active when at least one master is ON (CPU or DMA1)
2. The APBx Bridge is automatically active when at least one peripheral is ON on the same Bus.
3. The power consumption of the analog part (I_{DDA}) of peripherals such as ADC is not included. Refer to the tables of characteristics in the subsequent sections.

6.3.6 Wakeup time from low-power mode

The wakeup times given in [Table 32](#) are the latency between the event and the execution of the first user instruction. The device goes in low-power mode after the WFE (Wait For Event) instruction, in the case of a WFI (Wait For Interruption) instruction, 16 CPU cycles must be added to the following timings due to the interrupt latency in the Cortex M0 architecture.

The SYSCLK clock source setting is kept unchanged after wakeup from Sleep mode. During wakeup from Stop or Standby mode, SYSCLK takes the default setting: HSI 8 MHz.

The wakeup source from Sleep and Stop mode is an EXTI line configured in event mode. The wakeup source from Standby mode is the WKUP1 pin (PA0).

All timings are derived from tests performed under the ambient temperature and supply voltage conditions summarized in [Table 20: General operating conditions](#).

Table 32. Low-power mode wakeup timings

| Symbol | Parameter | Conditions | Typ @VDD = VDDA | | | | | Max | Unit |
|------------------------|--------------------------|-----------------------------|-----------------|---------|---------|-------|---------|-----|------|
| | | | = 2.0 V | = 2.4 V | = 2.7 V | = 3 V | = 3.3 V | | |
| t _{WUSTOP} | Wakeup from Stop mode | Regulator in run mode | 3.2 | 3.1 | 2.9 | 2.9 | 2.8 | 5 | μs |
| | | Regulator in low power mode | 7.0 | 5.8 | 5.2 | 4.9 | 4.6 | 9 | |
| t _{WUSTANDBY} | Wakeup from Standby mode | - | 60.4 | 55.6 | 53.5 | 52 | 51 | - | |
| t _{WUSLEEP} | Wakeup from Sleep mode | - | 4 SYSCLK cycles | | | | | - | |

6.3.7 External clock source characteristics

High-speed external user clock generated from an external source

In bypass mode the HSE oscillator is switched off and the input pin is a standard GPIO.

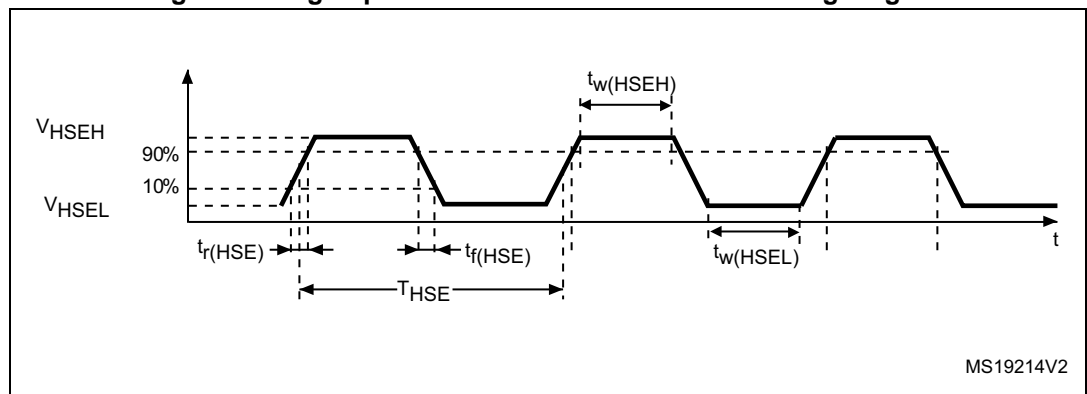
The external clock signal has to respect the I/O characteristics in [Section 6.3.14](#). However, the recommended clock input waveform is shown in [Figure 15: High-speed external clock source AC timing diagram](#).

Table 33. High-speed external user clock characteristics

| Symbol | Parameter ⁽¹⁾ | Min | Typ | Max | Unit |
|--------------------------------|--------------------------------------|-----------------|-----|-----------------|------|
| f_{HSE_ext} | User external clock source frequency | - | 8 | 32 | MHz |
| V_{HSEH} | OSC_IN input pin high level voltage | $0.7 V_{DDIOx}$ | - | V_{DDIOx} | V |
| V_{HSEL} | OSC_IN input pin low level voltage | V_{SS} | - | $0.3 V_{DDIOx}$ | |
| $t_{w(HSEH)}$ $t_{w(HSEL)}$ | OSC_IN high or low time | 15 | - | - | ns |
| $t_r(HSE)$ $t_f(HSE)$ | OSC_IN rise or fall time | - | - | 20 | |

1. Guaranteed by design, not tested in production.

Figure 15. High-speed external clock source AC timing diagram



Low-speed external user clock generated from an external source

In bypass mode the LSE oscillator is switched off and the input pin is a standard GPIO.

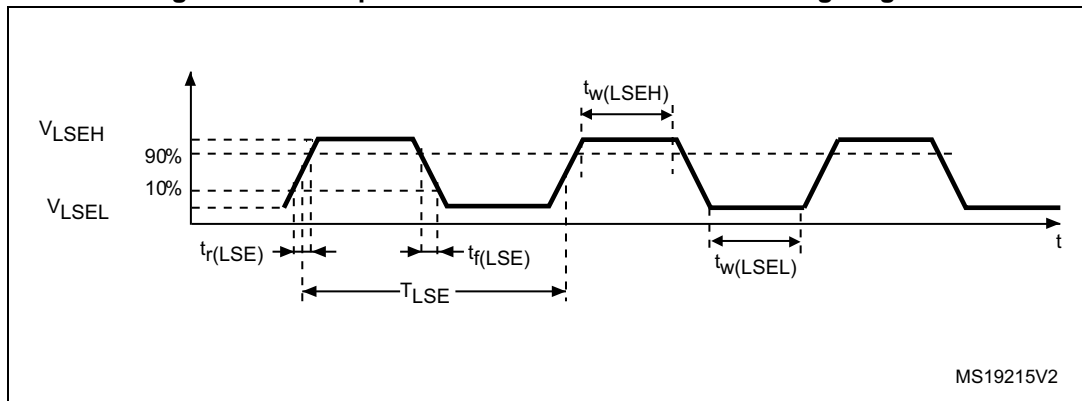
The external clock signal has to respect the I/O characteristics in [Section 6.3.14](#). However, the recommended clock input waveform is shown in [Figure 16](#).

Table 34. Low-speed external user clock characteristics

| Symbol | Parameter ⁽¹⁾ | Min | Typ | Max | Unit |
|--------------------------------|---------------------------------------|-----------------|--------|-----------------|------|
| f_{LSE_ext} | User external clock source frequency | - | 32.768 | 1000 | kHz |
| V_{LSEH} | OSC32_IN input pin high level voltage | $0.7 V_{DDIOx}$ | - | V_{DDIOx} | V |
| V_{LSEL} | OSC32_IN input pin low level voltage | V_{SS} | - | $0.3 V_{DDIOx}$ | |
| $t_{w(LSEH)}$ $t_{w(LSEL)}$ | OSC32_IN high or low time | 450 | - | - | ns |
| $t_r(LSE)$ $t_f(LSE)$ | OSC32_IN rise or fall time | - | - | 50 | |

1. Guaranteed by design, not tested in production.

Figure 16. Low-speed external clock source AC timing diagram



High-speed external clock generated from a crystal/ceramic resonator

The high-speed external (HSE) clock can be supplied with a 4 to 32 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on design simulation results obtained with typical external components specified in [Table 35](#). In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Table 35. HSE oscillator characteristics

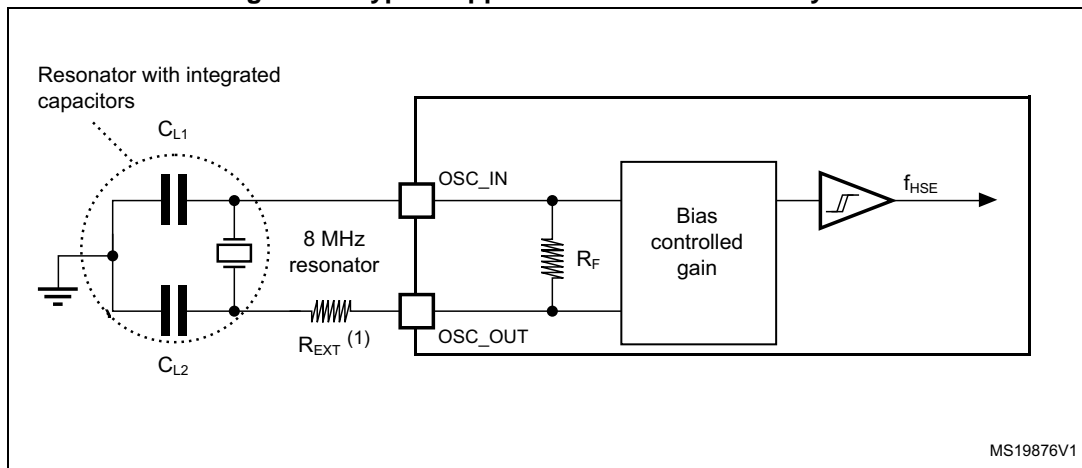
| Symbol | Parameter | Conditions ⁽¹⁾ | Min ⁽²⁾ | Typ | Max ⁽²⁾ | Unit |
|---------------------|-----------------------------|--|--------------------|-----|--------------------|------------|
| f_{OSC_IN} | Oscillator frequency | - | 4 | 8 | 32 | MHz |
| R_F | Feedback resistor | - | - | 200 | - | k Ω |
| I_{DD} | HSE current consumption | During startup ⁽³⁾ | - | - | 8.5 | mA |
| | | $V_{DD} = 3.3\text{ V}$, $R_m = 30\ \Omega$, $CL = 10\text{ pF}@8\text{ MHz}$ | - | 0.4 | - | |
| | | $V_{DD} = 3.3\text{ V}$, $R_m = 45\ \Omega$, $CL = 10\text{ pF}@8\text{ MHz}$ | - | 0.5 | - | |
| | | $V_{DD} = 3.3\text{ V}$, $R_m = 30\ \Omega$, $CL = 5\text{ pF}@32\text{ MHz}$ | - | 0.8 | - | |
| | | $V_{DD} = 3.3\text{ V}$, $R_m = 30\ \Omega$, $CL = 10\text{ pF}@32\text{ MHz}$ | - | 1 | - | |
| | | $V_{DD} = 3.3\text{ V}$, $R_m = 30\ \Omega$, $CL = 20\text{ pF}@32\text{ MHz}$ | - | 1.5 | - | |
| g_m | Oscillator transconductance | Startup | 10 | - | - | mA/V |
| $t_{SU(HSE)}^{(4)}$ | Startup time | V_{DD} is stabilized | - | 2 | - | ms |

1. Resonator characteristics given by the crystal/ceramic resonator manufacturer.
2. Guaranteed by design, not tested in production.
3. This consumption level occurs during the first 2/3 of the $t_{SU(HSE)}$ startup time
4. $t_{SU(HSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 8 MHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer

For C_{L1} and C_{L2} , it is recommended to use high-quality external ceramic capacitors in the 5 pF to 20 pF range (Typ.), designed for high-frequency applications, and selected to match the requirements of the crystal or resonator (see [Figure 17](#)). C_{L1} and C_{L2} are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of C_{L1} and C_{L2} . PCB and MCU pin capacitance must be included (10 pF can be used as a rough estimate of the combined pin and board capacitance) when sizing C_{L1} and C_{L2} .

Note: For information on selecting the crystal, refer to the application note AN2867 "Oscillator design guide for ST microcontrollers" available from the ST website www.st.com.

Figure 17. Typical application with an 8 MHz crystal



1. R_{EXT} value depends on the crystal characteristics.

Low-speed external clock generated from a crystal resonator

The low-speed external (LSE) clock can be supplied with a 32.768 kHz crystal resonator oscillator. All the information given in this paragraph are based on design simulation results obtained with typical external components specified in [Table 36](#). In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

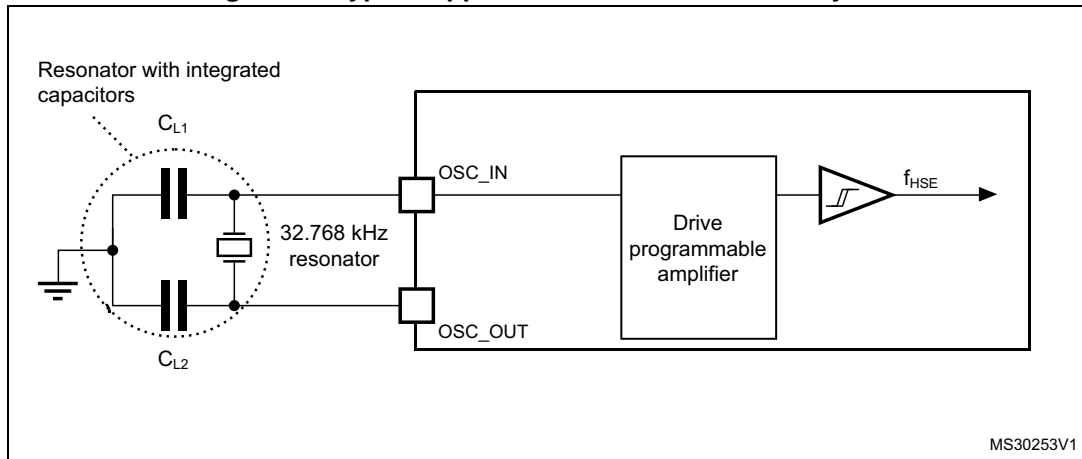
Table 36. LSE oscillator characteristics ($f_{LSE} = 32.768$ kHz)

| Symbol | Parameter | Conditions ⁽¹⁾ | Min ⁽²⁾ | Typ | Max ⁽²⁾ | Unit |
|---------------------|-----------------------------|--|--------------------|-----|--------------------|-----------|
| I_{DD} | LSE current consumption | LSEDRV[1:0]=00 lower driving capability | - | 0.5 | 0.9 | μA |
| | | LSEDRV[1:0]= 01 medium low driving capability | - | - | 1 | |
| | | LSEDRV[1:0] = 10 medium high driving capability | - | - | 1.3 | |
| | | LSEDRV[1:0]=11 higher driving capability | - | - | 1.6 | |
| g_m | Oscillator transconductance | LSEDRV[1:0]=00 lower driving capability | 5 | - | - | $\mu A/V$ |
| | | LSEDRV[1:0]= 01 medium low driving capability | 8 | - | - | |
| | | LSEDRV[1:0] = 10 medium high driving capability | 15 | - | - | |
| | | LSEDRV[1:0]=11 higher driving capability | 25 | - | - | |
| $t_{SU(LSE)}^{(3)}$ | Startup time | V_{DDIOX} is stabilized | - | 2 | - | s |

1. Refer to the note and caution paragraphs below the table, and to the application note AN2867 "Oscillator design guide for ST microcontrollers".
2. Guaranteed by design, not tested in production.
3. $t_{SU(LSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 32.768 kHz oscillation is reached. This value is measured for a standard crystal and it can vary significantly with the crystal manufacturer

Note: For information on selecting the crystal, refer to the application note AN2867 "Oscillator design guide for ST microcontrollers" available from the ST website www.st.com.

Figure 18. Typical application with a 32.768 kHz crystal



Note: An external resistor is not required between OSC32_IN and OSC32_OUT and it is forbidden to add one.

6.3.8 Internal clock source characteristics

The parameters given in [Table 37](#) are derived from tests performed under ambient temperature and supply voltage conditions summarized in [Table 20: General operating conditions](#). The provided curves are characterization results, not tested in production.

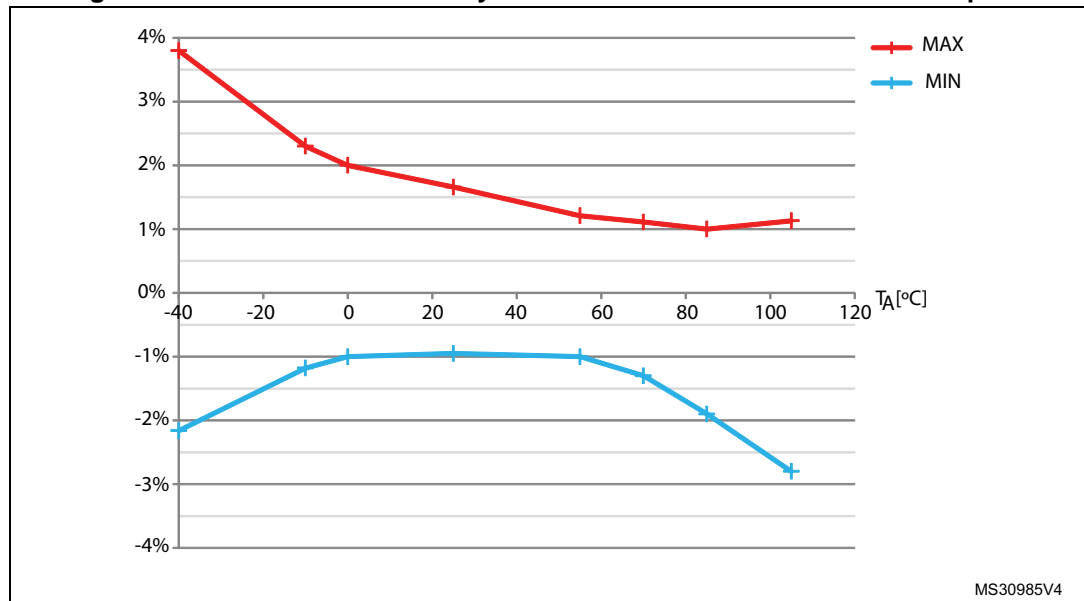
High-speed internal (HSI) RC oscillator

Table 37. HSI oscillator characteristics⁽¹⁾

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-----------------------|----------------------------------|-------------------------------|---------------------|-----|--------------------|------|
| f_{HSI} | Frequency | - | - | 8 | - | MHz |
| TRIM | HSI user trimming step | - | - | - | 1 ⁽²⁾ | % |
| DuCy _(HSI) | Duty cycle | - | 45 ⁽²⁾ | - | 55 ⁽²⁾ | % |
| ACC _{HSI} | Accuracy of the HSI oscillator | T _A = -40 to 105°C | -2.8 ⁽³⁾ | - | 3.8 ⁽³⁾ | % |
| | | T _A = -10 to 85°C | -1.9 ⁽³⁾ | - | 2.3 ⁽³⁾ | |
| | | T _A = 0 to 85°C | -1.9 ⁽³⁾ | - | 2 ⁽³⁾ | |
| | | T _A = 0 to 70°C | -1.3 ⁽³⁾ | - | 2 ⁽³⁾ | |
| | | T _A = 0 to 55°C | -1 ⁽³⁾ | - | 2 ⁽³⁾ | |
| | | T _A = 25°C | -1 ⁽⁴⁾ | - | 1 ⁽⁴⁾ | |
| t _{su(HSI)} | HSI oscillator startup time | - | 1 ⁽²⁾ | - | 2 ⁽²⁾ | µs |
| I _{DDA(HSI)} | HSI oscillator power consumption | - | - | 80 | 100 ⁽²⁾ | µA |

1. V_{DDA} = 3.3 V, T_A = -40 to 105°C unless otherwise specified.
2. Guaranteed by design, not tested in production.
3. Data based on characterization results, not tested in production.
4. Factory calibrated, parts not soldered.

Figure 19. HSI oscillator accuracy characterization results for soldered parts



MS30985V4

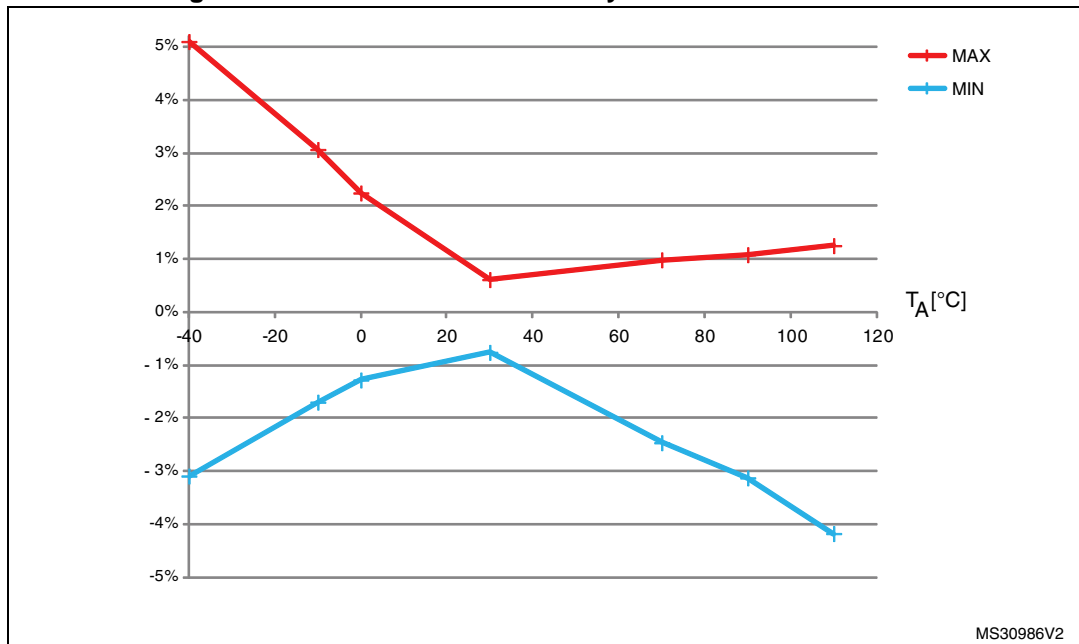
High-speed internal 14 MHz (HSI14) RC oscillator (dedicated to ADC)

Table 38. HSI14 oscillator characteristics⁽¹⁾

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|------------------|---|-------------------------|---------------------|-----|--------------------|---------|
| f_{HSI14} | Frequency | - | - | 14 | - | MHz |
| TRIM | HSI14 user-trimming step | - | - | - | 1 ⁽²⁾ | % |
| $DuCy_{(HSI14)}$ | Duty cycle | - | 45 ⁽²⁾ | - | 55 ⁽²⁾ | % |
| ACC_{HSI14} | Accuracy of the HSI14 oscillator (factory calibrated) | $T_A = -40$ to 105 °C | -4.2 ⁽³⁾ | - | 5.1 ⁽³⁾ | % |
| | | $T_A = -10$ to 85 °C | -3.2 ⁽³⁾ | - | 3.1 ⁽³⁾ | % |
| | | $T_A = 0$ to 70 °C | -2.5 ⁽³⁾ | - | 2.3 ⁽³⁾ | % |
| | | $T_A = 25$ °C | -1 | - | 1 | % |
| $t_{su(HSI14)}$ | HSI14 oscillator startup time | - | 1 ⁽²⁾ | - | 2 ⁽²⁾ | μs |
| $I_{DDA(HSI14)}$ | HSI14 oscillator power consumption | - | - | 100 | 150 ⁽²⁾ | μA |

1. $V_{DDA} = 3.3$ V, $T_A = -40$ to 105 °C unless otherwise specified.
2. Guaranteed by design, not tested in production.
3. Data based on characterization results, not tested in production.

Figure 20. HSI14 oscillator accuracy characterization results



Low-speed internal (LSI) RC oscillator

Table 39. LSI oscillator characteristics⁽¹⁾

| Symbol | Parameter | Min | Typ | Max | Unit |
|----------------------|----------------------------------|-----|------|-----|---------|
| f_{LSI} | Frequency | 30 | 40 | 50 | kHz |
| $t_{su(LSI)}^{(2)}$ | LSI oscillator startup time | - | - | 85 | μ s |
| $I_{DDA(LSI)}^{(2)}$ | LSI oscillator power consumption | - | 0.75 | 1.2 | μ A |

1. $V_{DDA} = 3.3$ V, $T_A = -40$ to 105 °C unless otherwise specified.

2. Guaranteed by design, not tested in production.

6.3.9 PLL characteristics

The parameters given in [Table 40](#) are derived from tests performed under ambient temperature and supply voltage conditions summarized in [Table 20: General operating conditions](#).

Table 40. PLL characteristics

| Symbol | Parameter | Value | | | Unit |
|----------------|--------------------------------|-------------------|-----|--------------------|---------|
| | | Min | Typ | Max | |
| f_{PLL_IN} | PLL input clock ⁽¹⁾ | 1 ⁽²⁾ | 8.0 | 24 ⁽²⁾ | MHz |
| | PLL input clock duty cycle | 40 ⁽²⁾ | - | 60 ⁽²⁾ | % |
| f_{PLL_OUT} | PLL multiplier output clock | 16 ⁽²⁾ | - | 48 | MHz |
| t_{LOCK} | PLL lock time | - | - | 200 ⁽²⁾ | μ s |
| $Jitter_{PLL}$ | Cycle-to-cycle jitter | - | - | 300 ⁽²⁾ | ps |

1. Take care to use the appropriate multiplier factors to obtain PLL input clock values compatible with the range defined by f_{PLL_OUT} .

2. Guaranteed by design, not tested in production.

6.3.10 Memory characteristics

Flash memory

The characteristics are given at $T_A = -40$ to 105 °C unless otherwise specified.

Table 41. Flash memory characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max ⁽¹⁾ | Unit |
|--------------------|-------------------------|--------------------------|-----|------|--------------------|---------------|
| t_{prog} | 16-bit programming time | $T_A = -40$ to $+105$ °C | 40 | 53.5 | 60 | μs |
| t_{ERASE} | Page (1 KB) erase time | $T_A = -40$ to $+105$ °C | 20 | - | 40 | ms |
| t_{ME} | Mass erase time | $T_A = -40$ to $+105$ °C | 20 | - | 40 | ms |
| I_{DD} | Supply current | Write mode | - | - | 10 | mA |
| | | Erase mode | - | - | 12 | mA |

1. Guaranteed by design, not tested in production.

Table 42. Flash memory endurance and data retention

| Symbol | Parameter | Conditions | Min ⁽¹⁾ | Unit |
|------------------|----------------|---|--------------------|--------|
| N_{END} | Endurance | $T_A = -40$ to $+105$ °C | 10 | kcycle |
| t_{RET} | Data retention | 1 kcycle ⁽²⁾ at $T_A = 85$ °C | 30 | Year |
| | | 1 kcycle ⁽²⁾ at $T_A = 105$ °C | 10 | |
| | | 10 kcycle ⁽²⁾ at $T_A = 55$ °C | 20 | |

1. Data based on characterization results, not tested in production.

2. Cycling performed over the whole temperature range.

6.3.11 EMC characteristics

Susceptibility tests are performed on a sample basis during device characterization.

Functional EMS (electromagnetic susceptibility)

While a simple application is executed on the device (toggling 2 LEDs through I/O ports), the device is stressed by two electromagnetic events until a failure occurs. The failure is indicated by the LEDs:

- **Electrostatic discharge (ESD)** (positive and negative) is applied to all device pins until a functional disturbance occurs. This test is compliant with the IEC 61000-4-2 standard.
- **FTB:** A Burst of Fast Transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a 100 pF capacitor, until a functional disturbance occurs. This test is compliant with the IEC 61000-4-4 standard.

A device reset allows normal operations to be resumed.

The test results are given in [Table 43](#). They are based on the EMS levels and classes defined in application note AN1709.

Table 43. EMS characteristics

| Symbol | Parameter | Conditions | Level/Class |
|-------------------|---|---|-------------|
| V _{FESD} | Voltage limits to be applied on any I/O pin to induce a functional disturbance | V _{DD} = 3.3 V, LQFP64, T _A = +25 °C, f _{HCLK} = 48 MHz, conforming to IEC 61000-4-2 | 2B |
| V _{EFTB} | Fast transient voltage burst limits to be applied through 100 pF on V _{DD} and V _{SS} pins to induce a functional disturbance | V _{DD} = 3.3 V, LQFP64, T _A = +25°C, f _{HCLK} = 48 MHz, conforming to IEC 61000-4-4 | 4B |

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

Software recommendations

The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical Data corruption (control registers...)

Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST pin or the Oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

Electromagnetic Interference (EMI)

The electromagnetic field emitted by the device are monitored while a simple application is executed (toggling 2 LEDs through the I/O ports). This emission test is compliant with IEC 61967-2 standard which specifies the test board and the pin loading.

Table 44. EMI characteristics

| Symbol | Parameter | Conditions | Monitored frequency band | Max vs. [f _{HSE} /f _{HCLK}] | Unit |
|------------------|------------|--|--------------------------|--|------|
| | | | | 8/48 MHz | |
| S _{EMI} | Peak level | V _{DD} = 3.6 V, T _A = 25 °C, LQFP64 package compliant with IEC 61967-2 | 0.1 to 30 MHz | -3 | dBμV |
| | | | 30 to 130 MHz | 28 | |
| | | | 130 MHz to 1 GHz | 23 | |
| | | | EMI Level | 4 | - |



6.3.12 Electrical sensitivity characteristics

Based on three different tests (ESD, LU) using specific measurement methods, the device is stressed in order to determine its performance in terms of electrical sensitivity.

Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × (n+1) supply pins). This test conforms to the JESD22-A114/C101 standard.

Table 45. ESD absolute maximum ratings

| Symbol | Ratings | Conditions | Packages | Class | Maximum value ⁽¹⁾ | Unit |
|-----------------------|---|--|----------|-------|------------------------------|------|
| V _{ESD(HBM)} | Electrostatic discharge voltage (human body model) | T _A = +25 °C, conforming to JESD22-A114 | All | 2 | 2000 | V |
| V _{ESD(CDM)} | Electrostatic discharge voltage (charge device model) | T _A = +25 °C, conforming to ANSI/ESD STM5.3.1 | All | C4 | 500 | V |

1. Data based on characterization results, not tested in production.

Static latch-up

Two complementary static tests are required on six parts to assess the latch-up performance:

- A supply overvoltage is applied to each power supply pin.
- A current injection is applied to each input, output and configurable I/O pin.

These tests are compliant with EIA/JESD 78A IC latch-up standard.

Table 46. Electrical sensitivities

| Symbol | Parameter | Conditions | Class |
|--------|-----------------------|--|------------|
| LU | Static latch-up class | T _A = +105 °C conforming to JESD78A | II level A |

6.3.13 I/O current injection characteristics

As a general rule, current injection to the I/O pins, due to external voltage below V_{SS} or above V_{DDIOx} (for standard, 3.3 V-capable I/O pins) should be avoided during normal product operation. However, in order to give an indication of the robustness of the microcontroller in cases when abnormal injection accidentally happens, susceptibility tests are performed on a sample basis during device characterization.

Functional susceptibility to I/O current injection

While a simple application is executed on the device, the device is stressed by injecting current into the I/O pins programmed in floating input mode. While current is injected into the I/O pin, one at a time, the device is checked for functional failures.

The failure is indicated by an out of range parameter: ADC error above a certain limit (higher than 5 LSB TUE), out of conventional limits of induced leakage current on adjacent pins (out of the $-5 \mu\text{A}/+0 \mu\text{A}$ range) or other functional failure (for example reset occurrence or oscillator frequency deviation).

The characterization results are given in [Table 47](#).

Negative induced leakage current is caused by negative injection and positive induced leakage current is caused by positive injection.

Table 47. I/O current injection susceptibility

| Symbol | Description | Functional susceptibility | | Unit |
|------------------|---|---------------------------|--------------------|------|
| | | Negative injection | Positive injection | |
| I_{INJ} | Injected current on BOOT0 | -0 | NA | mA |
| | Injected current on PA10, PA12, PB4, PB5, PB10, PB15 and PD2 pins with induced leakage current on adjacent pins less than $-10 \mu\text{A}$ | -5 | NA | |
| | Injected current on all other FT and FTf pins | -5 | NA | |
| | Injected current on PA6 and PC0 | -0 | +5 | |
| | Injected current on all other TTa, TC and RST pins | -5 | +5 | |

6.3.14 I/O port characteristics

General input/output characteristics

Unless otherwise specified, the parameters given in [Table 48](#) are derived from tests performed under the conditions summarized in [Table 20: General operating conditions](#). All I/Os are designed as CMOS- and TTL-compliant (except BOOT0).

Table 48. I/O static characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-----------------|-------------------------|---------------------------|-----|-----|------------------------------------|------|
| V_{IL} | Low level input voltage | TC and TTa I/O | - | - | $0.3 V_{\text{DDIOx}}+0.07^{(1)}$ | V |
| | | FT and FTf I/O | - | - | $0.475 V_{\text{DDIOx}}-0.2^{(1)}$ | |
| | | BOOT0 | - | - | $0.3 V_{\text{DDIOx}}-0.3^{(1)}$ | |
| | | All I/Os except BOOT0 pin | - | - | $0.3 V_{\text{DDIOx}}$ | |

Table 48. I/O static characteristics (continued)

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-----------|---|--|---------------------------------|-------------|-----------|------------|
| V_{IH} | High level input voltage | TC and TTa I/O | $0.445 V_{DDIOx} + 0.398^{(1)}$ | - | - | V |
| | | FT and FTf I/O | $0.5 V_{DDIOx} + 0.2^{(1)}$ | - | - | |
| | | BOOT0 | $0.2 V_{DDIOx} + 0.95^{(1)}$ | - | - | |
| | | All I/Os except BOOT0 pin | $0.7 V_{DDIOx}$ | - | - | |
| V_{hys} | Schmitt trigger hysteresis | TC and TTa I/O | - | $200^{(1)}$ | - | mV |
| | | FT and FTf I/O | - | $100^{(1)}$ | - | |
| | | BOOT0 | - | $300^{(1)}$ | - | |
| I_{lkg} | Input leakage current ⁽²⁾ | TC, FT and FTf I/O TTa in digital mode $V_{SS} \leq V_{IN} \leq V_{DDIOx}$ | - | - | ± 0.1 | μA |
| | | TTa in digital mode $V_{DDIOx} \leq V_{IN} \leq V_{DDA}$ | - | - | 1 | |
| | | TTa in analog mode $V_{SS} \leq V_{IN} \leq V_{DDA}$ | - | - | ± 0.2 | |
| | | FT and FTf I/O ⁽³⁾ $V_{DDIOx} \leq V_{IN} \leq 5 V$ | - | - | 10 | |
| R_{PU} | Weak pull-up equivalent resistor ⁽⁴⁾ | $V_{IN} = V_{SS}$ | 25 | 40 | 55 | k Ω |
| R_{PD} | Weak pull-down equivalent resistor ⁽⁴⁾ | $V_{IN} = V_{DDIOx}$ | 25 | 40 | 55 | k Ω |
| C_{IO} | I/O pin capacitance | - | - | 5 | - | pF |

1. Data based on design simulation only. Not tested in production.

2. The leakage could be higher than the maximum value, if negative current is injected on adjacent pins. Refer to [Table 47: I/O current injection susceptibility](#).

3. To sustain a voltage higher than $V_{DDIOx} + 0.3 V$, the internal pull-up/pull-down resistors must be disabled.

4. Pull-up and pull-down resistors are designed with a true resistance in series with a switchable PMOS/NMOS. This PMOS/NMOS contribution to the series resistance is minimal (~10% order).

All I/Os are CMOS- and TTL-compliant (no software configuration required). Their characteristics cover more than the strict CMOS-technology or TTL parameters. The coverage of these requirements is shown in [Figure 21](#) for standard I/Os, and in [Figure 22](#) for 5 V tolerant I/Os. The following curves are design simulation results, not tested in production.

Figure 21. TC and TTa I/O input characteristics

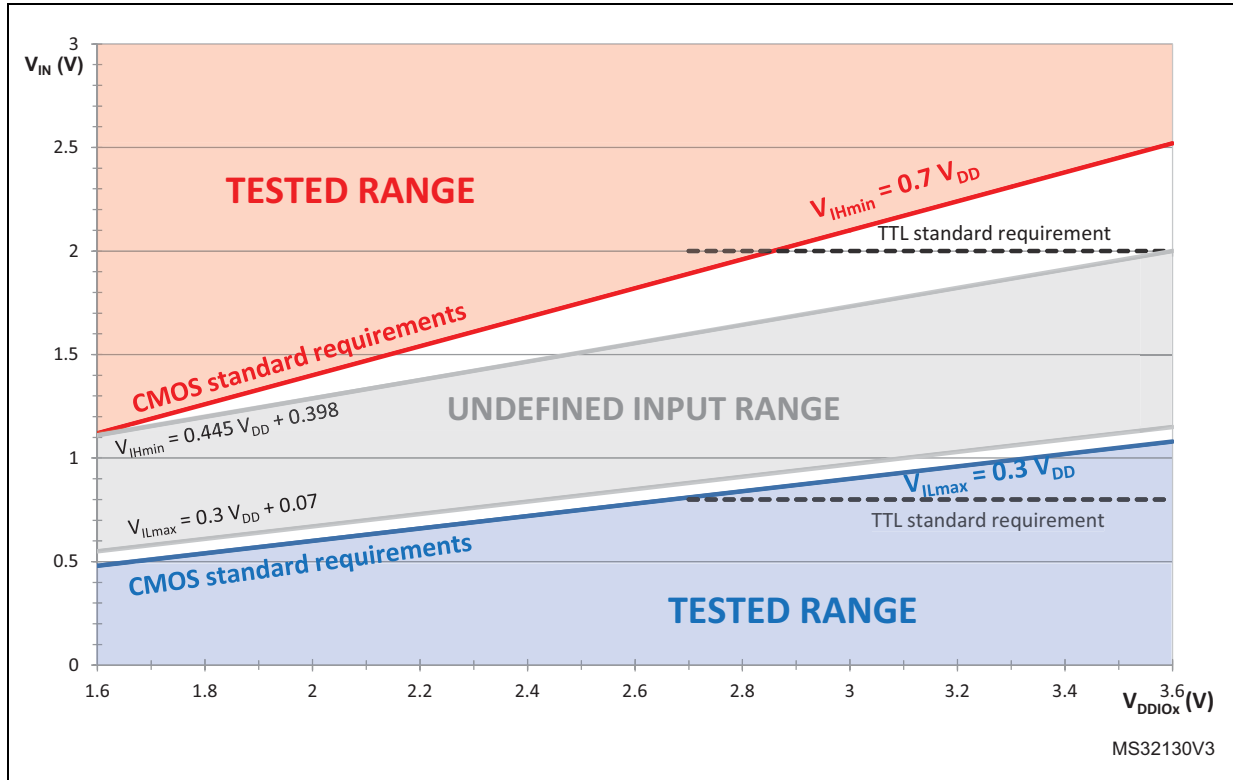
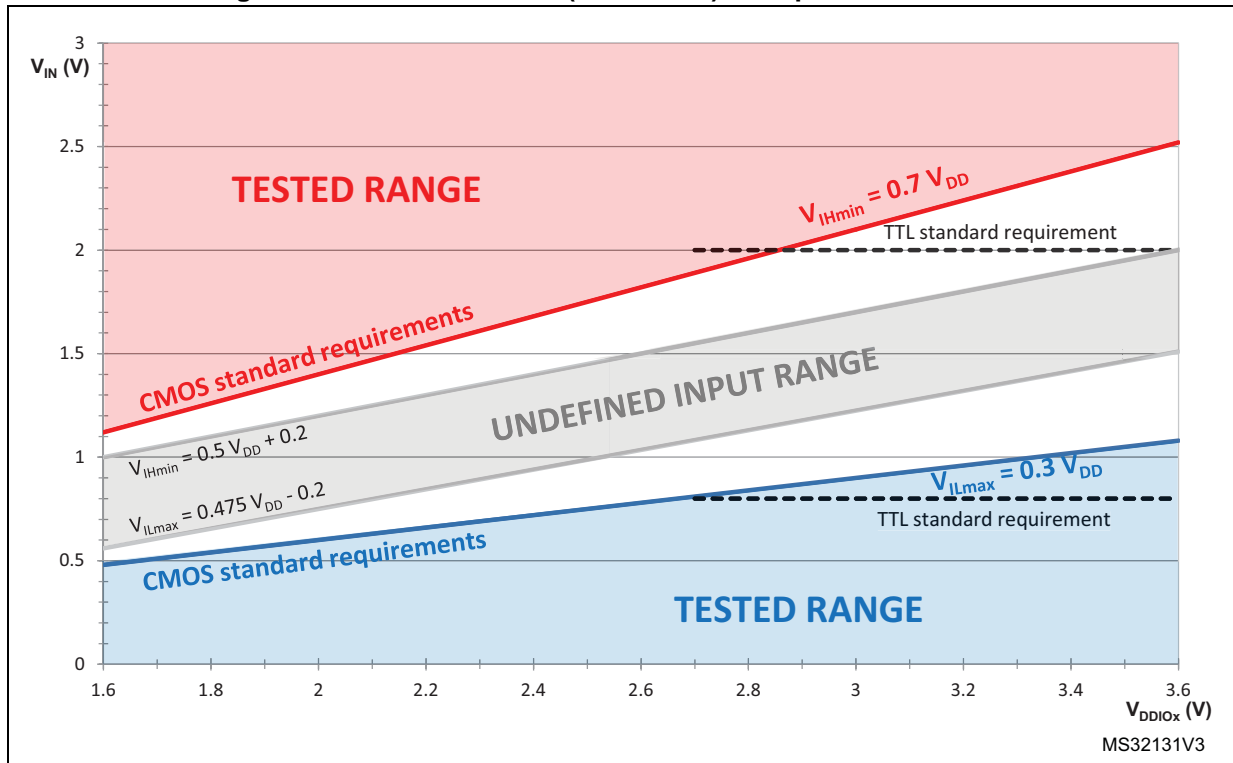


Figure 22. Five volt tolerant (FT and FTf) I/O input characteristics



Output driving current

The GPIOs (general purpose input/outputs) can sink or source up to +/-8 mA, and sink or source up to +/- 20 mA (with a relaxed V_{OL}/V_{OH}).

In the user application, the number of I/O pins which can drive current must be limited to respect the absolute maximum rating specified in [Section 6.2](#):

- The sum of the currents sourced by all the I/Os on V_{DDIOx} , plus the maximum consumption of the MCU sourced on V_{DD} , cannot exceed the absolute maximum rating ΣI_{VDD} (see [Table 17: Voltage characteristics](#)).
- The sum of the currents sunk by all the I/Os on V_{SS} , plus the maximum consumption of the MCU sunk on V_{SS} , cannot exceed the absolute maximum rating ΣI_{VSS} (see [Table 17: Voltage characteristics](#)).

Output voltage levels

Unless otherwise specified, the parameters given in the table below are derived from tests performed under the ambient temperature and supply voltage conditions summarized in [Table 20: General operating conditions](#). All I/Os are CMOS- and TTL-compliant (FT, TTa or TC unless otherwise specified).

Table 49. Output voltage characteristics⁽¹⁾

| Symbol | Parameter | Conditions | Min | Max | Unit |
|-------------------|---|---|-----------------|-----|------|
| V_{OL} | Output low level voltage for an I/O pin | CMOS port ⁽²⁾ $ I_{IO} = 8 \text{ mA}$ $V_{DDIOx} \geq 2.7 \text{ V}$ | - | 0.4 | V |
| V_{OH} | Output high level voltage for an I/O pin | | $V_{DDIOx}-0.4$ | - | |
| V_{OL} | Output low level voltage for an I/O pin | TTL port ⁽²⁾ $ I_{IO} = 8 \text{ mA}$ $V_{DDIOx} \geq 2.7 \text{ V}$ | - | 0.4 | V |
| V_{OH} | Output high level voltage for an I/O pin | | 2.4 | - | |
| $V_{OL}^{(3)}$ | Output low level voltage for an I/O pin | $ I_{IO} = 20 \text{ mA}$ $V_{DDIOx} \geq 2.7 \text{ V}$ | - | 1.3 | V |
| $V_{OH}^{(3)}$ | Output high level voltage for an I/O pin | | $V_{DDIOx}-1.3$ | - | |
| $V_{OL}^{(3)}$ | Output low level voltage for an I/O pin | $ I_{IO} = 6 \text{ mA}$ | - | 0.4 | V |
| $V_{OH}^{(3)}$ | Output high level voltage for an I/O pin | | $V_{DDIOx}-0.4$ | - | |
| $V_{OLFm+}^{(3)}$ | Output low level voltage for an FTf I/O pin in Fm+ mode | $ I_{IO} = 20 \text{ mA}$ $V_{DDIOx} \geq 2.7 \text{ V}$ | - | 0.4 | V |
| | | $ I_{IO} = 10 \text{ mA}$ | - | 0.4 | V |

1. The I_{IO} current sourced or sunk by the device must always respect the absolute maximum rating specified in [Table 17: Voltage characteristics](#), and the sum of the currents sourced or sunk by all the I/Os (I/O ports and control pins) must always respect the absolute maximum ratings ΣI_{IO} .
2. TTL and CMOS outputs are compatible with JEDEC standards JESD36 and JESD52.
3. Data based on characterization results. Not tested in production.

Input/output AC characteristics

The definition and values of input/output AC characteristics are given in [Figure 23](#) and [Table 50](#), respectively.

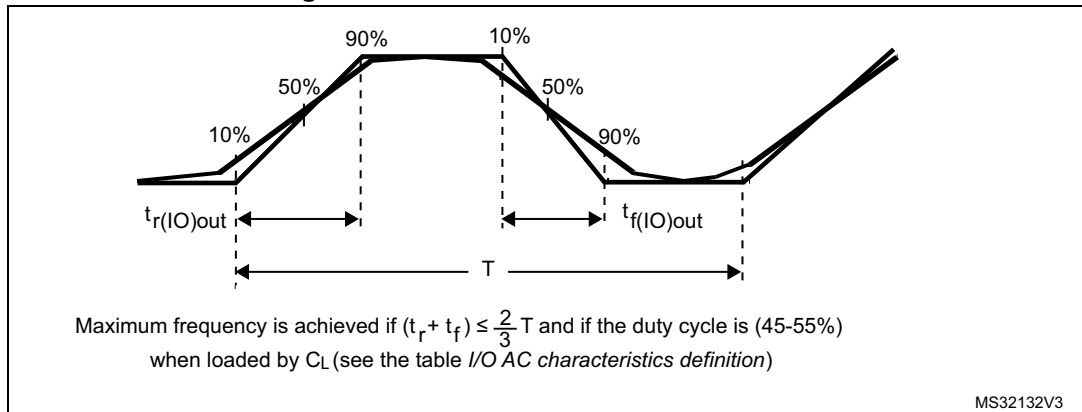
Unless otherwise specified, the parameters given are derived from tests performed under the ambient temperature and supply voltage conditions summarized in [Table 20: General operating conditions](#).

Table 50. I/O AC characteristics⁽¹⁾⁽²⁾

| OSPEEDRx [1:0] value ⁽¹⁾ | Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---------------------------------|---|--|-----|-----|------|
| x0 | $f_{\max(\text{IO})\text{out}}$ | Maximum frequency ⁽³⁾ | $C_L = 50 \text{ pF}$ | - | 2 | MHz |
| | $t_{f(\text{IO})\text{out}}$ | Output fall time | | - | 125 | ns |
| | $t_{r(\text{IO})\text{out}}$ | Output rise time | | - | 125 | |
| 01 | $f_{\max(\text{IO})\text{out}}$ | Maximum frequency ⁽³⁾ | $C_L = 50 \text{ pF}$ | - | 10 | MHz |
| | $t_{f(\text{IO})\text{out}}$ | Output fall time | | - | 25 | ns |
| | $t_{r(\text{IO})\text{out}}$ | Output rise time | | - | 25 | |
| 11 | $f_{\max(\text{IO})\text{out}}$ | Maximum frequency ⁽³⁾ | $C_L = 30 \text{ pF}, V_{\text{DDIOx}} \geq 2.7 \text{ V}$ | - | 50 | MHz |
| | | | $C_L = 50 \text{ pF}, V_{\text{DDIOx}} \geq 2.7 \text{ V}$ | - | 30 | |
| | | | $C_L = 50 \text{ pF}, V_{\text{DDIOx}} < 2.7 \text{ V}$ | - | 20 | |
| | $t_{f(\text{IO})\text{out}}$ | Output fall time | $C_L = 30 \text{ pF}, V_{\text{DDIOx}} \geq 2.7 \text{ V}$ | - | 5 | ns |
| | | | $C_L = 50 \text{ pF}, V_{\text{DDIOx}} \geq 2.7 \text{ V}$ | - | 8 | |
| | | | $C_L = 50 \text{ pF}, V_{\text{DDIOx}} < 2.7 \text{ V}$ | - | 12 | |
| | $t_{r(\text{IO})\text{out}}$ | Output rise time | $C_L = 30 \text{ pF}, V_{\text{DDIOx}} \geq 2.7 \text{ V}$ | - | 5 | |
| | | | $C_L = 50 \text{ pF}, V_{\text{DDIOx}} \geq 2.7 \text{ V}$ | - | 8 | |
| | | | $C_L = 50 \text{ pF}, V_{\text{DDIOx}} < 2.7 \text{ V}$ | - | 12 | |
| Fm+ configuration ⁽⁴⁾ | $f_{\max(\text{IO})\text{out}}$ | Maximum frequency ⁽³⁾ | $C_L = 50 \text{ pF}$ | - | 2 | MHz |
| | $t_{f(\text{IO})\text{out}}$ | Output fall time | | - | 12 | ns |
| | $t_{r(\text{IO})\text{out}}$ | Output rise time | | - | 34 | |
| | $t_{\text{EXTI}pw}$ | Pulse width of external signals detected by the EXTI controller | | 10 | - | ns |

1. The I/O speed is configured using the OSPEEDRx[1:0] bits. Refer to the STM32F0xxxx RM0091 reference manual for a description of GPIO Port configuration register.
2. Guaranteed by design, not tested in production.
3. The maximum frequency is defined in [Figure 23](#).
4. When Fm+ configuration is set, the I/O speed control is bypassed. Refer to the STM32F0xxxx reference manual RM0091 for a detailed description of Fm+ I/O configuration.

Figure 23. I/O AC characteristics definition



6.3.15 NRST pin characteristics

The NRST pin input driver uses the CMOS technology. It is connected to a permanent pull-up resistor, R_{PU} .

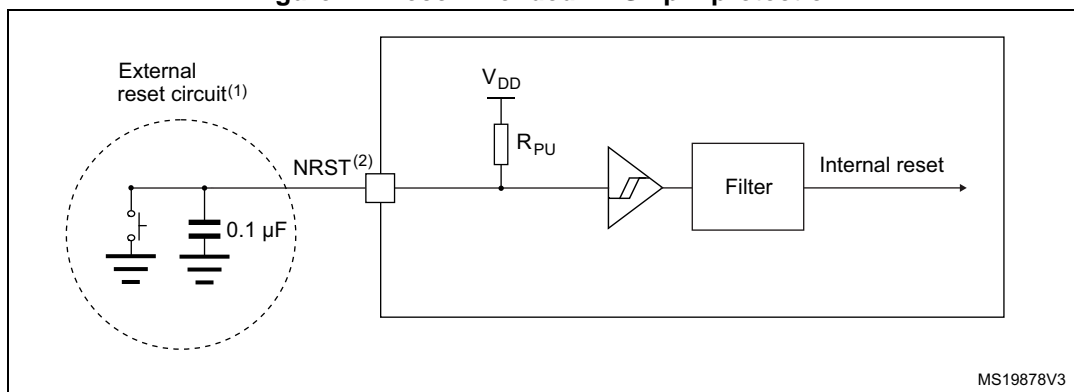
Unless otherwise specified, the parameters given in the table below are derived from tests performed under the ambient temperature and supply voltage conditions summarized in [Table 20: General operating conditions](#).

Table 51. NRST pin characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-----------------|---|----------------------|------------------------------|-----|---------------------------|------------|
| $V_{IL(NRST)}$ | NRST input low level voltage | - | - | - | $0.3 V_{DD} + 0.07^{(1)}$ | V |
| $V_{IH(NRST)}$ | NRST input high level voltage | - | $0.445 V_{DD} + 0.398^{(1)}$ | - | - | |
| $V_{hys(NRST)}$ | NRST Schmitt trigger voltage hysteresis | - | - | 200 | - | mV |
| R_{PU} | Weak pull-up equivalent resistor ⁽²⁾ | $V_{IN} = V_{SS}$ | 25 | 40 | 55 | k Ω |
| $V_F(NRST)$ | NRST input filtered pulse | - | - | - | $100^{(1)}$ | ns |
| $V_{NF(NRST)}$ | NRST input not filtered pulse | $2.7 < V_{DD} < 3.6$ | $300^{(3)}$ | - | - | ns |
| | | $2.0 < V_{DD} < 3.6$ | $500^{(3)}$ | - | - | |

1. Data based on design simulation only. Not tested in production.
2. The pull-up is designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance is minimal (~10% order).
3. Data based on design simulation only. Not tested in production.

Figure 24. Recommended NRST pin protection



1. The external capacitor protects the device against parasitic resets.
2. The user must ensure that the level on the NRST pin can go below the $V_{IL(NRST)}$ max level specified in [Table 51: NRST pin characteristics](#). Otherwise the reset will not be taken into account by the device.

6.3.16 12-bit ADC characteristics

Unless otherwise specified, the parameters given in [Table 52](#) are preliminary values derived from tests performed under ambient temperature, f_{PCLK} frequency and V_{DDA} supply voltage conditions summarized in [Table 20: General operating conditions](#).

Note: It is recommended to perform a calibration after each power-up.

Table 52. ADC characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|------------------|---|---|------|-----|-----------|-------------|
| V_{DDA} | Analog supply voltage for ADC ON | - | 2.4 | - | 3.6 | V |
| $I_{DDA(ADC)}$ | Current consumption of the ADC ⁽¹⁾ | $V_{DD} = V_{DDA} = 3.3\text{ V}$ | - | 0.9 | - | mA |
| f_{ADC} | ADC clock frequency | - | 0.6 | - | 14 | MHz |
| $f_S^{(2)}$ | Sampling rate | - | 0.05 | - | 1 | MHz |
| $f_{TRIG}^{(2)}$ | External trigger frequency | $f_{ADC} = 14\text{ MHz}$ | - | - | 823 | kHz |
| | | - | - | - | 17 | $1/f_{ADC}$ |
| V_{AIN} | Conversion voltage range | - | 0 | - | V_{DDA} | V |
| $R_{AIN}^{(2)}$ | External input impedance | See Equation 1 and Table 53 for details | - | - | 50 | kΩ |
| $R_{ADC}^{(2)}$ | Sampling switch resistance | - | - | - | 1 | kΩ |
| $C_{ADC}^{(2)}$ | Internal sample and hold capacitor | - | - | - | 8 | pF |
| $t_{CAL}^{(2)}$ | Calibration time | $f_{ADC} = 14\text{ MHz}$ | 5.9 | | | μs |
| | | - | 83 | | | $1/f_{ADC}$ |

Table 52. ADC characteristics (continued)

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-------------------------------------|---|--|---|-----|--|-------------------------|
| W _{LATENCY} ⁽²⁾ | ADC_DR register write latency | ADC clock = HSI14 | 1.5 ADC cycles + 2 f _{PCLK} cycles | - | 1.5 ADC cycles + 3 f _{PCLK} cycles | |
| | | ADC clock = PCLK/2 | - | 4.5 | - | f _{PCLK} cycle |
| | | ADC clock = PCLK/4 | - | 8.5 | - | f _{PCLK} cycle |
| t _{tr} ⁽²⁾ | Trigger conversion latency | f _{ADC} = f _{PCLK} /2 = 14 MHz | 0.196 | | | µs |
| | | f _{ADC} = f _{PCLK} /2 | 5.5 | | | 1/f _{PCLK} |
| | | f _{ADC} = f _{PCLK} /4 = 12 MHz | 0.219 | | | µs |
| | | f _{ADC} = f _{PCLK} /4 | 10.5 | | | 1/f _{PCLK} |
| | | f _{ADC} = f _{HSI14} = 14 MHz | 0.188 | - | 0.259 | µs |
| Jitter _{ADC} | ADC jitter on trigger conversion | f _{ADC} = f _{HSI14} | - | 1 | - | 1/f _{HSI14} |
| t _s ⁽²⁾ | Sampling time | f _{ADC} = 14 MHz | 0.107 | - | 17.1 | µs |
| | | - | 1.5 | - | 239.5 | 1/f _{ADC} |
| t _{STAB} ⁽²⁾ | Power-up time | - | - | - | 1 | Conversion cycle |
| t _{CONV} ⁽²⁾ | Total conversion time (including sampling time) | f _{ADC} = 14 MHz | 1 | - | 18 | µs |
| | | - | 14 to 252 (t _s for sampling + 12.5 for successive approximation) | | | 1/f _{ADC} |

1. During conversion of the sampled value (12.5 x ADC clock period), an additional consumption of 100 µA on I_DDA and 60 µA on I_DD should be taken into account.
2. Guaranteed by design, not tested in production.

Equation 1: R_{AIN} max formula

$$R_{AIN} < \frac{T_s}{f_{ADC} \times C_{ADC} \times \ln(2^{N+2})} - R_{ADC}$$

The formula above (Equation 1) is used to determine the maximum external impedance allowed for an error below 1/4 of LSB. Here N = 12 (from 12-bit resolution).

Table 53. R_{AIN} max for f_{ADC} = 14 MHz

| T _s (cycles) | t _s (µs) | R _{AIN} max (kΩ) ⁽¹⁾ |
|-------------------------|---------------------|--|
| 1.5 | 0.11 | 0.4 |
| 7.5 | 0.54 | 5.9 |
| 13.5 | 0.96 | 11.4 |
| 28.5 | 2.04 | 25.2 |
| 41.5 | 2.96 | 37.2 |



Table 53. R_{AIN} max for f_{ADC} = 14 MHz (continued)

| T _s (cycles) | t _s (μs) | R _{AIN} max (kΩ) ⁽¹⁾ |
|-------------------------|---------------------|--|
| 55.5 | 3.96 | 50 |
| 71.5 | 5.11 | NA |
| 239.5 | 17.1 | NA |

1. Guaranteed by design, not tested in production.

Table 54. ADC accuracy⁽¹⁾⁽²⁾⁽³⁾

| Symbol | Parameter | Test conditions | Typ | Max ⁽⁴⁾ | Unit |
|--------|------------------------------|---|------|--------------------|------|
| ET | Total unadjusted error | f _{PCLK} = 48 MHz, f _{ADC} = 14 MHz, R _{AIN} < 10 kΩ V _{DDA} = 3 V to 3.6 V T _A = 25 °C | ±1.3 | ±2 | LSB |
| EO | Offset error | | ±1 | ±1.5 | |
| EG | Gain error | | ±0.5 | ±1.5 | |
| ED | Differential linearity error | | ±0.7 | ±1 | |
| EL | Integral linearity error | | ±0.8 | ±1.5 | |
| ET | Total unadjusted error | f _{PCLK} = 48 MHz, f _{ADC} = 14 MHz, R _{AIN} < 10 kΩ V _{DDA} = 2.7 V to 3.6 V T _A = -40 to 105 °C | ±3.3 | ±4 | LSB |
| EO | Offset error | | ±1.9 | ±2.8 | |
| EG | Gain error | | ±2.8 | ±3 | |
| ED | Differential linearity error | | ±0.7 | ±1.3 | |
| EL | Integral linearity error | | ±1.2 | ±1.7 | |
| ET | Total unadjusted error | f _{PCLK} = 48 MHz, f _{ADC} = 14 MHz, R _{AIN} < 10 kΩ V _{DDA} = 2.4 V to 3.6 V T _A = 25 °C | ±3.3 | ±4 | LSB |
| EO | Offset error | | ±1.9 | ±2.8 | |
| EG | Gain error | | ±2.8 | ±3 | |
| ED | Differential linearity error | | ±0.7 | ±1.3 | |
| EL | Integral linearity error | | ±1.2 | ±1.7 | |

- ADC DC accuracy values are measured after internal calibration.
- ADC Accuracy vs. Negative Injection Current: Injecting negative current on any of the standard (non-robust) analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to standard analog pins which may potentially inject negative current. Any positive injection current within the limits specified for I_{INJ(PIN)} and ΣI_{INJ(PIN)} in [Section 6.3.14](#) does not affect the ADC accuracy.
- Better performance may be achieved in restricted V_{DDA}, frequency and temperature ranges.
- Data based on characterization results, not tested in production.

Figure 25. ADC accuracy characteristics

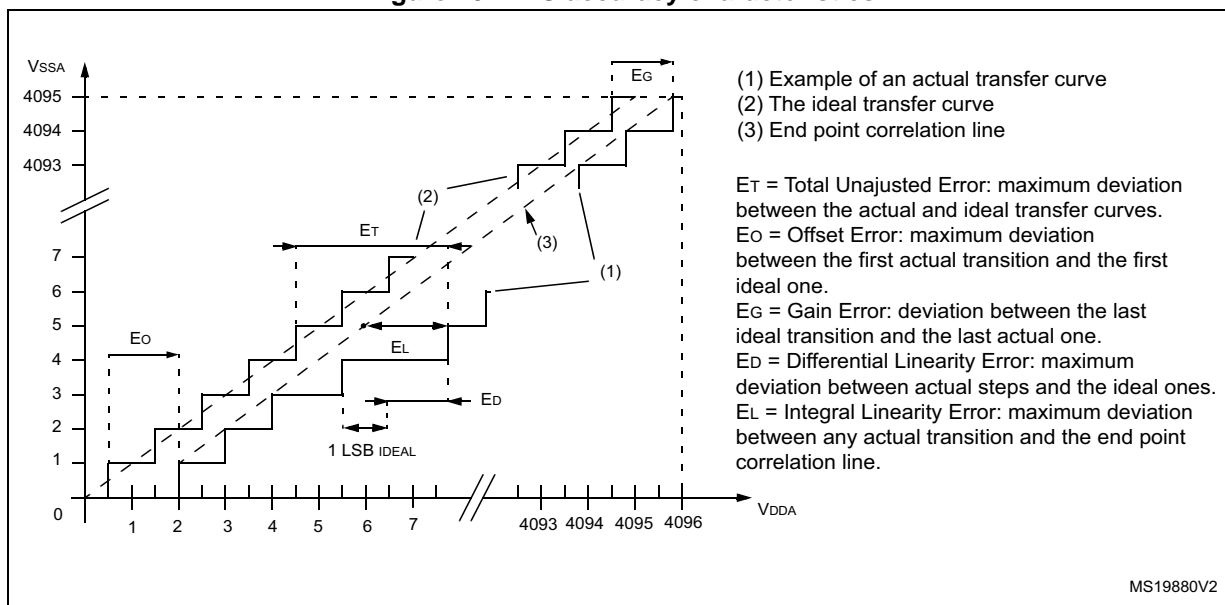
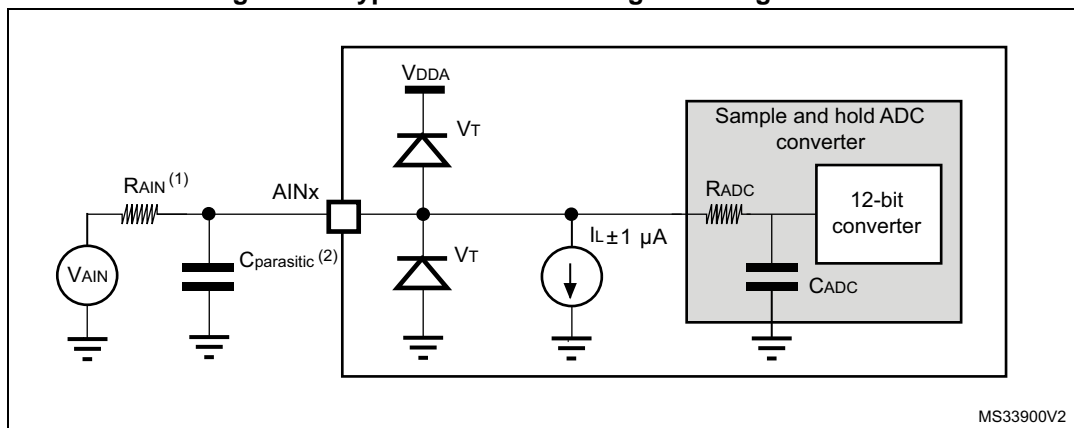


Figure 26. Typical connection diagram using the ADC



1. Refer to [Table 52: ADC characteristics](#) for the values of R_{AIN} , R_{ADC} and C_{ADC} .
2. $C_{parasitic}$ represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (roughly 7 pF). A high $C_{parasitic}$ value will downgrade conversion accuracy. To remedy this, f_{ADC} should be reduced.

General PCB design guidelines

Power supply decoupling should be performed as shown in [Figure 13: Power supply scheme](#). The 10 nF capacitor should be ceramic (good quality) and it should be placed as close as possible to the chip.

6.3.17 DAC electrical specifications

Table 55. DAC characteristics

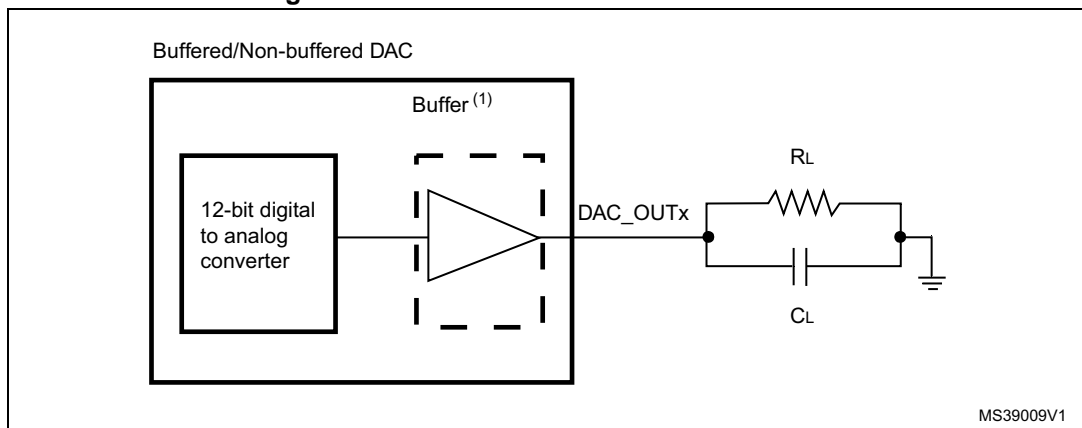
| Symbol | Parameter | Min | Typ | Max | Unit | Comments |
|----------------------------|---|-----|-----|------------------|------------|---|
| V_{DDA} | Analog supply voltage for DAC ON | 2.4 | - | 3.6 | V | |
| $R_{LOAD}^{(1)}$ | Resistive load with buffer ON | 5 | - | - | k Ω | Load is referred to ground |
| $R_O^{(1)}$ | Impedance output with buffer OFF | - | - | 15 | k Ω | When the buffer is OFF, the Minimum resistive load between DAC_OUT and V_{SS} to have a 1% accuracy is 1.5 M Ω |
| $C_{LOAD}^{(1)}$ | Capacitive load | - | - | 50 | pF | Maximum capacitive load at DAC_OUT pin (when the buffer is ON). |
| DAC_OUT min ⁽¹⁾ | Lower DAC_OUT voltage with buffer ON | 0.2 | - | - | V | It gives the maximum output excursion of the DAC. It corresponds to 12-bit input code (0x0E0) to (0xF1C) at $V_{DDA} = 3.6$ V and (0x155) and (0xEAB) at $V_{DDA} = 2.4$ V |
| DAC_OUT max ⁽¹⁾ | Higher DAC_OUT voltage with buffer ON | - | - | $V_{DDA} - 0.2$ | V | |
| DAC_OUT min ⁽¹⁾ | Lower DAC_OUT voltage with buffer OFF | - | 0.5 | - | mV | It gives the maximum output excursion of the DAC. |
| DAC_OUT max ⁽¹⁾ | Higher DAC_OUT voltage with buffer OFF | - | - | $V_{DDA} - 1LSB$ | V | |
| $I_{DDA}^{(1)}$ | DAC DC current consumption in quiescent mode ⁽²⁾ | - | - | 600 | μ A | With no load, middle code (0x800) on the input |
| | | - | - | 700 | μ A | With no load, worst code (0xF1C) on the input |
| DNL ⁽³⁾ | Differential non linearity Difference between two consecutive code-1LSB) | - | - | ± 0.5 | LSB | Given for the DAC in 10-bit configuration |
| | | - | - | ± 2 | LSB | Given for the DAC in 12-bit configuration |
| INL ⁽³⁾ | Integral non linearity (difference between measured value at Code i and the value at Code i on a line drawn between Code 0 and last Code 1023) | - | - | ± 1 | LSB | Given for the DAC in 10-bit configuration |
| | | - | - | ± 4 | LSB | Given for the DAC in 12-bit configuration |
| Offset ⁽³⁾ | Offset error (difference between measured value at Code (0x800) and the ideal value = $V_{DDA}/2$) | - | - | ± 10 | mV | |
| | | - | - | ± 3 | LSB | Given for the DAC in 10-bit at $V_{DDA} = 3.6$ V |
| | | - | - | ± 12 | LSB | Given for the DAC in 12-bit at $V_{DDA} = 3.6$ V |
| Gain error ⁽³⁾ | Gain error | - | - | ± 0.5 | % | Given for the DAC in 12-bit configuration |

Table 55. DAC characteristics (continued)

| Symbol | Parameter | Min | Typ | Max | Unit | Comments |
|----------------------------|--|-----|-----|-----|---------|--|
| $t_{SETTLING}^{(3)}$ | Settling time (full scale: for a 10-bit input code transition between the lowest and the highest input codes when DAC_OUT reaches final value $\pm 1LSB$) | - | 3 | 4 | μs | $C_{LOAD} \leq 50\text{ pF}$, $R_{LOAD} \geq 5\text{ k}\Omega$ |
| Update rate ⁽³⁾ | Max frequency for a correct DAC_OUT change when small variation in the input code (from code i to i+1LSB) | - | - | 1 | MS/s | $C_{LOAD} \leq 50\text{ pF}$, $R_{LOAD} \geq 5\text{ k}\Omega$ |
| $t_{WAKEUP}^{(3)}$ | Wakeup time from off state (Setting the ENx bit in the DAC Control register) | - | 6.5 | 10 | μs | $C_{LOAD} \leq 50\text{ pF}$, $R_{LOAD} \geq 5\text{ k}\Omega$ input code between lowest and highest possible ones. |
| PSRR+ ⁽¹⁾ | Power supply rejection ratio (to V_{DDA}) (static DC measurement) | - | -67 | -40 | dB | No R_{LOAD} , $C_{LOAD} = 50\text{ pF}$ |

1. Guaranteed by design, not tested in production.
2. The DAC is in “quiescent mode” when it keeps the value steady on the output so no dynamic consumption is involved.
3. Data based on characterization results, not tested in production.

Figure 27. 12-bit buffered / non-buffered DAC



1. The DAC integrates an output buffer that can be used to reduce the output impedance and to drive external loads directly without the use of an external operational amplifier. The buffer can be bypassed by configuring the BOFFx bit in the DAC_CR register.

6.3.18 Comparator characteristics

Table 56. Comparator characteristics

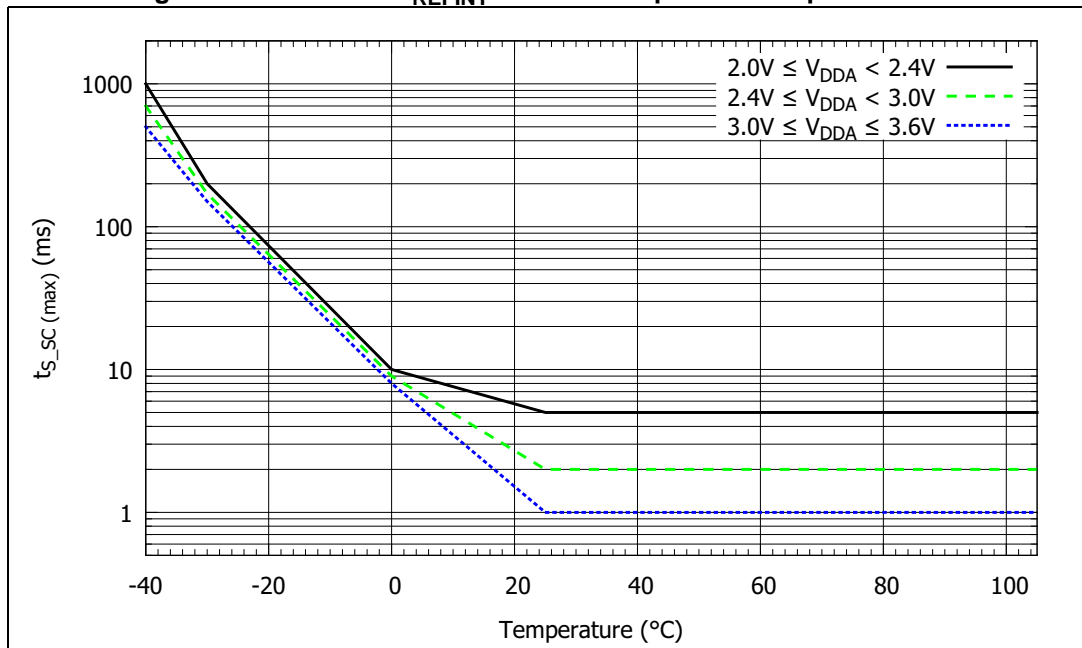
| Symbol | Parameter | Conditions | Min ⁽¹⁾ | Typ | Max ⁽¹⁾ | Unit |
|--------------------------|---|---|--------------------------|-----|---------------------|-------|
| V _{DDA} | Analog supply voltage | - | 2 | - | 3.6 | V |
| V _{IN} | Comparator input voltage range | - | 0 | - | V _{DDA} | |
| V _{SC} | V _{REFINT} scaler offset voltage | - | - | ±5 | ±10 | mV |
| t _{s_SC} | V _{REFINT} scaler startup time from power down | First V _{REFINT} scaler activation after device power on | - | - | 1000 ⁽²⁾ | ms |
| | | Next activations | - | - | 0.2 | |
| t _{START} | Comparator startup time | Startup time to reach propagation delay specification | - | - | 60 | µs |
| t _D | Propagation delay for 200 mV step with 100 mV overdrive | Ultra-low power mode | - | 2 | 4.5 | µs |
| | | Low power mode | - | 0.7 | 1.5 | |
| | | Medium power mode | - | 0.3 | 0.6 | |
| | | High speed mode | V _{DDA} ≥ 2.7 V | - | 50 | 100 |
| | V _{DDA} < 2.7 V | | - | 100 | 240 | |
| | Propagation delay for full range step with 100 mV overdrive | Ultra-low power mode | - | 2 | 7 | µs |
| | | Low power mode | - | 0.7 | 2.1 | |
| | | Medium power mode | - | 0.3 | 1.2 | |
| High speed mode | | V _{DDA} ≥ 2.7 V | - | 90 | 180 | ns |
| | V _{DDA} < 2.7 V | - | 110 | 300 | | |
| V _{offset} | Comparator offset error | | - | ±4 | ±10 | mV |
| dV _{offset} /dT | Offset error temperature coefficient | | - | 18 | - | µV/°C |
| I _{DD} (COMP) | COMP current consumption | Ultra-low power mode | - | 1.2 | 1.5 | µA |
| | | Low power mode | - | 3 | 5 | |
| | | Medium power mode | - | 10 | 15 | |
| | | High speed mode | - | 75 | 100 | |

Table 56. Comparator characteristics (continued)

| Symbol | Parameter | Conditions | Min ⁽¹⁾ | Typ | Max ⁽¹⁾ | Unit | |
|-----------------------|-----------------------|---------------------------------------|-----------------------|-----|--------------------|------|----|
| V _{hys} | Comparator hysteresis | No hysteresis (COMPxHYST[1:0]=00) | - | 0 | - | mV | |
| | | Low hysteresis (COMPxHYST[1:0]=01) | High speed mode | 3 | 8 | | 13 |
| | | | All other power modes | 5 | | | 10 |
| | | Medium hysteresis (COMPxHYST[1:0]=10) | High speed mode | 7 | 15 | | 26 |
| | | | All other power modes | 9 | | | 19 |
| | | High hysteresis (COMPxHYST[1:0]=11) | High speed mode | 18 | 31 | | 49 |
| All other power modes | 19 | | 40 | | | | |

1. Data based on characterization results, not tested in production.
2. For more details and conditions see [Figure 28: Maximum VREFINT scaler startup time from power down](#).

Figure 28. Maximum V_{REFINT} scaler startup time from power down



6.3.19 Temperature sensor characteristics

Table 57. TS characteristics

| Symbol | Parameter | Min | Typ | Max | Unit |
|-------------------------------|---|------|------|------|-------|
| T _L ⁽¹⁾ | V _{SENSE} linearity with temperature | - | ± 1 | ± 2 | °C |
| Avg_Slope ⁽¹⁾ | Average slope | 4.0 | 4.3 | 4.6 | mV/°C |
| V ₃₀ | Voltage at 30 °C (± 5 °C) ⁽²⁾ | 1.34 | 1.43 | 1.52 | V |

Table 57. TS characteristics

| Symbol | Parameter | Min | Typ | Max | Unit |
|---------------------|--|-----|-----|-----|---------|
| $t_{START}^{(1)}$ | ADC_IN16 buffer startup time | - | - | 10 | μs |
| $t_{S_temp}^{(1)}$ | ADC sampling time when reading the temperature | 4 | - | - | μs |

1. Guaranteed by design, not tested in production.
2. Measured at $V_{DDA} = 3.3 V \pm 10 mV$. The V_{30} ADC conversion result is stored in the TS_CAL1 byte. Refer to [Table 3: Temperature sensor calibration values](#).

6.3.20 V_{BAT} monitoring characteristics

Table 58. V_{BAT} monitoring characteristics

| Symbol | Parameter | Min | Typ | Max | Unit |
|---------------------|--|-----|--------|-----|-----------|
| R | Resistor bridge for V_{BAT} | - | 2 x 50 | - | $k\Omega$ |
| Q | Ratio on V_{BAT} measurement | - | 2 | - | |
| $E_r^{(1)}$ | Error on Q | -1 | - | +1 | % |
| $t_{S_vbat}^{(1)}$ | ADC sampling time when reading the V_{BAT} | 4 | - | - | μs |

1. Guaranteed by design, not tested in production.

6.3.21 Timer characteristics

The parameters given in the following tables are guaranteed by design.

Refer to [Section 6.3.14: I/O port characteristics](#) for details on the input/output alternate function characteristics (output compare, input capture, external clock, PWM output).

Table 59. TIMx characteristics

| Symbol | Parameter | Conditions | Min | Max | Unit |
|------------------|--|------------------------|--------|----------------------|---------------|
| $t_{res(TIM)}$ | Timer resolution time | - | 1 | - | $t_{TIMxCLK}$ |
| | | $f_{TIMxCLK} = 48 MHz$ | 20.8 | - | ns |
| f_{EXT} | Timer external clock frequency on CH1 to CH4 | - | 0 | $f_{TIMxCLK}/2$ | MHz |
| | | $f_{TIMxCLK} = 48 MHz$ | 0 | 24 | MHz |
| Res_{TIM} | Timer resolution | TIMx (except TIM2) | - | 16 | bit |
| | | TIM2 | - | 32 | |
| $t_{COUNTER}$ | 16-bit counter clock period | - | 1 | 65536 | $t_{TIMxCLK}$ |
| | | $f_{TIMxCLK} = 48 MHz$ | 0.0208 | 1365 | μs |
| t_{MAX_COUNT} | Maximum possible count with 32-bit counter | - | - | 65536×65536 | $t_{TIMxCLK}$ |
| | | $f_{TIMxCLK} = 48 MHz$ | - | 89.48 | s |

Table 60. IWDG min/max timeout period at 40 kHz (LSI)⁽¹⁾

| Prescaler divider | PR[2:0] bits | Min timeout RL[11:0]= 0x000 | Max timeout RL[11:0]= 0xFFFF | Unit |
|-------------------|--------------|--------------------------------|---------------------------------|------|
| /4 | 0 | 0.1 | 409.6 | ms |
| /8 | 1 | 0.2 | 819.2 | |
| /16 | 2 | 0.4 | 1638.4 | |
| /32 | 3 | 0.8 | 3276.8 | |
| /64 | 4 | 1.6 | 6553.6 | |
| /128 | 5 | 3.2 | 13107.2 | |
| /256 | 6 or 7 | 6.4 | 26214.4 | |

1. These timings are given for a 40 kHz clock but the microcontroller internal RC frequency can vary from 30 to 60 kHz. Moreover, given an exact RC oscillator frequency, the exact timings still depend on the phasing of the APB interface clock versus the LSI clock so that there is always a full RC period of uncertainty.

Table 61. WWDG min/max timeout value at 48 MHz (PCLK)

| Prescaler | WDGTB | Min timeout value | Max timeout value | Unit |
|-----------|-------|-------------------|-------------------|------|
| 1 | 0 | 0.0853 | 5.4613 | ms |
| 2 | 1 | 0.1706 | 10.9226 | |
| 4 | 2 | 0.3413 | 21.8453 | |
| 8 | 3 | 0.6826 | 43.6906 | |

6.3.22 Communication interfaces

I²C interface characteristics

The I2C interface meets the timings requirements of the I²C-bus specification and user manual rev. 03 for:

- Standard-mode (Sm): with a bit rate up to 100 kbit/s
- Fast-mode (Fm): with a bit rate up to 400 kbit/s
- Fast-mode Plus (Fm+): with a bit rate up to 1 Mbit/s.

The I2C timings requirements are guaranteed by design when the I2C peripheral is properly configured (refer to Reference manual).

The SDA and SCL I/O requirements are met with the following restrictions: the SDA and SCL I/O pins are not “true” open-drain. When configured as open-drain, the PMOS connected between the I/O pin and V_{DDIOx} is disabled, but is still present. Only FTf I/O pins support Fm+ low level output current maximum requirement. Refer to [Section 6.3.14: I/O port characteristics](#) for the I2C I/Os characteristics.

All I2C SDA and SCL I/Os embed an analog filter. Refer to the table below for the analog filter characteristics:

Table 62. I2C analog filter characteristics⁽¹⁾

| Symbol | Parameter | Min | Max | Unit |
|----------|--|-------------------|--------------------|------|
| t_{AF} | Maximum pulse width of spikes that are suppressed by the analog filter | 50 ⁽²⁾ | 260 ⁽³⁾ | ns |

1. Guaranteed by design, not tested in production.
2. Spikes with widths below $t_{AF(min)}$ are filtered.
3. Spikes with widths above $t_{AF(max)}$ are not filtered

SPI/I²S characteristics

Unless otherwise specified, the parameters given in [Table 63](#) for SPI or in [Table 64](#) for I²S are derived from tests performed under the ambient temperature, f_{PCLKX} frequency and supply voltage conditions summarized in [Table 20: General operating conditions](#).

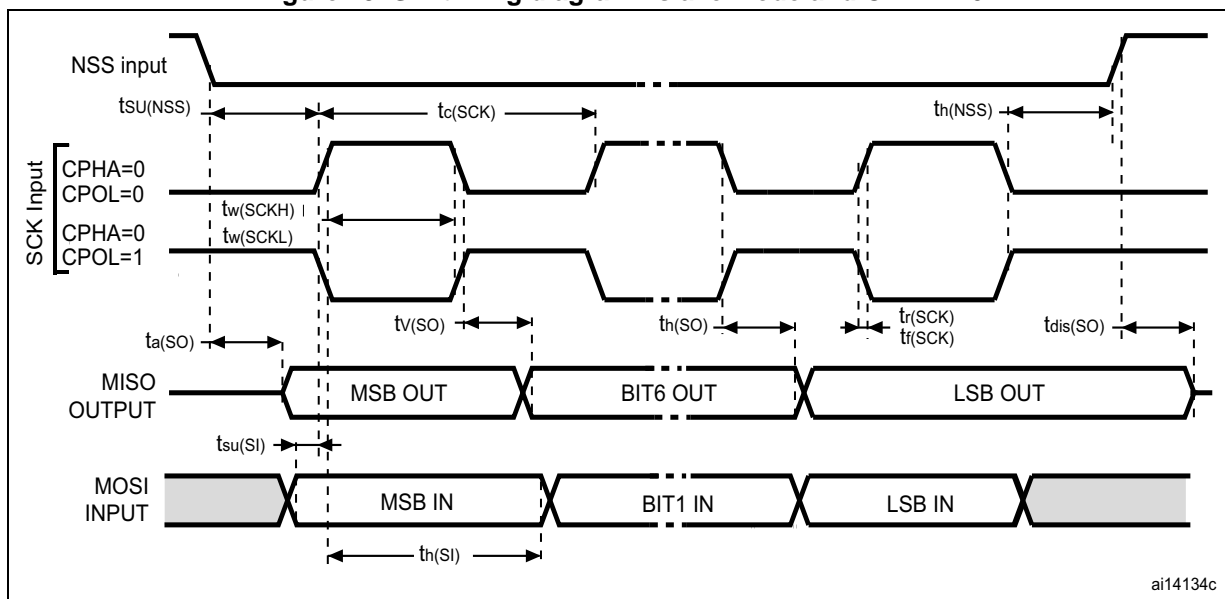
Refer to [Section 6.3.14: I/O port characteristics](#) for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO for SPI and WS, CK, SD for I²S).

Table 63. SPI characteristics⁽¹⁾

| Symbol | Parameter | Conditions | Min | Max | Unit |
|--------------------------------|----------------------------------|--|-------------|-------------|------|
| f_{SCK} $1/t_{c(SCK)}$ | SPI clock frequency | Master mode | - | 18 | MHz |
| | | Slave mode | - | 18 | |
| $t_{r(SCK)}$ $t_{f(SCK)}$ | SPI clock rise and fall time | Capacitive load: C = 15 pF | - | 6 | ns |
| $t_{su(NSS)}$ | NSS setup time | Slave mode | 4Tpclk | - | ns |
| $t_{h(NSS)}$ | NSS hold time | Slave mode | 2Tpclk + 10 | - | |
| $t_{w(SCKH)}$ $t_{w(SCKL)}$ | SCK high and low time | Master mode, $f_{PCLK} = 36$ MHz, presc = 4 | Tpclk/2 - 2 | Tpclk/2 + 1 | |
| $t_{su(MI)}$ $t_{su(SI)}$ | Data input setup time | Master mode | 4 | - | |
| | | Slave mode | 5 | - | |
| $t_{h(MI)}$ $t_{h(SI)}$ | Data input hold time | Master mode | 4 | - | |
| | | Slave mode | 5 | - | |
| $t_{a(SO)}^{(2)}$ | Data output access time | Slave mode, $f_{PCLK} = 20$ MHz | 0 | 3Tpclk | |
| $t_{dis(SO)}^{(3)}$ | Data output disable time | Slave mode | 0 | 18 | |
| $t_{v(SO)}$ | Data output valid time | Slave mode (after enable edge) | - | 22.5 | |
| $t_{v(MO)}$ | Data output valid time | Master mode (after enable edge) | - | 6 | |
| $t_{h(SO)}$ $t_{h(MO)}$ | Data output hold time | Slave mode (after enable edge) | 11.5 | - | |
| | | Master mode (after enable edge) | 2 | - | |
| DuCy(SCK) | SPI slave input clock duty cycle | Slave mode | 25 | 75 | |

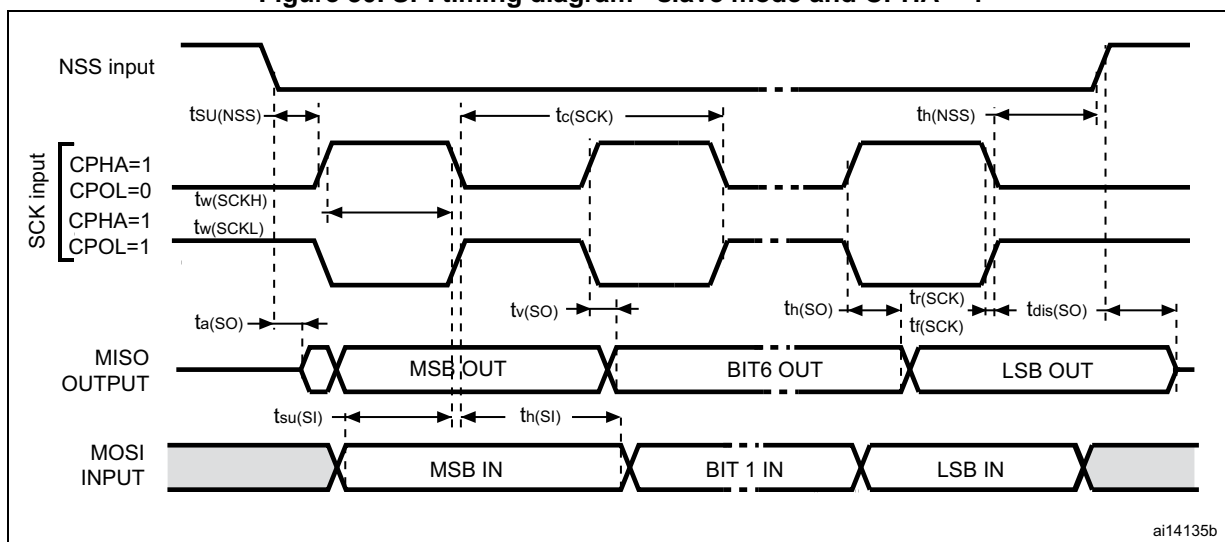
1. Data based on characterization results, not tested in production.
2. Min time is for the minimum time to drive the output and the max time is for the maximum time to validate the data.
3. Min time is for the minimum time to invalidate the output and the max time is for the maximum time to put the data in Hi-Z

Figure 29. SPI timing diagram - slave mode and CPHA = 0



ai14134c

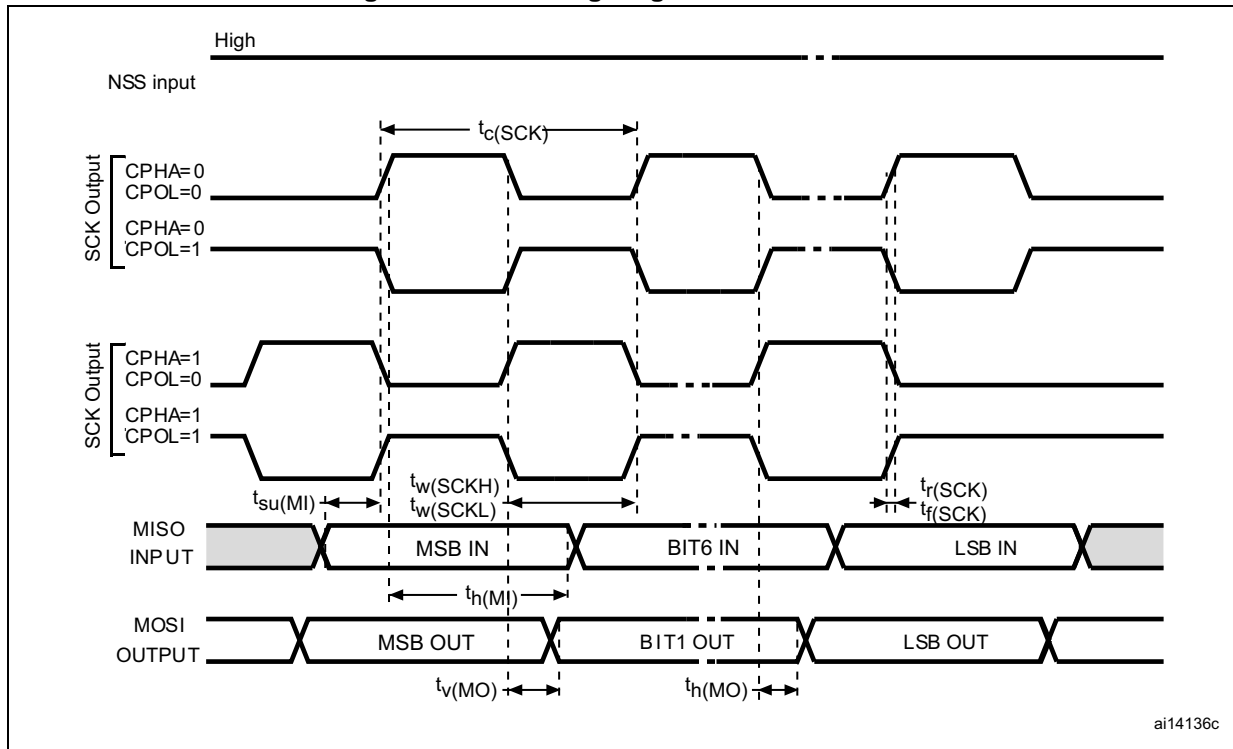
Figure 30. SPI timing diagram - slave mode and CPHA = 1



ai14135b

1. Measurement points are done at CMOS levels: 0.3 V_{DD} and 0.7 V_{DD} .

Figure 31. SPI timing diagram - master mode



1. Measurement points are done at CMOS levels: 0.3 V_{DD} and 0.7 V_{DD}.

Table 64. I²S characteristics⁽¹⁾

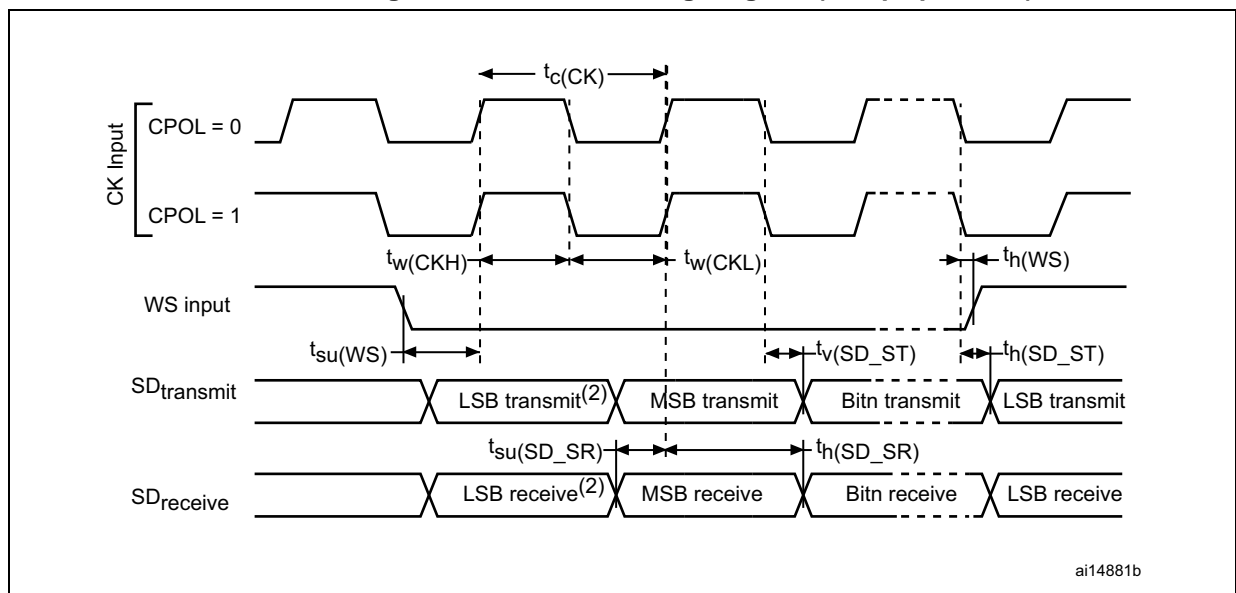
| Symbol | Parameter | Conditions | Min | Max | Unit |
|--------------------------|----------------------------------|---|-------|-------|------|
| f_{CK} 1/ $t_c(CK)$ | I ² S clock frequency | Master mode (data: 16 bits, Audio frequency = 48 kHz) | 1.597 | 1.601 | MHz |
| | | Slave mode | 0 | 6.5 | |
| $t_r(CK)$ | I ² S clock rise time | Capacitive load C _L = 15 pF | - | 10 | ns |
| $t_f(CK)$ | I ² S clock fall time | | - | 12 | |
| $t_w(CKH)$ | I2S clock high time | Master f_{PCLK} = 16 MHz, audio frequency = 48 kHz | 306 | - | |
| $t_w(CKL)$ | I2S clock low time | | 312 | - | |
| $t_v(WS)$ | WS valid time | Master mode | 2 | - | |
| $t_h(WS)$ | WS hold time | Master mode | 2 | - | |
| $t_{su}(WS)$ | WS setup time | Slave mode | 7 | - | |
| $t_h(WS)$ | WS hold time | Slave mode | 0 | - | |
| DuCy(SCK) | I2S slave input clock duty cycle | Slave mode | 25 | 75 | |

Table 64. I²S characteristics⁽¹⁾ (continued)

| Symbol | Parameter | Conditions | Min | Max | Unit |
|-----------------------|------------------------|--|-----|-----|------|
| $t_{su(SD_MR)}$ | Data input setup time | Master receiver | 6 | - | ns |
| $t_{su(SD_SR)}$ | Data input setup time | Slave receiver | 2 | - | |
| $t_{h(SD_MR)}^{(2)}$ | Data input hold time | Master receiver | 4 | - | |
| $t_{h(SD_SR)}^{(2)}$ | | Slave receiver | 0.5 | - | |
| $t_{v(SD_ST)}^{(2)}$ | Data output valid time | Slave transmitter (after enable edge) | - | 20 | |
| $t_{h(SD_ST)}$ | Data output hold time | Slave transmitter (after enable edge) | 13 | - | |
| $t_{v(SD_MT)}^{(2)}$ | Data output valid time | Master transmitter (after enable edge) | - | 4 | |
| $t_{h(SD_MT)}$ | Data output hold time | Master transmitter (after enable edge) | 0 | - | |

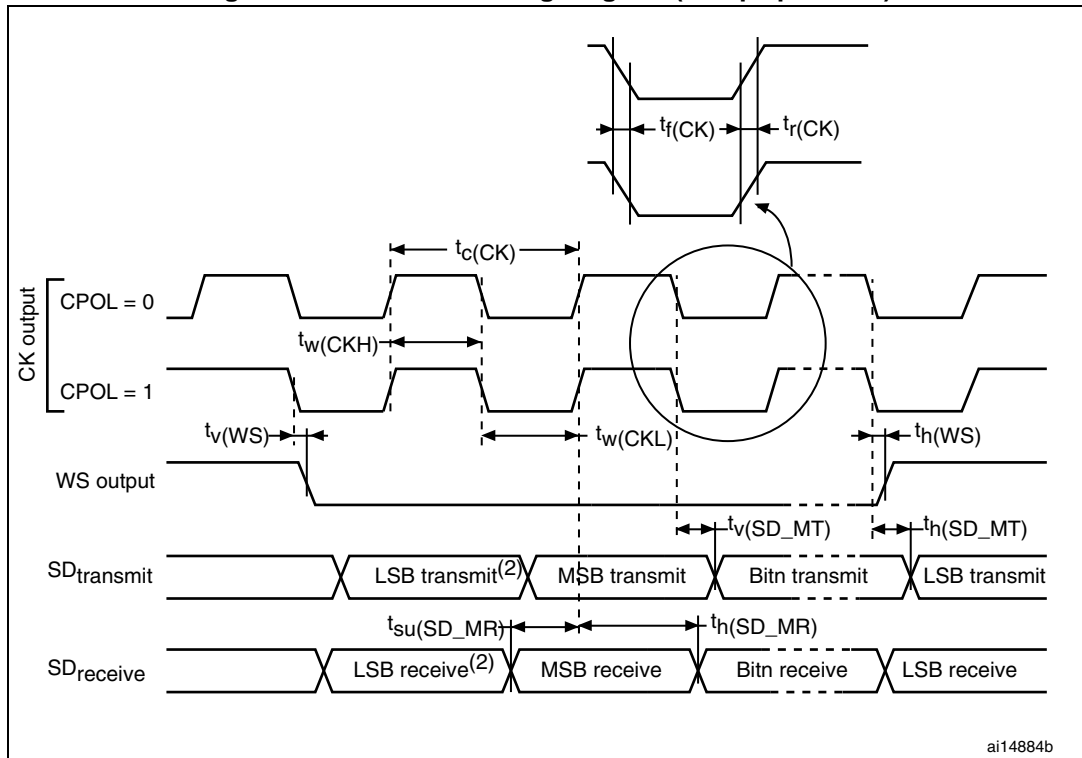
1. Data based on design simulation and/or characterization results, not tested in production.
2. Depends on f_{PCLK} . For example, if $f_{PCLK} = 8\text{ MHz}$, then $T_{PCLK} = 1/f_{PCLK} = 125\text{ ns}$.

Figure 32. I2S slave timing diagram (Philips protocol)



1. Measurement points are done at CMOS levels: $0.3 \times V_{DDIOx}$ and $0.7 \times V_{DDIOx}$.
2. LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

Figure 33. I2S master timing diagram (Philips protocol)



ai14884b

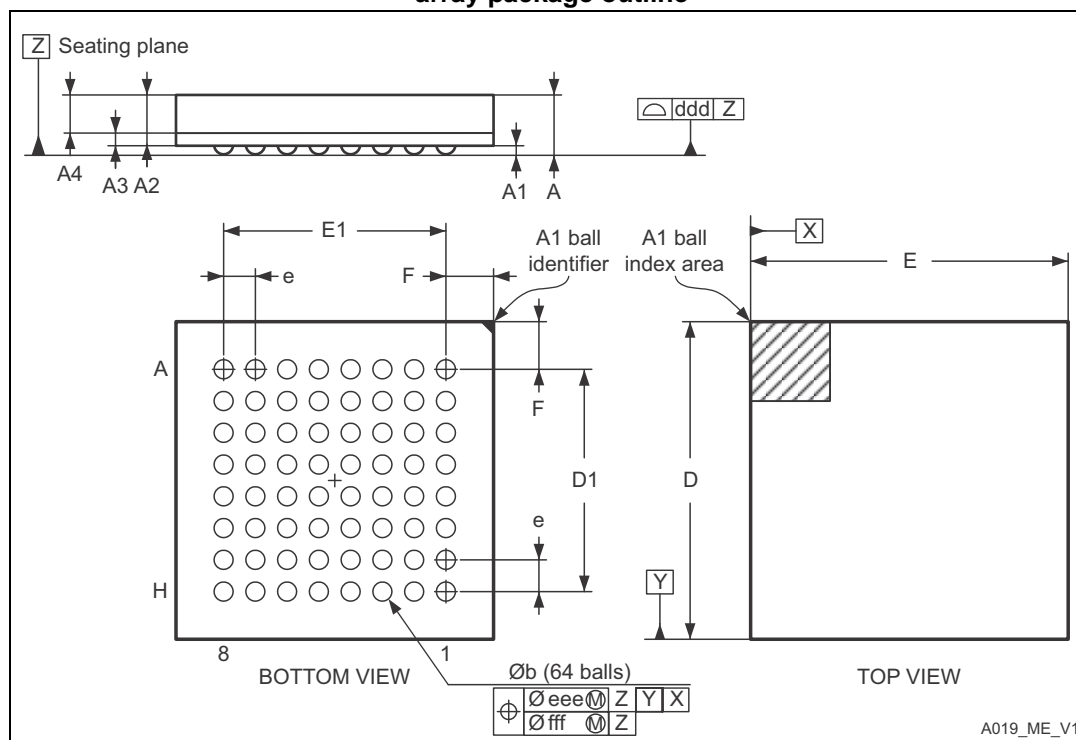
1. Data based on characterization results, not tested in production.
2. LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

7.1 UFBGA64 package information

Figure 34. UFBGA64 – 64-ball, 5 x 5 mm, 0.5 mm pitch ultra profile fine pitch ball grid array package outline



1. Drawing is not to scale.

Table 65. UFBGA64 – 64-ball, 5 x 5 mm, 0.5 mm pitch ultra profile fine pitch ball grid array package mechanical data

| Symbol | millimeters | | | inches ⁽¹⁾ | | |
|--------|-------------|-------|-------|-----------------------|--------|--------|
| | Min | Typ | Max | Min | Typ | Max |
| A | 0.460 | 0.530 | 0.600 | 0.0181 | 0.0209 | 0.0236 |
| A1 | 0.050 | 0.080 | 0.110 | 0.0020 | 0.0031 | 0.0043 |
| A2 | 0.400 | 0.450 | 0.500 | 0.0157 | 0.0177 | 0.0197 |
| A3 | 0.080 | 0.130 | 0.180 | 0.0031 | 0.0051 | 0.0071 |
| A4 | 0.270 | 0.320 | 0.370 | 0.0106 | 0.0126 | 0.0146 |

Table 65. UFBGA64 – 64-ball, 5 x 5 mm, 0.5 mm pitch ultra profile fine pitch ball grid array package mechanical data (continued)

| Symbol | millimeters | | | inches ⁽¹⁾ | | |
|--------|-------------|-------|-------|-----------------------|--------|--------|
| | Min | Typ | Max | Min | Typ | Max |
| A | 0.460 | 0.530 | 0.600 | 0.0181 | 0.0209 | 0.0236 |
| b | 0.170 | 0.280 | 0.330 | 0.0067 | 0.0110 | 0.0130 |
| D | 4.850 | 5.000 | 5.150 | 0.1909 | 0.1969 | 0.2028 |
| D1 | 3.450 | 3.500 | 3.550 | 0.1358 | 0.1378 | 0.1398 |
| E | 4.850 | 5.000 | 5.150 | 0.1909 | 0.1969 | 0.2028 |
| E1 | 3.450 | 3.500 | 3.550 | 0.1358 | 0.1378 | 0.1398 |
| e | - | 0.500 | - | - | 0.0197 | - |
| F | 0.700 | 0.750 | 0.800 | 0.0276 | 0.0295 | 0.0315 |
| ddd | - | - | 0.080 | - | - | 0.0031 |
| eee | - | - | 0.150 | - | - | 0.0059 |
| fff | - | - | 0.050 | - | - | 0.0020 |

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 35. UFBGA64 – 64-ball, 5 x 5 mm, 0.5 mm pitch ultra profile fine pitch ball grid array package recommended footprint

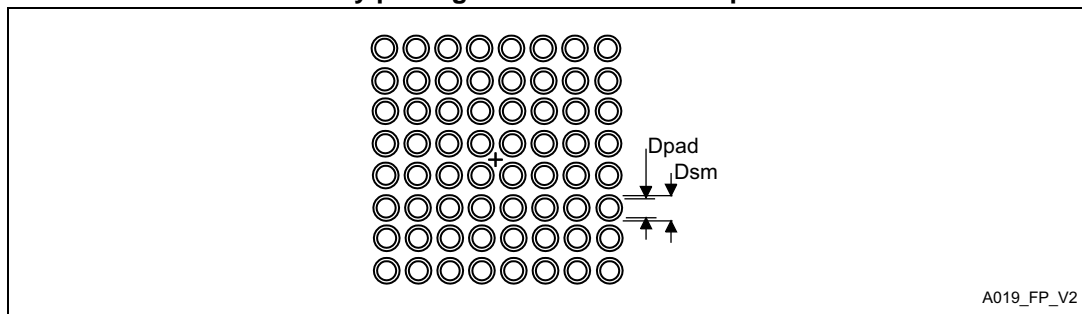


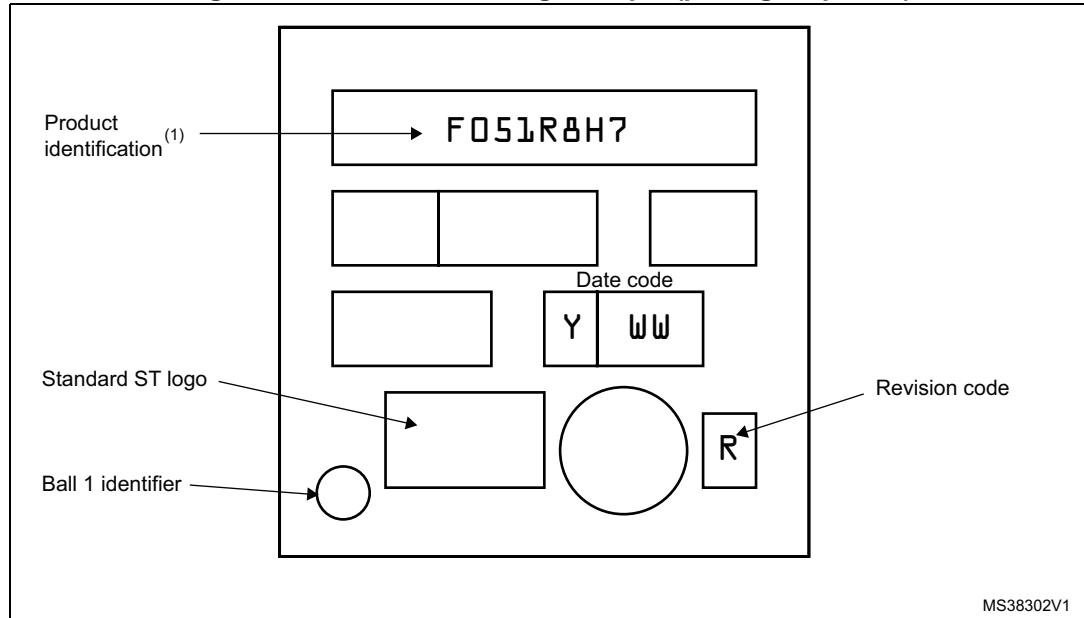
Table 66. UFBGA64 recommended PCB design rules (0.5 mm pitch BGA)

| Dimension | Recommended values |
|-------------------|--|
| Pitch | 0.5 |
| Dpad | 0.280 mm |
| Dsm | 0.370 mm typ. (depends on the soldermask registration tolerance) |
| Stencil opening | 0.280 mm |
| Stencil thickness | Between 0.100 mm and 0.125 mm |
| Pad trace width | 0.100 mm |

Device marking

The following figure gives an example of topside marking orientation versus ball A1 identifier location.

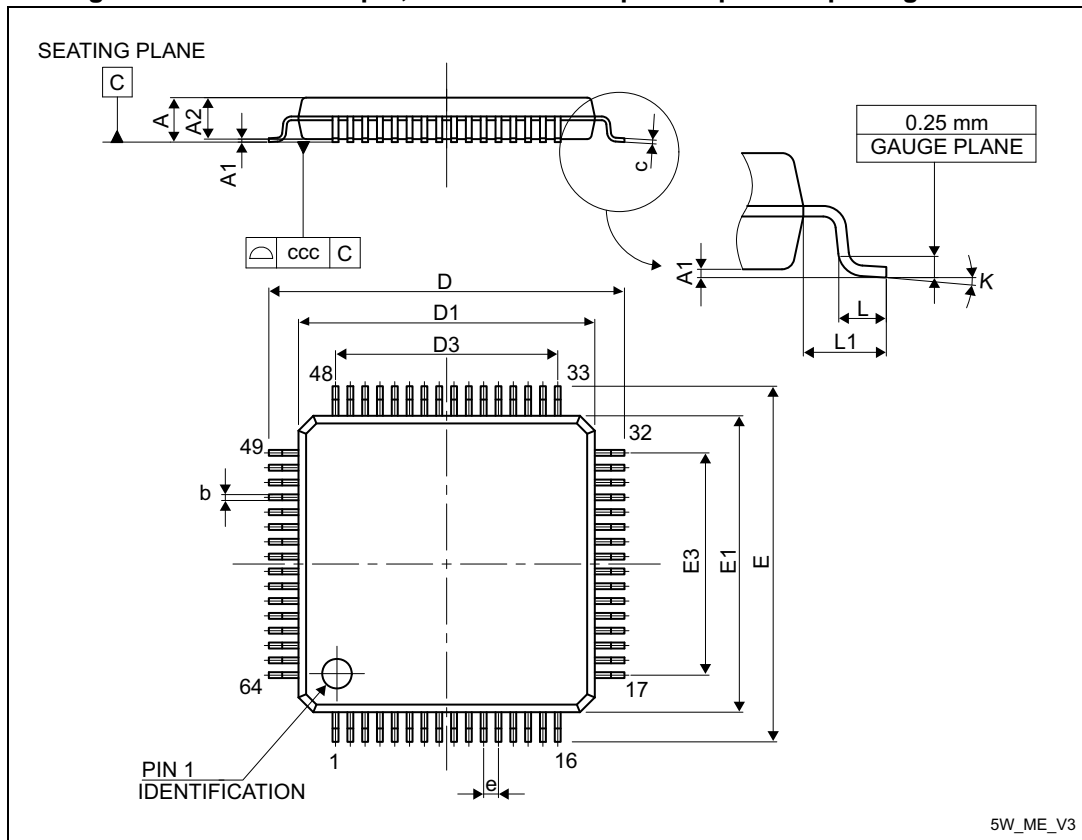
Figure 36. UFBGA64 marking example (package top view)



1. Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.

7.2 LQFP64 package information

Figure 37. LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package outline



1. Drawing is not to scale.

Table 67. LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package mechanical data

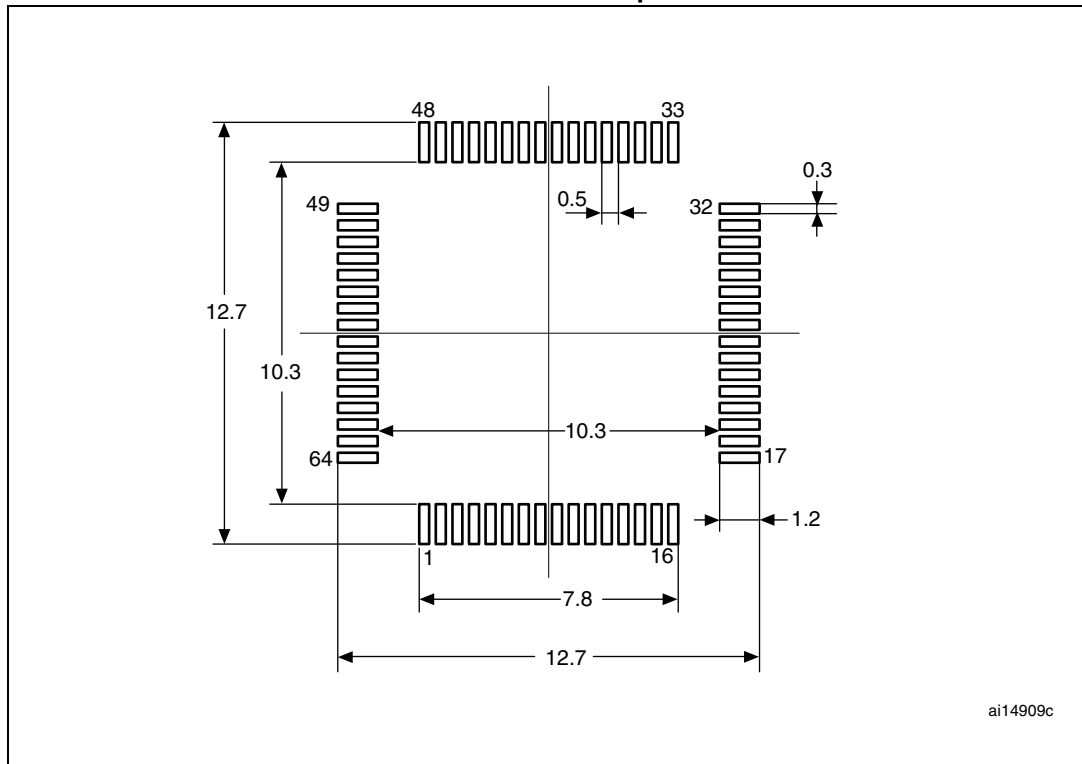
| Symbol | millimeters | | | inches ⁽¹⁾ | | |
|--------|-------------|--------|-------|-----------------------|--------|--------|
| | Min | Typ | Max | Min | Typ | Max |
| A | - | - | 1.600 | - | - | 0.0630 |
| A1 | 0.050 | - | 0.150 | 0.0020 | - | 0.0059 |
| A2 | 1.350 | 1.400 | 1.450 | 0.0531 | 0.0551 | 0.0571 |
| b | 0.170 | 0.220 | 0.270 | 0.0067 | 0.0087 | 0.0106 |
| c | 0.090 | - | 0.200 | 0.0035 | - | 0.0079 |
| D | - | 12.000 | - | - | 0.4724 | - |
| D1 | - | 10.000 | - | - | 0.3937 | - |
| D3 | - | 7.500 | - | - | 0.2953 | - |
| E | - | 12.000 | - | - | 0.4724 | - |
| E1 | - | 10.000 | - | - | 0.3937 | - |

Table 67. LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package mechanical data (continued)

| Symbol | millimeters | | | inches ⁽¹⁾ | | |
|--------|-------------|-------|-------|-----------------------|--------|--------|
| | Min | Typ | Max | Min | Typ | Max |
| E3 | - | 7.500 | - | - | 0.2953 | - |
| e | - | 0.500 | - | - | 0.0197 | - |
| K | 0° | 3.5° | 7° | 0° | 3.5° | 7° |
| L | 0.450 | 0.600 | 0.750 | 0.0177 | 0.0236 | 0.0295 |
| L1 | - | 1.000 | - | - | 0.0394 | - |
| ccc | - | - | 0.080 | - | - | 0.0031 |

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 38. LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package recommended footprint

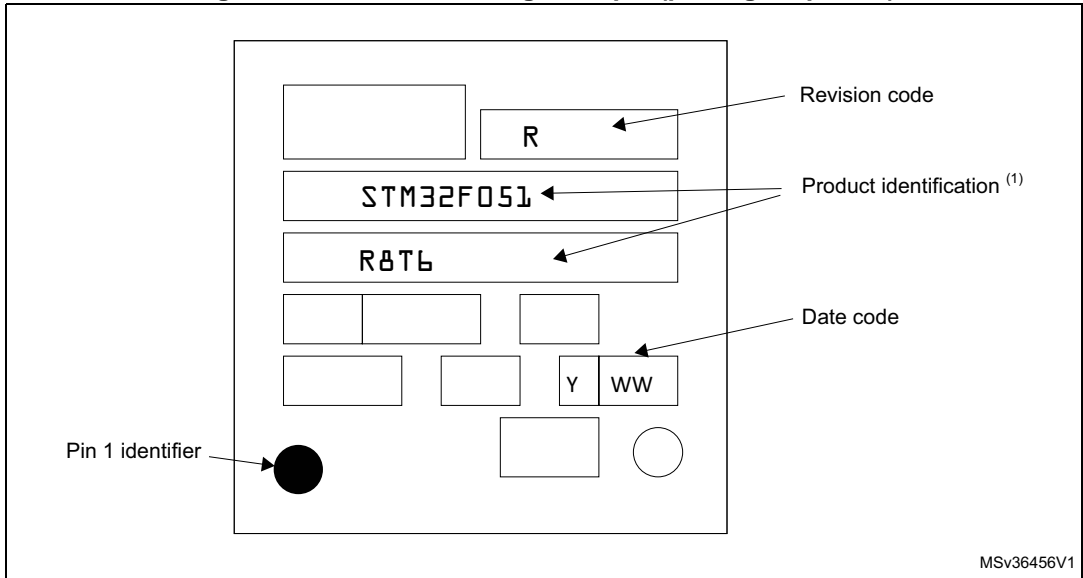


1. Dimensions are expressed in millimeters.

Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

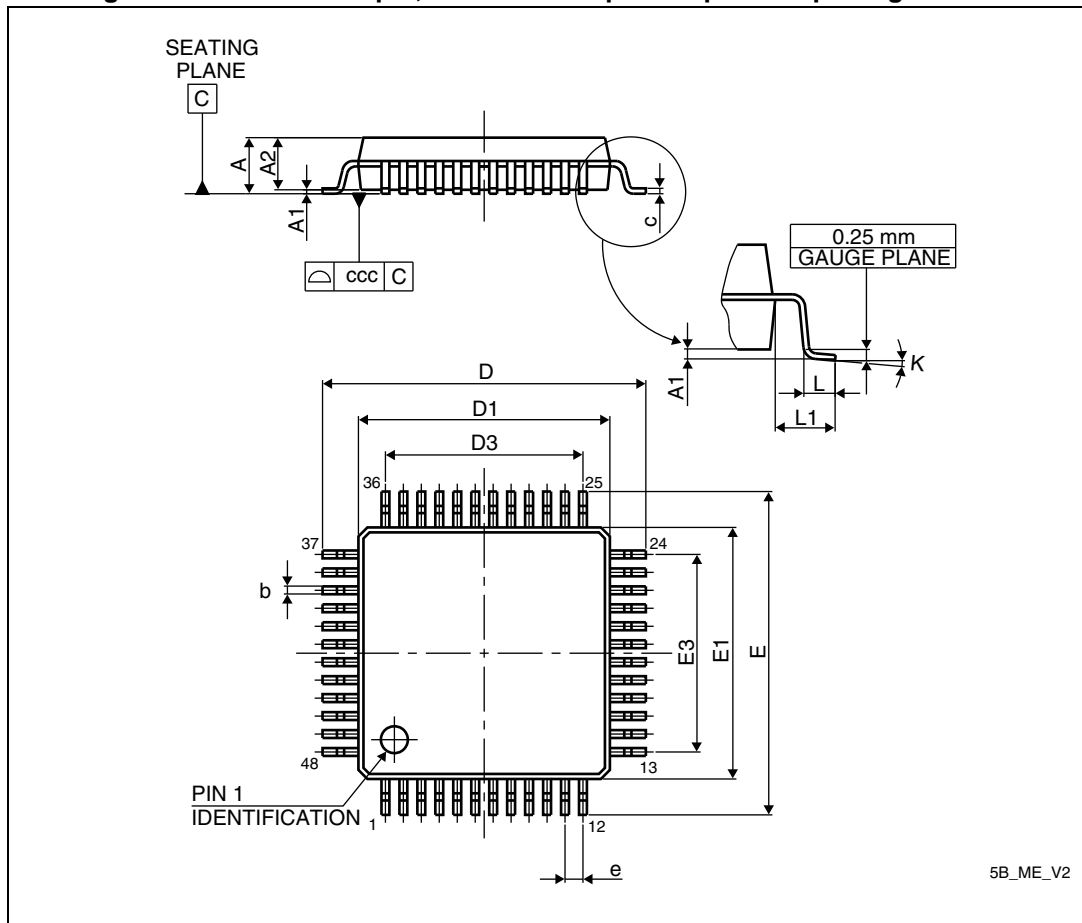
Figure 39. LQFP64 marking example (package top view)



1. Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.

7.3 LQFP48 package information

Figure 40. LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package outline



1. Drawing is not to scale.

**Table 68. LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package
mechanical data**

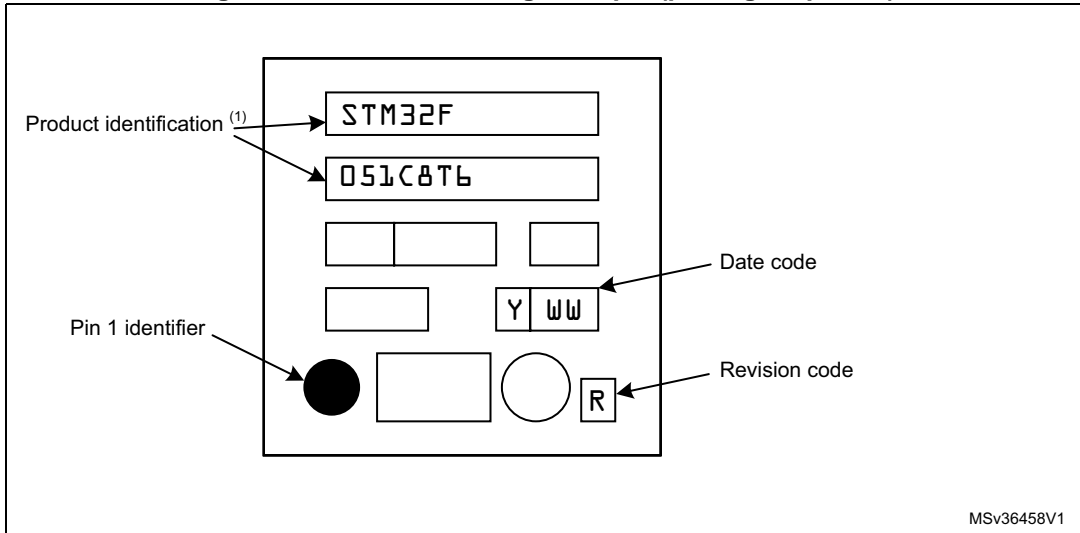
| Symbol | millimeters | | | inches ⁽¹⁾ | | |
|--------|-------------|-------|-------|-----------------------|--------|--------|
| | Min | Typ | Max | Min | Typ | Max |
| A | - | - | 1.600 | - | - | 0.0630 |
| A1 | 0.050 | - | 0.150 | 0.0020 | - | 0.0059 |
| A2 | 1.350 | 1.400 | 1.450 | 0.0531 | 0.0551 | 0.0571 |
| b | 0.170 | 0.220 | 0.270 | 0.0067 | 0.0087 | 0.0106 |
| c | 0.090 | - | 0.200 | 0.0035 | - | 0.0079 |
| D | 8.800 | 9.000 | 9.200 | 0.3465 | 0.3543 | 0.3622 |
| D1 | 6.800 | 7.000 | 7.200 | 0.2677 | 0.2756 | 0.2835 |
| D3 | - | 5.500 | - | - | 0.2165 | - |
| E | 8.800 | 9.000 | 9.200 | 0.3465 | 0.3543 | 0.3622 |
| E1 | 6.800 | 7.000 | 7.200 | 0.2677 | 0.2756 | 0.2835 |
| E3 | - | 5.500 | - | - | 0.2165 | - |
| e | - | 0.500 | - | - | 0.0197 | - |
| L | 0.450 | 0.600 | 0.750 | 0.0177 | 0.0236 | 0.0295 |
| L1 | - | 1.000 | - | - | 0.0394 | - |
| k | 0° | 3.5° | 7° | 0° | 3.5° | 7° |
| ccc | - | - | 0.080 | - | - | 0.0031 |

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

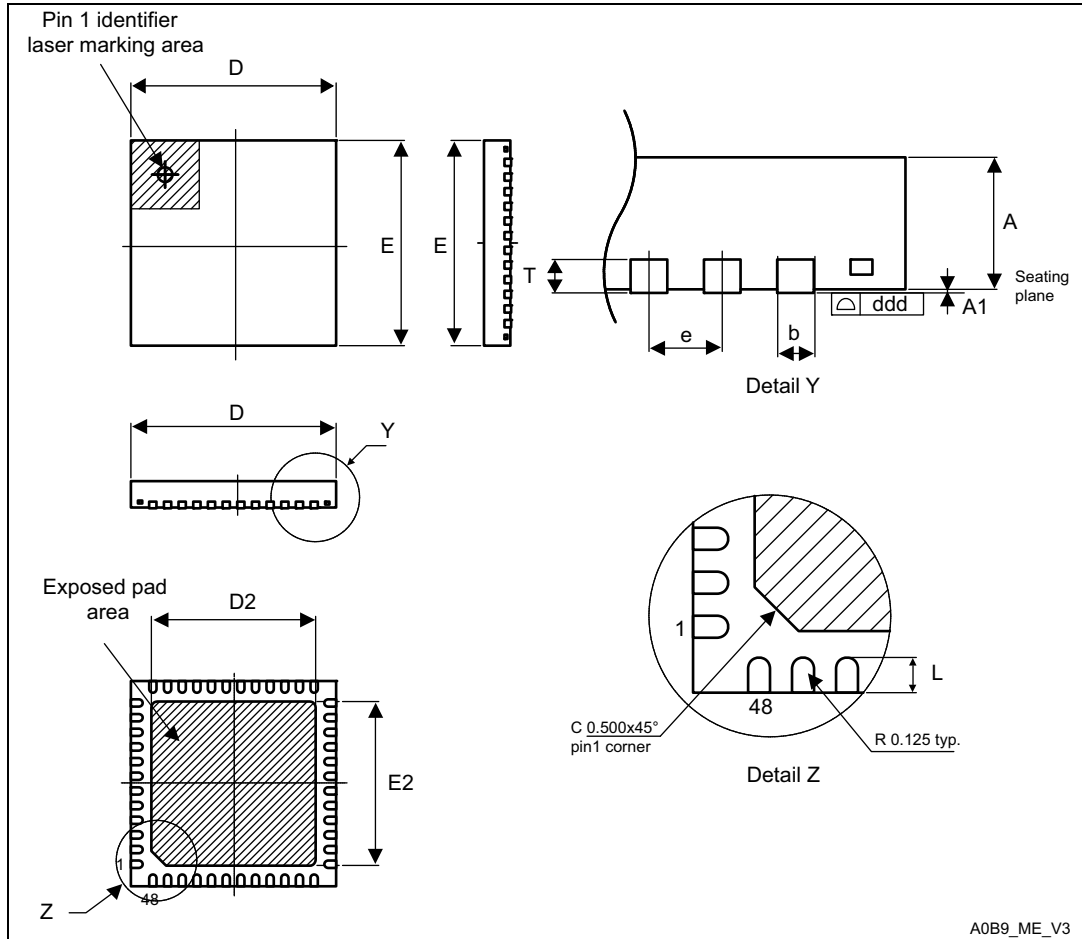
Figure 42. LQFP48 marking example (package top view)



1. Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.

7.4 UFQFPN48 package information

Figure 43. UFQFPN48 - 48-lead, 7x7 mm, 0.5 mm pitch, ultra thin fine pitch quad flat package outline

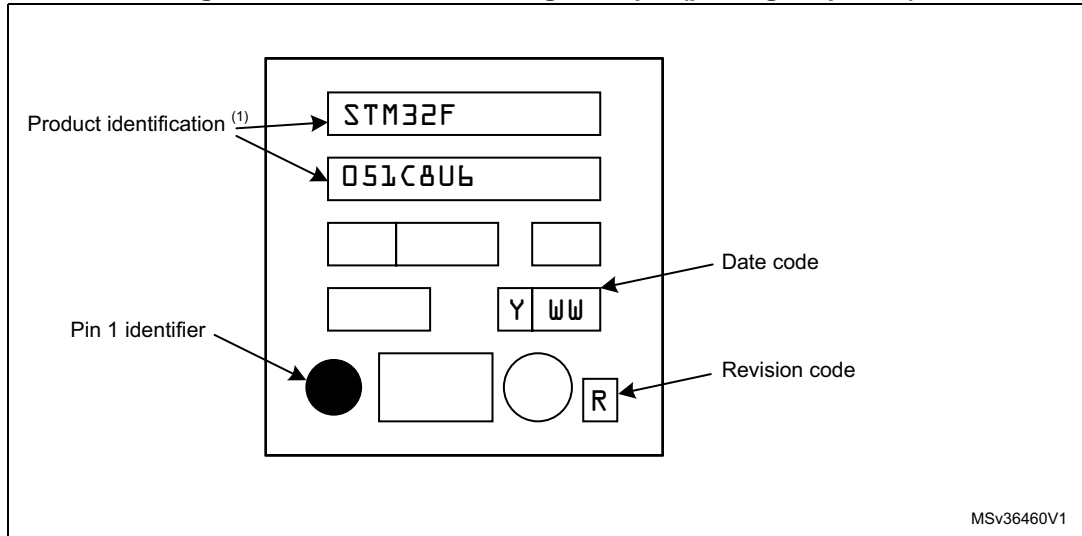


1. Drawing is not to scale.
2. All leads/pads should also be soldered to the PCB to improve the lead/pad solder joint life.
3. There is an exposed die pad on the underside of the UFQFPN package. It is recommended to connect and solder this back-side pad to PCB ground.

Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

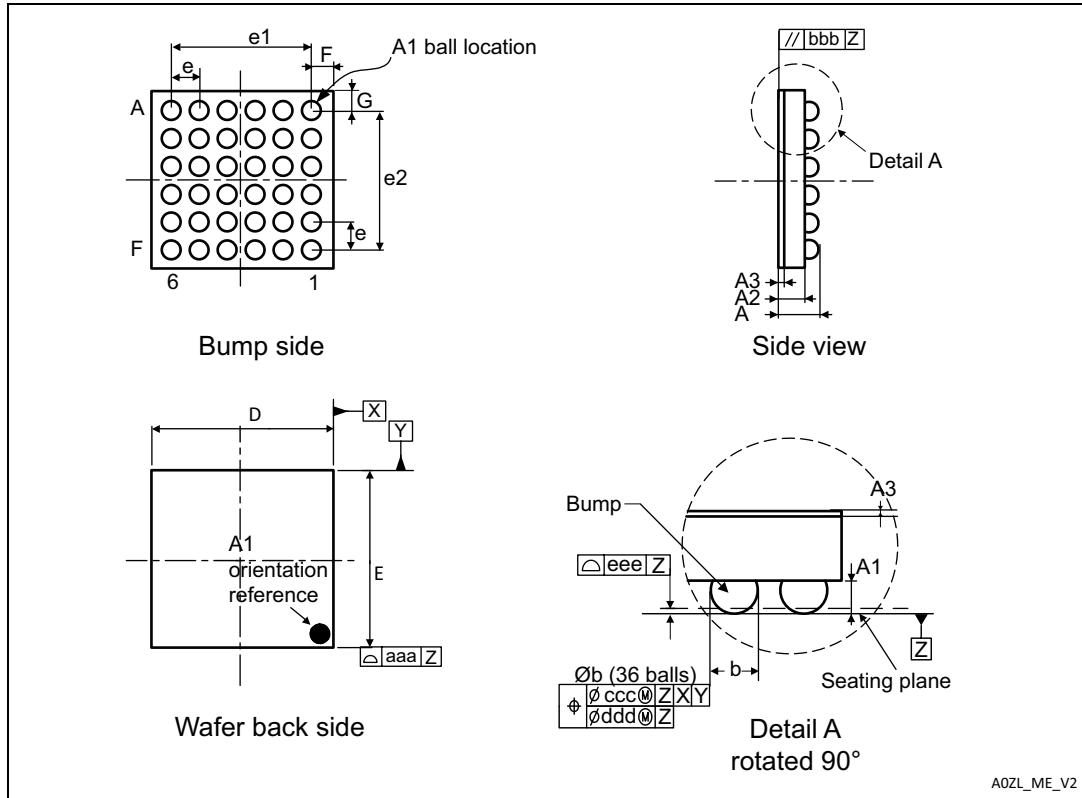
Figure 45. UFQFPN48 marking example (package top view)



1. Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.

7.5 WLCSP36 package information

Figure 46. WLCSP36 - 36-ball, 2.605 x 2.703 mm, 0.4 mm pitch wafer level chip scale package outline



1. Drawing is not to scale.

Table 70. WLCSP36 - 36-ball, 2.605 x 2.703 mm, 0.4 mm pitch wafer level chip scale package mechanical data

| Symbol | millimeters | | | inches ⁽¹⁾ | | |
|-------------------|-------------|-------|-------|-----------------------|--------|--------|
| | Min | Typ | Max | Min | Typ | Max |
| A | 0.525 | 0.555 | 0.585 | 0.0207 | 0.0219 | 0.0230 |
| A1 | - | 0.175 | - | - | 0.0069 | - |
| A2 | - | 0.380 | - | - | 0.0150 | - |
| A3 ⁽²⁾ | - | 0.025 | - | - | 0.0010 | - |
| b ⁽³⁾ | 0.220 | 0.250 | 0.280 | 0.0087 | 0.0098 | 0.0110 |
| D | 2.570 | 2.605 | 2.640 | 0.1012 | 0.1026 | 0.1039 |
| E | 2.668 | 2.703 | 2.738 | 0.1050 | 0.1064 | 0.1078 |
| e | - | 0.400 | - | - | 0.0157 | - |
| e1 | - | 2.000 | - | - | 0.0787 | - |
| e2 | - | 2.000 | - | - | 0.0787 | - |

Table 70. WLCSP36 - 36-ball, 2.605 x 2.703 mm, 0.4 mm pitch wafer level chip scale package mechanical data (continued)

| Symbol | millimeters | | | inches ⁽¹⁾ | | |
|--------|-------------|--------|-------|-----------------------|--------|--------|
| | Min | Typ | Max | Min | Typ | Max |
| F | - | 0.3025 | - | - | 0.0119 | - |
| G | - | 0.3515 | - | - | 0.0138 | - |
| aaa | - | - | 0.100 | - | - | 0.0039 |
| bbb | - | - | 0.100 | - | - | 0.0039 |
| ccc | - | - | 0.100 | - | - | 0.0039 |
| ddd | - | - | 0.050 | - | - | 0.0020 |
| eee | - | - | 0.050 | - | - | 0.0020 |

1. Values in inches are converted from mm and rounded to 4 decimal digits.
2. Back side coating.
3. Dimension is measured at the maximum bump diameter parallel to primary datum Z.

Figure 47. WLCSP36 - 36-ball, 2.605 x 2.703 mm, 0.4 mm pitch wafer level chip scale package recommended footprint

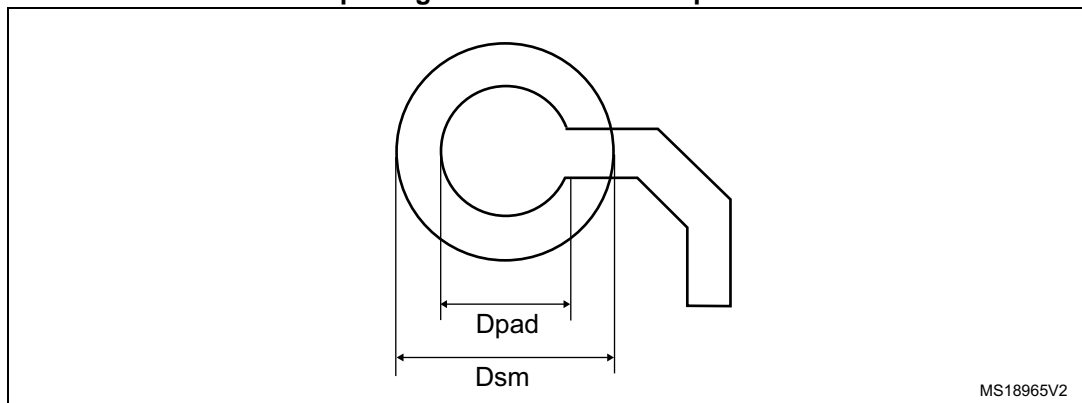


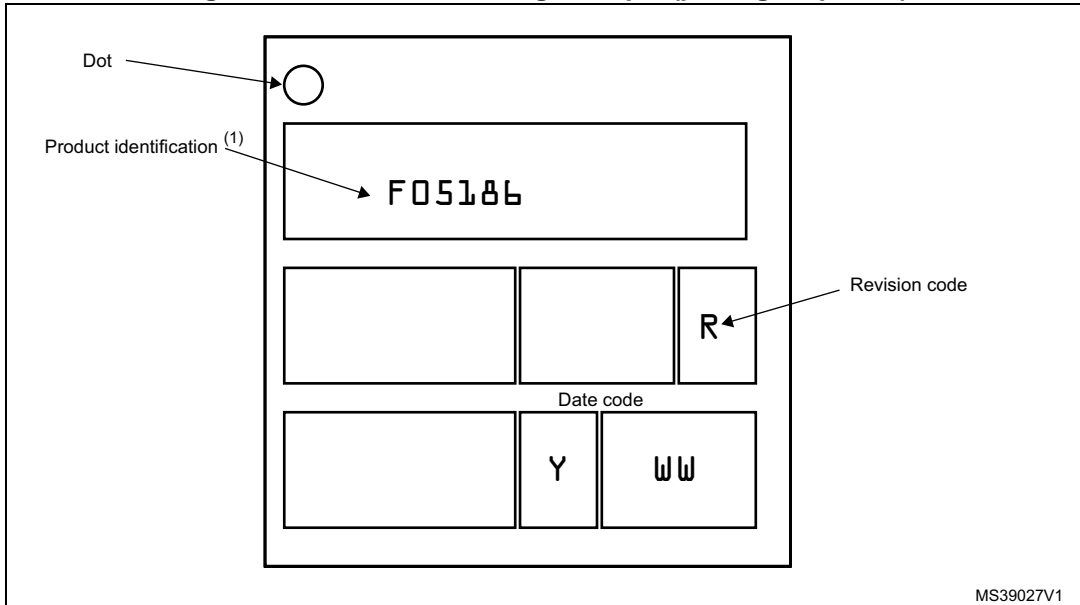
Table 71. WLCSP36 recommended PCB design rules

| Dimension | Recommended values |
|----------------|---|
| Pitch | 0.4 mm |
| Dpad | 260 μm max. (circular) 220 μm recommended |
| Dsm | 300 μm min. (for 260 μm diameter pad) |
| PCB pad design | Non-solder mask defined via underbump allowed |

Device marking

The following figure gives an example of topside marking orientation versus ball A1 identifier location.

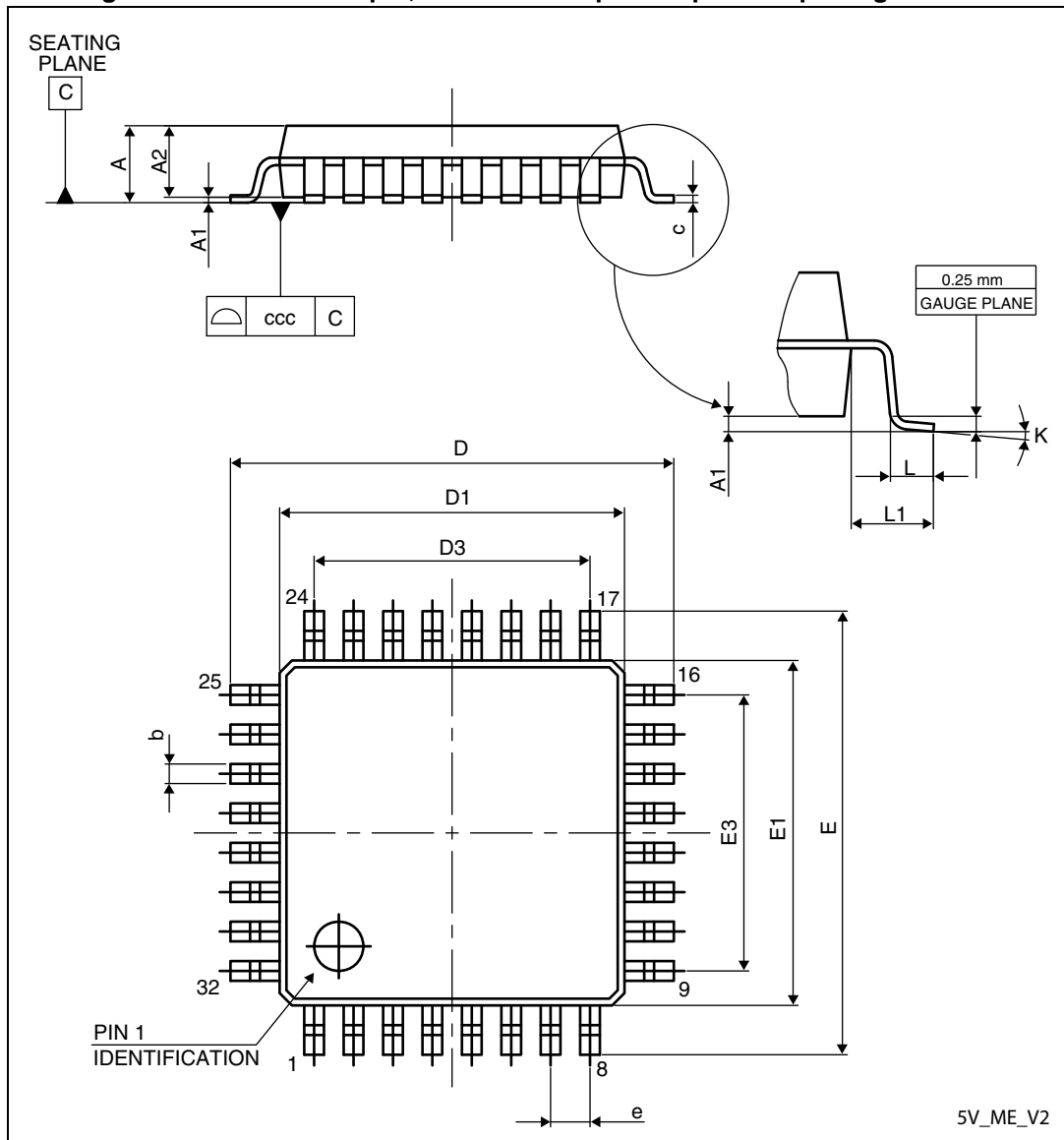
Figure 48. WLCSP36 marking example (package top view)



1. Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.

7.6 LQFP32 package information

Figure 49. LQFP32 - 32-pin, 7 x 7 mm low-profile quad flat package outline



5V_ME_V2

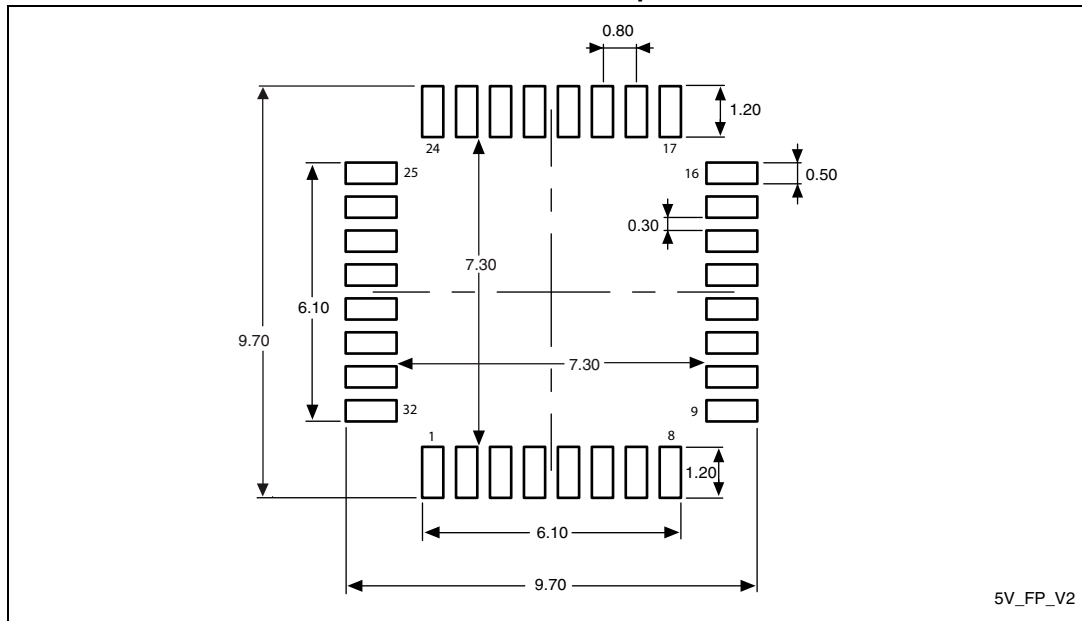
1. Drawing is not to scale.

Table 72. LQFP32 - 32-pin, 7 x 7 mm low-profile quad flat package mechanical data

| Symbol | millimeters | | | inches ⁽¹⁾ | | |
|--------|-------------|-------|-------|-----------------------|--------|--------|
| | Min | Typ | Max | Min | Typ | Max |
| A | - | - | 1.600 | - | - | 0.0630 |
| A1 | 0.050 | - | 0.150 | 0.0020 | - | 0.0059 |
| A2 | 1.350 | 1.400 | 1.450 | 0.0531 | 0.0551 | 0.0571 |
| b | 0.300 | 0.370 | 0.450 | 0.0118 | 0.0146 | 0.0177 |
| c | 0.090 | - | 0.200 | 0.0035 | - | 0.0079 |
| D | 8.800 | 9.000 | 9.200 | 0.3465 | 0.3543 | 0.3622 |
| D1 | 6.800 | 7.000 | 7.200 | 0.2677 | 0.2756 | 0.2835 |
| D3 | - | 5.600 | - | - | 0.2205 | - |
| E | 8.800 | 9.000 | 9.200 | 0.3465 | 0.3543 | 0.3622 |
| E1 | 6.800 | 7.000 | 7.200 | 0.2677 | 0.2756 | 0.2835 |
| E3 | - | 5.600 | - | - | 0.2205 | - |
| e | - | 0.800 | - | - | 0.0315 | - |
| L | 0.450 | 0.600 | 0.750 | 0.0177 | 0.0236 | 0.0295 |
| L1 | - | 1.000 | - | - | 0.0394 | - |
| k | 0° | 3.5° | 7° | 0° | 3.5° | 7° |
| ccc | - | - | 0.100 | - | - | 0.0039 |

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 50. LQFP32 - 32-pin, 7 x 7 mm low-profile quad flat package recommended footprint

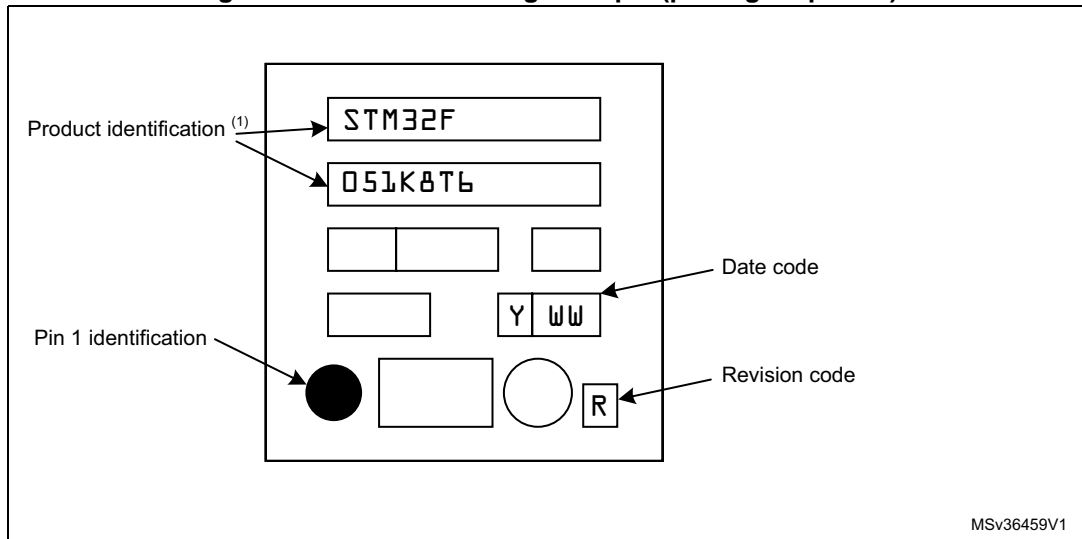


1. Dimensions are expressed in millimeters.

Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

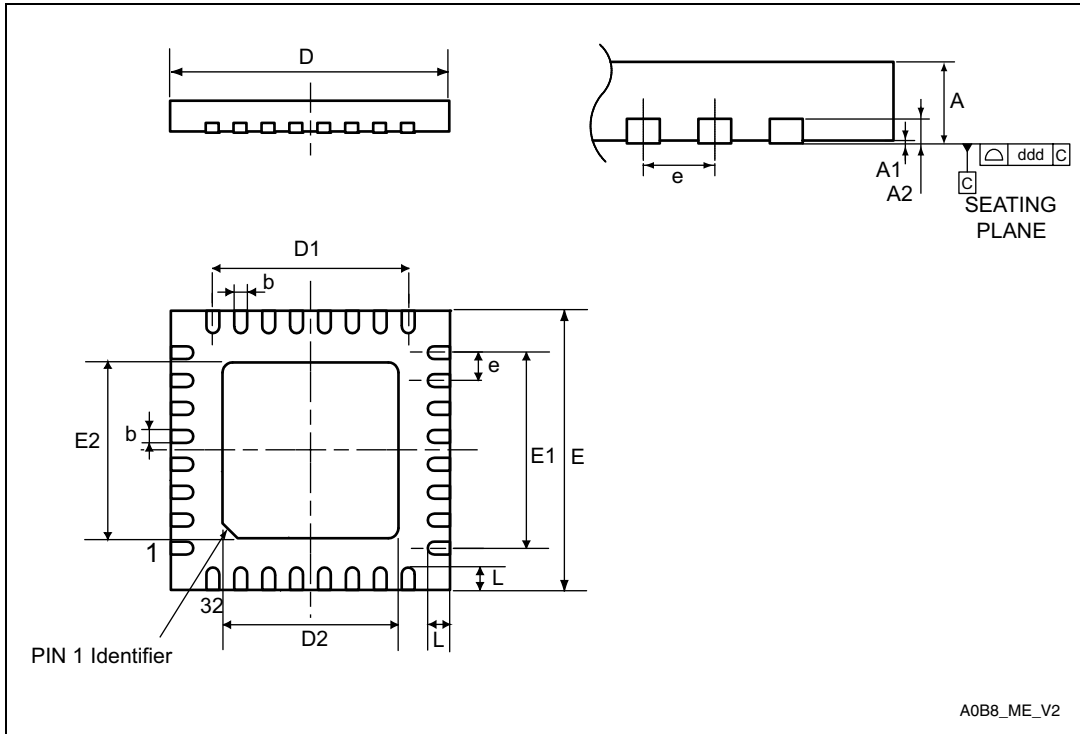
Figure 51. LQFP32 marking example (package top view)



1. Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.

7.7 UFQFPN32 package information

Figure 52. UFQFPN32 - 32-pin, 5x5 mm, 0.5 mm pitch ultra thin fine pitch quad flat package outline

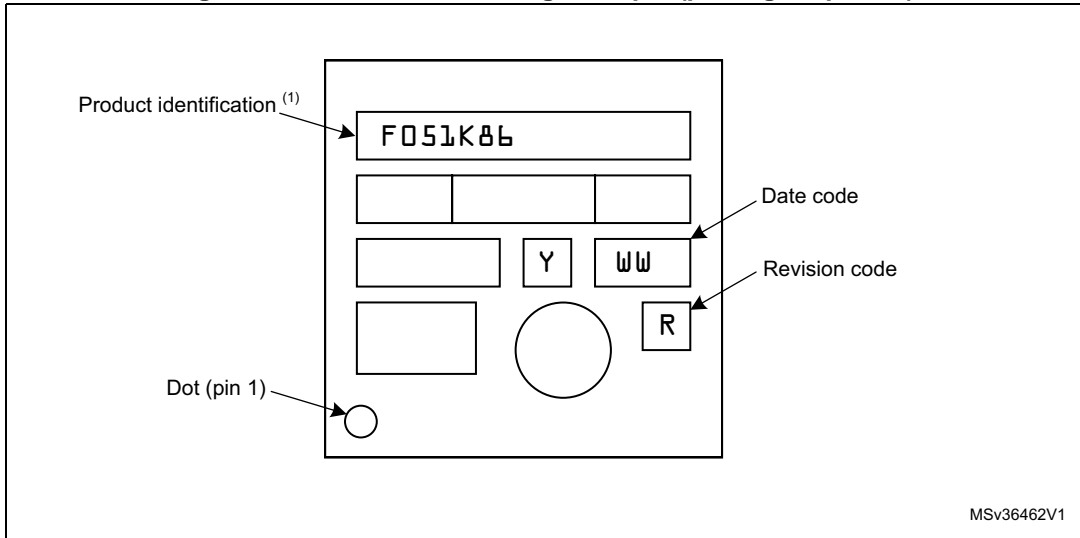


1. Drawing is not to scale.

Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Figure 54. UFQFPN32 marking example (package top view)



1. Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering Samples to run qualification activity.

7.8 Thermal characteristics

The maximum chip junction temperature (T_{Jmax}) must never exceed the values given in [Table 20: General operating conditions](#).

The maximum chip-junction temperature, T_J max, in degrees Celsius, may be calculated using the following equation:

$$T_J \text{ max} = T_A \text{ max} + (P_D \text{ max} \times \Theta_{JA})$$

Where:

- T_A max is the maximum ambient temperature in °C,
- Θ_{JA} is the package junction-to-ambient thermal resistance, in °C/W,
- P_D max is the sum of P_{INT} max and $P_{I/O}$ max (P_D max = P_{INT} max + $P_{I/O}$ max),
- P_{INT} max is the product of I_{DD} and V_{DD} , expressed in Watts. This is the maximum chip internal power.

$P_{I/O}$ max represents the maximum power dissipation on output pins where:

$$P_{I/O} \text{ max} = \sum (V_{OL} \times I_{OL}) + \sum ((V_{DDIOx} - V_{OH}) \times I_{OH}),$$

taking into account the actual V_{OL} / I_{OL} and V_{OH} / I_{OH} of the I/Os at low and high level in the application.

Table 74. Package thermal characteristics

| Symbol | Parameter | Value | Unit |
|---------------|---|-------|------|
| Θ_{JA} | Thermal resistance junction-ambient LQFP64 - 10 × 10 mm / 0.5 mm pitch | 45 | °C/W |
| | Thermal resistance junction-ambient LQFP48 - 7 × 7 mm | 55 | |
| | Thermal resistance junction-ambient LQFP32 - 7 × 7 mm | 56 | |
| | Thermal resistance junction-ambient UFBGA64 - 5 × 5 mm | 65 | |
| | Thermal resistance junction-ambient UFQFPN48 - 7 × 7 mm | 32 | |
| | Thermal resistance junction-ambient UFQFPN32 - 5 × 5 mm | 38 | |
| | Thermal resistance junction-ambient WLCSP36 - 2.6 × 2.7 mm | 60 | |

7.8.1 Reference document

JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air). Available from www.jedec.org

7.8.2 Selecting the product temperature range

When ordering the microcontroller, the temperature range is specified in the ordering information scheme shown in [Section 8: Part numbering](#).

Each temperature range suffix corresponds to a specific guaranteed ambient temperature at maximum dissipation and, to a specific maximum junction temperature.

As applications do not commonly use the STM32F051xx at maximum dissipation, it is useful to calculate the exact power consumption and junction temperature to determine which temperature range will be best suited to the application.

The following examples show how to calculate the temperature range needed for a given application.

Example 1: High-performance application

Assuming the following application conditions:

Maximum ambient temperature $T_{Amax} = 82\text{ °C}$ (measured according to JESD51-2),
 $I_{DDmax} = 50\text{ mA}$, $V_{DD} = 3.5\text{ V}$, maximum 20 I/Os used at the same time in output at low level with $I_{OL} = 8\text{ mA}$, $V_{OL} = 0.4\text{ V}$ and maximum 8 I/Os used at the same time in output at low level with $I_{OL} = 20\text{ mA}$, $V_{OL} = 1.3\text{ V}$

$$P_{INTmax} = 50\text{ mA} \times 3.5\text{ V} = 175\text{ mW}$$

$$P_{IOmax} = 20 \times 8\text{ mA} \times 0.4\text{ V} + 8 \times 20\text{ mA} \times 1.3\text{ V} = 272\text{ mW}$$

This gives: $P_{INTmax} = 175\text{ mW}$ and $P_{IOmax} = 272\text{ mW}$:

$$P_{Dmax} = 175 + 272 = 447\text{ mW}$$

Using the values obtained in [Table 74](#) T_{Jmax} is calculated as follows:

– For LQFP64, 45 °C/W

$$T_{Jmax} = 82\text{ °C} + (45\text{ °C/W} \times 447\text{ mW}) = 82\text{ °C} + 20.115\text{ °C} = 102.115\text{ °C}$$

This is within the range of the suffix 6 version parts ($-40 < T_J < 105\text{ °C}$) see [Table 20: General operating conditions](#).

In this case, parts must be ordered at least with the temperature range suffix 6 (see [Section 8: Part numbering](#)).

Note: With this given P_{Dmax} we can find the T_{Amax} allowed for a given device temperature range (order code suffix 6 or 7).

$$\text{Suffix 6: } T_{Amax} = T_{Jmax} - (45\text{ °C/W} \times 447\text{ mW}) = 105 - 20.115 = 84.885\text{ °C}$$

$$\text{Suffix 7: } T_{Amax} = T_{Jmax} - (45\text{ °C/W} \times 447\text{ mW}) = 125 - 20.115 = 104.885\text{ °C}$$

Example 2: High-temperature application

Using the same rules, it is possible to address applications that run at high ambient temperatures with a low dissipation, as long as junction temperature T_J remains within the specified range.

Assuming the following application conditions:

Maximum ambient temperature $T_{Amax} = 100\text{ °C}$ (measured according to JESD51-2),
 $I_{DDmax} = 20\text{ mA}$, $V_{DD} = 3.5\text{ V}$, maximum 20 I/Os used at the same time in output at low level with $I_{OL} = 8\text{ mA}$, $V_{OL} = 0.4\text{ V}$

$$P_{INTmax} = 20\text{ mA} \times 3.5\text{ V} = 70\text{ mW}$$

$$P_{IOmax} = 20 \times 8\text{ mA} \times 0.4\text{ V} = 64\text{ mW}$$

This gives: $P_{INTmax} = 70\text{ mW}$ and $P_{IOmax} = 64\text{ mW}$:

$$P_{Dmax} = 70 + 64 = 134\text{ mW}$$

Thus: $P_{Dmax} = 134\text{ mW}$

Using the values obtained in [Table 74](#) T_{Jmax} is calculated as follows:

– For LQFP64, 45 °C/W

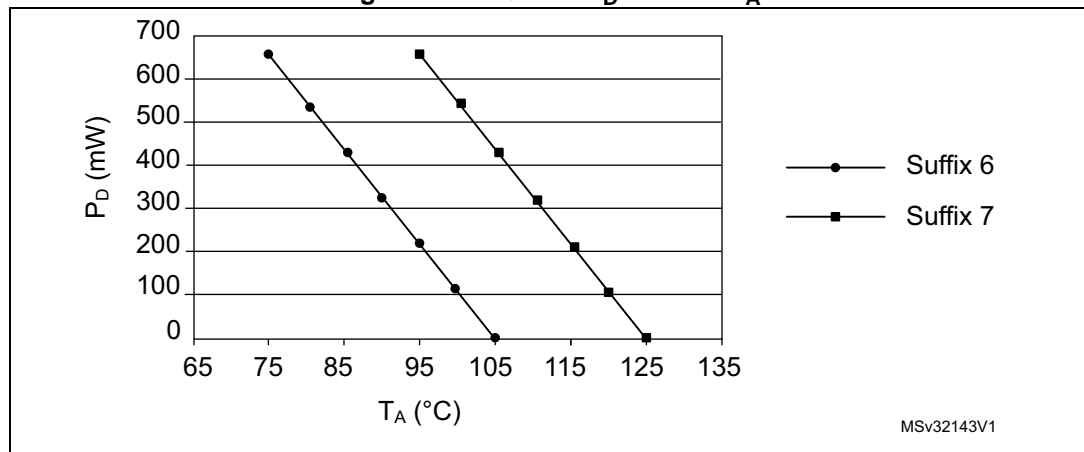
$$T_{Jmax} = 100\text{ °C} + (45\text{ °C/W} \times 134\text{ mW}) = 100\text{ °C} + 6.03\text{ °C} = 106.03\text{ °C}$$

This is above the range of the suffix 6 version parts ($-40 < T_J < 105\text{ °C}$).

In this case, parts must be ordered at least with the temperature range suffix 7 (see [Section 8: Part numbering](#)) unless we reduce the power dissipation in order to be able to use suffix 6 parts.

Refer to [Figure 55](#) to select the required temperature range (suffix 6 or 7) according to your ambient temperature or power requirements.

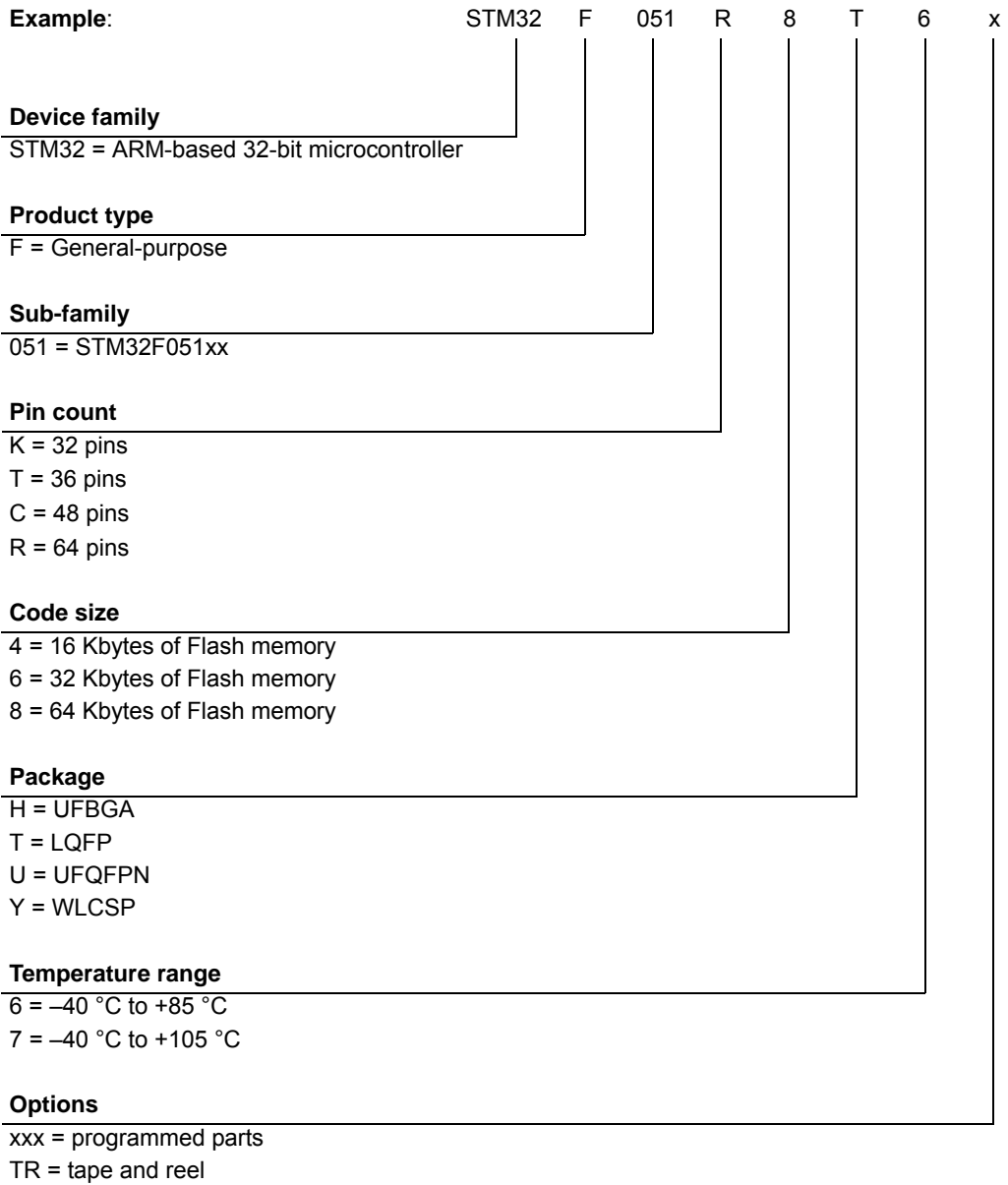
Figure 55. LQFP64 P_D max vs. T_A



8 Part numbering

For a list of available options (memory, package, and so on) or for further information on any aspect of this device, please contact your nearest ST sales office.

Table 75. Ordering information scheme



9 Revision history

Table 76. Document revision history

| Date | Revision | Changes |
|-------------|----------|---|
| 05-Apr-2012 | 1 | Initial release |
| 25-Apr-2012 | 2 | Updated <i>Table: STM32F051xx family device features and peripheral counts</i> for SPI and I2C in 32-pin package. Corrected Group 3 pin order in <i>Table: Capacitive sensing GPIOs available on STM32F051xx devices</i> . Updated the current consumption values in <i>Section: Electrical characteristics</i> . Updated <i>Table: HSI14 oscillator characteristics</i> |
| 23-Jul-2012 | 3 | Features reorganized and <i>Figure: Block diagram</i> structure changed. Added LQFP32 package. Updated <i>Section: Cyclic redundancy check calculation unit (CRC)</i> . Modified the number of priority levels in <i>Section: Nested vectored interrupt controller (NVIC)</i> . Added note 3. for PB2 and PB8, changed TIM2_CH_ETR into TIM2_CH1_ETR in <i>Table: Pin definitions</i> and <i>Table: Alternate functions selected through GPIOA_AFR registers for port A</i> . Added <i>Table: Alternate functions selected through GPIOB_AFR registers for port B</i> . Updated I_{VDD} , I_{VSS} , and $I_{INJ(PIN)}$ in <i>Table: Current characteristics</i> . Updated ACC_{HSI} in <i>Table: HSI oscillator characteristics</i> and <i>Table: HSI14 oscillator characteristics</i> . Updated <i>Table: I/O current injection susceptibility</i> . Added BOOT0 input low and high level voltage in <i>Table: I/O static characteristics</i> . Modified number of pins in V_{OL} and V_{OH} description, and changed condition for V_{OLFM+} in <i>Table: Output voltage characteristics</i> . Changed V_{DD} to V_{DDA} in <i>Figure: Typical connection diagram using the ADC</i> . Updated T_{s_temp} in <i>Table: TS characteristics</i> . Updated <i>Figure: I/O AC characteristics definition</i> . |

Table 76. Document revision history (continued)

| Date | Revision | Changes |
|-------------|----------|--|
| 13-Jan-2014 | 4 | <p>Modified datasheet title.</p> <p>Added packages UFQFPN48 and UFBGA64.</p> <p>Replaced “backup domain with “RTC domain” throughout the document.</p> <p>Changed SRAM value from “4 to 8 Kbyte” to “8 Kbyte”</p> <p>Replaced IWWDG with IWDG in <i>Figure: Block diagram</i>.</p> <p>Added inputs LSI and LSE to the multiplexer in <i>Figure: Clock tree</i>.</p> <p>Added feature “Reference clock detection” in <i>Section: Real-time clock (RTC) and backup registers</i>.</p> <p>Modified junction temperature in <i>Table: Thermal characteristics</i>.</p> <p>Renamed <i>Table: Internal voltage reference calibration values</i>.</p> <p>Replaced V_{DD} with V_{DDA} and V_{RERINT} with ΔV_{REFINT} in <i>Table: Embedded internal reference voltage</i>.</p> <p>Rephrased introduction of <i>Section: Touch sensing controller (TSC)</i>.</p> <p>Rephrased <i>Section: Voltage regulator</i>.</p> <p>Added sentence “If this is used when the voltage regulator is put in low power mode...” under “Stop mode” in <i>Section: Low-power modes</i>.</p> <p>Removed sentence “The internal voltage reference is also connected to ADC_IN17 input channel of the ADC.” in <i>Section: Comparators (COMP)</i>.</p> <p>Removed feature “Periodic wakeup from Stop/Standby” in <i>Section: Real-time clock (RTC) and backup registers</i>.</p> <p>Replaced I_{DD} with I_{DDA} in <i>Table: HSI oscillator characteristics</i>, <i>Table: HSI14 oscillator characteristics</i> and <i>Table: LSI oscillator characteristics</i>.</p> <p>Moved section “Wakeup time from low-power mode” to <i>Section 6.3.6</i> and rephrased the section.</p> <p>Added lines D2 and E2 in <i>Table: UFQFPN48 – 7 x 7 mm, 0.5 mm pitch, package mechanical data</i>.</p> <p>Added “The peripheral clock used is 48 MHz.” in <i>Section On-chip peripheral current consumption</i>.</p> |

Table 76. Document revision history (continued)

| Date | Revision | Changes |
|-------------|------------------|---|
| 13-Jan-2014 | 4 (continued) | <p>Added "Negative induced leakage current is caused by negative injection and positive induced leakage current is caused by positive injection" in <i>Section Functional susceptibility to I/O current injection</i>.</p> <p>Replaced reference "JESD22-C101" with "ANSI/ESD STM5.3.1" in <i>Table : ESD absolute maximum ratings</i>.</p> <p>Merged <i>Table: Typical and maximum VDD consumption in Stop and Standby modes</i> and <i>Table: Typical and maximum VDDA consumption in Stop and Standby modes</i> into <i>Table: Typical and maximum current consumption in Stop and Standby modes</i>.</p> <p>Updated:</p> <ul style="list-style-type: none"> - <i>Table: Temperature sensor calibration values</i>, - <i>Table: Internal voltage reference calibration values</i>, - <i>Table: Current characteristics</i>, - <i>Table: General operating conditions</i>, - <i>Table: Typical and maximum current consumption from the VDDA supply</i>, - <i>Table: Low-power mode wakeup timings</i>, - <i>Table: I/O current injection susceptibility</i>, - <i>Table: I/O static characteristics</i>, - <i>Table: Output voltage characteristics</i>, - <i>Table: NRST pin characteristics</i>, - <i>Table: I2C analog filter characteristics</i>, - <i>Figure: Power supply scheme</i>, - <i>Figure: TC and TTa I/O input characteristics</i>, - <i>Figure: Five volt tolerant (FT and FTf) I/O input characteristics</i>, - <i>Figure: I/O AC characteristics definition</i>, - <i>Figure: ADC accuracy characteristics</i>, - <i>Figure: Typical connection diagram using the ADC</i>, - <i>Figure: LQFP64 – 10 x 10 mm 64 pin low-profile quad flat package outline</i>, - <i>Figure: LQFP64 recommended footprint</i>, - <i>Figure: LQFP48 – 7 x 7 mm, 48 pin low-profile quad flat package outline</i>, - <i>Figure: LQFP48 recommended footprint</i>, - <i>Figure: LQFP32 – 7 x 7 mm 32-pin low-profile quad flat package outline</i>, - <i>Figure: LQFP32 recommended footprint</i>, - <i>Figure: UFQFPN48 – 7 x 7 mm, 0.5 mm pitch, package outline</i>. |

Table 76. Document revision history (continued)

| Date | Revision | Changes |
|-------------|----------|---|
| 28-Aug-2015 | 5 | <p>Updated the following:</p> <ul style="list-style-type: none"> – DAC and power management feature descriptions in <i>Features</i>, – <i>Table 2: STM32F051xx family device features and peripheral count</i>, – <i>Section 3.5.1: Power supply schemes</i>, – <i>Figure 13: Power supply scheme</i>, – <i>Table 17: Voltage characteristics</i>, – <i>Table 20: General operating conditions</i>: updated the footnote for V_{IN} parameter, – <i>Table 28: Typical and maximum current consumption from the VBAT supply</i>, – <i>Table 33: High-speed external user clock characteristics</i>: replaced V_{DD} with V_{DDIOX}, – <i>Table 34: Low-speed external user clock characteristics</i>: replaced V_{DD} with V_{DDIOX}, – <i>Table 37: HSI oscillator characteristics</i> and <i>Figure 19: HSI oscillator accuracy characterization results for soldered parts</i>, – <i>Table 38: HSI14 oscillator characteristics</i>: changed the min value for ACC_{HSI14}, – <i>Table 41: Flash memory characteristics</i>: changed the values for t_{ME} and I_{DD} in write mode, – <i>Table 43: EMS characteristics</i>: changed the value of V_{EFTB}. |

Table 76. Document revision history (continued)

| Date | Revision | Changes |
|-------------|---------------|---|
| 28-Aug-2015 | 5 (Continued) | <p>Updated the following:</p> <ul style="list-style-type: none"> – Figure 10: STM32F051xx memory map, – Figure 21: TC and TTa I/O input characteristics, – Figure 22: Five volt tolerant (FT and FTf) I/O input characteristics, – Figure 23: I/O AC characteristics definition, – t_{START} definition in Table 24: Embedded internal reference voltage, – t_{STAB} characteristics in Table 52: ADC characteristics, – Table 56: Comparator characteristics: changed the description and values for V_{SC}, V_{DDA} and V_{REFINT} parameters. Added Figure 28: Maximum VREFINT scaler startup time from power down, – Table 57: TS characteristics: changed the min value for T_{S-temp}, – Table 58: VBAT monitoring characteristics: changed the min value for T_{S-vbat} and the typical value for R parameters, – Section 6.3.22: Communication interfaces: updated the description and features in the subsection I2C interface characteristics, – Table 64: I2S characteristics: updated the min values for data input hold time (master and slave receiver). – Table 31: Peripheral current consumption, <p>Addition of WLCSP36 package. Updates in:</p> <ul style="list-style-type: none"> – Section 2: Description, – Table 2: STM32F051xx family device features and peripheral count, – Section 4: Pinouts and pin descriptions with the addition of Figure 7: WLCSP36 36-pin package ball-out, – Table 13: Pin definitions, – Table 20: General operating conditions, – Section 7: Package information with the addition of Section 7.5: WLCSP36 package information, – Table 74: Package thermal characteristics, – Section 8: Part numbering. <p>Update of the device marking examples in Section 7: Package information.</p> |

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