PIC16(L)F1454/1455/1459

PIC16(L)F1454/1455/1459 Family
Silicon Errata and Data Sheet Clarification

The PIC16(L)F1454/1455/1459 family devices that you have received conform functionally to the current Device Data Sheet (DS41639**A**), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in Table 1. The silicon issues are summarized in Table 2.

The errata described in this document will be addressed in future revisions of the PIC16(L)F1454/1455/1459 silicon.

Note:	This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated in the last column of Table 2 apply to the current silicon revision (**A6**).

Data Sheet clarifications and corrections start on page 4, following the discussion of silicon issues.

The silicon revision level can be identified using the current version of MPLAB® IDE and Microchip's programmers, debuggers, and emulation tools, which are available at the Microchip corporate web site (www.microchip.com).

For example, to identify the silicon revision level using MPLAB IDE in conjunction with a hardware debugger:

1. Using the appropriate interface, connect the device to the hardware debugger.
2. Open an MPLAB IDE project.
3. Configure the MPLAB IDE project for the appropriate device and hardware debugger.
4. Based on the version of MPLAB IDE you are using, do one of the following:
   a) For MPLAB IDE 8, select *Programmer > Reconnect*.
   b) For MPLAB X IDE, select *Window > Dashboard* and click the **Refresh Debug Tool Status** icon ( ).
5. Depending on the development tool used, the part number *and* Device Revision ID value appear in the **Output** window.

Note:	If you are unable to extract the silicon revision level, please contact your local Microchip sales office for assistance.

The DEVREV values for the various PIC16(L)F1454/1455/1459 silicon revisions are shown in Table 1.

TABLE 1: SILICON DEVREV VALUES

Part Number	Device ID(1)	Silicon Revision ID(2)		
		A2	A5	A6
PIC16F1454	3020h	—	1005h	1006h
PIC16LF1454	3024h	—	1005h	1006h
PIC16F1455	3021h	1003h	1005h	1006h
PIC16LF1455	3025h	1003h	1005h	1006h
PIC16F1459	3023h	1003h	1005h	1006h
PIC16LF1459	3027h	1003h	1005h	1006h

Note 1: The Device ID is located in the configuration memory at address 8006h.

2: Refer to the *"PIC16(L)F145X Memory Programming Specification"* (DS41620) for detailed information on Device and Revision IDs for your specific device.

TABLE 2: SILICON ISSUE SUMMARY

Module	Feature	Item Number	Issue Summary	Affected Revisions(1)		
				A2	A5	A6
Oscillator	HFINTOSC Ready/Stable bit	1.1	Bits remained set to '1' after initial trigger.	X		
Oscillator	Oscillator Start-up Timer (OST) bit	1.2	OST bit remains set.	X	X	
Fixed Voltage Reference (FVR)	Gain Amplifier Output	2.1	Use of FVR module can cause device Reset.	X		
Program Flash Memory (PFM)	PFM Self-Write	3.1	PFM self-write will not work depending on clock selection.	X		
CPU	BRA/BRW	4.1	An interrupt during the execution of a BRA or BRW instruction can return an incorrect PC value.	X	X	

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

Silicon Errata Issues

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated by the shaded column in the following tables apply to the current silicon revision (**A6**).

1. Module: Oscillator

1.1 OSCSTAT bits: HFIOFR and HFIOFS

When HFINTOSC is selected, the HFIOFR and HFIOFS bits will become set when the oscillator becomes ready and stable. Once these bits are set they become “stuck”, indicating that HFINTOSC is always ready and stable. If the HFINTOSC is disabled, the bits fail to be cleared.

Work around

None.

Affected Silicon Revisions

A2	A5	A6					
X							

1.2 Oscillator Start-up Timer (OST) bit

During the Two-Speed Start-up sequence, the OST is enabled to count 1024 clock cycles. After the count is reached, the OSTS bit is set, and the system clock is held low until the next falling edge of the external crystal (LP, XT or HS mode), before switching to the external clock source.

When an external oscillator is configured as primary clock and Fail-Safe Clock mode is enabled (FCMEN = 1), any of the following conditions will result in the Oscillator Start-up Timer (OST) failing to restart:

- $\overline{\text{MCLR}}$ Reset
- Wake from Sleep
- Clock change from INTOSC to Primary Clock

This anomaly will manifest itself as a clock failure condition for external oscillators which take longer than the clock failure time-out period to start.

Work around

None.

Affected Silicon Revisionss

A2	A5	A6					
X	X						

2. Module: Fixed Voltage Reference (FVR)

2.1 Gain Amplifier Output

When using the FVR module, if the gain amplifier outputs are set via the CDAFVR or ADFVR bits in FVRCON while the module is disabled (FVREN = 0), the internal oscillator frequency may shift, the device current consumption can increase, and a Brown-out Reset may occur.

Work around

Set the FVREN bit of FVRCON to enable the module prior to adjusting the amplifier output selections with the CDAFVR and ADFVR bits. If switching from the 4x output setting to the 1x output setting, select the 2x output setting as an intermediary step. Always set the amplifier output selections to off (’00’) before disabling the FVR module.

Affected Silicon Revisions

A2	A5	A6					
X							

3. Module: Program Flash Memory (PFM)

3.1 PFM Self Write

Writes to the PFM will not execute if the device’s clock source is HS or ECH, or if the internal oscillator is at either 8 MHz or 16 MHz. The DFM is unaffected.

Work around

To write to the PFM, the clock source must have one of the following settings: internal oscillator set to 4 MHz or lower, ECM, ECL, XT, External RC, LP or T1OSC.

Affected Silicon Revisions

A2	A5	A6					
X							

4. Module: CPU

4.1 BRA/BRW

If a BRA or BRW instruction is executed concurrently with an interrupt event, the ISR routine can restore the PC to an incorrect value.

Work around

Use the GOTO instruction rather than the BRA or BRW instruction.

Affected Silicon Revisions

A2	A5	A6					
X	X						

Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS41639**A**):

Note:	Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

1. Module: Electrical Specifications

29.9 AC Characteristics

Removed “No missing codes” from AD03 Conditions column, and modified Note 2. Under very rare circumstances, a single code can be missed.

TABLE 29-6: PIC16(L)F1454/1455/1459 A/D CONVERTER (ADC) CHARACTERISTICS

Standard Operating Conditions (unless otherwise stated) Operating temperature Tested at 25°C							
Param No.	**Sym.**	**Characteristic**	**Min.**	**Typ†**	**Max.**	**Units**	**Conditions**
AD01	NR	Resolution	—	—	10	bit	
AD02	EIL	Integral Error	—	—	±1.7	LSb	VREF = 3.0V
AD03	EDL	Differential Error	—	—	±1	LSb	VREF = 3.0V
AD04	EOFF	Offset Error	—	—	±2.5	LSb	VREF = 3.0V
AD05	EGN	Gain Error	—	—	±2.0	LSb	VREF = 3.0V
AD06	VREF	Reference Voltage**(3)**	1.8	—	VDD	V	VREF = (VREF+ minus VREF-)
AD07	VAIN	Full-Scale Range	VSS	—	VREF	V	
AD08	ZAIN	Recommended Impedance of Analog Voltage Source	—	—	10	kΩ	Can go higher if external 0.01µF capacitor is present on input pin.

* These parameters are characterized but not tested.

† Data in “Typ” column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Total Absolute Error includes integral, differential, offset and gain errors.

2: **The A/D conversion result never decreases with an increase in the input voltage.**

3: ADC VREF is from external VREF+ pin, VDD pin, whichever is selected as reference input.

4: When ADC is off, it will not consume any current other than leakage current. The power-down current specification includes any such leakage from the ADC module.

APPENDIX A: DOCUMENT REVISION HISTORY

Rev A Document (08/2012)

Initial release of this document.

Rev B Document (08/2012)

Corrected Device ID and Silicon Revision ID in Table 1.
Removed incorrect errata module.

Rev C Document (12/2012)

Added PIC16(L)F1454 devices; Added Silicon Revision A5; Updated Table 1 and Table 2.

Rev D Document (5/2013)

Added Module 4, CPU.

Rev E Document (10/2013)

Added Silicon Revision A6; Other minor corrections.

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
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- Microchip is willing to work with the customer who is concerned about the integrity of their code.
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