ON Semiconductor®

Product Bulletin

Document #:PB23478X
Issue Date:03 Aug 2020

Title of Change:	Datasheet Update for CAT24C128HU4IGT3,CAT24C128WI-GT3,and CAT24C128YI-GT3
Effective date:	03 Aug 2020
Contact information:	Contact your local ON Semiconductor Sales Office or Wirasa.Nontharith@onsemi.com
Type of notification:	This Product Bulletin is for notification purposes only. ON Semiconductor will proceed with implementation of this change upon publication of this Product Bulletin.
Change Category:	Documentation Change
Change Sub-Category(s):	Datasheet/Product Doc change

Sites Affected:

ON Semiconductor Sites	**External Foundry/Subcon Sites**
None	None

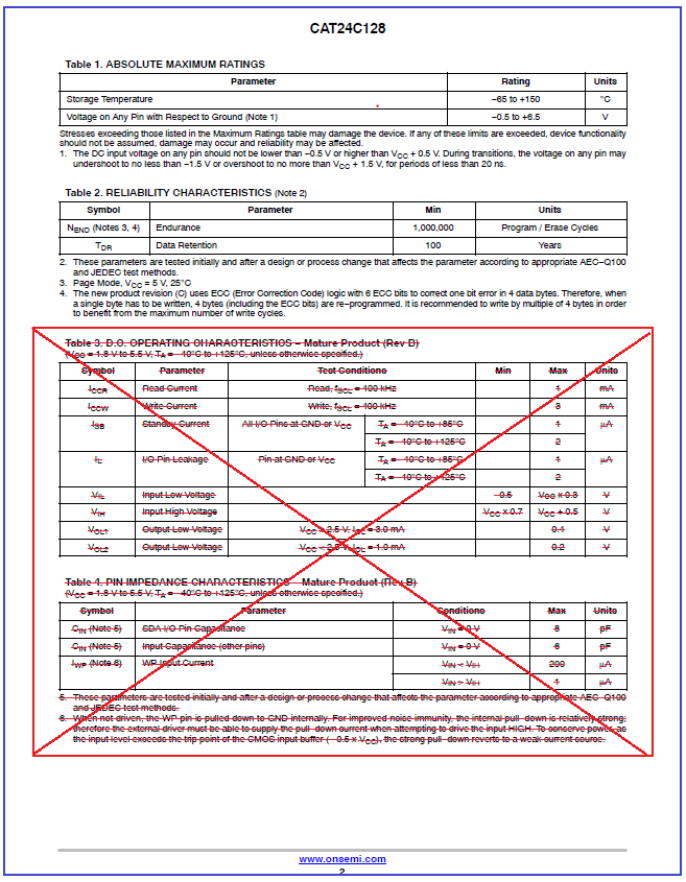
Description and Purpose:

CAT24C128HU4IGT3, CAT24C128WI-GT3, and CAT24C128YI-GT3 Datasheet was updated to remove information of old product revision rev.B (OKI die) as all OPNs now use Gresham die.

There are 2 minor corrections done in the datasheet to avoid confusions. Changes on Page 2, 3 and 10.
The change will not impact form, fit, or function of products.

CAT24C128 Datasheet Changes

1. Removing table 3, 4 and note # 5, 6, 7 on page#2-3.



CAT24C128

Table 1. ABSOLUTE MAXIMUM RATINGS

Parameter	Rating	Units
Storage Temperature	−65 to +150	°C
Voltage on Any Pin with Respect to Ground (Note 1)	−0.5 to +8.5	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
1. The DC input voltage on any pin should not be lower than −0.5 V or higher than V_{CC} + 0.5 V. During transitions, the voltage on any pin may undershoot to no less than −1.5 V or overshoot to no more than V_{CC} + 1.5 V, for periods of less than 20 ns.

Table 2. RELIABILITY CHARACTERISTICS (Note 2)

Symbol	Parameter	Min	Units
N_{END} (Notes 3, 4)	Endurance	1,000,000	Program / Erase Cycles
T_{DR}	Data Retention	100	Years

2. These parameters are tested initially and after a design or process change that affects the parameter according to appropriate AEC−Q100 and JEDEC test methods.
3. Page Mode, V_{CC} = 5 V, 25°C
4. The new product revision (C) uses ECC (Error Correction Code) logic with 8 ECC bits to correct one bit error in 4 data bytes. Therefore, when a single byte has to be written, 4 bytes (including the ECC bits) are re−programmed. It is recommended to write by multiple of 4 bytes in order to benefit from the maximum number of write cycles.

~~Table 3. D.C. OPERATING CHARACTERISTICS – Mature Product (Rev B)~~
~~(V_{CC} = 1.8 V to 5.5 V, T_A = −40°C to +125°C, unless otherwise specified.)~~

~~Symbol~~	~~Parameter~~	~~Test Conditions~~		~~Min~~	~~Max~~	~~Units~~
~~I_{CCR}~~	~~Read Current~~	~~Read, f_{SCL} = 100 kHz~~			~~1~~	~~mA~~
~~I_{CCW}~~	~~Write Current~~	~~Write, f_{SCL} = 100 kHz~~			~~3~~	~~mA~~
~~I_{SB}~~	~~Standby Current~~	~~All I/O Pins at GND or V_{CC}~~	~~T_A = −40°C to +85°C~~		~~1~~	~~μA~~
			~~T_A = −40°C to +125°C~~		~~2~~	
~~I_L~~	~~I/O Pin Leakage~~	~~Pin at GND or V_{CC}~~	~~T_A = −40°C to +85°C~~		~~1~~	~~μA~~
			~~T_A = −40°C to +125°C~~		~~2~~	
~~V_{IL}~~	~~Input Low Voltage~~			~~−0.5~~	~~V_{CC} x 0.3~~	~~V~~
~~V_{IH}~~	~~Input High Voltage~~			~~V_{CC} x 0.7~~	~~V_{CC} + 0.5~~	~~V~~
~~V_{OL1}~~	~~Output Low Voltage~~	~~V_{CC} ≥ 2.5 V, I_{OL} = 3.0 mA~~			~~0.4~~	~~V~~
~~V_{OL2}~~	~~Output Low Voltage~~	~~V_{CC} < 2.5 V, I_{OL} = 1.0 mA~~			~~0.2~~	~~V~~

~~Table 4. PIN IMPEDANCE CHARACTERISTICS – Mature Product (Rev B)~~
~~(V_{CC} = 1.8 V to 5.5 V, T_A = −40°C to +125°C, unless otherwise specified.)~~

~~Symbol~~	~~Parameter~~	~~Conditions~~	~~Max~~	~~Units~~
~~C_{IN} (Note 5)~~	~~SDA I/O Pin Capacitance~~	~~V_{IN} = 0 V~~	~~8~~	~~pF~~
~~C_{IN} (Note 5)~~	~~Input Capacitance (other pins)~~	~~V_{IN} = 0 V~~	~~6~~	~~pF~~
~~I_{WP}, I_A (Note 6)~~	~~WP Input Current~~	~~V_{IN} < V_{IH}~~	~~200~~	~~μA~~
		~~V_{IN} > V_{IH}~~	~~1~~	~~μA~~

~~5. These parameters are tested initially and after a design or process change that affects the parameter according to appropriate AEC−Q100 and JEDEC test methods.~~
~~6. When not driven, the WP pin is pulled down to GND internally. For improved noise immunity, the internal pull−down is relatively strong; therefore the external driver must be able to supply the pull−down current when attempting to drive the input HIGH. To conserve power, as the input level exceeds the trip point of the CMOS input buffer (~ 0.5 x V_{CC}), the strong pull−down reverts to a weak current source.~~

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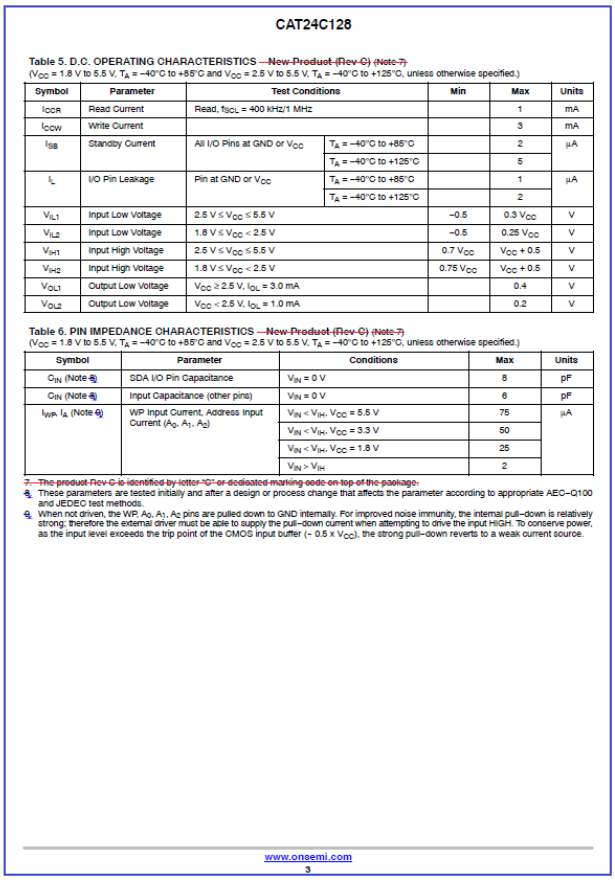

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Table 5. D.C. OPERATING CHARACTERISTICS ~~– New Product (Rev C) (Note 7)~~
(V_{CC} = 1.8 V to 5.5 V, T_A = −40°C to +85°C and V_{CC} = 2.5 V to 5.5 V, T_A = −40°C to +125°C, unless otherwise specified.)

Symbol	Parameter	Test Conditions		Min	Max	Units
I_{CCR}	Read Current	Read, f_{SCL} = 400 kHz/1 MHz			1	mA
I_{CCW}	Write Current				3	mA
I_{SB}	Standby Current	All I/O Pins at GND or V_{CC}	T_A = −40°C to +85°C		2	μA
			T_A = −40°C to +125°C		5	
I_L	I/O Pin Leakage	Pin at GND or V_{CC}	T_A = −40°C to +85°C		1	μA
			T_A = −40°C to +125°C		2	
V_{IL1}	Input Low Voltage	2.5 V ≤ V_{CC} ≤ 5.5 V		−0.5	0.3 V_{CC}	V
V_{IL2}	Input Low Voltage	1.8 V ≤ V_{CC} < 2.5 V		−0.5	0.25 V_{CC}	V
V_{IH1}	Input High Voltage	2.5 V ≤ V_{CC} ≤ 5.5 V		0.7 V_{CC}	V_{CC} + 0.5	V
V_{IH2}	Input High Voltage	1.8 V ≤ V_{CC} < 2.5 V		0.75 V_{CC}	V_{CC} + 0.5	V
V_{OL1}	Output Low Voltage	V_{CC} ≥ 2.5 V, I_{OL} = 3.0 mA			0.4	V
V_{OL2}	Output Low Voltage	V_{CC} < 2.5 V, I_{OL} = 1.0 mA			0.2	V

Table 6. PIN IMPEDANCE CHARACTERISTICS ~~– New Product (Rev C) (Note 7)~~
(V_{CC} = 1.8 V to 5.5 V, T_A = −40°C to +85°C and V_{CC} = 2.5 V to 5.5 V, T_A = −40°C to +125°C, unless otherwise specified.)

Symbol	Parameter	Conditions	Max	Units
C_{IN} (Note ~~5~~ 8)	SDA I/O Pin Capacitance	V_{IN} = 0 V	8	pF
C_{IN} (Note ~~5~~ 8)	Input Capacitance (other pins)	V_{IN} = 0 V	6	pF
I_{WP}, I_A (Note ~~6~~ 9)	WP Input Current, Address Input Current (A_0, A_1, A_2)	V_{IN} < V_{IH}, V_{CC} = 5.5 V	75	μA
		V_{IN} < V_{IH}, V_{CC} = 3.3 V	50	
		V_{IN} < V_{IH}, V_{CC} = 1.8 V	25	
		V_{IN} > V_{IH}	2	

~~7. The product Rev C is identified by letter "C" or dedicated marking code on top of the package.~~
8. These parameters are tested initially and after a design or process change that affects the parameter according to appropriate AEC−Q100 and JEDEC test methods.
9. When not driven, the WP, A_0, A_1, A_2 pins are pulled down to GND internally. For improved noise immunity, the internal pull−down is relatively strong; therefore the external driver must be able to supply the pull−down current when attempting to drive the input HIGH. To conserve power, as the input level exceeds the trip point of the CMOS input buffer (~ 0.5 x V_{CC}), the strong pull−down reverts to a weak current source.

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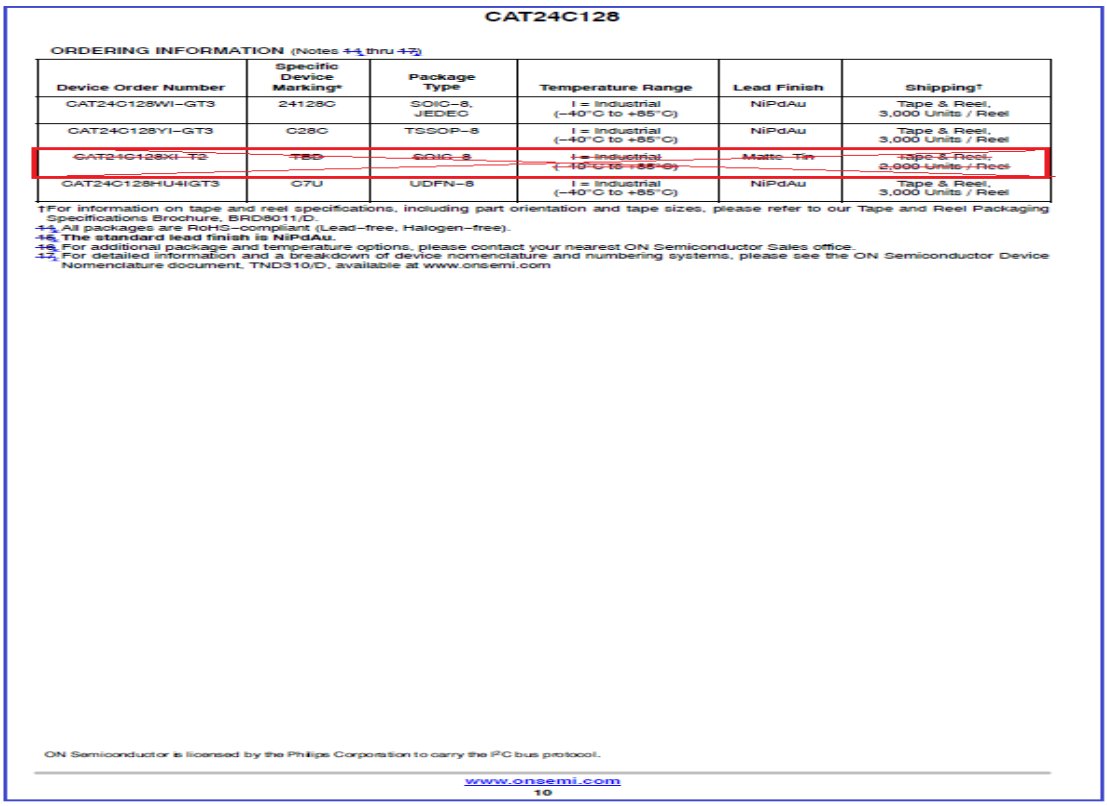
2. Removing CAT24C128XI-T2 from ordering information table on page#10 as this part is already obsoleted.



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ORDERING INFORMATION (Notes ~~14~~ thru ~~17~~)

Device Order Number	Specific Device Marking*	Package Type	Temperature Range	Lead Finish	Shipping†
CAT24C128WI−GT3	24128C	SOIC−8, JEDEC	I = Industrial (−40°C to +85°C)	NiPdAu	Tape & Reel, 3,000 Units / Reel
CAT24C128YI−GT3	C28C	TSSOP−8	I = Industrial (−40°C to +85°C)	NiPdAu	Tape & Reel, 3,000 Units / Reel
~~CAT24C128XI−T2~~	~~TBD~~	~~SOIC−8~~	~~I = Industrial (−40°C to +85°C)~~	~~Matte−Tin~~	~~Tape & Reel, 2,000 Units / Reel~~
CAT24C128HU4IGT3	C7U	UDFN−8	I = Industrial (−40°C to +85°C)	NiPdAu	Tape & Reel, 3,000 Units / Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
~~14.~~ All packages are RoHS−compliant (Lead−free, Halogen−free).
~~15.~~ **The standard lead finish is NiPdAu.**
~~16.~~ For additional package and temperature options, please contact your nearest ON Semiconductor Sales office.
~~17.~~ For detailed information and a breakdown of device nomenclature and numbering systems, please see the ON Semiconductor Device Nomenclature document, TND310/D, available at www.onsemi.com

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List of Affected Standard Parts:

***Note**: Only the standard (off the shelf) part numbers are listed in the parts list. Any custom parts affected by this PCN are shown in the customer specific PCN addendum in the PCN email notification, or on the **PCN Customized Portal**.*

CAT24C128HU4IGT3	CAT24C128WI-GT3	CAT24C128YI-GT3

Japanese translation of the notification starts here.

通知の日本語訳はここから始まります。

Note*: The Japanese version is for reference only. In case of any differences between the English and Japanese version, the English version shall control.*

注：日本語版は参照用です。英語版と日本語版の違いがある場合は、英語版が優先されます.

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製品速報

文書番号:PB23478X
発行日 03 Aug 2020

PPP 変更件名:	CAT24C128HU4IGT3、CAT24C128WI-GT3、CAT24C128YI-GT3 のデータシート更新
発効日:	03 Aug 2020
連絡先情報:	現地のオン・セミコンダクター営業所または < Wirasa.Nontharith@onsemi.com > にお問い合わせください。
通知種別:	本製品速報は通知目的のみのものです。オン・セミコンダクターは本製品速報の発行により本変更を実行します。
変更カテゴリ:	文書の変更
変更サブカテゴリ:	データシート/製品文書の変更
影響を受ける拠点:	

オン・セミコンダクター拠点:	**外部製造工場 / 下請業者拠点:**
なし	なし

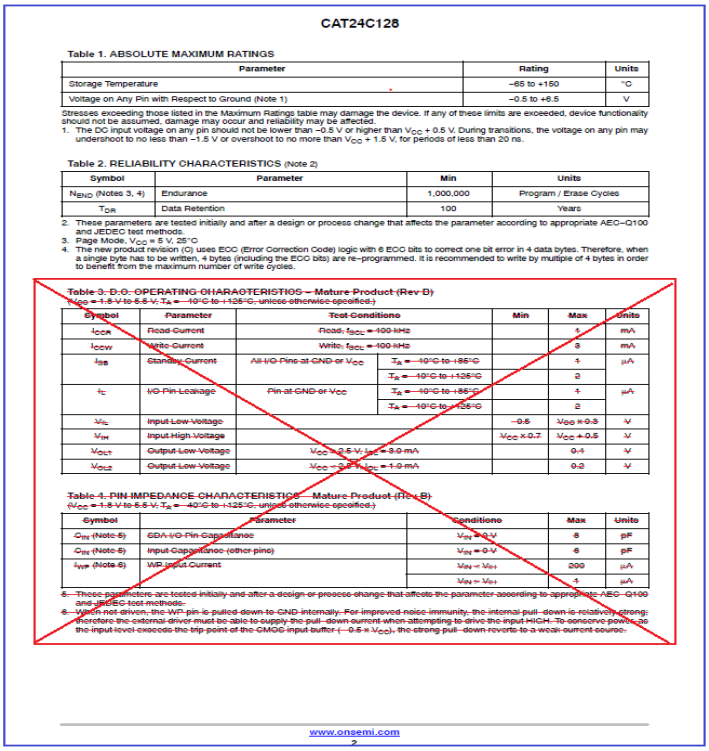
説明および目的:

CAT24C128HU4IGT3、CAT24C128WI-GT3、CAT24C128YI-GT3 のデータシートは、現在すべての製品はグレシャムのダイを使用しているので、旧製品改訂版 rev.B (OKI ダイ) の情報を削除するために更新されました。

混乱を避けるためにデータシート内で 2 つのマイナーな修正があります。ページ 2、3、10 に変更があります。
この変更は製品の形状、適合性、または機能に影響を及ぼしません。

CAT24C128 のデータシートの変更

1. ページ 2 ～ 3 の表 3、4 および注 5、6、7 を削除します。



CAT24C128

Table 1. ABSOLUTE MAXIMUM RATINGS

Parameter	Rating	Units
Storage Temperature	−65 to +150	°C
Voltage on Any Pin with Respect to Ground (Note 1)	−0.5 to +6.5	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
1. The DC input voltage on any pin should not be lower than −0.5 V or higher than V_{CC} + 0.5 V. During transitions, the voltage on any pin may undershoot to no less than −1.5 V or overshoot to no more than V_{CC} + 1.5 V, for periods of less than 20 ns.

Table 2. RELIABILITY CHARACTERISTICS (Note 2)

Symbol	Parameter	Min	Units
N_{END} (Notes 3, 4)	Endurance	1,000,000	Program / Erase Cycles
T_{DR}	Data Retention	100	Years

2. These parameters are tested initially and after a design or process change that affects the parameter according to appropriate AEC−Q100 and JEDEC test methods.
3. Page Mode, V_{CC} = 5 V, 25°C
4. The new product revision (C) uses ECC (Error Correction Code) logic with 8 ECC bits to correct one bit error in 4 data bytes. Therefore, when a single byte has to be written, 4 bytes (including the ECC bits) are re−programmed. It is recommended to write by multiple of 4 bytes in order to benefit from the maximum number of write cycles.

~~Table 3. D.C. OPERATING CHARACTERISTICS − Mature Product (Rev B)~~
~~(V_{CC} = 1.8 V to 5.5 V, T_A = −40°C to +125°C, unless otherwise specified.)~~

Symbol	Parameter	Test Conditions		Min	Max	Units
I_{CCR}	Read Current	Read, f_{SCL} = 400 kHz			1	mA
I_{CCW}	Write Current	Write, f_{SCL} = 400 kHz			3	mA
I_{SB}	Standby Current	All I/O Pins at GND or V_{CC}	T_A = −40°C to +85°C		1	μA
			T_A = −40°C to +125°C		2	
I_L	I/O Pin Leakage	Pin at GND or V_{CC}	T_A = −40°C to +85°C		1	μA
			T_A = −40°C to +125°C		2	
V_{IL}	Input Low Voltage			−0.5	V_{CC} x 0.3	V
V_{IH}	Input High Voltage			V_{CC} x 0.7	V_{CC} + 0.5	V
V_{OL1}	Output Low Voltage	V_{CC} ≥ 2.5 V, I_{OL} = 3.0 mA			0.4	V
V_{OL2}	Output Low Voltage	V_{CC} < 2.5 V, I_{OL} = 1.0 mA			0.2	V

~~Table 4. PIN IMPEDANCE CHARACTERISTICS − Mature Product (Rev B)~~
~~(V_{CC} = 1.8 V to 5.5 V, T_A = −40°C to +125°C, unless otherwise specified.)~~

Symbol	Parameter	Conditions	Max	Units
C_{IN} (Note 5)	SDA I/O Pin Capacitance	V_{IN} = 0 V	8	pF
C_{IN} (Note 5)	Input Capacitance (other pins)	V_{IN} = 0 V	6	pF
I_{WP} (Note 6)	WP Input Current	V_{IN} < V_{IH}	200	μA
		V_{IN} > V_{IH}	1	μA

5. These parameters are tested initially and after a design or process change that affects the parameter according to appropriate AEC−Q100 and JEDEC test methods.
6. When not driven, the WP pin is pulled down to GND internally. For improved noise immunity, the internal pull−down is relatively strong; therefore the external driver must be able to supply the pull−down current when attempting to drive the input HIGH. To conserve power, as the input level exceeds the trip point of the CMOS input buffer (~ 0.5 x V_{CC}), the strong pull−down reverts to a weak current source.

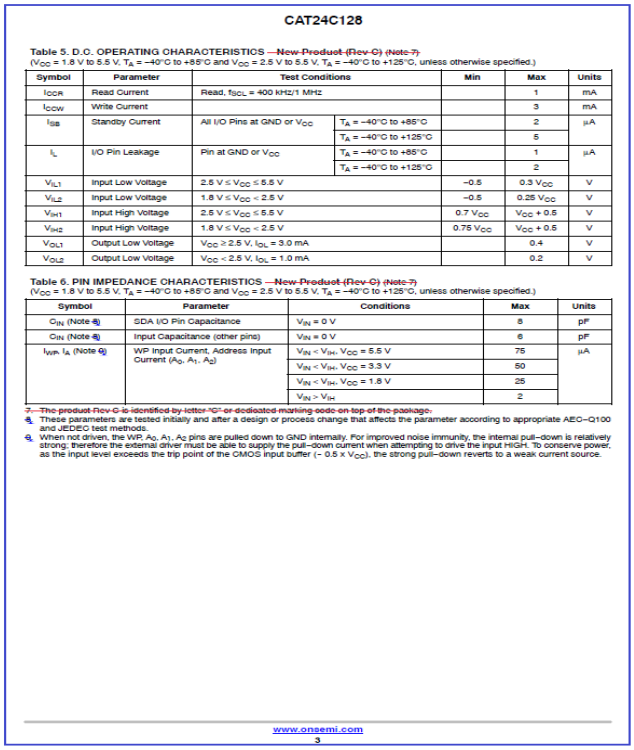


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Table 5. D.C. OPERATING CHARACTERISTICS ~~− New Product (Rev C) (Note 7)~~
(V_{CC} = 1.8 V to 5.5 V, T_A = −40°C to +85°C and V_{CC} = 2.5 V to 5.5 V, T_A = −40°C to +125°C, unless otherwise specified.)

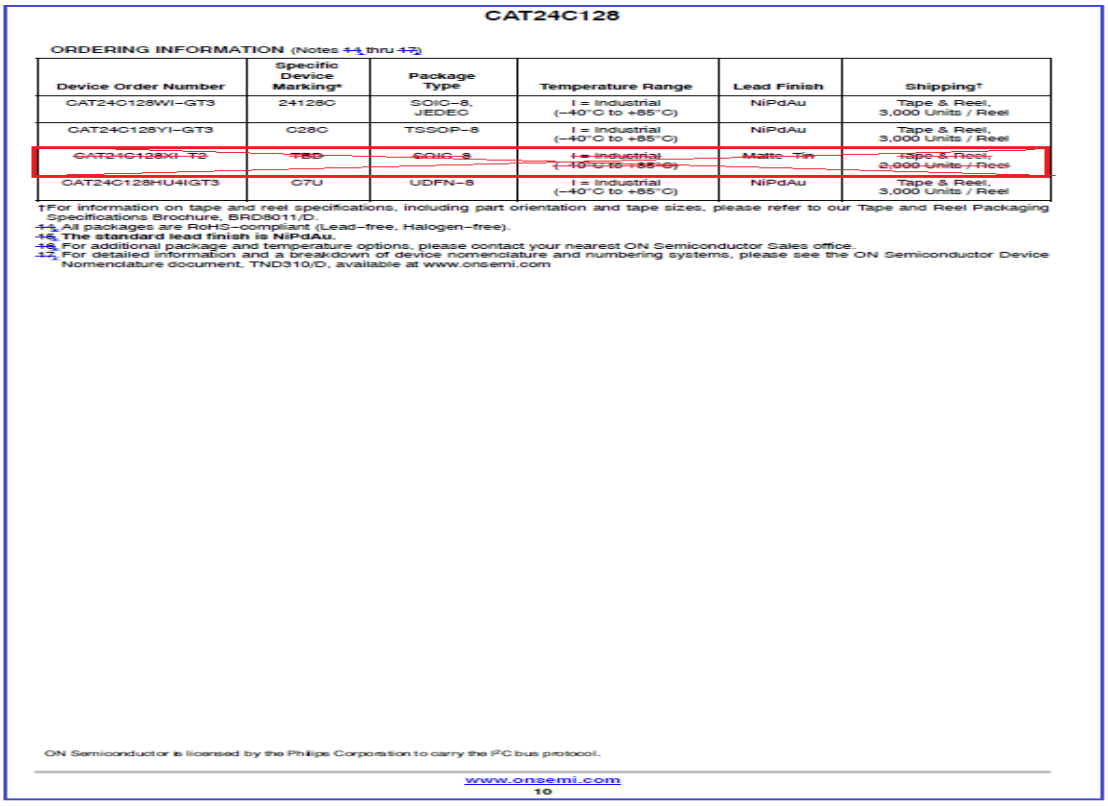
Symbol	Parameter	Test Conditions		Min	Max	Units
I_{CCR}	Read Current	Read, f_{SCL} = 400 kHz/1 MHz			1	mA
I_{CCW}	Write Current				3	mA
I_{SB}	Standby Current	All I/O Pins at GND or V_{CC}	T_A = −40°C to +85°C		2	μA
			T_A = −40°C to +125°C		5	
I_L	I/O Pin Leakage	Pin at GND or V_{CC}	T_A = −40°C to +85°C		1	μA
			T_A = −40°C to +125°C		2	
V_{IL1}	Input Low Voltage	2.5 V ≤ V_{CC} ≤ 5.5 V		−0.5	0.3 V_{CC}	V
V_{IL2}	Input Low Voltage	1.8 V ≤ V_{CC} < 2.5 V		−0.5	0.25 V_{CC}	V
V_{IH1}	Input High Voltage	2.5 V ≤ V_{CC} ≤ 5.5 V		0.7 V_{CC}	V_{CC} + 0.5	V
V_{IH2}	Input High Voltage	1.8 V ≤ V_{CC} < 2.5 V		0.75 V_{CC}	V_{CC} + 0.5	V
V_{OL1}	Output Low Voltage	V_{CC} ≥ 2.5 V, I_{OL} = 3.0 mA			0.4	V
V_{OL2}	Output Low Voltage	V_{CC} < 2.5 V, I_{OL} = 1.0 mA			0.2	V

Table 6. PIN IMPEDANCE CHARACTERISTICS ~~− New Product (Rev C) (Note 7)~~
(V_{CC} = 1.8 V to 5.5 V, T_A = −40°C to +85°C and V_{CC} = 2.5 V to 5.5 V, T_A = −40°C to +125°C, unless otherwise specified.)

Symbol	Parameter	Conditions	Max	Units
C_{IN} (Note 8)	SDA I/O Pin Capacitance	V_{IN} = 0 V	8	pF
C_{IN} (Note 8)	Input Capacitance (other pins)	V_{IN} = 0 V	6	pF
I_{WP}, I_A (Note 9)	WP Input Current, Address Input Current (A_0, A_1, A_2)	V_{IN} < V_{IH}, V_{CC} = 5.5 V	75	μA
		V_{IN} < V_{IH}, V_{CC} = 3.3 V	50	
		V_{IN} < V_{IH}, V_{CC} = 1.8 V	25	
		V_{IN} > V_{IH}	2	

~~7. The product Rev C is identified by letter "C" or dedicated marking code on top of the package.~~
8. These parameters are tested initially and after a design or process change that affects the parameter according to appropriate AEC−Q100 and JEDEC test methods.
9. When not driven, the WP, A_0, A_1, A_2 pins are pulled down to GND internally. For improved noise immunity, the internal pull−down is relatively strong; therefore the external driver must be able to supply the pull−down current when attempting to drive the input HIGH. To conserve power, as the input level exceeds the trip point of the CMOS input buffer (~ 0.5 x V_{CC}), the strong pull−down reverts to a weak current source.

2. CAT24C128XI-T2 は既に廃止されたので、ページ 10 の注文情報表から削除します。



CAT24C128

ORDERING INFORMATION (Notes ~~14~~ thru ~~17~~)

Device Order Number	Specific Device Marking†	Package Type	Temperature Range	Lead Finish	Shipping†
CAT24C128WI−GT3	24128C	SOIC−8, JEDEC	I = Industrial (−40°C to +85°C)	NiPdAu	Tape & Reel, 3,000 Units / Reel
CAT24C128YI−GT3	C28C	TSSOP−8	I = Industrial (−40°C to +85°C)	NiPdAu	Tape & Reel, 3,000 Units / Reel
~~CAT24C128XI−T2~~	~~TBD~~	~~SOIC−8~~	~~I = Industrial (−40°C to +85°C)~~	~~Matte−Tin~~	~~Tape & Reel, 2,000 Units / Reel~~
CAT24C128HU4IGT3	C7U	UDFN−8	I = Industrial (−40°C to +85°C)	NiPdAu	Tape & Reel, 3,000 Units / Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
~~14~~ All packages are RoHS−compliant (Lead−free, Halogen−free).
~~15~~ **The standard lead finish is NiPdAu.**
~~16~~ For additional package and temperature options, please contact your nearest ON Semiconductor Sales office.
~~17~~ For detailed information and a breakdown of device nomenclature and numbering systems, please see the ON Semiconductor Device Nomenclature document, TND310/D, available at www.onsemi.com

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影響を受ける部品の一覧:

注: 標準の部品番号(既製品)のみが部品一覧に記載されます。 本 PCN に影響を受けるカスタム 部品は、PCN メールの顧客の特定の PCN の付属文書、または PCN カスタマイズポータルに記載されています。

CAT24C128HU4IGT3	CAT24C128WI-GT3	CAT24C128YI-GT3