Product Change Notification - SYST-13ICTN430

Date:

14 Nov 2018

Product Category:

8-bit Microcontrollers

Affected CPNs:

Notification subject:

ERRATA - PIC16(L)F18455/56 Family Silicon Errata and Data Sheet Clarification

Notification text:

SYST-13ICTN430

Microchip has released a new DeviceDoc for the PIC16(L)F18455/56 Family Silicon Errata and Data Sheet Clarification of devices. If you are using one of these devices please read the document located at PIC16(L)F18455/56 Family Silicon Errata and Data Sheet Clarification.

Notification Status: Final

Description of Change: Initial document release

Impacts to Data Sheet: None

Reason for Change: To Improve Productivity

Change Implementation Status: Complete

Date Document Changes Effective: 14 Nov 2018

NOTE: Please be advised that this is a change to the document only the product has not been changed.

Markings to Distinguish Revised from Unrevised Devices: N/A

Attachment(s):

PIC16(L)F18455/56 Family Silicon Errata and Data Sheet Clarification

Please contact your local Microchip sales office with questions or concerns regarding this notification.

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Affected Catalog Part Numbers (CPN)

PIC16F18455-E/SO
PIC16F18455-E/SP
PIC16F18455-E/SS
PIC16F18455-E/STX
PIC16F18455-I/SO
PIC16F18455-I/SP
PIC16F18455-I/SS
PIC16F18455-I/STX
PIC16F18455T-I/SO
PIC16F18455T-I/SS
PIC16F18455T-I/STX
PIC16F18456-E/SO
PIC16F18456-E/SP
PIC16F18456-E/SS
PIC16F18456-E/STX
PIC16F18456-I/SO
PIC16F18456-I/SP
PIC16F18456-I/SS
PIC16F18456-I/STX
PIC16F18456T-I/SO
PIC16F18456T-I/SS
PIC16F18456T-I/STX
PIC16LF18455-E/SO
PIC16LF18455-E/SP
PIC16LF18455-E/SS
PIC16LF18455-E/STX
PIC16LF18455-I/SO
PIC16LF18455-I/SP
PIC16LF18455-I/SS
PIC16LF18455-I/STX
PIC16LF18455T-I/SO
PIC16LF18455T-I/SS
PIC16LF18455T-I/STX
PIC16LF18456-E/SO
PIC16LF18456-E/SP
PIC16LF18456-E/SS
PIC16LF18456-E/STX
PIC16LF18456-I/SO
PIC16LF18456-I/SP
PIC16LF18456-I/SS
PIC16LF18456-I/STX
PIC16LF18456T-I/SO
PIC16LF18456T-I/SS
PIC16LF18456T-I/STX

PIC16(L)F18455/56

PIC16(L)F18455/56 Family Silicon Errata and Data Sheet Clarification

Preface

The PIC16(L)F18455/56 devices that you have received conform functionally to the current device data sheet (DS40002038**B**), except for the anomalies described in this document. The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in the table below. The errata described in this document will be addressed in future revisions of the PIC16(L)F18455/56 silicon.

Notice: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated in the last column of the *'Silicon Issue Summary'* table apply to the current silicon revision (A0).

The silicon revision level can be identified using the current version of MPLAB® IDE and Microchip's programmers, debuggers, and emulation tools, which are available at the Microchip corporate website (http://www.microchip.com).

For example, to identify the silicon revision level using MPLAB IDE in conjunction with a hardware debugger:

1. Using the appropriate interface, connect the device to the hardware debugger.
2. Open an MPLAB IDE project.
3. Configure the MPLAB IDE project for the appropriate device and hardware debugger.
4. Based on the version of MPLAB IDE you are using, do one of the following:
   4.1. For MPLAB IDE 8, select ***Programmer*** > ***Reconnect***.
   4.2. For MPLAB X IDE, select ***Window*** > ***Dashboard*** and click the **Refresh Debug Tool Status** icon ().
5. Depending on the development tool used, the part number and Device Revision ID value appear in the **Output** window.

Table 1. Silicon Device Identification

Part Number	Device ID	Revision ID
		A0
PIC16F18455	0x30D7	0x8005
PIC16LF18455	0x30D8	0x8005
PIC16F18456	0x30D9	0x8005
PIC16LF18456	0x30DA	0x8005

Note: Refer to the **Device/Revision ID** section in the current *"PIC16(L)F184XX Memory Programming Specification"* (DS40001970) for detailed information on Device Identification and Revision IDs for your specific device.

Silicon Issue Summary

Module	Feature	Item No.	Issue Summary	Affected Revisions
				A0
NVM	WRERR bit Operation	1.1.1	NVMERR bit is set by device Reset after being cleared by software.	X
Electrical Specifications	FVR Specification	1.2.1	FVR specifications require use above -20°C.	X
Electrical Specifications	Nonvolatile Memory (NVM) for LF Devices	1.2.2	NVM on LF devices may not work properly at specified voltage levels and temperatures.	X
Analog-to-Digital Converter With Computation (ADC^2)	ADC^2 Burst Average mode	1.3.1	ADC^2 Burst Average mode while in "Non-Continuous Double Sample" mode may not operate as intended.	X
Windowed Watchdog Timer	Window Operation	1.4.1	Window feature of the WWDT does not operate correctly in DOZE mode.	X

Note: Only those issues indicated in the last column apply to the current silicon revision.

Table of Contents

1. Silicon Errata Issues

Notice: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated by the bold font in the following tables apply to the current silicon revision.

1.1 Module: Nonvolatile Memory (NVM)

1.1.1 WRERR Bit Operation

When a Reset is issued while an NVM high voltage operation is in progress, the WRERR bit in the NVMCON1 register is set as expected. After clearing the WRERR bit, if a Reset reoccurs, the WRERR bit is set again regardless of whether an NVM operation is in progress or not. A successful write operation will clear the WRERR condition.

Work around

None.

Affected Silicon Revisions

A0							
X							

1.2 Module: Electrical Specifications

1.2.1 Fixed Voltage Reference (FVR)

At temperatures below -20°C, the output voltage for the FVR may be greater than the levels specified in the data sheet. This will apply to all three gain amplifier settings, (1X, 2X, 4X). The affected parameter numbers found in the data sheet are: FVR01 (1X gain setting), FVR02 (2X gain setting), and FVR03 (4X gain setting).

Work around

At temperatures above -20°C, the stated tolerances in the data sheet remain in effect. Operate the FVR only at temperatures above -20°C.

Affected Silicon Revisions

A0							
X							

1.2.2 Electrical Specifications for LF Devices

Nonvolatile memory (NVM) access on LF devices may not work when operating at temperatures between -40°C and +25°C and V_{DD} levels below 2.0V.

V_{DD_MIN} for parameter (D002) is 2.0V for temperatures between -40°C and 25°C.

Work around
None.

Affected Silicon Revisions

A0							
X							

1.3 Module: Analog-to-Digital Converter with Computation (ADCC)

1.3.1 ADC^2 Burst Average Mode

When the ADC^2 is operated in Burst Average mode (MD = `0b011` in the ADCON2 register) while enabling non-continuous operation and double-sampling (CONT = `0` in the ADCON0 register and DSEN = `1` in the ADCON1 register), the value in the ADCNT register does not increment beyond '`0b1`' toward the value in the ADRPT register.

Work around
When operating the ADC^2 in Burst Average mode with double-sampling, enable continuous operation of the module (CONT = `1` in the ADCON0 register) and set the Stop-on-Interrupt bit (SOI bit in the ADCON3 register). After the interrupt occurs, perform appropriate threshold calculations in the software and re-trigger ADC^2 as necessary.

If the CPU is in Low-Power Sleep mode, alternatively the ADC^2 in non-continuous Burst Average mode can be operated with single ADC conversion (DSEN = `0` in the ADCON1 register) compromising noise immunity for lower power consumption by preventing the device from waking up to perform threshold calculations in the software.

Affected Silicon Revisions

A0							
X							

1.4 Module: Windowed Watchdog Timer (WWDT)

1.4.1 Window Operation in DOZE Mode

When the Windowed mode of operation is enabled in DOZE mode, a window violation error is issued even though the window is open and has been armed. This condition occurs only when the window size is set to a value other than 100% open.

Work around
Method 1:

Use the Windowed mode of operation in any other than DOZE mode. If disabling the DOZE mode is not an option, use the WWDT module without the Window being enabled.

Method 2:

If the device is in DOZE mode, perform the arming process for the window in NORMAL mode and return to the DOZE mode.

Method 3:

If there is an ISR in the application code, the arming within the window can be done inside the ISR with the ROI bit of the CPUDOZE register being set.

Affected Silicon Revisions

A0							
X							

2. Revision History

Doc Rev.	Date	Comments
A	11/2018	Initial document release.

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