# 74HC1G04; 74HCT1G04

#### Inverter

Rev. 6 — 21 January 2022

**Product data sheet** 

### 1. General description

The 74HC1G04; 74HCT1G04 is a single inverter. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of  $V_{CC}$ .

### 2. Features and benefits

- Wide supply voltage range from 2.0 V to 6.0 V
- Input levels:
  - For 74HC1G04: CMOS level
  - For 74HCT1G04: TTL level
- · Symmetrical output impedance
- High noise immunity
- · CMOS low power dissipation
- · Balanced propagation delays
- Latch-up performance exceeds 100 mA per JESD 78 Class II Level B
- · Complies with JEDEC standards:
  - JESD8C (2.7 V to 3.6 V)
  - JESD7A (2.0 V to 6.0 V)
- ESD protection:
  - HBM JESD22-A114E exceeds 2000 V
  - MM JESD22-A115-A exceeds 200 V
- Specified from -40 °C to +85 °C and -40 °C to +125 °C

# 3. Ordering information

### **Table 1. Ordering information**

Type number	Package						
	Temperature range	Name	Description	Version			
74HC1G04GW	-40 °C to +125 °C	TSSOP5	plastic thin shrink small outline package; 5 leads;	SOT353-1			
74HCT1G04GW			body width 1.25 mm				
74HC1G04GV	-40 °C to +125 °C	SC-74A	plastic surface-mounted package; 5 leads	SOT753			
74HCT1G04GV							



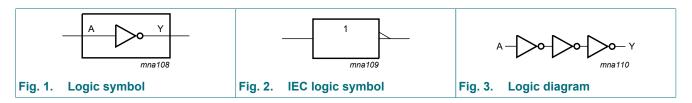
# 4. Marking

#### Table 2. Marking codes

Type number	Marking[1]
74HC1G04GW	HC
74HCT1G04GW	TC
74HC1G04GV	H04
74HCT1G04GV	Т04

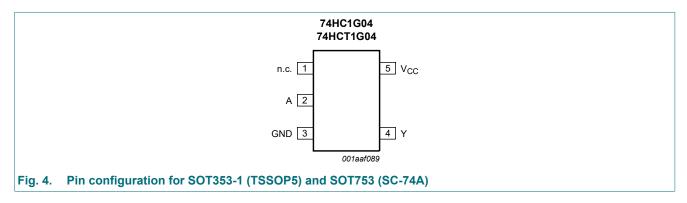
<sup>[1]</sup> The pin 1 indicator is located on the lower left corner of the device, below the marking code.

# 5. Functional diagram



# 6. Pinning information

### 6.1. Pinning



### 6.2. Pin description

Table 3. Pin description

Symbol	Pin	Description
n.c.	1	not connected
A	2	data input
GND	3	ground (0 V)
Υ	4	data output
V <sub>CC</sub>	5	supply voltage

## 7. Functional description

#### **Table 4. Function table**

H = HIGH voltage level; L = LOW voltage level

Input	Output
A	Υ
L	Н
Н	L

### 8. Limiting values

#### Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V <sub>CC</sub>	supply voltage			-0.5	+7.0	V
I <sub>IK</sub>	input clamping current	$V_{I} < -0.5 \text{ V or } V_{I} > V_{CC} + 0.5 \text{ V}$	[1]	-	±20	mA
I <sub>OK</sub>	output clamping current	$V_{O} < -0.5 \text{ V or } V_{O} > V_{CC} + 0.5 \text{ V}$	[1]	-	±20	mA
Io	output current	-0.5 V < V <sub>O</sub> < V <sub>CC</sub> + 0.5 V	[1]	-	±12.5	mA
I <sub>CC</sub>	supply current		[1]	-	25	mA
I <sub>GND</sub>	ground current			-25	-	mA
T <sub>stg</sub>	storage temperature			-65	+150	°C
P <sub>tot</sub>	total power dissipation	T <sub>amb</sub> = -40 °C to +125 °C	[2]	-	250	mW

<sup>[1]</sup> The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

# 9. Recommended operating conditions

#### Table 6. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	7	4HC1G0	4	74	4HCT1G	04	Unit
			Min	Тур	Max	Min	Тур	Max	
V <sub>CC</sub>	supply voltage		2.0	5.0	6.0	4.5	5.0	5.5	V
VI	input voltage		0	-	V <sub>CC</sub>	0	-	V <sub>CC</sub>	V
Vo	output voltage		0	-	V <sub>CC</sub>	0	-	V <sub>CC</sub>	V
T <sub>amb</sub>	ambient temperature		-40	+25	+125	-40	+25	+125	°C
Δt/ΔV	input transition rise and	V <sub>CC</sub> = 2.0 V	-	-	625	-	-	-	ns/V
	fall rate	V <sub>CC</sub> = 4.5 V	-	-	139	-	-	139	ns/V
		V <sub>CC</sub> = 6.0 V	-	-	83	-	-	-	ns/V

<sup>[2]</sup> For SOT353-1 (TSSOP5) package: P<sub>tot</sub> derates linearly with 3.3 mW/K above 74 °C. For SOT753 (SC-74A) package: P<sub>tot</sub> derates linearly with 3.8 mW/K above 85 °C.

### 10. Static characteristics

**Table 7. Static characteristics** 

Voltages are referenced to GND (ground = 0 V). All typical values are measured at  $T_{amb}$  = 25 °C.

Symbol	Parameter Conditions -40 °C to +		°C to +8	5°C	-40 °C t	o +125 °C	Unit	
			Min	Тур	Max	Min	Max	
74HC1G0	4				'			
V <sub>IH</sub>	HIGH-level input	V <sub>CC</sub> = 2.0 V	1.5	1.2	-	1.5	-	V
	voltage	V <sub>CC</sub> = 4.5 V	3.15	2.4	-	3.15	-	V
	V <sub>CC</sub> = 6.0 V	4.2	3.2	-	4.2	-	V	
V <sub>IL</sub>	LOW-level input	V <sub>CC</sub> = 2.0 V	-	0.8	0.5	-	0.5	V
	voltage	V <sub>CC</sub> = 4.5 V	-	2.1	1.35	-	1.35	V
		V <sub>CC</sub> = 6.0 V	-	2.8	1.8	-	1.8	V
V <sub>OH</sub>	HIGH-level output	$V_I = V_{IH}$ or $V_{IL}$						
	voltage	I <sub>O</sub> = -20 μA; V <sub>CC</sub> = 2.0 V	1.9	2.0	-	1.9	-	V
		I <sub>O</sub> = -20 μA; V <sub>CC</sub> = 4.5 V	4.4	4.5	-	4.4	-	V
		$I_{O} = -20 \mu\text{A};  V_{CC} = 6.0 \text{V}$	5.9	6.0	-	5.9	-	V
		$I_O = -2.0 \text{ mA}; V_{CC} = 4.5 \text{ V}$	4.13	4.32	-	3.7	_	V
		$I_{O}$ = -2.6 mA; $V_{CC}$ = 6.0 V	5.63	5.81	-	5.2	_	V
V <sub>OL</sub>	LOW-level output	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>						
OL	voltage	$I_O = 20 \mu A; V_{CC} = 2.0 V$	-	0	0.1	-	0.1	V
		$I_{O} = 20 \mu A; V_{CC} = 4.5 V$	_	0	0.1	_	0.1	V
		$I_{O} = 20 \mu A; V_{CC} = 6.0 \text{ V}$	_	0	0.1	-	0.1	V
		$I_O = 2.0 \text{ mA}; V_{CC} = 4.5 \text{ V}$	_	0.15	0.33	_	0.4	V
		$I_0 = 2.6 \text{ mA}; V_{CC} = 6.0 \text{ V}$	_	0.16	0.33	-	0.4	V
l <sub>l</sub>	input leakage current	$V_1 = V_{CC}$ or GND; $V_{CC} = 6.0 \text{ V}$	_	-	1.0	_	1.0	μA
I <sub>CC</sub>	supply current	V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0 A; V <sub>CC</sub> = 6.0 V	-	-	10	-	20	μA
Cı	input capacitance		_	1.5	-	-	-	pF
74HCT1G		I .						•
V <sub>IH</sub>	HIGH-level input voltage	V <sub>CC</sub> = 4.5 V to 5.5 V	2.0	1.6	-	2.0	-	V
V <sub>IL</sub>	LOW-level input voltage	V <sub>CC</sub> = 4.5 V to 5.5 V	-	1.2	0.8	-	0.8	V
V <sub>OH</sub>	HIGH-level output	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>						
<b></b>	voltage	$I_{O} = -20 \mu A; V_{CC} = 4.5 V$	4.4	4.5	-	4.4	-	V
		$I_{\rm O}$ = -2.0 mA; $V_{\rm CC}$ = 4.5 V	4.13	4.32	-	3.7	-	V
V <sub>OL</sub>	LOW-level output	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>						
OL.	voltage	I <sub>O</sub> = 20 μA; V <sub>CC</sub> = 4.5 V	_	0	0.1	-	0.1	V
		I <sub>O</sub> = 2.0 mA; V <sub>CC</sub> = 4.5 V	_	0.15	0.33	-	0.4	V
l <sub>l</sub>	input leakage current	$V_1 = V_{CC}$ or GND; $V_{CC} = 5.5 \text{ V}$	_	-	1.0	-	1.0	μA
I <sub>CC</sub>	supply current	V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0 A; V <sub>CC</sub> = 5.5 V	-	-	10	-	20	μA
ΔI <sub>CC</sub>	additional supply current	per input; V <sub>CC</sub> = 4.5 V to 5.5 V; V <sub>I</sub> = V <sub>CC</sub> - 2.1 V; I <sub>O</sub> = 0 A	-	-	500	-	850	μA
C <sub>I</sub>	input capacitance		_	1.5	-	_	-	pF

# 11. Dynamic characteristics

#### **Table 8. Dynamic characteristics**

GND = 0 V;  $t_r = t_f \le 6.0$  ns; All typical values are measured at  $T_{amb} = 25$  °C. For test circuit, see Fig. 6.

Symbol	Parameter	Conditions		-40	°C to +8	5 °C	-40 °C t	o +125 °C	Unit
				Min	Тур	Max	Min	Max	
74HC1G	04		'						
t <sub>pd</sub>	propagation delay	A to Y; see Fig. 5	[1]						
		V <sub>CC</sub> = 2.0 V; C <sub>L</sub> = 50 pF		-	25	105	-	135	ns
		V <sub>CC</sub> = 4.5 V; C <sub>L</sub> = 50 pF		-	9	21	-	27	ns
		V <sub>CC</sub> = 5.0 V; C <sub>L</sub> = 15 pF		-	7	-	-	-	ns
		V <sub>CC</sub> = 6.0 V; C <sub>L</sub> = 50 pF		-	8	18	-	23	ns
C <sub>PD</sub>	power dissipation capacitance	$V_I = GND \text{ to } V_{CC}$	[2]	-	16	-	-	-	pF
74HCT10	G04		·						
t <sub>pd</sub>	propagation delay	A to Y; see Fig. 5	[1]						
		V <sub>CC</sub> = 4.5 V; C <sub>L</sub> = 50 pF		-	10	24	-	27	ns
		V <sub>CC</sub> = 5.0 V; C <sub>L</sub> = 15 pF		-	8	-	-	-	ns
C <sub>PD</sub>	power dissipation capacitance	$V_I = GND \text{ to } V_{CC} - 1.5 \text{ V}$	[2]	-	18	-	-	-	pF

 $t_{pd}$  is the same as  $t_{PLH}$  and  $t_{PHL}$ .  $C_{PD}$  is used to determine the dynamic power dissipation  $P_D$  ( $\mu$ W).  $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$  where:

f<sub>i</sub> = input frequency in MHz

fo = output frequency in MHz

C<sub>L</sub> = output load capacitance in pF

 $V_{CC}$  = supply voltage in V  $\Sigma(C_L \times V_{CC}^2 \times f_o)$  = sum of outputs

#### 11.1. Waveforms and test circuit

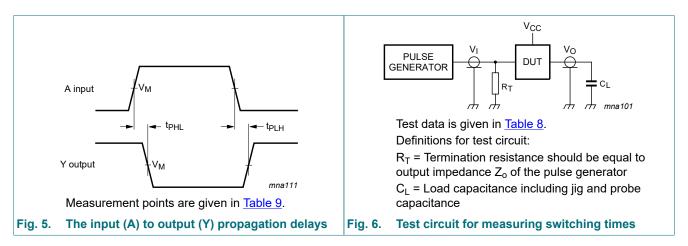


Table 9. Measurement points

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Туре	V <sub>I</sub>	V <sub>M</sub>			
74HC1G04	GND to V <sub>CC</sub>	0.5 × V <sub>CC</sub>			
74HCT1G04	GND to 3.0 V	1.3 V			

# 12. Package outline

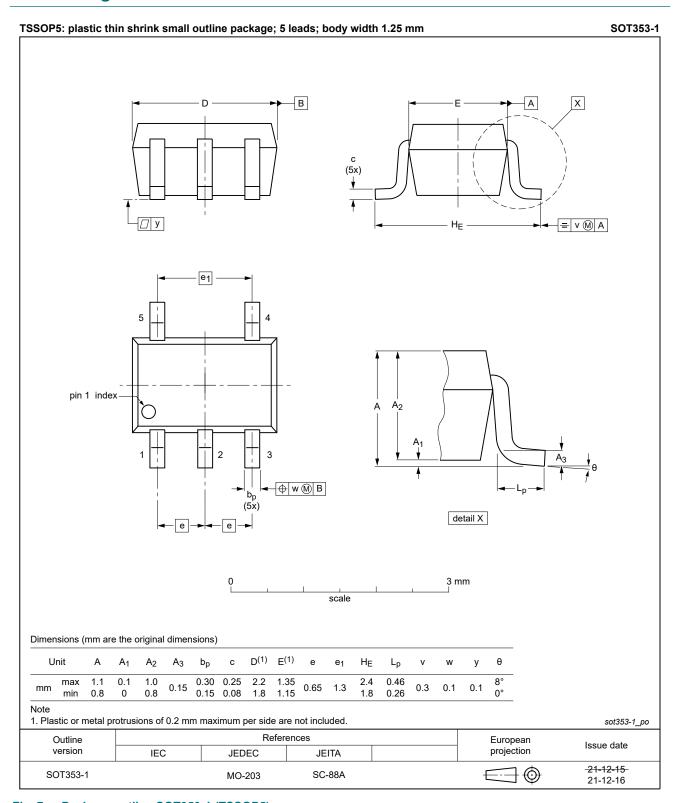


Fig. 7. Package outline SOT353-1 (TSSOP5)

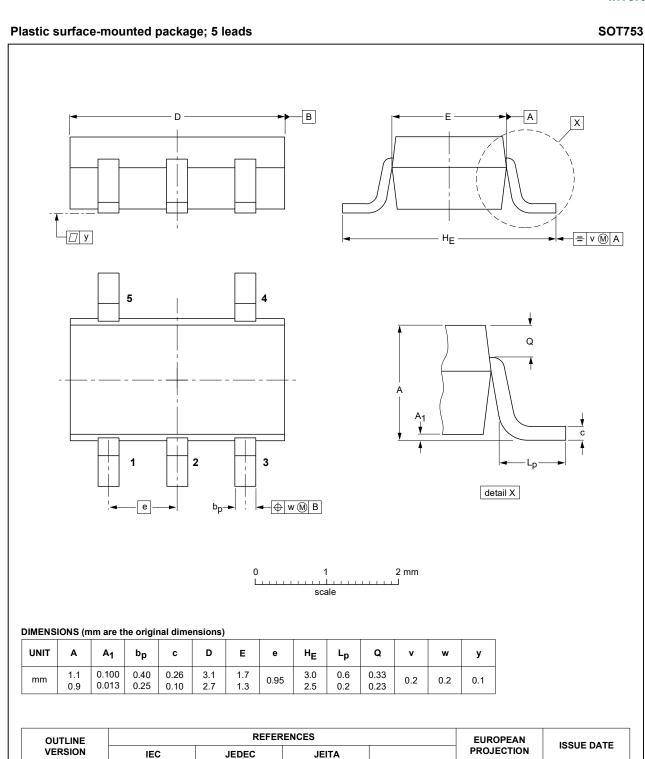


Fig. 8. Package outline SOT753 (SC-74A)

SC-74A

02-04-16

06-03-16

SOT753

### 13. Abbreviations

#### **Table 10. Abbreviations**

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
НВМ	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

# 14. Revision history

### Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes	
74HC_HCT1G04 v.6	20220121	Product data sheet	-	74HC_HCT1G04 v.5	
Modifications:	<ul> <li>The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia.</li> <li>Legal texts have been adapted to the new company name where appropriate.</li> <li>Section 1 and Section 2 updated.</li> <li>Table 5: Derating values for P<sub>tot</sub> total power dissipation updated.</li> <li>Fig. 7: Package outline drawing SOT353-1 (TSSOP5) has changed.</li> </ul>				
74HC_HCT1G04 v.5	20130925	Product data sheet	-	74HC_HCT1G04 v.4	
Modifications:	• Section 1 u	ıpdated.			
74HC_HCT1G04 v.4	20070716	Product data sheet	-	74HC_HCT1G04 v.3	
Modifications:	<ul> <li>The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.</li> <li>Legal texts have been adapted to the new company name where appropriate.</li> <li>Package SOT353 changed to SOT353-1 in Table 1 and Fig. 7.</li> <li>Quick Reference Data and Soldering sections removed.</li> <li>Section 2 updated.</li> </ul>				
74HC_HCT1G04 v.3	20020517	Product specification	-	74HC_HCT1G04 v.2	
74HC_HCT1G04 v.2	20010302	Product specification	-	74HC_HCT1G04 v.1	
74HC_HCT1G04 v.1	19980831	Preliminary specification	-	-	

### 15. Legal information

#### Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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