MP3421

5.5A, 600kHz High-Efficiency, Synchronous Step-Up Converter with True Output Disconnect in a 2mmx2mm QFN Package

The Future of Analog IC Technology

DESCRIPTION

The MP3421 is a high-efficiency, synchronous, current–mode, step-up converter with true output disconnect.

The MP3421 starts up from low input voltage (as low as 1.9V) while providing in-rush current limiting and output short-circuit protection. The integrated, P-channel synchronous rectifier improves efficiency and eliminates the need for an external Schottky diode; the P-channel disconnects the output load from the input during shutdown.

The MP3421 has 600kHz switching frequency, which accommodates small external components. In addition, its internal compensation and soft-start functions minimize external component count. The MP3421 provides a compact solution for a 5V output, 2.1A load requirement, using a supply voltage as low as 2.8V.

The MP3421 is available in a 14-pin QFN 2mmx2mm package.

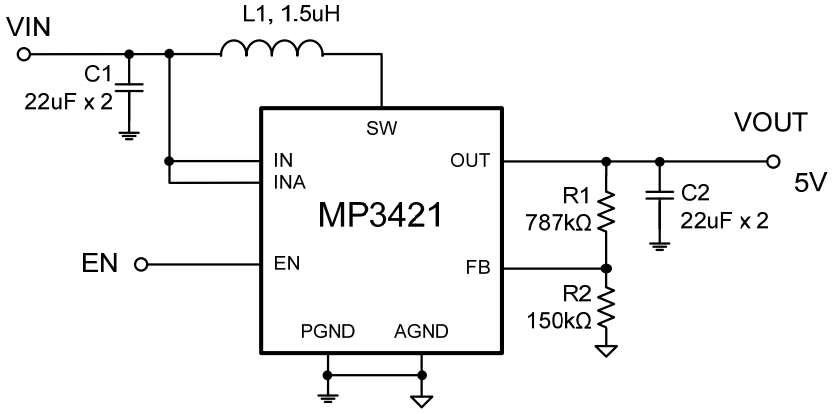
FEATURES

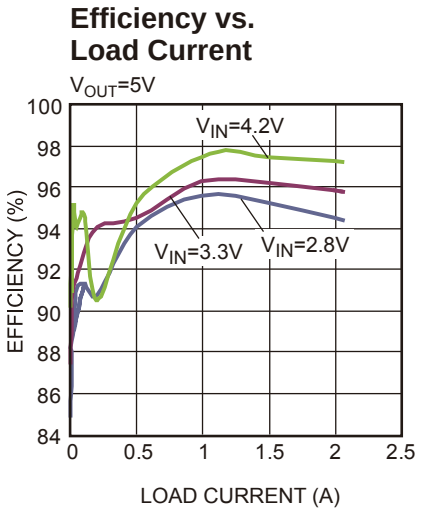
- Support 5V/2.1A Output at 2.8V Input
- Up to 98% Efficiency
- 1.9V to 5.5V Input Range
- 2.5V to 5.5V Output Range
- Internal Synchronous Rectifier
- 600kHz Fixed-Switching Frequency
- >5.5A Switch-Current Limit Capability
- 43uA Quiescent Current
- High-Efficiency over Full-Load Range
- Internal Soft-start and Compensation
- Output-Load Disconnect from Input
- OCP, SCP, OVP and OTP Protection
- Small 2x2mm QFN14 Package

APPLICATIONS

- Battery-Powered Products
- Power Banks, Juice Packs, Battery Back-up Units
- USB Power Supply
- Consumer Electronic Accessories
- Tablets

TYPICAL APPLICATION





ORDERING INFORMATION

Part Number*	Package	Top Marking
MP3421GG	QFN-14 (2mmX2mm)	*See Below*

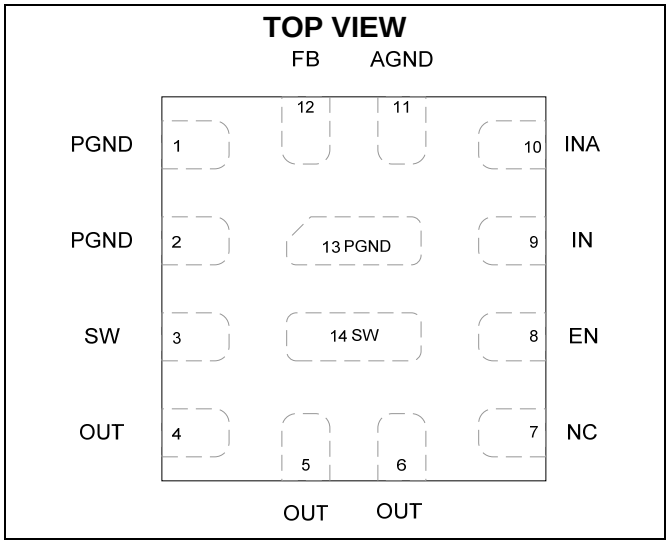
* For Tape & Reel, add suffix –Z (e.g. MP3421GG–Z)

TOP MARKING

DKY
LLL

DK: product code of MP3421GG;
Y: year code;
LLL: lot number;

PACKAGE REFERENCE



ABSOLUTE MAXIMUM RATINGS (1)

SW .. ..-0.3V to +6.5V (9V for <5ns)
All other Pins.....-0.3V to +6.5V
Continuous Power Dissipation (T_A = +25°C) **(2)**
..... 1.56W
Junction Temperature.....150°C
Lead Temperature .....260°C
Storage Temperature..... -65°C to +150°C

Recommended Operating Conditions (3)

Supply Voltage V_{IN} .....1.9V to 5.5V
V_{OUT}.....2.5V to 5.5V
Operating Junction Temp. (T_J). -40°C to +125°C

Thermal Resistance (4)

	θ_{JA}	θ_{JC}	
QFN-14 (2mmx2mm).....	80.....	16	°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

V_{IN} = V_{EN} = 3.3V, V_{OUT} = 5V, T_J= -40°C to125°C, typical values are tested at T_J =25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Voltage Range						
Start-Operating Input Voltage	V_{IN}		1.9		5.5	V
Quiescent Current	I_{Q_NS}	V_{EN}=V_{IN}=3.3V, V_{OUT}=5V, no load Measured on OUT, T_J=25°C		43	57	μA
		V_{EN}=V_{IN}=3.3V, V_{OUT}=5V, no load Measured on IN		0.3		μA
Shutdown Current	I_{SD}	V_{EN}=V_{OUT}=0V, Measured on IN, T_J=25°C		0.1	1	μA
IN UVLO Rising Threshold	V_{UVLO_IN-R}	V_{IN} Rising T_J=25°C	1	1.3	1.6	V
IN UVLO Falling Threshold	V_{UVLO_IN-F}	V_{IN} Falling, V_{OUT}=5V		650		mV
VOUT Start-Switching Rising Threshold	$V_{UVLO\_OUT\_R}$	T_J=25°C		1.7	1.79	V
Step-up Converter						
Operation Frequency	F_{SW}	T_J=25°C	500	600	700	kHz
		-40°C≤T_J≤125°C	440	600	760	
Feedback Voltage	V_{FB}	T_J=25°C	795	807	819	mV
		-40°C≤T_J≤125°C	791	807	823	
Feedback Input Current	I_{FB}	V_{FB}=850mV		1	50	nA
NMOS On-Resistance	R_{NDS_ON}			15		mΩ
NMOS Leakage Current	I_{N_LK}	V_{SW}=5V		100		nA
PMOS On-Resistance	R_{PDS_ON}			20		mΩ
PMOS Leakage Current	I_{P_LK}	V_{SW}=5V, V_{OUT}=0V		0.1		μA
Maximum Duty Cycle	D_{MAX}		90	95		%
Linear-Charge Current Limit(5)	I_{CH_LIMIT}	V_{OUT}=1.7V		0.7		A
		V_{OUT}=0V		0.2		A
NMOS Current Limit(5)	I_{SW_LIMIT1}	V_{IN}=5V, V_{OUT}=3.3V		4		A
	I_{SW_LIMIT2}	Duty=44%, V_{IN}=2.8V, V_{OUT}=5V	5.5			A
Logic Interface						
EN High-Level Voltage	V_{EN_H}		1.2			V
EN Low-Level Voltage	V_{EN_L}				0.4	V
EN Input Current	I_{EN}	Connect to V_{IN}		10		nA
Protection						
Thermal Shutdown(5)				150		°C
Over Temperature Hysteresis(5)				20		°C

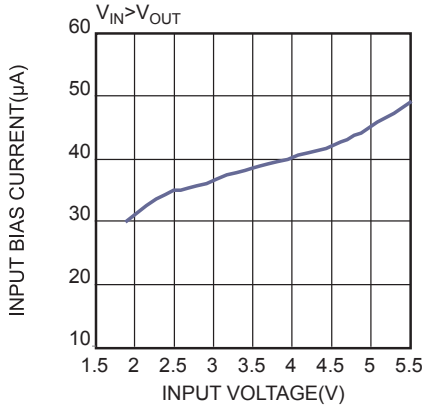
Notes:

5) Guaranteed by characterization, not production tested.

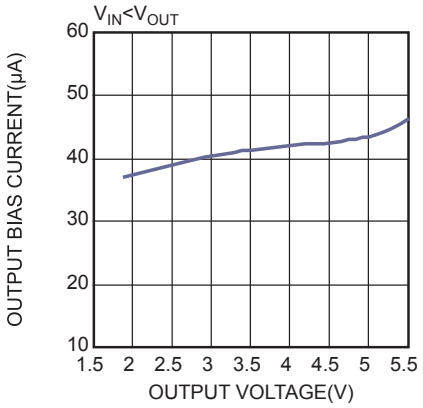
TYPICAL CHARACTERISTICS

V_{IN} = V_{EN} = 3.3V, V_{OUT} = 5V, L = 1.5µH, T_A = 25°C, unless otherwise noted.

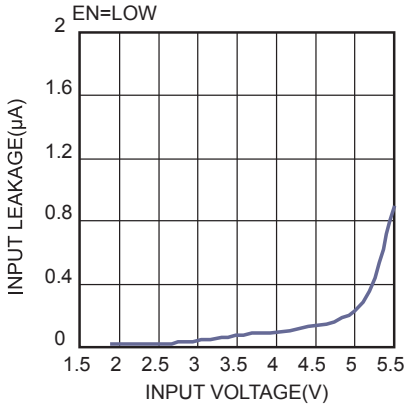
Quiescent Current vs. Input Voltage



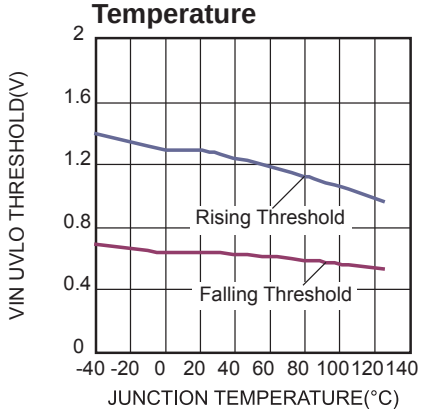
Quiescent Current vs. Output Voltage



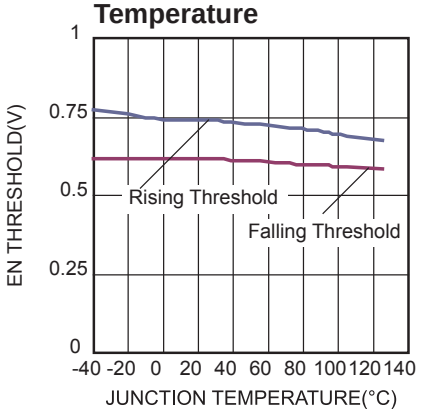
Shutdown Current vs. Input Voltage



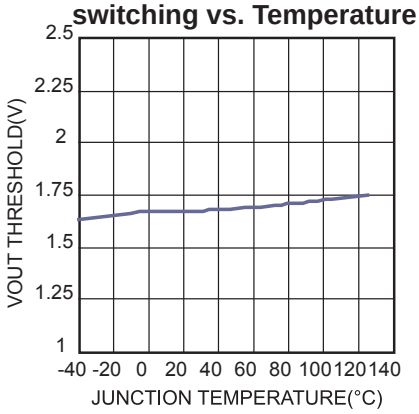
Input UVLO Threshold vs. Temperature



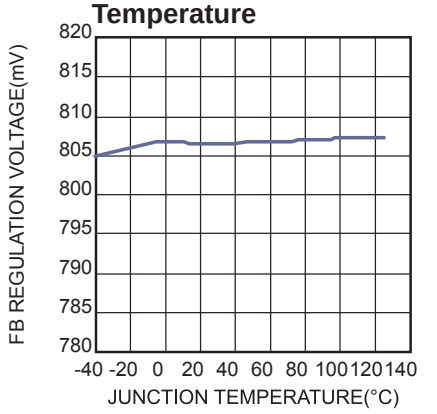
EN Threshold vs. Temperature



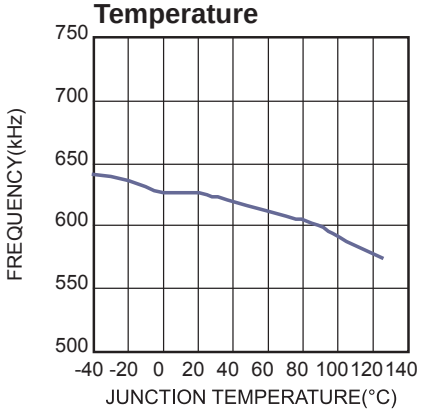
VOUT Rising Threshold for switching vs. Temperature



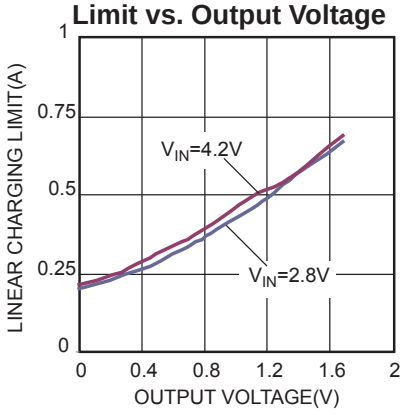
Feedback Voltage vs. Temperature



Frequency vs. Temperature



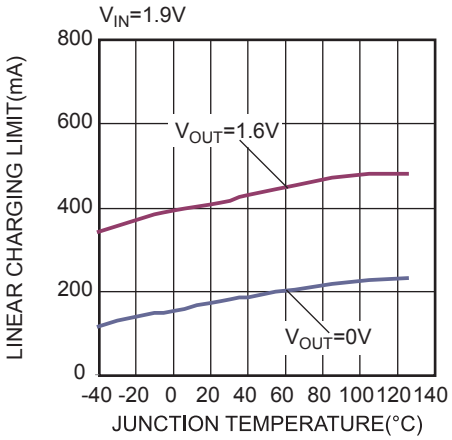
Linear-Charging Current Limit vs. Output Voltage



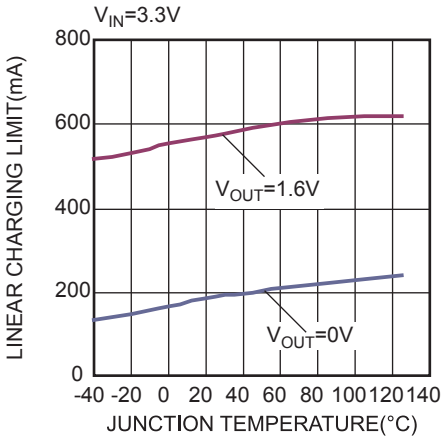
TYPICAL CHARACTERISTICS *(continued)*

V_{IN} = V_{EN} = 3.3V, V_{OUT} = 5V, L = 1.5µH, T_A = 25°C, unless otherwise noted.

Linear-Charging Current Limit vs. Temperature



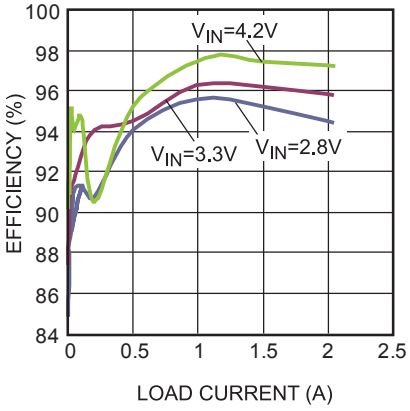
Linear-Charging Current Limit vs. Temperature



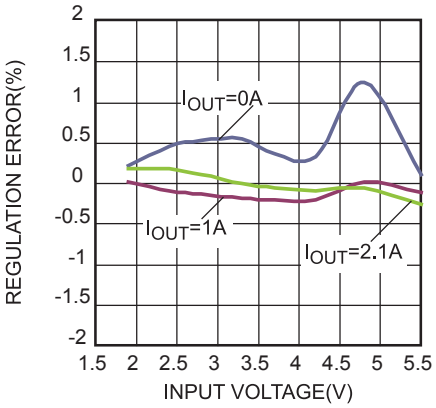
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 3.3V, V_{OUT} = 5V, L=1.5uH, T_A = 25°C, tested on standard EVB, unless otherwise noted.

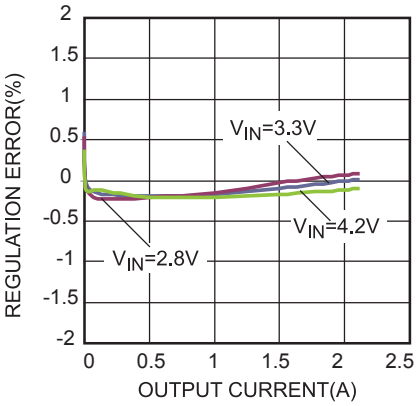
Efficiency vs. Load Current



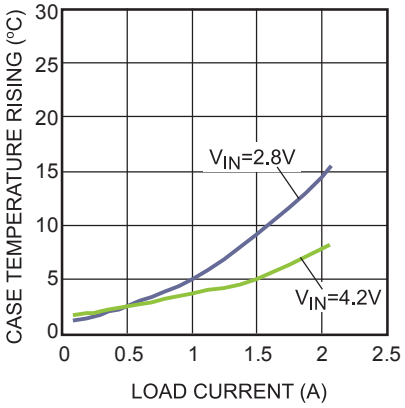
Line Regulation



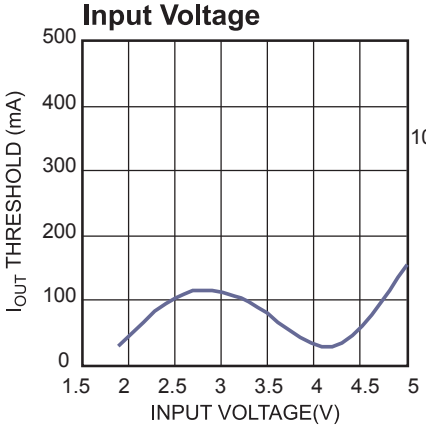
Load Regulation



Case Temperature Rising vs. Load Current

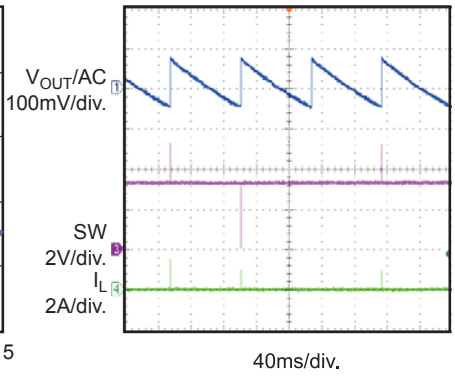


PSM Threshold vs. Input Voltage



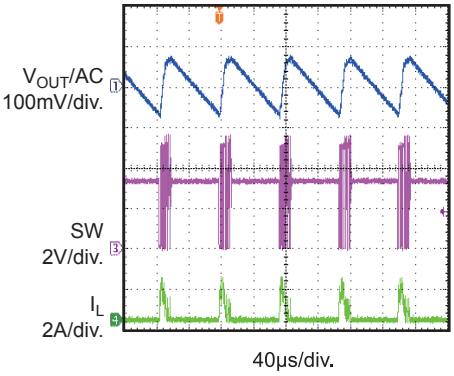
Output-Voltage Ripple

Load = 0A



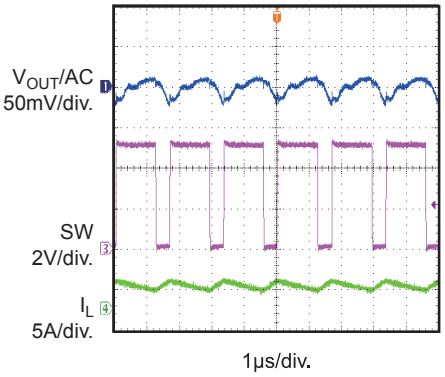
Output-Voltage Ripple

Load = 0.1A



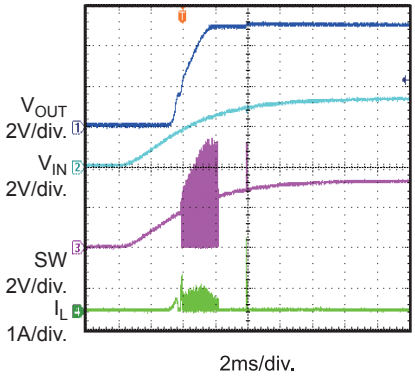
Output-Voltage Ripple

Load = 2.1A



VIN Startup

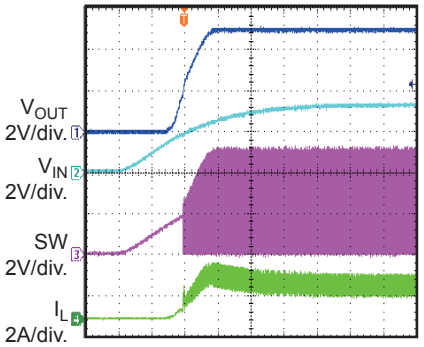
Load = 0A



TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

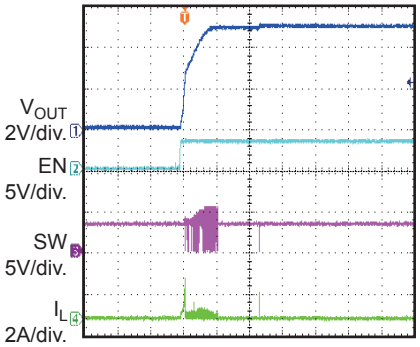
V_{IN} = 3.3V, V_{OUT} = 5V, L=1.5uH, T_A = 25°C, tested on standard EVB, unless otherwise noted.

V_{IN} Startup
Load = 5Ω



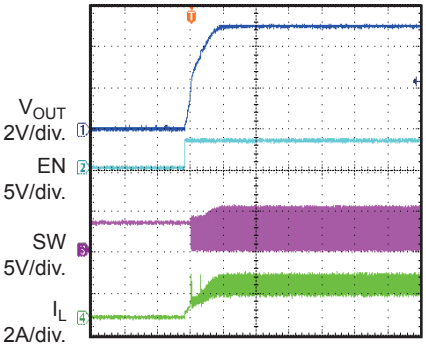
2ms/div.

EN Start up
Load = 0A



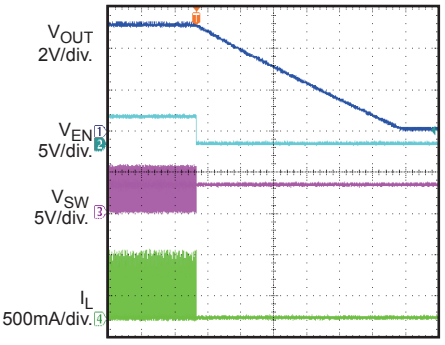
2ms/div.

EN Startup
Load = 5Ω



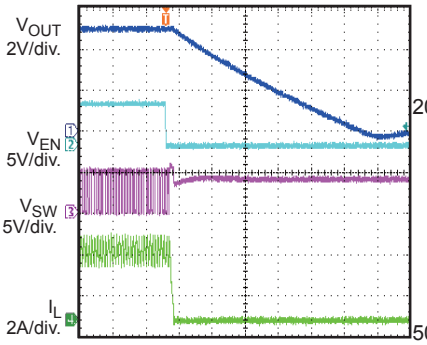
2ms/div.

EN Shutdown
Load=0.1A



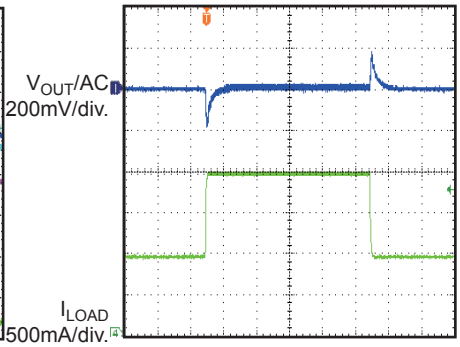
400µs/div.

EN Shutdown
Load=2.1A



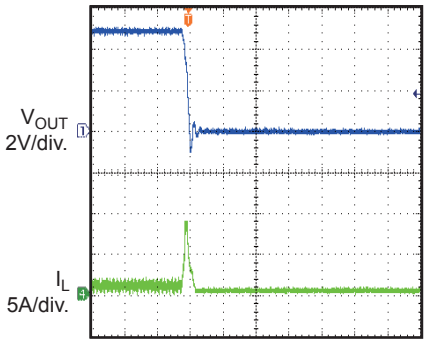
20µs/div.

Load Transient
Load = 1A <-> 2A at 50mA/µs



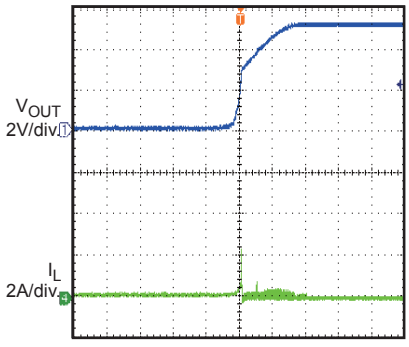
400µs/div.

Short-Circuit Entry
0.6A load to short



200µs/div.

Short-Circuit Recovery
Recover to 0A load



1ms/div.

PIN FUNCTIONS

Pin #	Name	Pin Function
1, 2, 13	PGND	Power Ground.
3, 14	SW	Power-Switch Output. SW is the internal NMOS switch and synchronous switch connection node . Connect the power inductor between SW and input power. Keep these PCB trace lengths as short and wide as possible to reduce EMI and voltage spikes.
4, 5, 6	OUT	Output. OUT is the internal synchronous rectifier MOSFET drain. Bias is derived from OUT when V_{OUT} is higher than V_{IN}. PCB trace length from OUT to the output filter capacitor(s) should be as short and wide as possible. Due to the output disconnect feature, OUT is completely disconnected from IN when EN is low.
7	NC	No Connect. Reserved for factory use only. Float or connect NC to GND in the application.
8	EN	Enable Control Input.
9	IN	Power-Supply Input. The startup bias is derived from IN. It must be locally bypassed. Once OUT exceeds IN, bias comes from OUT. Once started, operation is completely independent from IN.
10	INA	Power-Supply Input (for factory use only). INA must be connected to IN in the application.
11	AGND	Analog Signal Ground.
12	FB	Feedback Input to Error Amplifier. Connect resistor divider tap to FB. The output voltage can be adjusted from 2.5V to 5.5V

FUNCTION DIAGRAM

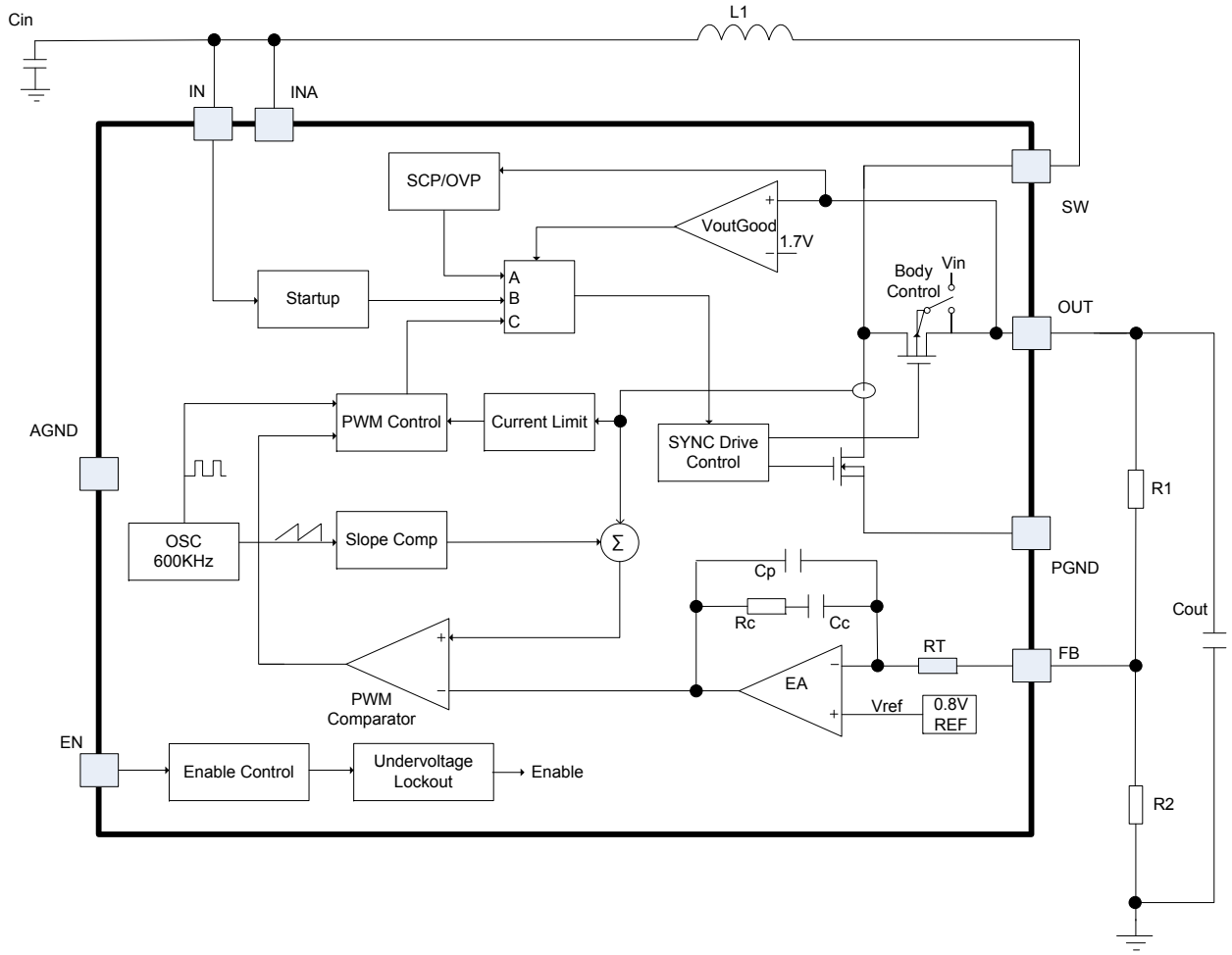


Figure 1: Functional Block Diagram

OPERATION

The MP3421 is a 600kHz, synchronous step-up converter with true output disconnect offered in a compact QFN 2X2-14 lead package. It features fixed-frequency current mode PWM controls for excellent line and load regulation. Internal soft-start and loop compensation simplifies the design process and minimizes external components. The internal, $R_{DS(ON)}$ low MOSFETs, combined with frequency-stretching operation, allows the device to maintain high efficiency over a wide-load current range.

Start-Up

When the IC is enabled and IN voltage exceeds V_{uvlo_in-R}, the MP3421 starts up in the linear charge period. During this period, the PMOS rectifier turns on until the output capacitor is charged to 1.7V. The PMOS current is limited to 0.2A when V_{OUT} is 0V to avoid an inrush current. While the output ramps, the PMOS current limit increases and ramps to 0.7A at 1.7V output. This circuit helps to limit the output current under short-circuit conditions. Once the output is charged to 1.7V, the linear charge period elapses and the MP3421 starts switching in normal closed-loop operation. In normal operation, with Vo lower than V_{in} +0.3V, the MP3421 operates in step-down mode with 4A typical peak-current limit. Also it works in boost mode when Vo is higher than V_{in} +0.3V with more than 5.5A current limit (see Table 1).

Table 1: Work Mode during Startup

V_{OUT}<1.7V	Linear Charge Mode
$V_{OUT} \geqslant$1.7V & $V_{OUT} < V_{IN}$ + 0.3V	Down Mode
$V_{OUT} \geqslant$1.7V & $V_{OUT} \geqslant V_{IN}$ + 0.3V	Boost Mode

In down mode (if HS-FET is on), the HS-FET gate is pulled to VIN and works with high impedance. In down mode, power loss is high and regulation is poor. Down mode is designed to work in startup and SCP conditions; do not set MP3421 in down mode for normal operation (unless the thermal temperature and regulation do not affect system performance).

Once the output voltage exceeds the input voltage, the MP3421 powers its internal circuits from V_{OUT} instead of V_{in}.

Soft-Start (SS)

The MP3421 provides soft-start by charging an internal capacitor with a current source. During the linear-charge period, the soft-start voltage rises, following the FB voltage. Once the linear charge period elapses and the voltage on the capacitor is charged, the reference voltage slowly ramps. The reference soft-start time is typically 2ms from 0V to 0.807V.

The soft-start capacitor is discharged completely at output in the event of a commanded shutdown, thermal shutdown, or short circuit.

Enable (EN)

Operation is enabled when EN is switched high; it enters shutdown mode when EN is switched low. In shutdown mode, the regulator stops switching and all internal control circuitry is turned off; the load is isolated from the input.

Power-Save Mode (PSM)

The MP3421 automatically enters power-save mode (PSM) when the load decreases; it resumes PWM mode when the load increases. When the device goes into PSM, it lowers the switching frequency. This prevents switching and driver losses and switches to pulse-skip mode if the load continues to decrease.

Error Amplifier (EA)

The error amplifier (EA) is an internally-compensated amplifier. The EA compares the internal 0.807V reference voltage against V_{FB} to generate an error signal. The output voltage of the MP3421 is adjusted by an external resistor divider. A voltage divider from V_{OUT} to ground programs the output voltage via the FB from 2.5V to 5.5V using the equation:

$$V_{OUT}=0.807V \times (1+R1/R2)$$

Set the value of R1 and R2 to achieve low-quiescent current. R1 values larger than 600k

are recommended for good stability and transient balance.

Current Sensing

Lossless-current sensing converts the NMOS switch current signal to voltage, which is summed with the internal slope compensation. The summed signal is compared to the error amplifier output to provide a peak-current control command for the PWM. The minimum peak-switch current limit is 5.5A. Internally, the switch-current signal is blanked for about 60ns to enhance noise rejection.

Output Disconnect

The MP3421 has true output disconnect by eliminating body diode conduction from the internal PMOS rectifier. This allows V_{OUT} to go to 0V during shutdown or isolate and maintain an external bias on V_{OUT}. Also, it allows for inrush-current limit at startup, minimizing surge current from the input supply. To efficiently utilize output disconnect, eliminate (if necessary) the external Schottky diode connection between the switch and V_{OUT}.

Over-Load (OLP)and Short-Circuit (SCP) Protection

If an overload or short circuit occurs, the output voltage drops. If V_{OUT} drops below V_{in} +0.3 V, MP3421 converts to step-down mode. If V_{OUT} drops below 1.7V, the device enters linear charge mode. If V_{OUT} drops below 70% of the nominal output voltage, the MP3421 immediately shuts down and re-starts in a power-on cycle after 40μs.

Over-Voltage Protection (OVP)

If V_{OUT} is higher than 7V, boost switching stops. This prevents overvoltage from damaging the internal power MOSFET. When the output drops below 7V, the device resumes switching automatically.

Thermal Shutdown (TSD)

The device contains an internal temperature monitor. The switches turn off if the die temperature exceeds 150°C. The device resumes normal operation below 130°C.

APPLICATION INFORMATION

COMPONENT SELECTION

Input Capacitor Selection

Low ESR input capacitors reduce input-switching noise and reduce the peak current drawn from the battery. Ceramic capacitors are recommended for input decoupling and should be located as close to the device as possible. A ceramic capacitor larger than 22μF is recommended to restrain the V_{IN} ripple.

Output Capacitor Selection

To ensure stability over the full-operating range, the output capacitor requires a minimum capacitance value of 22μF at the programmed output voltage. A higher capacitance value may be required to lower both the output ripple and the transient ripple. Low ESR capacitors, such as X5R or X7R type ceramic capacitors are recommended. Supposing that ESR is zero, the minimum output capacitor to support the ripple in the PWM mode can be calculated by:

$$C_O \geq \frac{I_O \times (V_{OUT(MAX)} - V_{IN(MIN)})}{f_S \times V_{OUT(MAX)} \times \Delta V}$$

Where,
$V_{OUT(MAX)}$ = Maximum output voltage
$V_{IN(MIN)}$ = Minimum Input voltage
I_O=Output current
f_S = Switching frequency
ΔV= Acceptable output ripple

A 1μF ceramic capacitor is recommended between the OUT and PGND. This reduces spikes on the SW node and improves EMI performance.

Inductor Selection

Due to the 600kHz switching frequency, the MP3421 utilizes small surface mount-chip inductors, Inductor values run between 1μH and 2.2μH, and they are suitable for most applications. Larger inductance values allow slightly greater output-current capability by reducing the inductor-ripple current. However, larger inductance values also increase component size. The minimum inductance value is given by:

$$L \geq \frac{V_{IN(MIN)} \times (V_{OUT(MAX)} - V_{IN(MIN)})}{V_{OUT(MAX)} \times \Delta I_L \times f_S} \quad (3)$$

Where ΔI_L=Acceptable inductor-current ripple.

The inductor-current ripple is typically set at 30% to 40% of the maximum inductor current. The inductor should have low DCR (inductor current series resistance without saturating windings) to reduce the resistive power loss. The saturated current (I_{SAT}) should be large enough to support the peak current.

PCB Layout Considerations

Proper PCB layout for high-frequency switching power supplies is critical. Poor layout results in weak performance, excessive EMI, resistive loss and system instability.

The steps below ensure a good layout design:

1. The output capacitor must be placed as close as possible to the OUT, with minimal distance from PGND. A small decoupling capacitor should be parallel with the bulk output capacitor and placed as close as possible to the OUT. This is critical for reducing spikes on the SW and improving EMI performance.
2. The input capacitor and inductor should be as close as possible to the IN and SW. The trace between the inductor and the SW should be as wide and short as possible.
3. The feedback loop should be far from any noise sources, such as the SW. The feedback divider resistors should be as close as possible to the FB and AGND.
4. The ground return of the input/output capacitors should be tied as close as possible to the PGND with a large copper GND area. Vias around the GND are recommended to lower the die temperature.
5. INA must be connected to IN. NC can either float or be connected to GND.

Figure 2 shows recommended component placement for the MP3421.

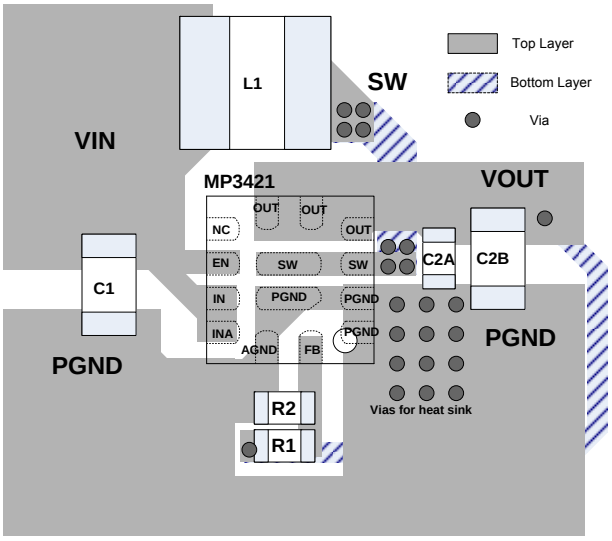


Figure 2: Layout Recommendation

Design Example

Table 2 shows a design example (using the application guidelines) for the following specifications:

Table 2: Design Example

V_{IN}	2.8V-4.2V
V_{OUT}	5V
I_{OUT}	0A-2.1A

See Figure 3 for the detailed application schematic. The typical application circuit for V_{OUT} = 5V is the basis for the typical performance waveforms. For details on additional device applications, please refer to the related evaluation board datasheets.

TYPICAL APPLICATION CIRCUITS

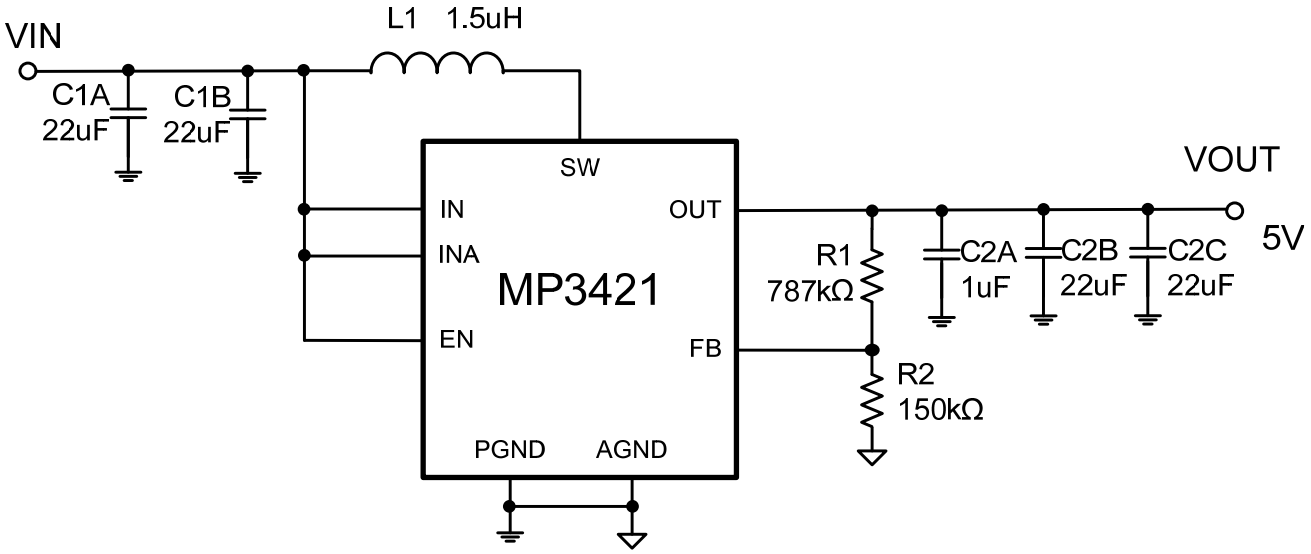
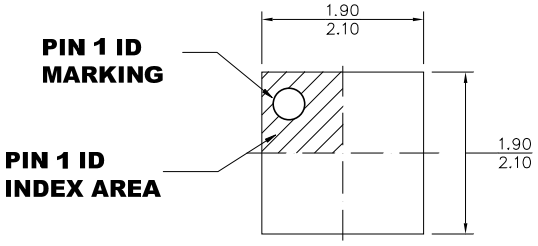


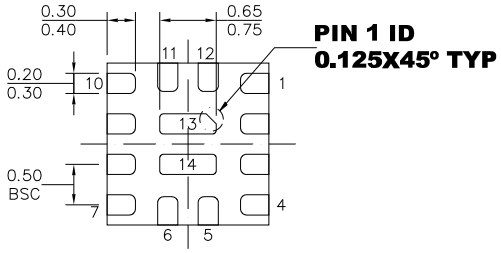
Figure 3: Typical Boost Application Circuit, V_{IN}=2.8V to 4.2V, V_{OUT}=5V, I_{OUT}=0A-2.1A

PACKAGE INFORMATION

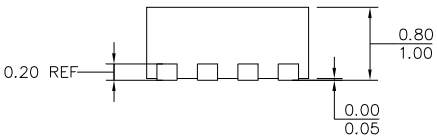
QFN-14 (2mmX2mm)



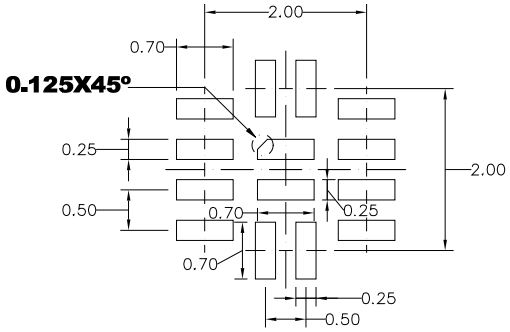
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.