# 32-Bit Microcontroller

## SAM L22G / L22J / L22N

## Introduction

The SAM L22 is a series of Ultra low-power segment LCD microcontrollers using the 32-bit ARM® Cortex®-M0+ processor, ranging from 48- to 100-pins with up to 256KB Flash and 32KB of SRAM and to drive up to 320 LCD segments. The SAM L22 devices operate at a maximum frequency of 32MHz and reach 2.46 CoreMark®/MHz. With sophisticated power management technologies the SAM L22 devices run down to 39µA/MHz (CPU running CoreMark) in active mode and down to 490nA in ultra low-power backup mode with RTC.

## Features

- Processor
  - ARM Cortex-M0+ CPU running at up to 32MHz
    - Single-cycle hardware multiplier
    - Micro Trace Buffer
    - Memory Protection Unit (MPU)
- Memories
  - 64/128/256KB in-system self-programmable Flash
  - 2/4/8KB Flash Read-While-Write section
  - 8/16/32KB SRAM Main Memory
- System
  - Power-on reset (POR) and programmable brown-out detection (BOD)
  - Internal and external clock options
  - External Interrupt Controller (EIC)
    - 16 external interrupts that can use any I/O-Pin
    - One non-maskable interrupt on one I/O-Pin
  - Two-pin Serial Wire Debug (SWD)
- Low Power
  - Idle, Standby, Backup, and Off sleep modes
  - SleepWalking peripherals
  - Battery backup support
  - Two runtime selectable power/performance levels
  - Embedded Buck/LDO regulator supporting on-the-fly selection
  - Active mode: <50µA/MHz
  - Standby with full retention, RTC and LCD = 3.47µA
    - 2.1µs wake-up time

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  - Standby with full retention and RTC: 1.87µA
    - 2.1µs wake-up time
  - Ultra low power Backup mode with RTC: 490nA
    - 90µs wake-up time

- Peripherals
  - Segment LCD controller
    - Up to 8 (4) common and 40 (44) segment terminals to drive 320 (176) segments
    - Static, ½, 1/3, ¼ bias
    - Internal charge pump able to generate VLCD higher than VDDIO
  - 16-channel Direct Memory Access Controller (DMAC)
  - 8-channel Event System
  - Up to four 16-bit Timer/Counters (TC), each configurable as:
    - 16-bit TC with two compare/capture channels
    - 8-bit TC with two compare/capture channels
    - 32-bit TC with two compare/capture channels, by using two TCs
  - One 24-bit Timer/Counters for Control (TCC), with extended functions:
    - Four compare channels with optional complementary output
    - Generation of synchronized pulse width modulation (PWM) pattern across port pins
    - Deterministic fault protection, fast decay and configurable dead-time between complementary output
    - Dithering that increase resolution with up to 5 bit and reduce quantization error
  - Frequency Meter
  - 32-bit Real Time Counter (RTC) with clock/calendar function
    - 8x32-bit Backup Register
    - Tamper Detection
  - Watchdog Timer (WDT)
  - CRC-32 generator
  - One full-speed (12Mbps) Universal Serial Bus (USB) 2.0 Device
    - Eight endpoints
    - Crystal less operation
  - Up to six Serial Communication Interfaces (SERCOM), each configurable as:
    - USART with full-duplex and single-wire half-duplex configuration
    - ISO7816
    - $I^2C$ up to 3.4MHz[1]
    - SPI
  - One AES encryption engine
  - One True Random Generator (TRNG)
  - One Configurable Custom Logic (CCL)
  - One 12-bit, 1MSPS Analog-to-Digital Converter (ADC) with up to 20 channels
    - Differential and single-ended input
    - Oversampling and decimation in hardware to support 13-, 14-, 15-, or 16-bit resolution
  - Two Analog Comparators (AC) with window compare function

[1] Max 1 high-speed mode and max 3 fast mode $I^2C$

  - Peripheral Touch Controller (PTC)
    - Up to 256-Channel capacitive touch sensing
      - Maximum Mutual-Cap up to 16x16 channels
      - Maximum Self-Cap up to 24 channels
    - Wake-up on touch in standby mode

- Oscillators
  - 32.768kHz crystal oscillator (XOSC32K)
  - 0.4-32MHz crystal oscillator (XOSC)
  - 32.768kHz ultra-low-power internal oscillator (OSCULP32K)
  - 16/12/8/4MHz high-accuracy internal oscillator (OSC16M)
  - 48MHz Digital Frequency Locked Loop (DFLL48M)
  - 96MHz Fractional Digital Phased Locked Loop (FDPLL96M)
- I/O
  - Up to 82 programmable I/O pins
  - Up to 52 segment LCD pins can be used as GPIO/GPI
  - Up to 5 wake-up pins with optional debouncing
  - Up to 5 tamper input pins
  - 1 tamper output pin
- Pin and code compatible with SAM D and SAM L Cortex-M0+ Families[2]
- Packages
  - 100-pin TQFP, UFBGA
  - 64-pin TQFP, QFN
  - 49-pin WLCSP
  - 48-pin TQFP, QFN
- Operating Voltage
  - 1.62V – 3.63V

[2] except the VLCD

# 1. Description

The SAM L22 is a series of Ultra low-power segment LCD microcontrollers using the 32-bit ARM® Cortex®-M0+ processor, ranging from 48- to 100-pins with up to 256KB Flash and 32KB of SRAM and can drive up to 320 LCD segments. The SAM L22 devices operate at a maximum frequency of 32MHz and reach 2.46 Coremark/MHz. They are designed for simple and intuitive migration with identical peripheral modules, hex compatible code, identical linear address map and pin compatible migration paths between all devices in the product series. All devices include intelligent and flexible peripherals, an Event System for inter-peripheral signaling, and support for capacitive touch button, slider and wheel user interfaces.

The SAM L22 devices provide the following features: Segment LCD (SLCD) controller with up to 48 selectable SLCD pins from max. 52 pins to drive up to 320 segments, all SLCD Pins can be used also as GPIOs (100-pin package: 8 of the SLCD pins can be used only as GP input), in-system programmable Flash, sixteen-channel direct memory access (DMA) controller, 8 channel Event System, programmable interrupt controller, up to 82 programmable I/O pins, 32-bit real-time clock and calendar, up to four 16-bit Timer/Counters (TC) and one 24-bit Timer/Counters for Control (TCC), where each TC can be configured to perform frequency and waveform generation, accurate program execution timing or input capture with time and frequency measurement of digital signals. The TCs can operate in 8- or 16-bit mode, selected TCs can be cascaded to form a 32-bit TC, and the TCC has extended functions optimized for motor, lighting and other control applications. The series provide one full-speed USB 2.0 device interface; up to six Serial Communication Modules (SERCOM) that each can be configured to act as an USART, UART, SPI, $I^2C$ up to 3.4MHz, SMBus, PMBus, and ISO7816 smart card interface; up to twenty channel 1Msps 12-bit ADC with optional oversampling and decimation supporting up to 16-bit resolution, two analog comparators with window mode, Peripheral Touch Controller supporting up to 256 buttons, sliders, wheels and proximity sensing; programmable Watchdog Timer, brown-out detector and power-on reset and two-pin Serial Wire Debug (SWD) program and debug interface.

All devices have accurate and low-power external and internal oscillators. All oscillators can be used as a source for the system clock. Different clock domains can be independently configured to run at different frequencies, enabling power saving by running each peripheral at its optimal clock frequency, and thus maintaining a high CPU frequency while reducing power consumption.

The SAM L22 devices have four software-selectable sleep modes, idle, standby, backup and off. In idle mode the CPU is stopped while all other functions can be kept running. In standby all clocks and functions are stopped expect those selected to continue running. In this mode all RAMs and logic contents are retained. The device supports SleepWalking. This feature allows the peripheral to wake up from sleep based on predefined conditions, and thus allows some internal operation like DMA transfer and/or the CPU to wake up only when needed, e.g. when a threshold is crossed or a result is ready. The Event System supports synchronous and asynchronous events, allowing peripherals to receive, react to and send events even in standby mode.

The SAM L22 devices have two software-selectable performance level (PL0 and PL2) allowing the user to scale the lowest core voltage level that will support the operating frequency.

The Flash program memory can be reprogrammed in-system through the SWD interface. The same interface can be used for nonintrusive on-chip debugging of application code. A boot loader running in the device can use any communication interface to download and upgrade the application program in the Flash memory.

The SAM L22 devices are supported with a full suite of program and system development tools, including C compilers, macro assemblers, program debugger/simulators, programmers and evaluation kits.

## 2. Configuration Summary

| | SAM L22N | SAM L22J | SAM L22G |
|---|---|---|---|
| Pins | 100 | 64 | 48 (QFN and TQFP)<br>49 (WLCSP) |
| General Purpose I/O-pins (GPIOs)(1) | 82 | 50 | 36 |
| Flash | 256/128/64KB | 256/128/64KB | 256/128/64KB |
| Flash RWW section | 8/4/2KB | 8/4/2KB | 8/4/2KB |
| System SRAM | 32/16/8KB | 32/16/8KB | 32/16/8KB |
| Segment LCD (SLCD) Pins(1) | 48 selectable from 52 | 31 | 23 |
| Timer Counter (TC) instances | 4 | 4 | 4 |
| Waveform output channels per TC instance | 2 | 2 | 2 |
| Timer Counter for Control (TCC) instances | 1 | 1 | 1 |
| Waveform output channels per TCC | 4 | 4 | 4 |
| DMA channels | 16 | 16 | 16 |
| USB interface | 1 | 1 | 1 |
| AES engine | 1 | 1 | 1 |
| Configurable Custom Logic (CCL) (LUTs) | 4 | 4 | 4 |
| True Random Generator (TRNG) | 1 | 1 | 1 |
| Serial Communication Interface (SERCOM) instances | 6 | 4(2) | 4(2) |
| Analog-to-Digital Converter (ADC) channels | 20 | 16 | 10 |
| Two Analog Comparators (AC) with number of external input channels | 4 | 4 | 2 |
| Tamper Input Pins | 5 | 3 | 2 |

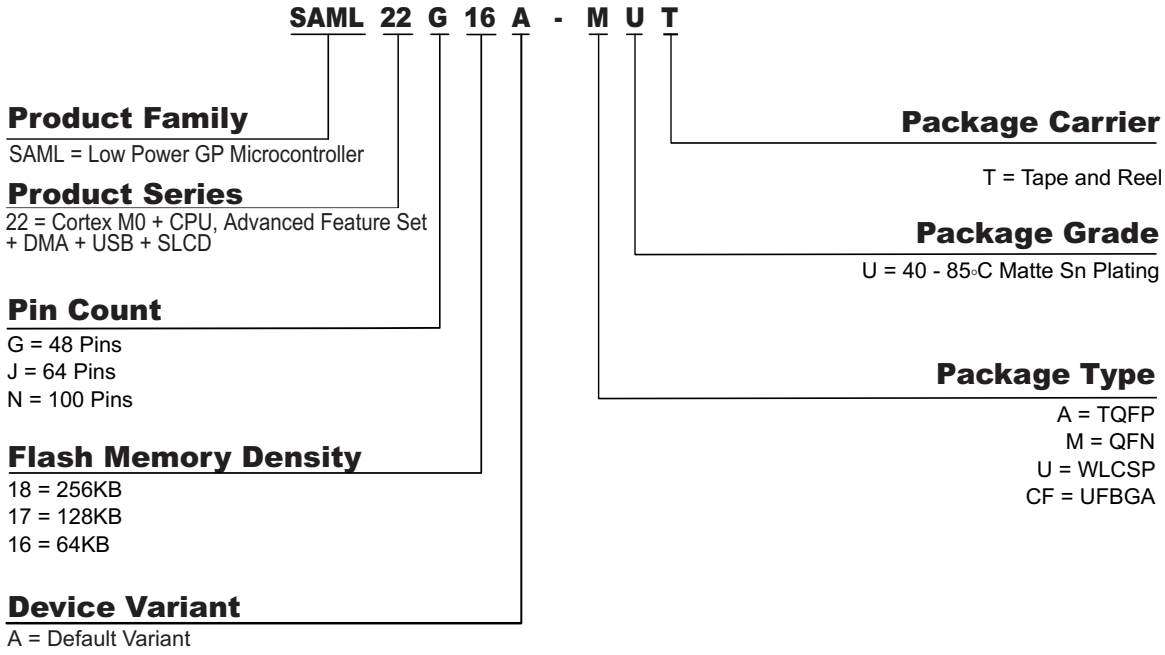
| | SAM L22N | SAM L22J | SAM L22G |
|---|---|---|---|
| Wake-up Pins with debouncing | 5 | 3 | 2 |
| Real-Time Counter (RTC) | Yes | Yes | Yes |
| RTC alarms | 1 | 1 | 1 |
| RTC compare values | One 32-bit value or<br>two 16-bit values | One 32-bit value or<br>two 16-bit values | One 32-bit value or<br>two 16-bit values |
| External Interrupt lines | 16 | 16 | 16 |
| Peripheral Touch Controller (PTC) channels (X- x Y-lines) for mutual capacitance(3) | 256 (16x16) | 182 (13x14) | 132 (11x12) |
| Peripheral Touch Controller (PTC) channels for self capacitance (Y-lines only)(4) | 24 | 19 | 15 |
| Maximum CPU frequency | 32MHz | 32MHz | 32MHz |
| Packages | TQFP<br>UFBGA | QFN<br>TQFP | QFN<br>TQFP<br>WLCSP |
| Oscillators | 32.768kHz crystal oscillator (XOSC32K)<br>0.4-32MHz crystal oscillator (XOSC)<br>32KHz ultra-low-power internal oscillator (OSCULP32K)<br>16/12/8/4MHz high-accuracy internal oscillator (OSC16M)<br>48MHz Digital Frequency Locked Loop (DFLL48M)<br>96MHz Fractional Digital Phased Locked Loop (FDPLL96M) | | |
| Event System channels | 8 | 8 | 8 |
| SW Debug Interface | Yes | Yes | Yes |
| Watchdog Timer (WDT) | Yes | Yes | Yes |

**Note:**

1. L22J, L22G: All SLCD Pins can be configured also as GPIOs. L22N: 44 SLCD Pins can be configured as GPIOs, 8 SLCD Pins can be used as GP input.
2. SAM L22N: SERCOM[5:0]. L22G, L22J: SERCOM[3:0].
3. The number of X- and Y-lines depends on the configuration of the device, as some I/O lines can be configured as either X-lines or Y-lines.

4. The number of Y-lines depends on the configuration of the device, as some I/O lines can be configured as either X-lines or Y-lines. The number given here is the maximum number of Y-lines that can be obtained.

# 3. Ordering Information




**Note:** The device variant (last letter of the ordering number) is independent of the die revision (DSU.DID.REVISION): The device variant denotes functional differences, whereas the die revision marks evolution of the die.

## 3.1 SAM L22N

**Table 3-1. SAM L22N Ordering Codes**

| Ordering Code | FLASH (bytes) | SRAM (bytes) | Package | Carrier Type |
|---|---|---|---|---|
| ATSAML22N16A-AUT | 64K | 8K | TQFP100 | Tape & Reel |
| ATSAML22N16A-CFUT | | | UFBGA100 | |
| ATSAML22N17A-AUT | 128K | 16K | TQFP100 | Tape & Reel |
| ATSAML22N17A-CFUT | | | UFBGA100 | |
| ATSAML22N18A-AUT | 256K | 32K | TQFP100 | Tape & Reel |
| ATSAML22N18A-CFUT | | | UFBGA100 | |

## 3.2 SAM L22J

**Table 3-2. SAM L22J Ordering Codes**

| Ordering Code | FLASH (bytes) | SRAM (bytes) | Package | Carrier Type |
|---|---|---|---|---|
| ATSAML22J16A-AUT | 64K | 8K | TQFP64 | Tape & Reel |
| ATSAML22J16A-MUT | | | QFN64 | |

| Ordering Code | FLASH (bytes) | SRAM (bytes) | Package | Carrier Type |
|---|---|---|---|---|
| ATSAML22J17A-AUT | 128K | 16K | TQFP64 | Tape & Reel |
| ATSAML22J17A-MUT | | | QFN64 | |
| ATSAML22J18A-AUT | 256K | 32K | TQFP64 | Tape & Reel |
| ATSAML22J18A-MUT | | | QFN64 | |

## 3.3 SAM L22G

**Table 3-3. SAM L22G Ordering Codes**

| Ordering Code | FLASH (bytes) | SRAM (bytes) | Package | Carrier Type |
|---|---|---|---|---|
| ATSAML22G16A-AUT | 64K | 8K | TQFP48 | Tape & Reel |
| ATSAML22G16A-MUT | | | QFN48 | |
| ATSAML22G17A-AUT | 128K | 16K | TQFP48 | Tape & Reel |
| ATSAML22G17A-MUT | | | QFN48 | |
| ATSAML22G17A-UUT | | | WLCSP49 | |
| ATSAML22G18A-AUT | 256K | 32K | TQFP48 | Tape & Reel |
| ATSAML22G18A-MUT | | | QFN48 | |
| ATSAML22G18A-UUT | | | WLCSP49 | |

## 3.4 Device Identification

The DSU - Device Service Unit peripheral provides the Device Selection bits in the Device Identification register (DID.DEVSEL) in order to identify the device by software. The SAM L22 variants have a reset value of DID=0x10820xxx, with the last digits identifying the variant:

**Table 3-4. SAM L22 Device Identification Values**

| DSU DID.DEVSEL | Device |
|---|---|
| 0x0 | L22N18 |
| 0x1 | L22N17 |
| 0x2 | L22N16 |
| 0x3-0x4 | Reserved |
| 0x5 | L22J18 |
| 0x6 | L22J17 |
| 0x7 | L22J16 |
| 0x8-0x9 | Reserved |
| 0xA | L22G18 |
| 0xB | L22G17 |