SiT5156

PRELIMINARY

1 to 60 MHz, ±0.5 ppm Elite Platform™ Super-TCXO

Description

The SiT5156 is a ±0.5 to ±2.5 ppm MEMS Super-TCXO engineered for best dynamic performance. It is ideal for high reliability telecom, wireless and networking, industrial, precision GNSS and audio/video applications.

By leveraging SiTime's unique DualMEMS™ temperature sensing and TurboCompensation™ technology, the SiT5156 delivers the most stable timing in the presence of environmental stressors – air flow, temperature perturbation, vibration, shock and electromagnetic interference (EMI). This device also integrates multiple on-chip regulators, providing power supply noise filtering and eliminating the need for a dedicated external LDO.

The SiT5156 offers three device configurations that can be ordered with the associated Ordering Codes:

1) TCXO with non-pullable output frequency
2) VCTCXO allowing voltage control of output frequency
3) DCTCXO enabling digital control of the output frequency through the I^2C interface

SiT5156 can be factory-programmed to any combination of frequency, stability, voltage, and pull range. This programmability enables designers to optimize the clock configuration while eliminating the long lead time and customization cost associated with quartz TCXOs where each frequency is custom built.

Refer to Manufacturing Guideline for proper reflow profile and PCB cleaning recommendations to ensure best performance.

Features

- Any frequency between 1 MHz and 60 MHz in 1 Hz steps
- Excellent dynamic stability under airflow and rapid temperature change
  - ±500 ppb over-temperature stability
  - ±15 ppb/°C frequency slope (ΔF/ΔT)
  - 3e-11 ADEV at 10 second averaging time
- -40°C to +105°C operating temperature
- No activity dips or micro jumps
- Resistant to shock, vibration and board bending
- Up to ±3200 ppm pull range (VCTCXO or DCTCXO)
- Digital frequency pulling (DCTCXO) via I^2C
  - Digital control of output frequency and pull range
  - Frequency pull resolution as low as 5 ppt (0.005 ppb)
- 2.5V, 2.8V, 3.0V and 3.3V supply voltage
- On-chip regulators, eliminating the need for the external LDO
- LVCMOS or clipped sinewave output
- RoHS and REACH compliant, Pb-free, Halogen-free and Antimony-free

Applications

- Precision GNSS
- Microwave backhaul
- Network switches and routers
- Professional audio and video equipment
- Storage and servers
- Test and measurement

Block Diagram

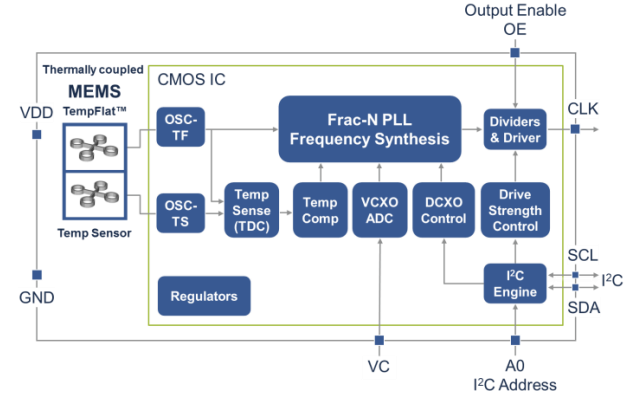

Figure 1. SiT5156 Block Diagram

5.0 x 3.2 mm Package Pinout

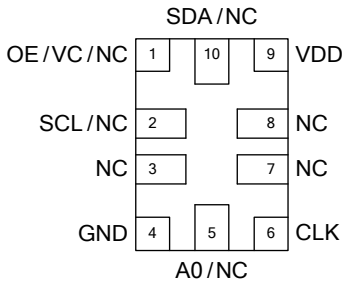

Figure 2. Pin Assignments (Top view)
(Refer to Table 9 for Pin Descriptions)

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Electrical Characteristics

All Min and Max limits are specified over temperature and rated operating voltage with 15 pF output load unless otherwise stated. Typical values are at 25°C and 3.3V Vdd

Table 1. Output Characteristics

Parameters	Symbol	Min.	Typ.	Max.	Unit	Condition
Frequency Coverage						
Output Frequency Range	F	1	–	60	MHz	LVCMOS output
		1	–	50	MHz	Clipped sinewave output
LVCMOS Output Characteristics						
Duty Cycle	DC	45	–	55	%	
Rise/Fall Time	Tr, Tf	–	1	–	ns	10% - 90% Vdd
Output Voltage High	VOH	90%	–	–	Vdd	I_{OH} = -6 mA, (Vdd = 3.3 V, 3.0 V, 2.8 V, 2.5 V)
Output Voltage Low	VOL	–	–	10%	Vdd	I_{OL} = 6 mA, (Vdd = 3.3 V, 3.0 V, 2.8 V, 2.5 V)
Clipped Sinewave Output Characteristics						
Output Voltage Level	V_out	0.8	–	1.2	V	Measured peak-to-peak swing at any Vdd
Frequency Stability - Stratum 3 Grade						
Frequency Stability over Temperature	F_stab	-0.5	–	+0.5	ppm	Referenced to (fmax + fmin)/2 over the specified temperature range See "Ordering Information" for frequency stability ordering codes (K, A, D)
		-1.0	–	+1.0	ppm	
		-2.5	–	+2.5	Ppm	
Frequency vs. Temperature Slope	ΔF/ΔT	–	±15	–	ppb/°C	F_stab = ±0.5 ppm
		–	±25	–	ppb/°C	F_stab = ±1 ppm
		–	±60	–	ppb/°C	F_stab = ±2.5 ppm
Dynamic Frequency Change during Temperature Ramp	F_dynamic	–	±0.13	–	ppb/s	F_stab = ±0.5 ppm , 0.5°C/min temperature ramp rate
		–	±0.21	–	ppb/s	F_stab = ±1.0 ppm , 0.5°C/min temperature ramp rate
		–	±0.5	–	ppb/s	F_stab = ±2.5 ppm , 0.5°C/min temperature ramp rate
Initial Tolerance	F_init	-1	–	+1	ppm	Initial frequency at 25°C inclusive of solder-down shift at 48 hours after 2 reflows
Supply Voltage Sensitivity	F_vdd	–	±20	–	ppb	Vdd ±5%
Output Load Sensitivity	F_load	–	±10	–	ppb	LVCMOS output, 15 pF ±10%
		–	±10	–	ppb	Clipped sinewave output, 10kΩ, 10 pF ±10%
First Year Aging	F_1y	–	±1	–	ppm	At 25°C
Start-up Characteristics						
Start-up Time	T_start	–	5	–	ms	Time to first pulse, measured from the time Vdd reaches 90% of its final value
First Pulse Accuracy	T_stability	–	10	–	ms	Time to first accurate pulse within rated stability, measured from the time Vdd reaches 90% of its final value

Table 2. DC Characteristics

Parameters	Symbol	Min.	Typ.	Max.	Unit	Condition
Supply Voltage						
Supply Voltage	Vdd	2.25	2.5	2.75	V	Contact SiTime for 2.25V to 3.63V continuous supply voltage support
		2.52	2.8	3.08	V	
		2.7	3.0	3.3	V	
		2.97	3.3	3.63	V	
Current Consumption						
Current Consumption	IDD	–	40.5	–	mA	F = 19.2 MHz, No Load
OE Disable Current	I_od	–	40	–	mA	OE = GND, output is weakly pulled down
Temperature Range						
Operating Temperature Range	T_use	-20	–	+70	°C	Extended Commercial
		-40	–	+85	°C	Industrial. Contact SiTime for 105 °C support
		-40	–	+105	°C	Extended Industrial

Table 3. Input Characteristics

Parameters	Symbol	Min.	Typ.	Max.	Unit	Condition
Input Characteristics – OE Pin						
Input Impedance	Z_in	–	100	–	kΩ	Internal pull up to Vdd
Input High Voltage	VIH	70	–	–	%	
Input Low Voltage	VIL	–	–	30	%	
Frequency Tuning Range – Voltage Control or I^2C mode						
Pull Range	PR	±6.25, ±10, ±12.5, ±25, ±50, ±80, ±100, ±125, ±150, ±200, ±400, ±600, ±800, ±1200, ±1600, ±3200			ppm	
Voltage Control Characteristics						
Upper Control Voltage	VC_U	90%	–	–	Vdd	
Lower Control Voltage	VC_L	–	–	10%	Vdd	
Control Voltage Input Impedance	VC_z	10	–	–	MΩ	
Control Voltage Input Bandwidth	VC_c	–	10	–	kHz	Contact SiTime for other input bandwidth options
Frequency Change Polarity		Positive				
Pull Range Linearity		–	0.5	–	%	
I^2C Interface Characteristics, 1 MHz, 200 Ohm, 550 pF (Max I^2C Bus Load)						
Input Voltage Low	VIL	–	–	0.3	V	
Input Voltage High	VIH	0.7	–	–	V	
Output Voltage Low	VOL	–	–	0.4	V	
Output Current High	IOL	21	–	–	mA	
Leakage in high impedance mode	I_leak	5.5	–	24	µA	0.1 Vdd< VOUT < 0.9 Vdd
Input Hysteresis	V_hys	0.2	–	0.4	V	Vdd = 3.3V
		0.2	–	0.3	V	Vdd = 2.5V
Input Capacitance	C_in	–	–	3	pF	
Rise Time	Tr	–	–	120	ns	
Fall Time	Tf	30	–	60	ns	Vdd = 3.3V, 30% to 70%
		40	–	75	ns	Vdd = 2.5V, 30% to 70%

Table 4. Jitter & Phase Noise

Parameters	Symbol	Min.	Typ.	Max.	Unit	Condition
Jitter						
RMS Phase Jitter (random)	T_phj	–	0.35	–	ps	f = 10 MHz, Integration bandwidth = 12 kHz to 5 MHz
		–	0.33	–	ps	f = 50 MHz, Integration bandwidth = 12 kHz to 20 MHz
Spurs		–	-104	–	dBc	f = 10 MHz, 12 kHz to 5 MHz offsets
RMS Period Jitter	T_jitt	–	2	–	ps	f = 10 MHz per JESD65 standard
Peak Cycle-to-Cycle Jitter	T_jitt_cc	–	10	–	ps	f = 10 MHz per JESD65 standard
Phase Noise						
1 Hz offset		–	-70	–	dBc/Hz	f = 10 MHz, TCXO and DCTCXO modes, and VCTCXO mode with ±6.25 ppm pull range
10 Hz offset		–	-100	–	dBc/Hz	
100 Hz offset		–	-130	–	dBc/Hz	
1 kHz offset		–	-145	–	dBc/Hz	
10 kHz offset		–	-152	–	dBc/Hz	
100 kHz offset		–	-155	–	dBc/Hz	
1 MHz offset		–	-162	–	dBc/Hz	
5 MHz offset		–	-165	–	dBc/Hz	

Table 5. Absolute Maximum Limits

Attempted operation outside the absolute maximum ratings may cause permanent damage to the part.
Actual performance of the IC is only guaranteed within the operational specifications, not at absolute maximum ratings.

Parameter	Test Conditions	Value	Unit
Storage Temperature		-65 to 125	°C
Continuous Power Supply Voltage Range (Vdd)		-0.5 to 4	V
Human Body Model (HBM) ESD Protection	JESD22-A114	–	V
Soldering Temperature (follow standard Pb-free soldering guidelines)		260	°C
Junction Temperature[1]		130	°C

Note:

1. Exceeding this temperature for an extended period of time may damage the device.

Table 6. Thermal Considerations[2]

Package	θJA (°C/W)	θJC, Bottom (°C/W)
Ceramic 5.0 x 3.2 mm	54	15

Note:

2. Measured in still air.

Table 7. Environmental Compliance

Parameter	Test Conditions	Value	Unit
Mechanical Shock Resistance	**MIL-STD-883F, Method 2002**	**20,000**	*g*
Mechanical Vibration Resistance	**MIL-STD-883F, Method 2007**	**70**	*g*
Temperature Cycle	**JESD22, Method A104**	–	–
Solderability	**MIL-STD-883F, Method 2003**	–	–
Moisture Sensitivity Level	**MSL1 @260°C**	–	–

Device Configurations and Pin-outs

Table 8. Device Configurations

Configuration	Pin 1	Pin 5	I²C Function	I²C Programmable Parameters
TCXO	OE/NC	NC	No	N/A
VCTCXO	VC	NC	No	N/A
DCTCXO	OE/NC	A0/NC	Yes	Frequency Pull Range, Frequency Pull Value, Output Enable control

Pin-out Top Views

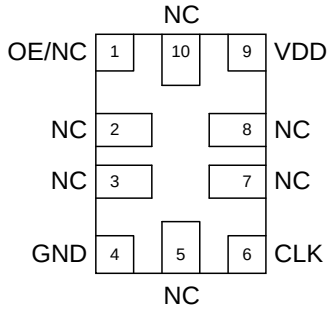


Figure 3. TCXO

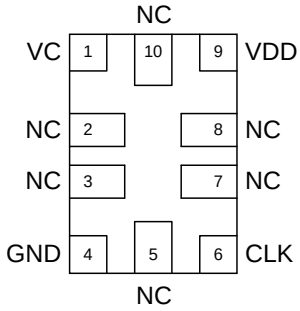


Figure 4. VCTCXO

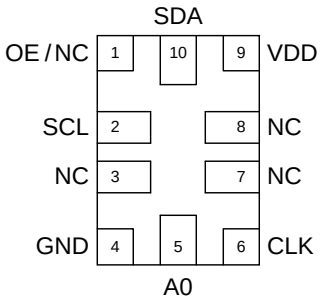


Figure 5. DCTCXO

Table 9. Pin Description

Pin	Symbol	I/O	Internal Pull-up/Pull Down Resistor	Function
1	OE/NC/VC	OE – Input	100 kΩ Pull-Up	H[3]: specified frequency output L: output is high impedance. Only output driver is disabled
		NC – No Connect	-	H or L or Open: No effect on output frequency or other device functions
		VC – Input	-	Control Voltage in VCTCXO Mode
2	SCL/NC	SCL - Input	200 kΩ Pull-Up	I²C Serial Clock Input for DCTCXO Option. NC for TCXO and VCTCXO Options.
		NC – No Connect	-	H or L or Open: No effect on output frequency or other device functions
3	NC	No Connect	-	H or L or Open: No effect on output frequency or other device functions
4	GND	Power	-	Connect to ground
5	A0/NC	A0 – Input	100 kΩ Pull-Up	Device I²C address when the address selection mode is via the A0 pin. This pin is NC when the I²C device address is specified in the ordering code. A0 Logic Level I²C Address 0 1100010 1 1101010
		NC – No Connect	-	H or L or Open: No effect on output frequency or other device functions
6	CLK	Output	-	LVCMOS or clipped sinewave oscillator output
7	NC	No Connect	-	H or L or Open: No effect on output frequency or other device functions
8	NC	No Connect	-	H or L or Open: No effect on output frequency or other device functions
9	VDD	Power	-	Connect to VDD[4]
10	SDA/NC	SDA – Input/Output	200 kΩ Pull-Up	I²C Serial Data for DCTCXO Option. NC for TCXO and VCTCXO Options.
		NC - No Connect	-	H or L or Open: No effect on output frequency or other device functions

Notes:

3. In OE mode, a pull-up resistor of 10 kΩ or less is recommended if pin 1 is not externally driven. If pin 1 needs to be left floating, use the NC option.
4. 0.1 µF capacitor in parallel with a 10 µF capacitor are required between Vdd and GND.

Test Circuit Diagrams for LVCMOS and Clipped Sinewave Outputs

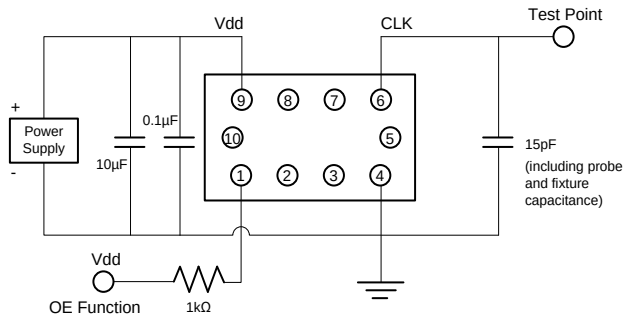


Figure 6. LVCMOS Test Circuit (OE Function)

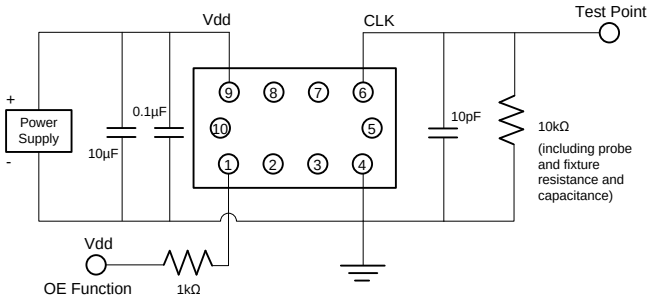


Figure 7. Clipped Sinewave Test Circuit (OE Function)

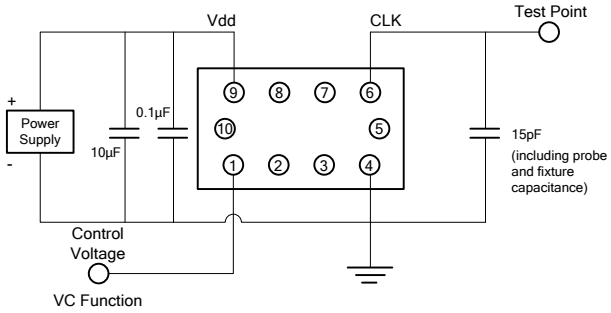


Figure 8. LVCMOS Test Circuit (VC Function)

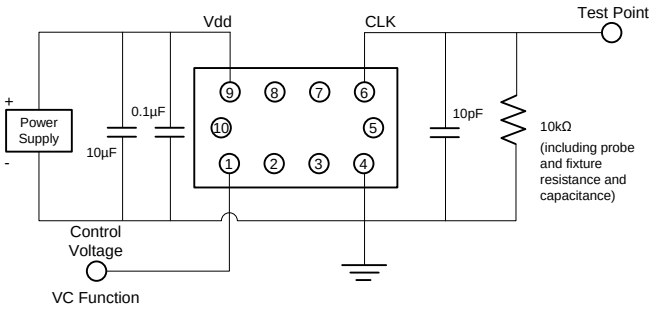


Figure 9. Clipped Sinewave Test Circuit (VC Function)

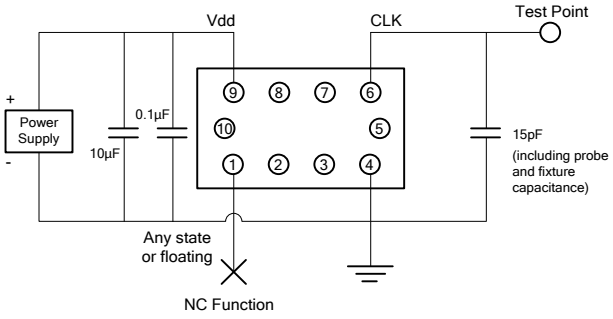


Figure 10. LVCMOS Test Circuit (NC Function)

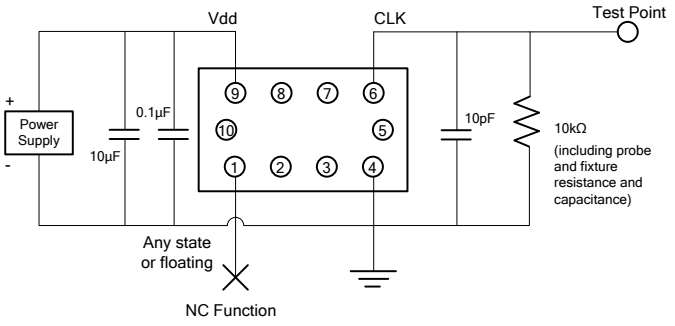


Figure 11. Clipped Sinewave Test Circuit (NC Function)

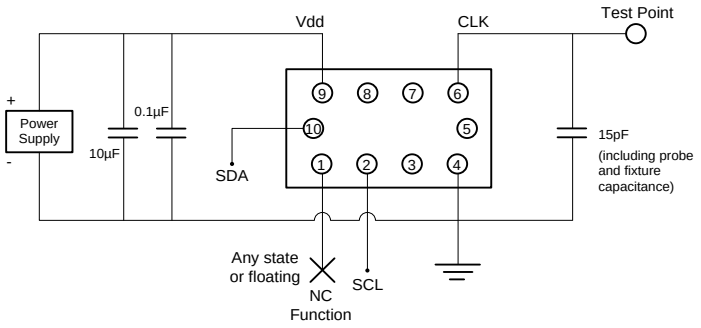


Figure 12. LVCMOS Test Circuit (I²C Control)

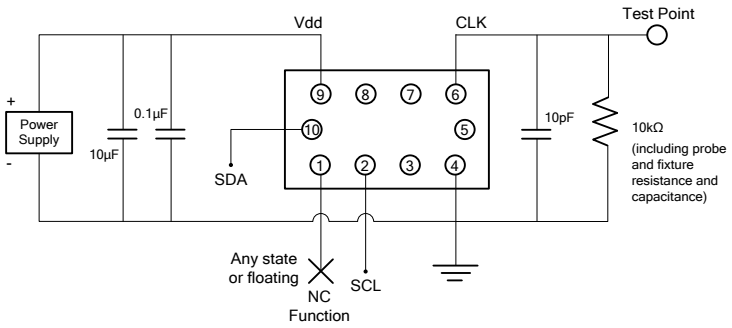


Figure 13. Clipped Sinewave Test Circuit (I²C Control)

Waveforms[5]

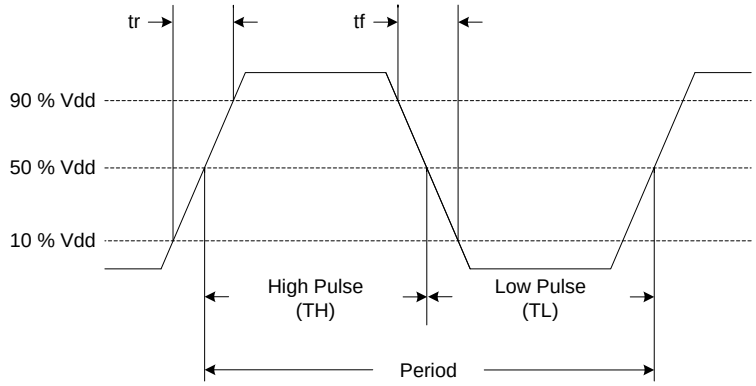


Figure 14. LVCMOS Waveform Diagram

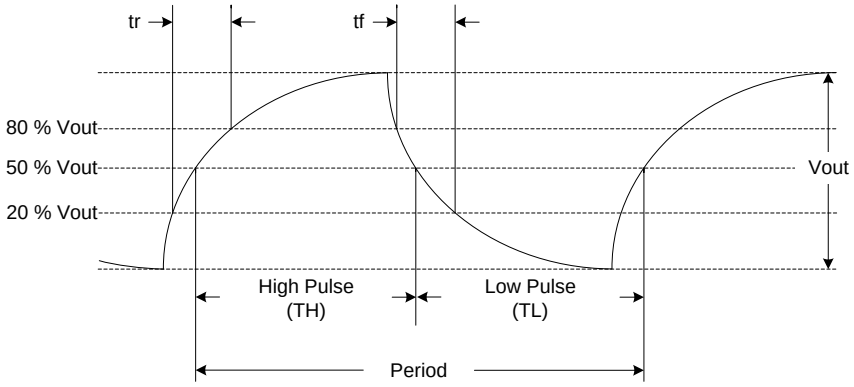
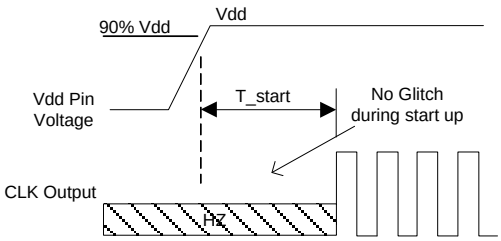


Figure 15. Clipped Sinewave Waveform Diagram

Notes

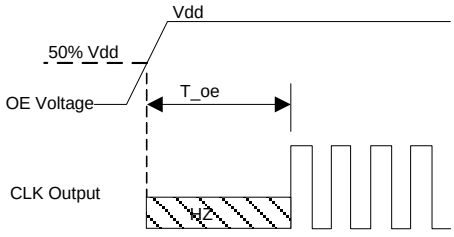
5. Duty Cycle is computed as Duty Cycle = TH/Period.

Timing Diagrams



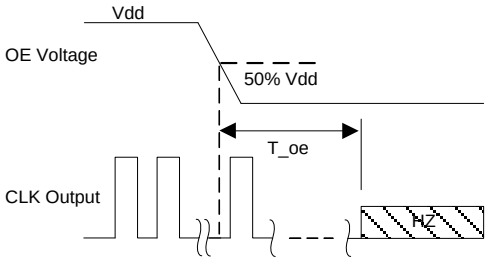
T_start: Time to start from power-off

Figure 16. Startup Timing (OE Mode)



T_oe: Time to re-enable the clock output

Figure 17. OE Enable Timing (OE Mode Only)



T_oe: Time to put the output in High Z mode

Figure 18. OE Disable Timing (OE Mode Only)

Architecture Overview

Based on SiTime's innovative Elite Platform™, the SiT5156 delivers exceptional dynamic performance, i.e. resilience to environmental stressors such as shock, vibration and fast temperature transients. Underpinning the Elite platform are SiTime's unique DualMEMS™ temperature sensing architecture and TurboCompensation™ technology.

DualMEMS is a noiseless temperature sensing scheme. It consists of two MEMS resonators fabricated on the same die substrate. The TempFlat™ resonator is designed with a flat frequency characteristic over temperature whereas the temperature sensing resonator is by design sensitive to temperature changes. The ratio of frequencies between these two resonators provides an accurate reading of the resonator temperature with 30 µK resolution.

By placing the two MEMS resonators on the same die, this temperature sensing scheme eliminates the thermal lag and gradients between the resonator and the temperature sensor, an inherent weakness of legacy quartz TCXOs.

The DualMEMS temperature sensor is then combined with a state-of-the-art temperature compensation circuit in the CMOS IC. The TurboCompensation design, with >100 Hz compensation bandwidth, achieves dynamic frequency stability that is far superior to any quartz TCXO. The 7th order compensation polynomial enables additional optimization of frequency stability and frequency slope over temperature within any specific temperature range of choice for a given system design.

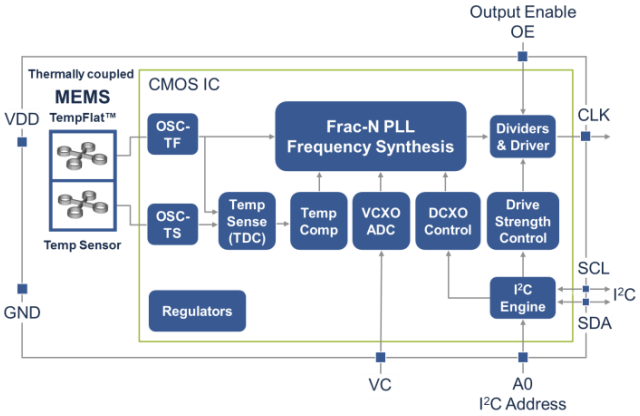


Figure 19. Elite Architecture

The Elite platform also incorporates a high resolution, low noise frequency synthesizer along with the industry standard I²C bus. This unique combination enables system designers to digitally control the output frequency in steps as low as 5 ppt (parts per trillion) and over a wide range up to ±3200 ppm.

For more information regarding the Elite platform and its benefits please visit:

- SiTime's breakthroughs section
- TechPaper: DualMEMS Temperature Sensing Technology
- TechPaper: DualMEMS Resonator TDC

Functional Overview

The SiT5156 is designed for maximum flexibility with an array of factory programmable options, enabling system designers to configure this precision device for optimal performance in a given application.

Frequency Stability

The SiT5156 comes in three factory-trimmed stability grades, each of which is associated with a specific ΔF/ΔT. The lower ΔF/ΔT ensures better immunity to air flow and rapid temperature changes.

Table 10. Stability Grades vs. Ordering Codes

Frequency Stability Over Temperature	Frequency Slope (ΔF/ΔT)	Ordering Code
±0.5 ppm	±15 ppb/°C	K
±1 ppm	±25 ppb/°C	A
±2.5 ppm	±60 ppb/°C	D

Output frequency and format

The SiT5156 can be programmable for any output frequency from 1 MHz to 60 MHz in steps of 1 Hz without sacrificing lead time or incurring upfront customization cost typically associated with custom frequency quartz TCXO.

The device supports both LVCMOS and clipped sinewave output. Ordering codes for the output format are shown below:

Table 11. Output Formats vs. Ordering Codes

Output Format	Ordering Code
LVCMOS	"-"
Clipped Sinewave	"C"

Output Frequency Tuning

In addition to the non-pullable TCXO, the SiT5156 can also support output frequency tuning through either an analog control voltage (VCTCXO) or I²C (DCTCXO).

Sixteen pull range options from ±6.25 ppm to ±3200 ppm are supported in both VCTCXO and DCTCXO configurations. The DCTCXO is recommended to ensure the best phase noise for pull range of ±12.5 ppm or above. It also eliminates any sensitivity to the voltage control line noise in a typical VCTCXO implementation, therefore simplifying board level design and layout.

In the DCTCXO configuration, a user can either specify a desired I²C bus address via the appropriate order code, or choose a pre-configured address with pull up/pull down resistors on the A0 pin (pin 5). The pull range can also be reprogrammed via I²C to any supported pull range option.

Pin 1 Configuration (OE, VC, or NC)

Pin 1 of the SiT5156 can be factory-programmed to support three modes: Output Enable (OE), Voltage Control (VC) or No Connect (NC).

Table 12. Pin Configuration Options

Pin 1 Configuration	Operating Mode	Output
OE	TCXO	Active or High-Z
NC	TCXO/DCTCXO	Active
VC	VCTCXO	Active

When pin 1 configured as OE pin, the device output is guaranteed to operate in one of the following two states:

- At the frequency specified in the part number when Pin 1 is pulled to logic high
- In Hi-Z mode with weak pull down when pin 1 is pulled to logic low.
- No Connect (NC) mode

When pin 1 is NC, the device is guaranteed to output the frequency specified in the part number at all times, regardless of the logic level on pin 1.

In the VCTCXO configuration, the user can fine-tune the output frequency from the nominal frequency specified in the part number by varying pin 1 voltage. The guaranteed allowable variation of the output frequency is specified as pull range. A VCTCXO part number must contain a valid pull range ordering code.

Device Configurations and Design Considerations

The SiT5156 supports 3 device configurations – TCXO, VCTCXO and DCTCXO. The TCXO and VCTCXO options are directly compatible with the quartz TCXO and VCTCXO. The DCTCXO configuration provides performance enhancement by eliminating VCTCXO's sensitivity to control voltage noise with an I^2C digital interface for frequency tuning.

TCXO Configuration

In the TCXO configuration, the device generates a fixed frequency output. The frequency is specified by the user in the frequency field of the device ordering code and factory-programmed. Other factory programmable options include supply voltage, output types (LVCMOS or clipped sinewave) and pin 1 functionality (OE or NC)

Refer to the Ordering Information section at the end of the datasheet for a list of all ordering options.

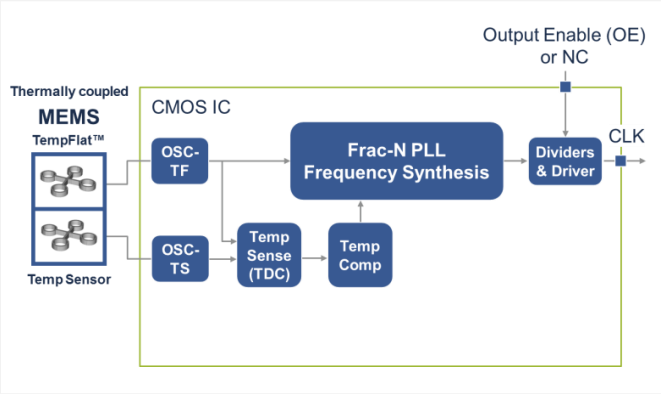


Figure 20. Block Diagram - TCXO

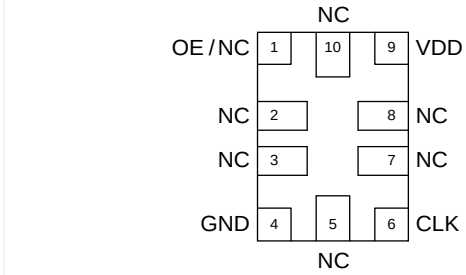


Figure 21. Top View – TCXO

VCTCXO Configuration

VCTCXO is a frequency control device whose output frequency is an approximately linear function of control voltage applied to the voltage control pin, VCTCXOs have a number of use cases including the VCO portion of a jitter attenuation/jitter cleaner PLL Loop.

The SiT5156 VCTCXO has several inherent advantages over quartz VCTCXOs:

1) <0.5% frequency pull linearity vs 5% to 10% typical of quartz VCTCXOs.
2) Widest pull range with 16 options: ±6.25ppm, ±10 ppm, ±12.5 ppm, ±25 ppm, ±50 ppm, ±80 ppm, ±100 ppm, ±125 ppm, ±150 ppm, ±200 ppm, ±400 ppm, ±600 ppm, ±800 ppm, ±1200 ppm, ±1600 ppm, ±3200 ppm vs. ±5 ppm pull range from quartz VCTCXOs.

The SiT5156 achieves 10x better linearity and more pull range options via the fractional feedback divider of the PLL rather than pulling the resonator. Quartz based VCTCXOs by contrast changes output frequency by varying the capacitive load of the crystal resonator with varactor diodes, resulting in poor linearity and limited pull ranges.

Note that the output frequency of the VCTCXO is proportional to the analog control voltage applied to pin 1. Because this control signal is analog and directly controls the output frequency, care must be taken to minimize noise on this pin.

The nominal output frequency is factory programmed per the customer's request to 6 digits of precision and is defined as the output frequency when the control voltage equals Vdd/2. The maximum output frequency variation from this nominal value is set by the pull range which is also factory programmed to the customer's desired value and specified by the ordering code. The Ordering Information section shows all the ordering options and associated ordering codes.

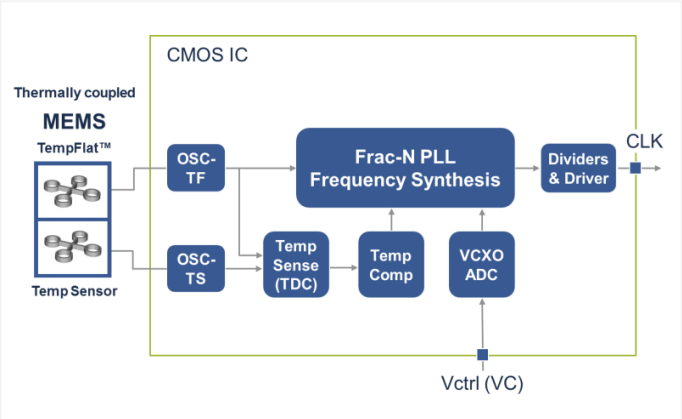


Figure 22. Block Diagram - VCTCXO

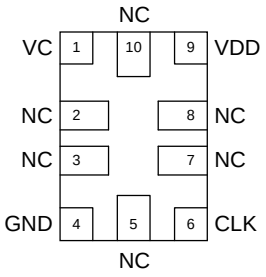


Figure 23. Top View - VCTCXO

Linearity

In any VCTCXO, there will be some deviation of the FV characteristic from an ideal straight line. Linearity is the ratio of this maximum deviation to the total pull range, expressed as a percentage. Figure 24 below shows the typical pull linearity of a SiTime VCTCXO. The linearity is very high relative to most quartz offerings because the frequency pulling is achieved with the PLL rather than varactor diodes used in quartz and is 0.5% maximum.

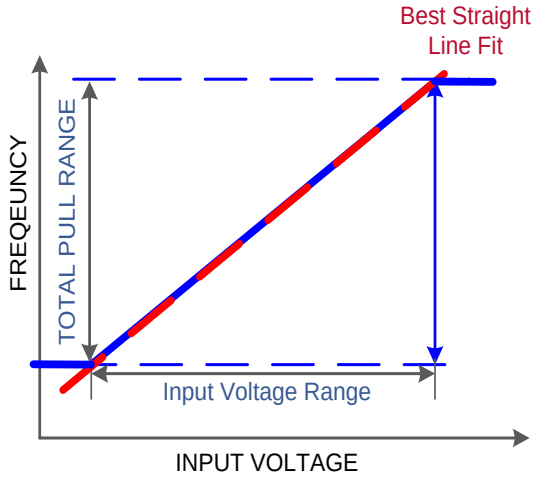


Figure 24. Typical SiTime VCTCXO Linearity

FV Characteristic Slope K_V

The slope of the FV characteristic is a critical design parameter in many low bandwidth PLL applications. The slope is the derivative of the FV characteristic – the deviation of frequency divided by the control voltage change needed to produce that frequency deviation, over a small voltage span, as shown below:

$$K_V = \frac{\Delta f_{out}}{\Delta V_{in}}$$

It is typically expressed in kHz/volt, MHz/volt, ppm/volt, or similar units. Slope is usually called "K_V" based on terminology used in PLL designs.

The extreme linear characteristic of the SiTime SiT5156 VCTCXO family means that there is very little K_V variation across the whole input voltage range (typically <1%), significantly reducing the design burden on the PLL designer. Figure 25 below illustrates the typical K_V variation.

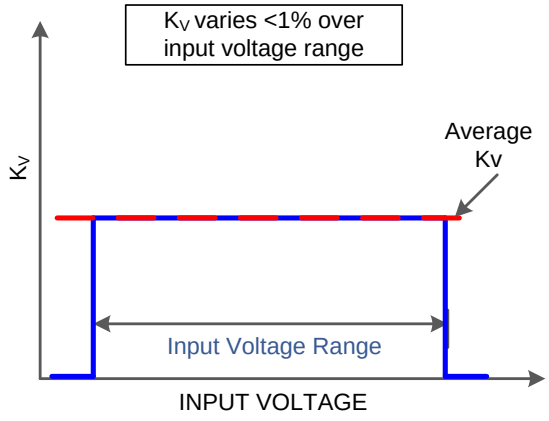


Figure 25. Typical SiTime K_V Variation

Control Voltage Bandwidth

Control voltage bandwidth, sometimes called "modulation rate" or "modulation bandwidth", is the rate at which the output frequency can track an input voltage change. The ratio of the output frequency variation to the input voltage variation, previously denoted by K_V, has a low-pass characteristic in most VCTCXOs. The modulation rate is defined as the modulation rate for which the K_V is reduced by 3 dB relative to K_V for DC inputs swept in the same voltage range.

For example, a part with a ±25 ppm pull range and a 0-3V control voltage can be regarded as having an average K_V of 16.67 ppm/V (50ppm/3V = 16.67 ppm/V). Applying an input of 1.5V DC ± 0.5V (1.0 V to 2.0V) causes an output frequency change of 16.67 ppm (±8.33 ppm). If the control voltage bandwidth is specified as 8 kHz, the peak-to-peak value of the output frequency change will be reduced to 16.67 ppm/√2 or 11.8 ppm, as the frequency of the control voltage change is increased to 8 kHz.

Pull Range, Absolute Pull Range

Pull range (PR) is the amount of frequency deviation that will result from changing the control voltage over its maximum range under nominal conditions.

Absolute pull range (APR) is the guaranteed controllable frequency range over all environmental and aging conditions. Effectively, it is the amount of pull range remaining after taking into account frequency stability tolerances over variables such as temperature, power supply voltage, and aging, i.e.:

$$APR = PR - F_{stability} - F_{aging}$$

where $F_{stability}$ is the device frequency stability due to initial tolerance and variations on temperature, power supply, and load.

Figure 26 shows a typical SiTime VCTCXO FV characteristic. The FV characteristic varies with conditions, so that the frequency output at a given input voltage can vary by as much as the specified frequency stability of the VCTCXO. For such VCTCXOs, the frequency stability and APR are independent of each other. This allows very wide range of pull options without compromising frequency stability.

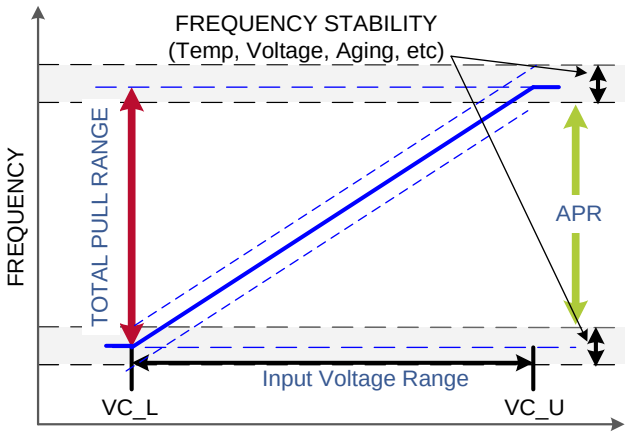


Figure 26. Typical SiTime VCTCXO FV Characteristic

The upper and lower control voltages are the specified limits of the input voltage range as shown on Figure 26 above. Applying voltages beyond the upper and lower voltages do not result in noticeable changes of output frequency. In other words, the FV characteristic of the VCTCXO saturates beyond these voltages. Figures 1 and 2 show these voltages as Lower Control Voltage (VC_L) and Upper Control Voltage (VC_U).

Table 13 below shows the pull range and corresponding APR values for each of the frequency vs. temperature ordering options for both the VCTCXO and the DCTCXO which will be described in the next section.

Table 13. VCTCXO, DCXO Pull Range, APR Options[6]

Pull Range Ordering Code	Device Option(s)	Pull Range ppm	APR ppm ±0.5 ppm option	APR ppm ±1.0 ppm option	APR ppm ±2.5 ppm option
T	VCTCXO, DCTCXO	±6.25	±2.75	±2.25	±0.75
R	VCTCXO, DCTCXO	±10	±6.5	±6.0	±4.5
Q	VCTCXO, DCTCXO	±12.5	±9.0	±8.5	±7.0
M	VCTCXO, DCTCXO	±25	±21.5	±21.0	±19.5
B	VCTCXO, DCTCXO	±50	±46.5	±46.0	±44.5
C	VCTCXO, DCTCXO	±80	±76.5	±76.0	±74.5
E	VCTCXO, DCTCXO	±100	±96.5	±96.0	±94.5
F	VCTCXO, DCTCXO	±125	±121.5	±121.0	±119.5
G	VCTCXO, DCTCXO	±150	±146.5	±146.0	±144.5
H	VCTCXO, DCTCXO	±200	±196.5	±196.0	±194.5
X	VCTCXO, DCTCXO	±400	±396.5	±396.0	±394.5
L	VCTCXO, DCTCXO	±600	±596.5	±596.0	±594.5
Y	VCTCXO, DCTCXO	±800	±796.5	±796.0	±794.5
S	VCTCXO, DCTCXO	±1200	±1196.5	±1196.0	±1194.5
Z	VCTCXO, DCTCXO	±1600	±1596.5	±1596.0	±1594.5
U	VCTCXO, DCTCXO	±3200	±3196.5	±3196.0	±3194.5

Notes:

6. APR includes ±1 ppm solder down shift, frequency stability vs. temperature (±0.5 ppm, ±1.0 ppm, ±2.5 ppm) and 20-year aging (±2 ppm)

DCTCXO Configuration

The DCTCXO option offers digital control of the output frequency. The output frequency is controlled by writing frequency control words over the I^2C interface.

There are several advantages of DCTCXOs relative to VCTCXOs:

1) Frequency Control Resolution as low as 5 ppt. This high resolution minimizes accumulated time error in synchronization applications.
2) Lower system cost – A VCTCXO may need a Digital to Analog Converter (DAC) to drive the control voltage input. In a DCTXCO, the frequency control is achieved digitally by register writes to the control registers via I^2C, thereby eliminating the need for a DAC.
3) Better Noise Immunity – The analog signal used to drive the voltage control pin of a VCTCXO can be sensitive to noise and the trace over which the signal is routed can be susceptible to noise coupling from the system. The DCTCXO does not suffer from analog noise coupling since the frequency control is performed digitally through I^2C.
4) No Frequency Pull non-linearity. The frequency pulling is achieved via fractional feedback divider of the PLL, eliminating any pull non-linearity concern which is typical of quartz based VCTCXOs. This improves dynamic performance in closed loop operations.
5) Programmable Wide Pull Range – The DCTCXO pulling mechanism is via the fractional feedback divider and is therefore not constrained by resonator pullability as in quartz based solutions. The SiT5156 offers 16 frequency pull range options from ±6.25ppm to ±3200ppm, thereby giving system designers great flexibility.

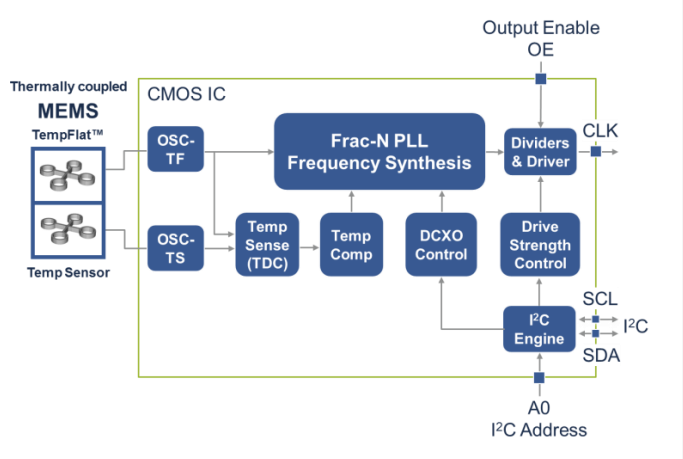


Figure 27. Block Diagram - DCTCXO

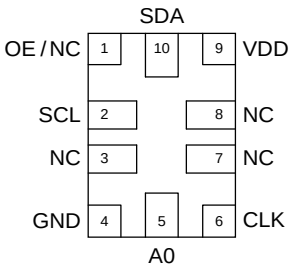


Figure 28. Top-View - DCTCXO

In the DCTCXO mode, the device powers up at the nominal operating frequency and pull range specified by the ordering code. After power-up both the pull range and output frequency can be controlled via I^2C writes to the respective control registers. The maximum output frequency change is constrained by the pull range limits.

The pull range is specified by the value loaded in the digital pull range control register. The 16 pull range choices are specified in the control register and range from ±6.25ppm to ±3200ppm.

Table 14 below shows the frequency resolution vs. pull range programmed value

Table 14. Frequency Resolution vs. Pull Range

Programmed Pull Range	Frequency Resolution
±6.25ppm	$5x10^{-12}$
±10ppm	$5x10^{-12}$
±12.5ppm	$5x10^{-12}$
±25ppm	$5x10^{-12}$
±50ppm	$5x10^{-12}$
±80ppm	$5x10^{-12}$
±100ppm	$5x10^{-12}$
±120ppm	$5x10^{-12}$
±150ppm	$5x10^{-12}$
±200ppm	$5x10^{-12}$
±400ppm	$1x10^{-11}$
±600ppm	$1.4x10^{-11}$
±800ppm	$2.1x10^{-11}$
±1200ppm	$3.2x10^{-11}$
±1600ppm	$4.7x10^{-11}$
±3200ppm	$9.4x10^{-11}$

The ppm frequency offset is specified by the 26 bit DCXO frequency control register in two's complement format as described in the I^2C Register Descriptions. The power up default value is 00000000000000000000000000b which sets the output frequency at its nominal value (0 ppm). To change the output frequency, a frequency control word is written to 0x00[15:0] (Least Significant Word) and 0x01[9:0] (Most Significant Word). The LSW value should be written first followed by the MSW value; the frequency change is initiated after the MSW value is written.

Bits	25:24	23:20	19:16	15:12	11:8	7:4	3:0
Value (Hex)	01	1111	1111	1111	1111	1111	1111
Dec. Value	2^{25} -1 = 33,554,431						

Bits	25:24	23:20	19:16	15:12	11:8	7:4	3:0
Value (Hex)	00	0000	0000	0000	0000	0000	0000
Dec. Value	0						

Bits	25:24	23:20	19:16	15:12	11:8	7:4	3:0
Value (Hex)	10	0000	0000	0000	0000	0000	0000
Dec. Value	-(2^{25}) = -33,554,432						

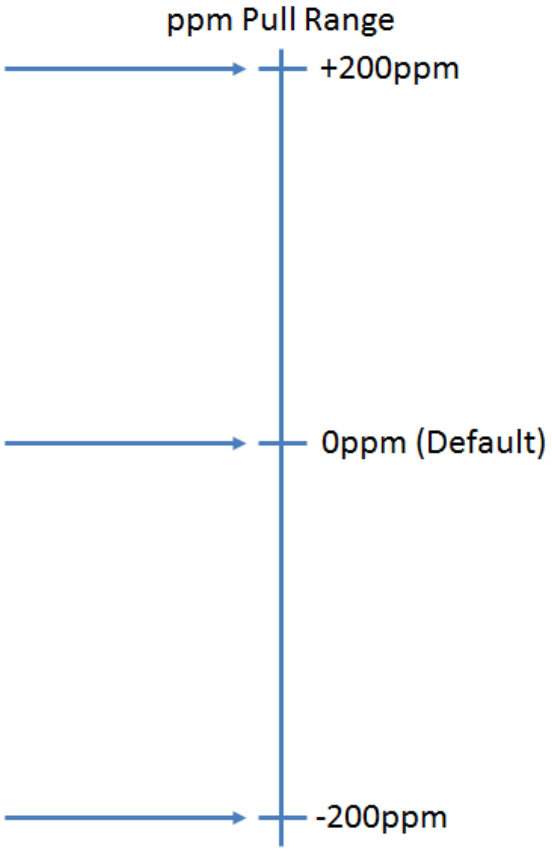


Figure 29. Pull range and Frequency Control Word

Figure 29 shows how the two's complement signed value of the frequency control word sets the output frequency within the ppm pull range set by 0x02:[3:0]. This example shows use of the ±200 ppm pull range. Therefore to set the desired output frequency, one just needs to calculate the fraction of full scale value ppm, convert to two's complement binary and then write the values to the frequency control registers.

The following formula generates the control word value:

Control word Value = RND((2^{25}-1) * ppm shift from nominal/pull range), where RND is the rounding function which rounds the number to the nearest whole number. Two examples follow, assuming the ±200 ppm pull range:

Example 1:

- Default Output Frequency = 19.2 MHz
- Desired Output Frequency = 19.201728 MHz (+90 ppm)

2^{25}-1 corresponds to +200 ppm, and the fractional value required for +90 ppm can be calculated as follows.

- 90 ppm / 200 ppm * (2^{25}-1) = 15,099,493.95.

Rounding to the nearest whole number yields 15,099,494 and converting to two's complement gives a binary value of 111001100110011001100110 and E66666 in hex.

Example 2:

- Default Output Frequency = 10 MHz
- Desired Output Frequency = 9.998 MHz (-50 ppm)

Following the formula shown above,

- (-50 ppm / 200 ppm) * (2^{25}-1) = -8,388,607.75.

Rounding to the nearest whole number results in -8,388,608.

Converting to two's complement binary results in 111000000000000000000000000 and 3800000 in hex.

To summarize, the procedure for calculating the frequency control word associated with a given ppm offset is as follows:

1) Calculate the fraction of the half pull range needed. For example, if the total pull range is set for ±100 ppm and a +20 ppm shift from the nominal frequency is needed, this fraction is 20 ppm/100 ppm = 0.2
2) Multiply this fraction by the full half scale word value, 2^{25}-1 = 33,554,431, round to the nearest whole number and convert the result to two's complement binary. Following the +20ppm example, this value is 0.2 * 33,554,431 = 6,710,886.2 and rounded to 6,710,886.
3) Write the two's complement binary value starting with the Least Significant Word (LSW) 0x00[16:0], followed by the Most Significant Word (MSW), 0x01[9:0]. If the user desires that the output remains enabled while changing the frequency, a 1 must also be written to the OE control bit 0x01[10] if the device has software OE Control Enabled.

It is important to note that the maximum Digital Control update rate is 38 kHz regardless of I^{2}C bus speed.

I²C Control Registers

The DCTCXO option enables control of frequency pull range, frequency pull value, Output Enable and drive strength control via I²C writes to the control registers. Table 15 below shows the register map summary and the detailed register descriptions follow.

Table 15. Register Map Summary

Address	Bits	Access	Description
0x00	[15:0]	RW	DIGITAL FREQUENCY CONTROL LEAST SIGNIFICANT WORD (LSW)
0x01	[15:11]	R	NOT USED
	[10]	RW	OE Control. This bit is only active if the output enable function is under software control. If the device is configured for hardware control using the OE pin, writing to this bit has no effect.
	[9:0]	RW	DIGITAL FREQUENCY CONTROL MOST SIGNIFICANT WORD (MSW)
0x02	[15:4]	R	NOT USED
	[3:0]	RW	DIGITAL PULL RANGE CONTROL
0x05	[15:4]	R	NOT USED
	[3:0]	RW	PULL-UP DRIVE STRENGTH CONTROL
0x06	[15:4]	R	NOT USED
	[3:0]	RW	PULL-DOWN DRIVE STRENGTH CONTROL

Register Descriptions

Register Address: 0x00. Digital Frequency Control Least Significant Word (LSW)

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Name	DIGITAL FREQUENCY CONTROL LEAST SIGNIFICANT WORD (LSW)[15:0]															

Bits	Name	Access	Description
15:0	DIGITAL FREQUENCY CONTROL LEAST SIGNIFICANT WORD	RW	Bits [15:0] are the lower 16 bits of the 26 bit FrequencyControlWord and are the Least Significant Word (LSW). The upper 10 bits are in regsiter 0x01[9:0] and are the Most Significant Word (MSW). The lower 16 bits together with the upper 10 bits specify a 26-bit frequency control word. This power-up default values of all 26 bits are 0 which sets the output frequency at its nominal value. After power-up, the system can write to these two registers to pull the frequency across the pull range. The register values are two's complement to support positive and negative control values. The LSW value should be written before the MSW value because the frequency change is initiated when the new values are loaded into the MSW. More details and examples are discussed in the next section.

Register Address: 0x01. OE Control, Digital Frequency Control Most Significant Word (MSW)

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Name	NOT USED					OE	DCXO FREQUENCY CONTROL[9:0] MSW									

Bits	Name	Access	Description
15:11	NOT USED	R	Bits [15:10] are read only and return all 0's when read. Writing to these bits has no effect.
10	OE Control	RW	Output Enable Software Control. Allows the user to enable and disable the output driver via I^2C. 0 = Output Disabled (Default) 1 = Output Enabled This bit is only active if the Output Enable function is under software control. If the device is configured for hardware control using the OE pin, writing to this bit has no effect.
9:0	DIGITAL FREQUENCY CONTROL MOST SIGNIFICANT WORD (MSW)	RW	Bits [9:0] are the upper 10 bits of the 26 bit FrequencyControlWord and are the Most Significant Word (MSW). The lower 16 bits are in register 0x00[15:0] and are the Least Significant Word (LSW). These lower 16 bits together with the upper 10 bits specify a 26-bit frequency control word. This power-up default values of all 26 bits are 0 which sets the output frequency at its nominal value. After power-up, the system can write to these two registers to pull the frequency across the pull range. The register values are two's complement to support positive and negative control values. The LSW value should be written before the MSW value because the frequency change is initiated when the new values are loaded into the MSW. More details and examples are discussed in the next section.

Register Address: 0x02. DIGITAL PULL RANGE CONTROL[7]

Bit	15	14	13	12	11	10	9	6	5	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	RW	RW	RW	RW
Default	0	0	0	0	0	0	0	0	0	0	0	0	X	X	X	X
Name	NONE												DIGITAL PULL RANGE CONTROL			

Notes:

7. Default values are factory set but can be over-written after power-up.

Bits	Name	Access	Description
15:4	NONE	R	Bits [15:4] are read only and return all 0's when read. Writing to these bits has no effect.
3:0	DIGITAL PULL RANGE CONTROL	RW	Sets the digital pull range of the DCXO. The table below shows the available pull range values and associated bit settings. The default value is factory programmed **Bit** **3 2 1 0** 0 0 0 0: ±6.25ppm 0 0 0 1: ±10ppm 0 0 1 0: ±12.5ppm 0 0 1 1: ±25ppm 0 1 0 0: ±50ppm 0 1 0 1: ±80ppm 0 1 1 0: ±100ppm 0 1 1 1: ±125ppm 1 0 0 0: ±150ppm 1 0 0 1: ±200ppm 1 0 1 0: ±400ppm 1 0 1 1: ±600ppm 1 1 0 0: ±800ppm 1 1 0 1: ±1200ppm 1 1 1 0: ±1600ppm 1 1 1 1: ±3200ppm

Register Address: 0x05. PULL-UP DRIVE STRENGTH CONTROL

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	RW	RW	RW	RW
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Name	NONE												PULL-UP DRIVE STRENGTH CONTROL			

Bits	Name	Access	Description
15:4	NONE	R	Bits [15:4] are read only and return all 0's when read. Writing to these bits has no effect.
3:0	PULL-UP DRIVE STRENGTH CONTROL	RW	Sets the pull-up drive strength of the output driver. The below table shows the range of values. **Bit** **3 2 1 0** 0 0 0 0: 5x (Default) 0 0 0 1: 6x 0 0 1 0: 7x 0 0 1 1: 8x 0 1 0 0: 9x 0 1 0 1: 10x 0 1 1 0: 11x 0 1 1 1: 12x 1 0 0 0: 13x 1 0 0 1: 14x 1 0 1 0: 15x 1 0 1 1: 16x 1 1 0 0: 17x 1 1 0 1: 18x 1 1 1 0: 19x 1 1 1 1: 20x

Register Address: 0x06. PULL-DOWN DRIVE STRENGTH CONTROL

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	RW	RW	RW	RW
Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Name	NONE												PULL-DOWN DRIVE STRENGTH CONTROL			

Bits	Name	Access	Description
5:4	NONE	R	Bits [15:4] are read only and return all 0's when read. Writing to these bits has no effect.
3:0	PULL-DOWN DRIVE STRENGTH CONTROL	RW	Sets the pull-down drive strength of the output driver. The below table shows the range of values. **Bit** **3 2 1 0** 0 0 0 0: 5x (Default) 0 0 0 1: 6x 0 0 1 0: 7x 0 0 1 1: 8x 0 1 0 0: 9x 0 1 0 1: 10x 0 1 1 0: 11x 0 1 1 1: 12x 1 0 0 0: 13x 1 0 0 1: 14x 1 0 1 0: 15x 1 0 1 1: 16x 1 1 0 0: 17x 1 1 0 1: 18x 1 1 1 0: 19x 1 1 1 1: 20x

Serial Interface Configuration Description

The SiT5156 may be ordered with the I^2C interface to access registers which control the DCTCXO frequency pull range, frequency pull value, and output drive strength. The SiT5156 I^2C slave only interface supports clock speeds up to 1 MHz. The SiT5156 I^2C module is based on the I^2C specification, UM1024 (Rev.6 April 4, 2014 of NXP Semiconductor).

Serial Signal Format

The SDA line must be stable during the high period of the SCL. SDA transitions are allowed only during SCL low level for data communication. Only one transition is allowed during the low SCL state to communicate one bit of data. Figure 30 shows the detailed timing diagram.

The idle I^2C bus state occurs when both SCL and SDA are not being driven by any master and are therefore in a logic HI state due to the pull up resistors. Every transaction begins with a START (S) signal and ends with a STOP (P) signal. A START condition is defined by a high to low transition on the SDA while SCL is high. A STOP condition is defined by a low to high transition on the SDA while SCL is high. START and STOP conditions are always generated by the master. This slave module also supports repeated START (Sr) condition which is same as START condition instead of STOP condition (Blue color line shows repeated START in Figure 31).

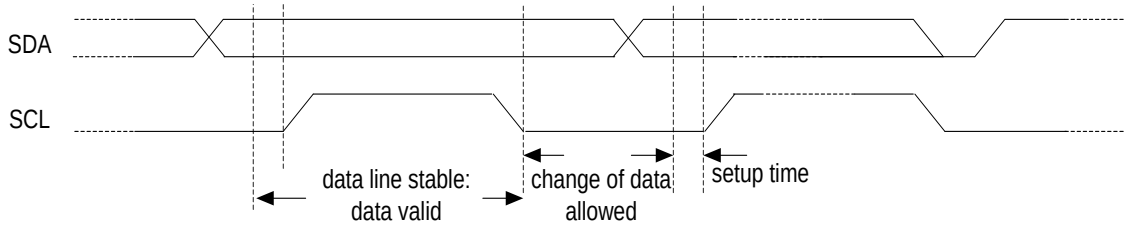


Figure 30. Data and clock timing relation in I^2C bus

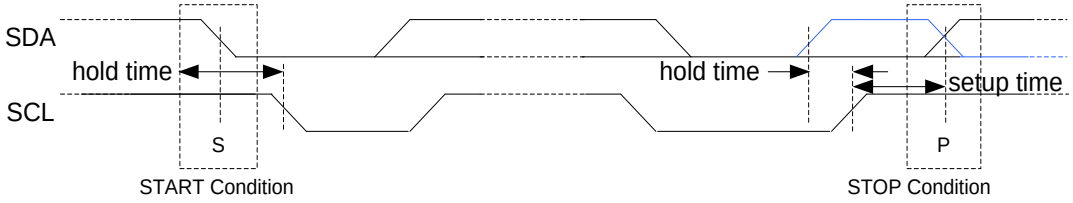


Figure 31. START and STOP (or repeated START) condition

Parallel Signal Format

Every data byte is eight bits long. The number of bytes that can be transmitted per transfer is unrestricted. Data is transferred with the MSB (Most Significant Bit) first. The detailed data transfer format is shown in Figure 33 below.

The acknowledge bit must occur after every byte transfer and it allows the receiver to signal the transmitter that the byte was successfully received and another byte may be sent. The acknowledge signal is defined as follows: the transmitter releases the SDA line during the acknowledge clock pulse so the receiver can pull the SDA line low and it remains stable low during the high period of this clock pulse. Setup and hold times must also be taken into account. When SDA remains high during this ninth clock pulse, this is defined as the Not-Acknowledge signal (NACK). The master can then generate either a STOP condition to abort the transfer, or a repeated START condition to start a new transfer. The only condition that leads to the generation of NACK from the SiT5156 is when the transmitted address does not match the slave address. When the master is reading data from the SiT5156, the SiT5156 expects the ACK from the master at the end of received data, so that the slave releases the SDA line and the master can generate the STOP or repeated START. If there is a NACK signal at the end of the data, then the SiT5156 tries to send the next data. If the first bit of the next data is “0”, then the SiT5156 holds the SDA line to “0”, thereby blocking the master from generating a STOP/(re)START signal.

Parallel Data Format

This I^2C slave module supports 7-bit device addressing format. The 8^{th} bit is a read/write bit and “0” indicates a read transaction and a “1” indicates a write transaction. The register addresses are 8-bits long with an address range of 0 to 255 (00h to FFh). Auto address incrementing is supported which allows data to be transferred to contiguous addresses without the need to write each address beyond the first address. Since the maximum register address value is 255, the address will roll from 255 back to 0 when auto address incrementing is used. Obviously, auto address incrementing should only be used for writing to contiguous addresses. The data format is 16-bit (two bytes) with the most significant byte being transferred first.

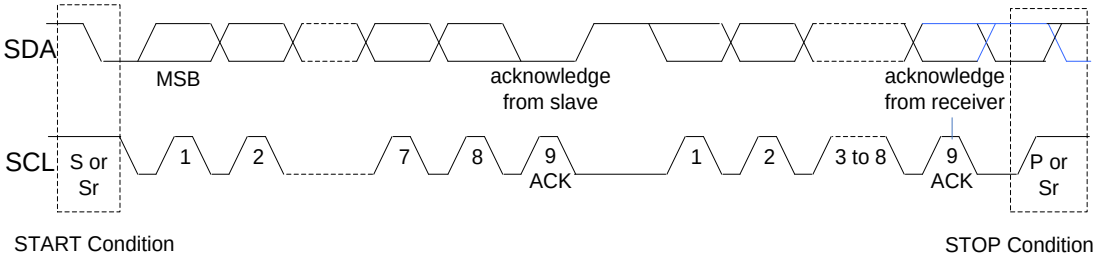


Figure 32. Parallel Signaling Format

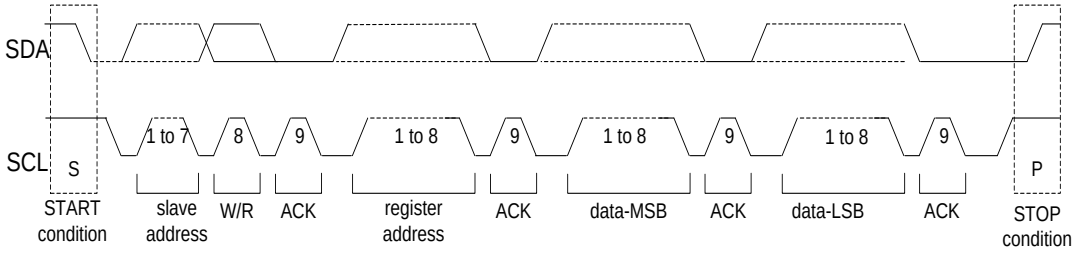


Figure 33. Parallel Data Byte Format

Figure 34 below shows the I²C sequence for writing the 4-byte control word using auto address incrementing.

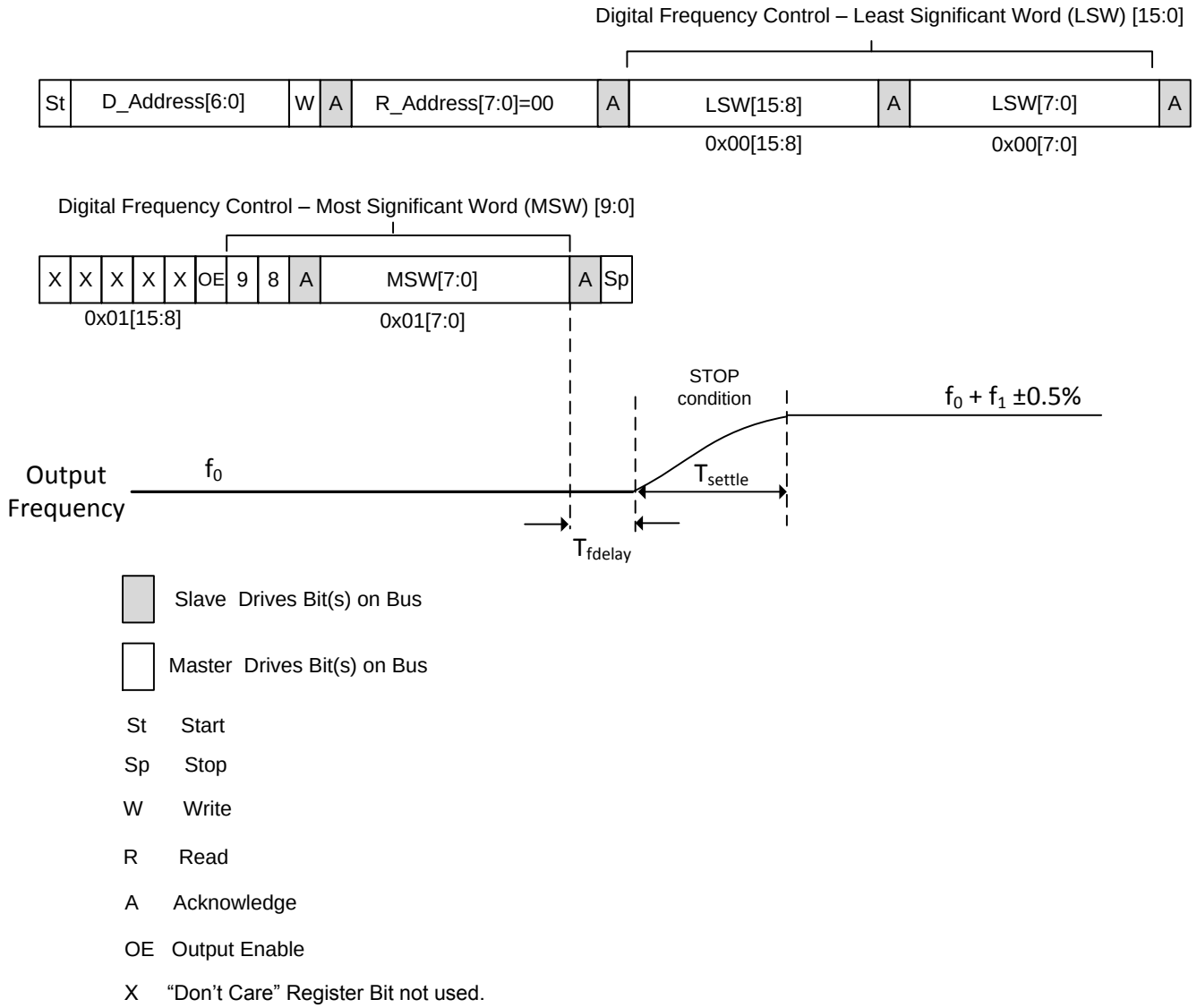


Figure 34. Writing the Frequency Control Word

Table 16. DCTCXO Delay and Settling Time

Parameter	Symbol	Minimum	Typical	Maximum	Units	Notes
Frequency Change Delay	T_{fdelay}	–	22	–	µsec	
Frequency Settling Time	T_{settle}	–	30	–	µsec	Time to settle to 1% of final frequency value

I²C Timing Specification

The below timing diagram and table illustrate the timing relationships for both master and slave.

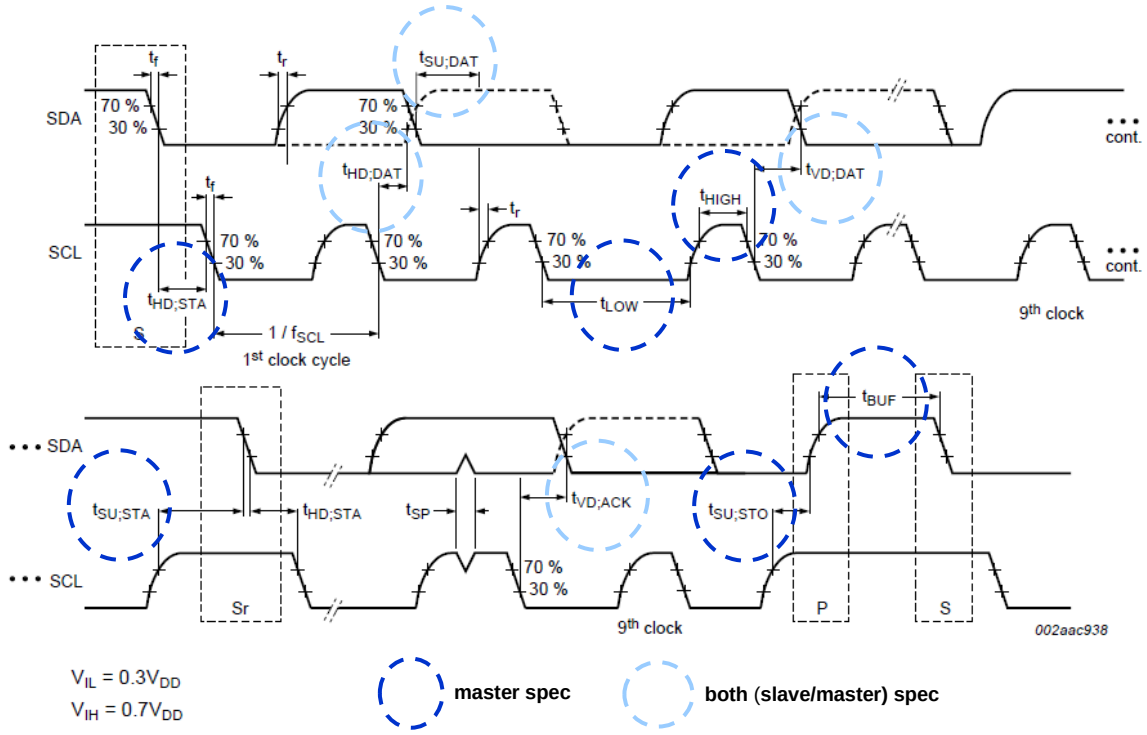


Figure 35. I²C Timing Diagram

Table 17. I²C Timing Requirements

Parameter	Speed Mode	Value	Unit
t_{SETUP}	FM+ (1 MHz)	> 50	nsec
	FM (400KHz)	> 100	nsec
	SM (100KHz)	> 250	nsec
t_{HOLD}	FM+ (1 MHz)	> 0	nsec
	FM (400KHz)	> 0	nsec
	SM (100KHz)	> 0	nsec
$t_{VD:AWK}$	FM+	> 450	nsec
	FM (400KHz)	> 900	nsec
	SM (100KHz)	> 3450	nsec
$t_{VD:DAT}$		NA (s-awk + s-data)/(m-awk/s-data)	

I²C Device Address Modes

There are two I²C address modes:

1) Factory Programmed Mode. The lower 4 bits of the 7-bit device address are set by ordering code as shown in Table 18 below. There are 16 factory programmed addresses available. In this mode, pin 5 is NC and the A0 I²C address pin control function is not available.

2) A0 Pin Control. This mode allows the user to select between two I²C Device addresses as shown in Table 19.

Table 18. Factory Programmed I²C Address Control[8]

I²C Address Ordering Code	Device I²C Address
0	1100000
1	1100001
2	1100010
3	1100011
4	1100100
5	1100101
6	1100110
7	1100111
8	1101000
9	1101001
A	1101010
B	1101011
C	1101100
D	1101101
E	1101110
F	1101111

Notes:

8. Table 18 is only valid for the DCTCXO device option which supports I²C Control.

Table 19. Pin Selectable I²C Address Control[9]

A0 Pin 5	I²C Address
0	1100010
1	1101010

Notes:

9. Table 19 is only valid for the DCTCXO device option which supports I²C control and A0 Device Address Control Pin.

Schematic Example

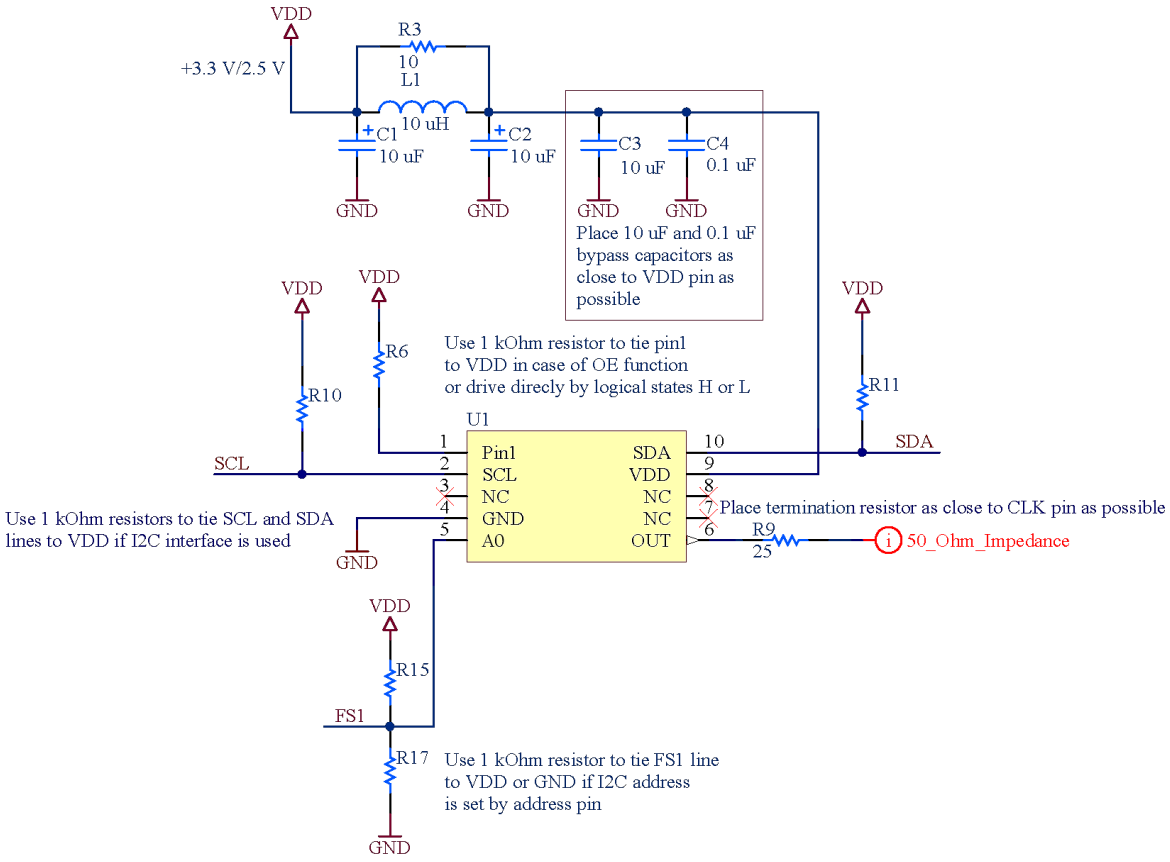
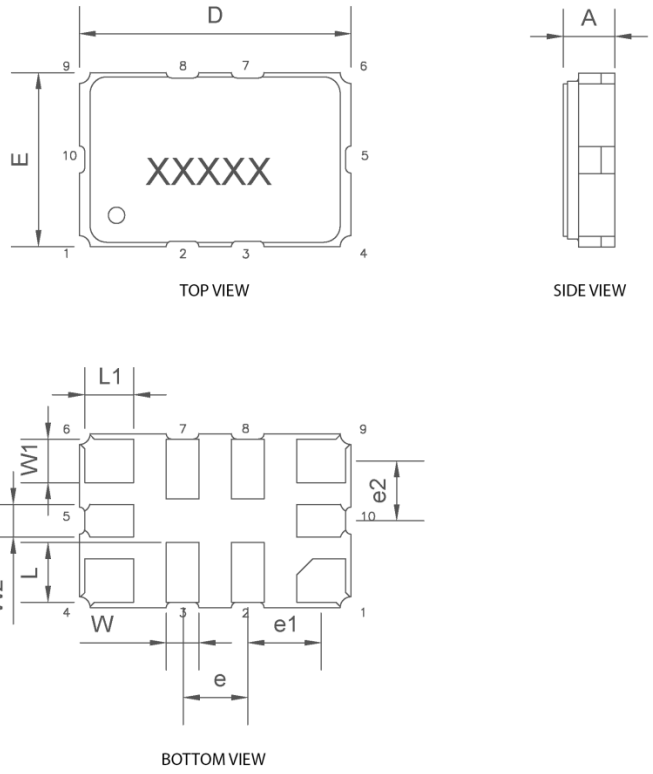


Figure 36. Schematic Example - DCTCXO

Dimensions and Patterns

Package Size – Dimensions (Unit: mm)

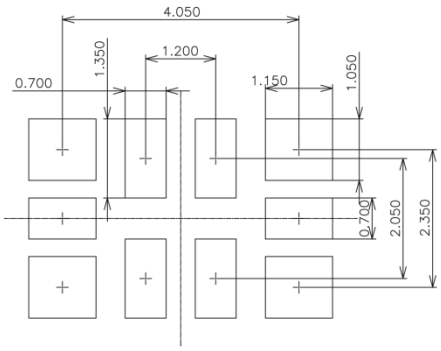


Dimension Table

		Symbol	Min	Nom	Max
TOTAL THICKNESS		A	0.840	0.950	1.060
BODY SIZE	X	D	4.850	5.000	5.150
	Y	E	3.050	3.200	3.350
LEAD PITCH		e	1.070	1.200	1.330
		e1	1.220	1.350	1.480
		e2	0.970	1.100	1.230
LEAD LENGTH		L	0.970	1.100	1.230
		L1	0.770	0.900	1.030
LEAD WIDTH		W	0.470	0.600	0.730
		W1	0.670	0.800	0.930
		W2	0.470	0.600	0.730

Package Outline	
10L Ceramic	POD-036-RevA
5.0x3.2x0.87	
2018/02/05	

Recommended Land Pattern (Unit: mm)



Solder Print Layout	
10L Ceramic	SPL-001-RevA
5.0x3.2x0.87	
2017/06/20	

Layout Guidelines

- SiT5156 uses internal regulators to minimize the impact of the power supply noise. For further reduction of noise, it is essential to use two bypass capacitors (0.1 µF and 10 µF). Place the bypass capacitors as close to the Vdd as possible, typically within 1 to 2 mm. Ensure that the 0.1uF cap is the closest to the device Vdd and GND power pins
- It is also recommended to connect all NC pins to the ground plane and place multiple vias under the GND pin for maximum heat dissipation.
- For additional layout recommendations, refer to the Best Design Layout Practices.

Manufacturing Guidelines

The SiT5156 Super-TCXOs is a precision timing device. **Proper PCB solder and cleaning process** must be followed in order to ensure best performance and long-term reliability.

- **No Ultrasonic or Megasonic Cleaning:** Do not subject the SiT5156 to an ultrasonic or megasonic cleaning environment. Permanent damage or long-term reliability issues to the device may occur in such an event.
- **No external cover.** Unlike legacy quartz TCXOs, the SiT5156 is engineered to operate reliably without performance degradation, in the presence of ambient disturbers such as airflow and sudden temperature changes. Therefore, the use of an external cover typical of quartz TCXOs is not needed.
- **Reflow profile:** For mounting these devices to the PCB, IPC/JEDEC J-STD-020 compliant reflow profile must be used. Device performance is not guaranteed if soldered manually or with a non-compliant reflow profile.
- **PCB cleaning:** after the surface mount (SMT)/reflow process, solder flux residues may be present on the PCB and around the pads of the device. Excess residual solder flux may lead to problems such as pad corrosion, elevate leakage currents, increased frequency aging, or other performance degradation. For optimal device performance and long-term reliability, thorough cleaning and drying of the PCB is required as shortly after the reflow process as possible, even when using a “no clean” flux. Care should be taken to remove all residual flux between the SiTime device and the PCB. Note that ultrasonic PCB cleaning should not be used with SiTime oscillators.
- For additional manufacturing guidelines and marking/ tape-reel instructions, refer to SiTime Manufacturing Notes.

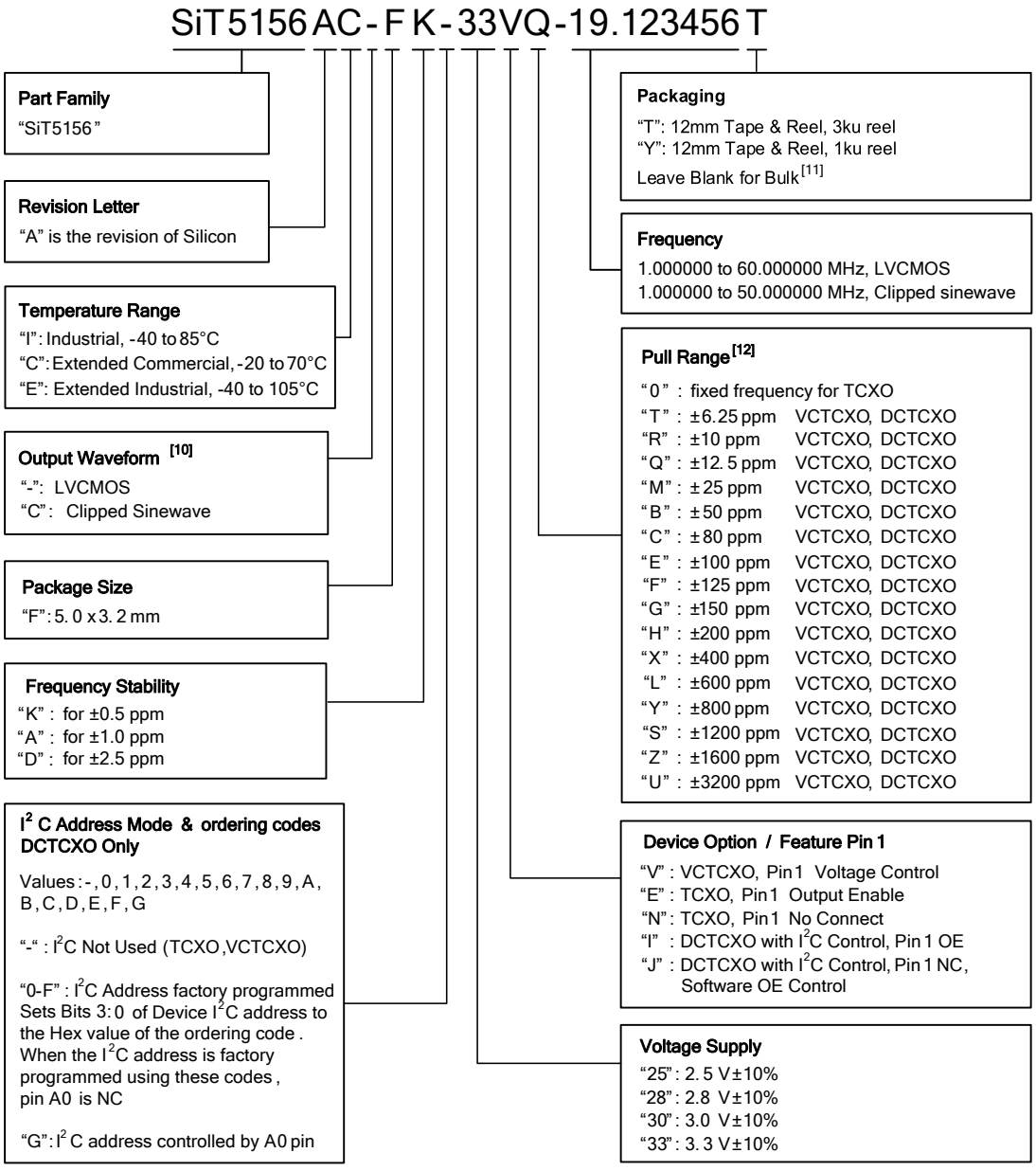
Ordering Information

The Part No. Guide is for reference only.

To customize and build an exact part number, use the SiTime Part Number Generator.

Use the Part Number Decoder to validate the part number.

Refer to Table 20 for Ordering Code combinations regarding device configuration, Pin 1 functionality and I^2C address mode.



Notes:

10. "-" corresponds to the default rise/fall time for LVCMOS output as specified in Table 1 (Electrical Characteristics). Contact SiTime for other rise/fall time options for best EMI.
11. Bulk is available for sampling only
12. "0" is selected when the device is configured as a TCXO (pin 1 = "E" or "N"). "T" to "U" are applicable in VCTCXO mode (pin 1 = "V") and DCTCXO mode (pin 1 = "E" or "N")

Table 20. Ordering Codes for Device Configuration vs. Feature Pin 1 and I²C Address Mode

Device Configuration	Feature Pin 1	I²C Address Mode
TCXO	"E": Pin 1 Output Enable "N": Pin 1 No Connect	–
VCTCXO	"V": Pin 1 Voltage Control	–
DCTCXO	"I": Pin 1 Output Enable "J": Pin 1 No Connect, Output Enable under Software Control	"0-F": factory programmed I²C address "G": I²C address controlled by A0 pin

Table 21. Ordering Codes for Supported Tape & Reel Packing Method

Device Size (mm x mm)	16 mm T&R(3ku)	16 mm T&R(1ku)	12 mm T&R(3ku)	12 mm T&R(1ku)	8 mm T&R(3ku)	8 mm T&R(1ku)
5.0 x 3.2	–	–	T	Y	–	–

Table 22. Additional Information

Document	Description	Download Link
Time Machine II	MEMS oscillator programmer	http://www.sitime.com/support/time-machine-oscillator-programmer
Field Programmable Oscillators	Devices that can be programmable in the field by Time Machine II	http://www.sitime.com/products/field-programmable-oscillators
Manufacturing Notes	Tape & Reel dimension, reflow profile and other manufacturing related info	http://www.sitime.com/manufacturing-notes
Qualification Reports	RoHS report, reliability reports, composition reports	http://www.sitime.com/support/quality-and-reliability
Performance Reports	Additional performance data such as phase noise, current consumption and jitter for selected frequencies	http://www.sitime.com/support/performance-measurement-report
Termination Techniques	Termination design recommendations	http://www.sitime.com/support/application-notes
Layout Techniques	Layout recommendations	http://www.sitime.com/support/application-notes

Table 23. Revision History

Version	Release Date	Change Summary
0.1	05/10/2016	First release, advanced information
0.15	08/04/2016	Replaced QFN package with SOIC-8 package Added 10 µF bypass cap requirement Updated test circuits to reflect both new bypass cap requirement and SOIC-8 package Update Table 1 (Electrical Characteristics)
0.16	09/12/2016	Updated test circuit diagrams
0.2	09/21/2016	Revised Table 1 (Electrical Characteristics)
0.4	12/19/2016	Added DCTCXO mode Added I2C information Added I2C
0.5	07/21/2017	Added 5.0x3.2 mm package information Updated Table 1: Electrical Characteristics
0.51	08/20/2017	Changed to preliminary Updated 5.0x3.2 mm package dimensions Updated test circuits Updated Table 1 (Electrical Characteristics) Updated part ordering info Misc. corrections
0.52	11/27/2017	Updated the Thermal Characteristics table Added more on Manufacturing Guideline section
0.55	02/05/2018	Added View labels to Package Drawings Updated the freq vs. output type changes to 60 Mhz Updated links and notes
0.60	03/01/2018	Added 105°C support, updated Ordering Information

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