



Product Change Notification / SYST-12IILY127

Date:

17-Nov-2020

PCN Type:

Silicon Die Revision

Notification Subject:

ERRATA - PIC32CM MC00 Family Data Sheet Clarifications and Silicon Errata

Affected CPNs:

[SYST-12IILY127_Affected_CPN_11172020.pdf](#)

[SYST-12IILY127_Affected_CPN_11172020.csv](#)

Notification Text:

SYST-12IILY127

Microchip has released a new Product Documents for the PIC32CM MC00 Family Data Sheet Clarifications and Silicon Errata of devices. If you are using one of these devices please read the document located at [PIC32CM MC00 Family Data Sheet Clarifications and Silicon Errata](#).

Notification Status: Final

Description of Change:

This revision includes the following updates to Data Sheet Clarifications:

- 1) Updated Silicon Die Revision from A0 to A1
- 2) Updated the errata numbering schema to reflect those errata which were removed

Impacts to Data Sheet: None

Reason for Change: To Improve Productivity

Change Implementation Status: Complete

Date Document Changes Effective: 17 Nov 2020

NOTE: Please be advised that this is a change to the document only the product has not been changed.

Markings to Distinguish Revised from Unrevised Devices: N/A

Attachments:

[PIC32CM MC00 Family Data Sheet Clarifications and Silicon Errata](#)

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Affected Catalog Part Numbers (CPN)

PIC32CM1216MC00032-I/PT
PIC32CM1216MC00032-I/RTB
PIC32CM1216MC00032T-I/PT
PIC32CM1216MC00032T-I/RTB
PIC32CM1216MC00048-I/U5B
PIC32CM1216MC00048-I/Y8X
PIC32CM1216MC00048T-I/U5B
PIC32CM1216MC00048T-I/Y8X
PIC32CM6408MC00032-I/PT
PIC32CM6408MC00032-I/RTB
PIC32CM6408MC00032T-I/PT
PIC32CM6408MC00032T-I/RTB
PIC32CM6408MC00048-I/U5B
PIC32CM6408MC00048-I/Y8X
PIC32CM6408MC00048T-I/U5B
PIC32CM6408MC00048T-I/Y8X

PIC32CM MC00 Family Data Sheet Clarifications and Silicon Errata

PIC32CM MC00 Family

The PIC32CM MC00 family of devices that you have received conforms functionally to the current Device Data Sheet (TBDA), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in the following table.

The errata described in this document will be addressed in future revisions of the PIC32CM MC00 family silicon.

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current.

Data Sheet clarifications and corrections (if applicable) are located in [Data Sheet Clarifications](#), following the discussion of silicon issues.

Table 1. PIC32CM MC00 Family Silicon Device Identification

Devices	Device ID (DID[31:0])	Silicon Revision ID (DID.REVISION[3:0])
		A1
PIC32CM1216MC00032	0x11070x00	0x0
PIC32CM6408MC00032	0x11070x01	0x0
PIC32CM1216MC00048	0x11070x06	0x0
PIC32CM6408MC00048	0x11070x07	0x0

Note:

1. Refer to the “*Device Service Unit*” chapter in the current Device Data Sheet (TBDA) for a detailed information on Device Identification and Revision IDs for a specific device.

Silicon Errata Summary

Module	Feature	Errata Number	Issue Summary	Affected Revisions
				A1
NVMCTRL	DATA FLASH	1.1.1	CPU writes to any memory or register while a write or erase operation is ongoing in the Data Flash address space will stall the AHB bus for the duration of the write or erase operation. CPU reads are not impacted..	X
NVMCTRL	CEHL	1.1.2	The CEHL feature is not functional.	X
SERCOM I²C	Repeated Start	1.2.1	For Master Write operations (excluding High-Speed mode) in 10-bit addressing mode, writing CTRLB.CMD = 0x1 does not correctly issue a Repeated Start command.	X
SERCOM I²C	Repeated Start	1.2.2	For High-Speed Master Write operations, writing CTRLB.CMD = 0x1 issues a STOP command instead of a Repeated Start, making repeated start not possible in that mode.	X
SERCOM I²C	NACK and Repeated Start	1.2.3	For High-Speed Master Read operations, sending a NACK (CTRLB.CMD = 0x2) forces a STOP to be issued, making repeated start not possible in that mode.	X

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1. PIC32CM MC00 Errata Issues

The following issues apply to the PIC32CM MC00 family of devices.

1.1 Non-Volatile Memory Controller (NVMCTRL)

1.1.1 DATA FLASH

CPU writes to any memory or register while a write or erase operation is ongoing in the Data Flash address space will stall the AHB bus for the duration of the write or erase operation. CPU reads are not impacted.

The stall duration will be up to the maximum time of the Flash write or erase operation:

Page Write time: 2.5 ms

Row Erase time: 6 ms

Sector Erase time: 8 ms

Workaround

Perform Data Flash modify operations in a safe region of the application where CPU writes are not required.

Affected Silicon Revisions

A1				
X				

1.1.2 CEHL

The Chip Erase Hard Lock (CEHL) feature is not functional and will not provide any code protection capabilities. The Secure Bit (SB) is not affected, and can be used for code protection.

Workaround

None.

Affected Silicon Revisions

A1				
X				

1.2 SERCOM I²C

1.2.1 Repeated Start

For Master Write operations (excluding High-Speed mode) in 10-bit Addressing mode, writing CTRLB.CMD = 0x1 does not correctly issue a Repeated Start command.

Workaround

Write the same 10-bit address with the same direction bit to the ADDR.ADDR register to generate a Repeated Start.

Affected Silicon Revisions

A1				
X				

1.2.2 Repeated Start

For High-Speed Master Write operations, writing CTRLB.CMD = 0x1 issues a STOP command instead of a Repeated Start, making repeated start is not possible in that mode.

Workaround
None.

Affected Silicon Revisions

A1				
X				

1.2.3 NACK and Repeated Start

For High-Speed Master Read operations, sending a NACK (CTRLB.CMD = 0x2) forces a STOP to be issued, making repeated start is not possible in that mode.

Workaround
None.

Affected Silicon Revisions

A1				
X				

2. Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (TBDA):

Note: Corrections in tables, registers, and text are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

There are no Data Sheet Clarifications to report at this time.

3. Appendix A: Revision History

Revision B - 11/2020

The following updates were performed for this revision:

- Updated Silicon Die Revision from A0 to A1
- Updated the errata numbering schema to reflect those errata which were removed

Revision A - 07/2020

This is the initial released version of this document.

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