



Product Change Notification / KSRA-23AGSP046

Date:

04-Mar-2021

Product Category:

Memory

PCN Type:

Manufacturing Change

Notification Subject:

Memolog # ML0220210049 Final Notice: Qualification of 66.88K process technology for selected Microchip products of the 24AA512, 24FC512 and 24LC512 device families.

Affected CPNs:

[KSRA-23AGSP046_Affected_CPN_03042021.pdf](#)
[KSRA-23AGSP046_Affected_CPN_03042021.csv](#)

Notification Text:

PCN Status: Final notification.

PCN Type: Manufacturing Change

Microchip Parts Affected: Please open one of the files found in the Affected CPNs section.

NOTE: For your convenience Microchip includes identical files in two formats (.pdf and .xls).

Description of Change: Qualification of 66.88K process technology for selected Microchip products of the 24AA512, 24FC512 and 24LC512 device families.

Pre and Post Change Summary:

| | Pre Change | | Post Change |
|-----------------------------|-----------------------|-----------------------------|-------------------------|
| Wafer Technology | 160K wafer technology | 160K wafer technology | 66.88K wafer technology |
| Fabrication Location | Microchip Fabrication | Microchip Fabrication Sites | UMC Fab 8D (Hsin-Chu, |

| | | | |
|------------------------------|---|--|--------------------------|
| | Sites FAB 2 and FAB4 (Tempe, AZ and Gresham, OR, USA) | FAB 2 and FAB4 (Tempe, AZ and Gresham, OR, USA) | Taiwan) |
| Wafer Diameter | 8 inches (200 mm) | 8 inches (200 mm) | 8 inches (200 mm) |
| Quality certification | ISO/TS16949 | ISO/TS16949 | ISO/TS16949 |

Impacts to Data Sheet: None

Change Impact:None

Reason for Change:To improve manufacturability by qualifying an additional fabrication site.

Change Implementation Status:In Progress

Estimated First Ship Date:

April 19, 2021 (date code: 2117)

NOTE: Please be advised that after the estimated first ship date customers may receive pre and post change parts.

Time Table Summary:

| Workweek | March 2021 | | | | | → | April 2021 | | | | |
|-------------------------------|------------|----|----|----|----|---|------------|----|----|----|----|
| | 10 | 11 | 12 | 13 | 14 | | 14 | 15 | 16 | 17 | 18 |
| Qual Report Availability | X | | | | | | | | | | |
| Final PCN Issue Date | X | | | | | | | | | | |
| Estimated Implementation Date | | | | | | | | | | X | |

Method to Identify Change: Traceability code

Qualification Report:Please open the attachments included with this PCN labeled as PCN_#_Qual_Report.

Revision History:March 04, 2021: Issued final notification. Attached the Qualification Report. Provided estimated first ship date to be on April 19, 2021.

The change described in this PCN does not alter Microchip's current regulatory compliance regarding the material content of the applicable products.

Attachments:

[PCN_KSRA-23AGSP046_Qual_Report.pdf](#)

Please contact your local [Microchip sales office](#) with questions or concerns regarding this notification.

Terms and Conditions:

If you wish to receive Microchip PCNs via email please register for our PCN email service at our [PCN home page](#) select register then fill in the required fields. You will find instructions about registering for Microchips PCN email service in the [PCN FAQ](#) section.

If you wish to change your PCN profile, including opt out, please go to the [PCN home page](#) select login and sign into your myMicrochip account. Select a profile option from the left navigation bar and make the applicable selections.

Affected Catalog Part Numbers (CPN)

24AA512-I/MF
24AA512-I/P
24AA512-I/SM
24AA512-I/SN
24AA512-I/ST
24AA512T-I/MF
24AA512T-I/SM
24AA512T-I/SN
24AA512T-I/ST
24FC512-I/MF
24FC512-I/P
24FC512-I/SM
24FC512-I/SN
24FC512-I/ST
24FC512T-I/SM
24FC512T-I/SN
24FC512T-I/ST
24LC512-E/MF
24LC512-E/P
24LC512-E/SM
24LC512-E/SN
24LC512-E/ST
24LC512-I/MF
24LC512-I/P
24LC512-I/SM
24LC512-I/SN
24LC512-I/ST
24LC512T-E/MF
24LC512T-E/SM
24LC512T-E/SN
24LC512T-E/ST
24LC512T-I/MF
24LC512T-I/SM
24LC512T-I/SN
24LC512T-I/ST
24FC512T-I/MF



QUALIFICATION REPORT SUMMARY
RELIABILITY LABORATORY

PCN #: KSRA-23AGSP046

Date:
February 18, 2021

**Qualification of 66.88K process technology for selected
Microchip products of the 24AA512, 24FC512 and 24LC512
device families.**

Purpose: Qualification of 66.88K process technology for selected Microchip products of the 24AA512, 24FC512 and 24LC512 device families.

I. Summary:

In keeping with guidelines established in Microchip specification QCI-39000, four lots of 66829 B3 product were stressed to meet AEC Grade 1 Qualification. The lots were processed using Process Flow MSL5366 in which the NLDD Implants for low voltage (<5.5V) and high voltage (<15V) transistors are performed separately. This the same flow used by the 668LC product. This qualification also covers the Production Mask (the B4 version of the device) which removes passivation openings for internal probe points.

II. Conclusion:

Based on the results, 66829 product built at UMC meets the guidelines specified in the qualification plan. Therefore, the device can be released to production as an Automotive Grade 1 product as per guidelines established in Microchip specification QCI-39000, "Worldwide Quality Conformance Requirements

II. Device Description:

| | |
|-------------------------|---|
| Device | AT24C512C, 24CS512, 24FC512, 24LC512, 24AA512 |
| MSL | 5366 |
| Product | 512kBit I2C SEEPROM Memory |
| Document Control Number | ML09202000IS |
| Document Revision | B- or C |
| Memolog No. | MLxxxxx |

III. Qualification Material:

| Test Lot | Lot 1 | Lot 2 | Lot 3 | Lot 4 |
|--------------------|---------------|---------------|---------------|-----------------|
| CPN | 24CS512 | 24CS512 | 24CS512 | 24CS512 |
| MASK | 66829-B3 | 66829-B3 | 66829-B3 | 66829-B3 |
| WAFER FAB | UMC | UMC | UMC | UMC |
| ASSEMBLY LOT | MTAI204401928 | MTAI210902449 | MTAI211103063 | MTAI211103064 |
| PACKAGE | 8L SOIC | 8L SOIC | 8L SOIC | 8L SOIC |
| ASSEMBLY SITE | MTAI | MTAI | MTAI | MTAI |
| FINAL TEST | MTAI | MTAI | MTAI | MTAI |
| QUAL TESTS –SJ | END, ESD/LU | END/DLT, | END/DLT, | END/DLT, END/DR |
| ASSEMBLY LOT | | MMT-210900044 | MMT-211300072 | MMT-211300073 |
| PACKAGE | | 8L PDIP | 8L PDIP | 8L PDIP |
| ASSEMBLY SITE | | MMT | MMT | MMT |
| FINAL TEST | | MMT | MMT | MMT |
| QUAL TESTS – MTHAI | | ELFR / DLT | ELFR / DLT | ELFR / DLT |

IV. Qualification Data:

Endurance / Dynamic Life Test (Stress conducted at MCHP San Jose)

| | | | |
|--------------------------------------|--|---------------------|---------------------|
| Stress Method | MIL-STD 883 Method 1033 | | |
| Stress Condition | $T_a = 85^{\circ}\text{C} / V_{cc} = 5\text{V} / 100,000 \text{ cycles (Write 0x00h)}$ | | |
| Min Sample Size Test Temperatures | 77 pieces/lot 25C, -40C, 85C, 125C | | |
| Lot #; Fail / Pass | Lot 2; 0 Fails / 92 | Lot 3; 0 Fails / 92 | Lot 4; 0 Fails / 92 |
| Stress Method | MIL-STD 883 Method 1005 | | |
| Stress Condition | $T_a = 150^{\circ}\text{C} / V_{cc} = 5.5\text{V} / 408 \text{ hours}$ | | |
| Min Sample Size Test Temperatures | 77 pieces/lot 25C, -40C, 85C, 125C | | |
| Readpoint 1 | 408 hours | | |
| Lot #; Fail / Pass | Lot 2; 0 Fails / 92 | Lot 3; 0 Fails / 92 | Lot 4; 0 Fails / 92 |
| Readpoint 2 | +600 hours (1008 Total) | | |
| Lot # Fail / Pass | Lot 2; 0 Fails / 92 | Lot 3; 0 Fails / 92 | Lot 4; 0 Fails / 92 |

Endurance / Data Retention (Stress conducted at MCHP San Jose)

| | | | |
|--------------------------------------|--|----------------------|----------------------|
| Stress Method | MIL-STD 883 Method 1033 | | |
| Stress Condition | $T_a = 85^{\circ}\text{C} / V_{cc} = 5\text{V} / 100,000 \text{ cycles (Write 0x00h)}$ | | |
| Min Sample Size Test Temperatures | 231 pieces/lot 25C, -40C, 85C, 125C | | |
| Lot #; Fail / Pass | Lot 2 0 Fails / 246 | Lot 3 0 Fails / 246 | Lot 4 0 Fails / 246 |
| Stress Method | JESD22A-103 | | |
| Stress Condition | $T_a = 175^{\circ}\text{C} 504 \text{ hours}$ | | |
| Min Sample Size Test Temperatures | 231 pieces/lot 25C, -40C, 85C, 125C | | |
| Readpoint 1 | 504 hours | | |
| Lot #; Fail / Pass | Lot 2; 0 Fails / 246 | Lot 3; 0 Fails / 246 | Lot 4; 0 Fails / 246 |

Endurance Testing (Stress conducted at MCHP San Jose)

| | |
|--------------------------------------|---|
| Test Method | MIL-STD 883 Method 1033 |
| Test Condition | T _a = +25 ⁰ C / V _{CC} = 5V / 1,000,000 cycles Write 0x00h |
| Min Sample Size | Not Required |
| Readpoint 1 – 9 | Every 100,000 Cycles |
| Lot #; Fail / Pass, Test Criteria | Lot 2; 0 / 92, QC Test +25C |
| Readpoint 10 | 1,000,000 Cycles |
| Lot #; Fail / Pass, Test Criteria | Lot 2; 0 / 92, QC Test +25C, -40C, +85C, +125C 0 / 10. Margin Test at +25C |

Early Life Reliability (ELFR) + Dynamic Life Test (Stress conducted at MTAI)

| | | | |
|-------------------|---|---------------------|---------------------|
| Stress Method | MIL-STD 883 Method 1005 | | |
| Stress Condition | T _a = 150°C / V _{CC} = 5.5V / 408 hours | | |
| Min Sample Size | ELFR 800 Pieces/Lot, 0 Fails | | |
| Readpoint 1 | 24 hours | | |
| Test Temperatures | 25C, -40C, 85C, 125C | | |
| Lot# Fail / Pass | Lot 2 0 / 815 | Lot 3 0 Fails / 815 | Lot 4 0 Fails / 814 |
| Min Sample Size | DLT 600 Pieces/Lot, 0 Fails | | |
| Readpoint 2 | +312 hours (408 Total) | | |
| Test Temperatures | 25C, -40C, 85C, 125C | | |
| Lot# Fail / Pass | Lot 2 0 / 615 | Lot 3 0 Fails / 615 | Lot 4 0 Fails / 615 |

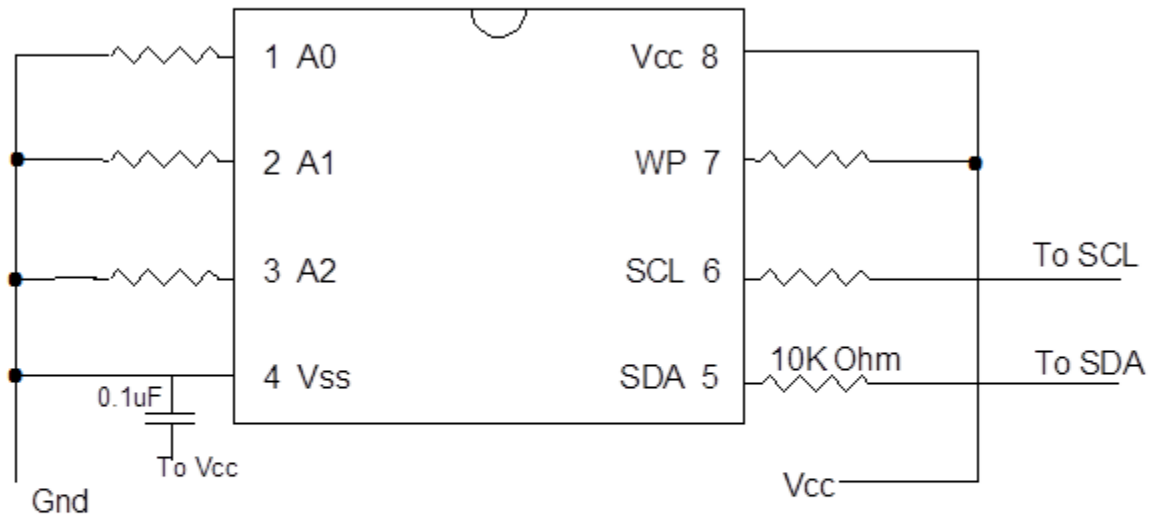
Note: Lot 4 had one device fail due to an ESD/EOS event after 24 hours stress that is unrelated to any deficiency in the product and is not considered a stress fail. Corrective Actions have been defined by MTHAI

ESD & Latchup Characterization (Stress conducted at MCHP San Jose)

| Test | Sample Size | Reference Method | Result |
|------------------|-------------|-------------------|--------------|
| ESD – HBM | 12 | JEDEC JS-001-2017 | Pass ±5000 V |
| CDM | 18 | JEDEC JS-002 | Pass ±1500 V |
| Latch Up @ 25°C | 6 | JESD78 | 200mAmp Pass |
| Latch Up @ 125°C | 6 | JESD78 | 200mAmp Pass |

V. Burn-in schematic for DLT, ELFR, and END Stress Tests:

66829 DLT SCHEMATIC
24xx512 8L DIP/SO1x PACKAGE



Notes: All resistors are 1K, 1/4 Watt, except where noted.

Only Vss and Vcc are hardwired. All other pins are wired through a programmable header at the top of the burn-in board.

Use standard 2-wire burn-in program, 400KHz, 5.5V.