
HM628512B Series

4 M SRAM (512-kword × 8-bit)

HITACHI

ADE-203-903D (Z)

Rev. 3.0

Aug. 24, 1999

Description

The Hitachi HM628512B is a 4-Mbit static RAM organized 512-kword × 8-bit. It realizes higher density, higher performance and low power consumption by employing 0.35 μm Hi-CMOS process technology. The device, packaged in a 525-mil SOP (foot print pitch width) or 400-mil TSOP TYPE II or 600-mil plastic DIP, is available for high density mounting. The HM628512B is suitable for battery backup system.

Features

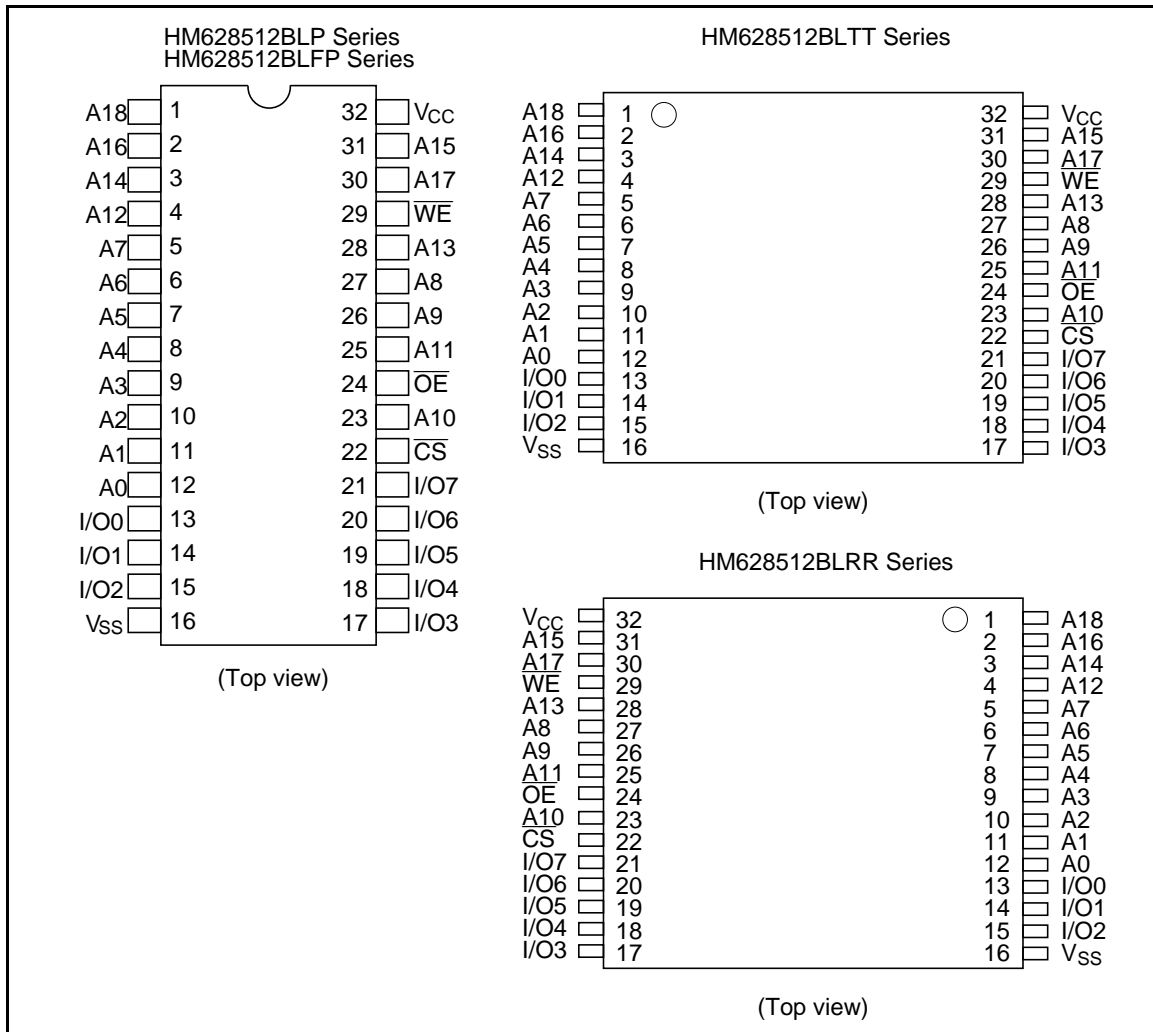
- Single 5 V supply
- Access time: 55/70 ns (max)
- Power dissipation
 - Active: 50 mW/MHz (typ)
 - Standby: 10 μW (typ)
- Completely static memory. No clock or timing strobe required
- Equal access and cycle times
- Common data input and output: Three state output
- Directly TTL compatible: All inputs and outputs
- Battery backup operation

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Ordering Information

Type No.	Access time	Package
HM628512BLP-5	55 ns	600-mil 32-pin plastic DIP (DP-32)
HM628512BLP-7	70 ns	
HM628512BLP-5SL	55 ns	
HM628512BLP-7SL	70 ns	
HM628512BLP-5UL	55 ns	
HM628512BLP-7UL	70 ns	
HM628512BLFP-5	55 ns	525-mil 32-pin plastic SOP (FP-32D)
HM628512BLFP-7	70 ns	
HM628512BLFP-5SL	55 ns	
HM628512BLFP-7SL	70 ns	
HM628512BLFP-5UL	55 ns	
HM628512BLFP-7UL	70 ns	
HM628512BLTT-5	55 ns	400-mil 32-pin plastic TSOP II (TTP-32D)
HM628512BLTT-7	70 ns	
HM628512BLTT-5SL	55 ns	
HM628512BLTT-7SL	70 ns	
HM628512BLTT-5UL	55 ns	
HM628512BLTT-7UL	70 ns	
HM628512BLRR-5	55 ns	400-mil 32-pin plastic TSOP II reverse (TTP-32DR)
HM628512BLRR-7	70 ns	
HM628512BLRR-5SL	55 ns	
HM628512BLRR-7SL	70 ns	
HM628512BLRR-5UL	55 ns	
HM628512BLRR-7UL	70 ns	

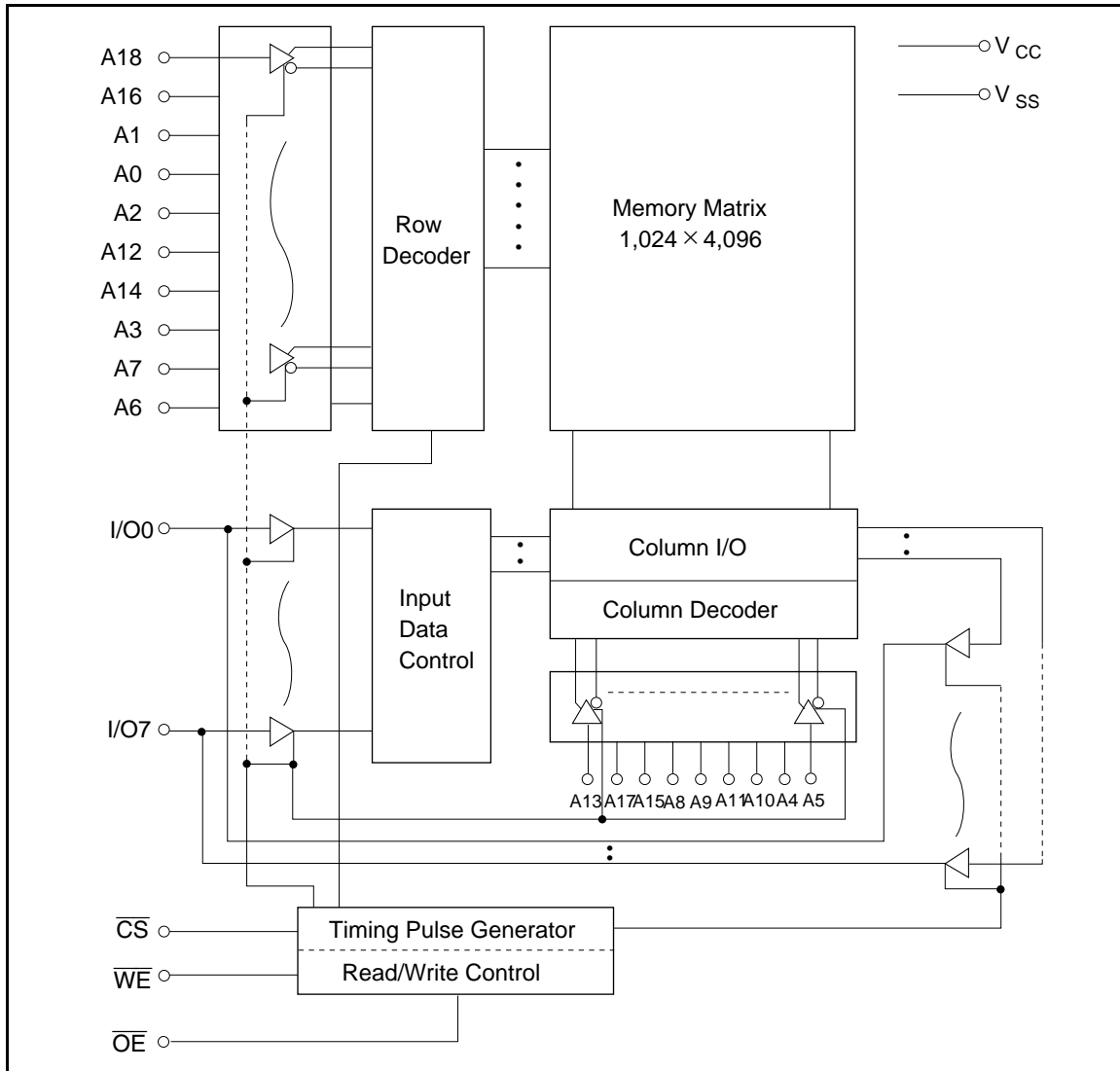
Pin Arrangement



Pin Description

Pin name	Function
A0 to A18	Address input
I/O0 to I/O7	Data input/output
CS	Chip select
OE	Output enable
WE	Write enable
V _{CC}	Power supply
V _{SS}	Ground

Block Diagram



Function Table

\overline{WE}	\overline{CS}	\overline{OE}	Mode	V_{CC} current	Dout pin	Ref. cycle
x	H	x	Not selected	I_{SB}, I_{SB1}	High-Z	—
H	L	H	Output disable	I_{CC}	High-Z	—
H	L	L	Read	I_{CC}	Dout	Read cycle
L	L	H	Write	I_{CC}	Din	Write cycle (1)
L	L	L	Write	I_{CC}	Din	Write cycle (2)

Note: x: H or L

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Power supply voltage	V_{CC}	-0.5 to +7.0	V
Voltage on any pin relative to V_{SS}	V_T	-0.5 ^{*1} to $V_{CC} + 0.3$ ^{*2}	V
Power dissipation	P_T	1.0	W
Operating temperature	T_{opr}	-20 to +70	°C
Storage temperature	T_{stg}	-55 to +125	°C
Storage temperature under bias	T_{bias}	-20 to +85	°C

Notes: 1.-3.0 V for pulse half-width ≤ 30 ns
2.Maximum voltage is 7.0 V

Recommended DC Operating Conditions ($T_a = -20$ to $+70$ °C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input high voltage	V_{IH}	2.2	—	$V_{CC} + 0.3$	V
Input low voltage	V_{IL}	-0.3 ^{*1}	—	0.8	V

Note: 1.-3.0 V for pulse half-width ≤ 30 ns

DC Characteristics ($T_a = -20$ to $+70$ °C, $V_{CC} = 5$ V ±10% , $V_{SS} = 0$ V)

Parameter	Symbol	Min	Typ ^{*1}	Max	Unit	Test conditions
Input leakage current	$ I_{LI} $	—	—	1	μA	$V_{in} = V_{SS}$ to V_{CC}
Output leakage current	$ I_{LO} $	—	—	1	μA	$\overline{CS} = V_{IH}$ or $\overline{OE} = V_{IH}$ or $\overline{WE} = V_{IL}$, $V_{I/O} = V_{SS}$ to V_{CC}
Operating power supply current: DC	I_{CC}	—	8	15	mA	$\overline{CS} = V_{IL}$, others = V_{IH}/V_{IL} , $I_{I/O} = 0$ mA
Operating power supply current	I_{CC1}	—	40	60	mA	Min cycle, duty = 100% $\overline{CS} = V_{IL}$, others = V_{IH}/V_{IL} $I_{I/O} = 0$ mA
Operating power supply current	I_{CC2}	—	10	20	mA	Cycle time = 1 μs, duty = 100% $I_{I/O} = 0$ mA, $\overline{CS} \leq 0.2$ V $V_{IH} \geq V_{CC} - 0.2$ V, $V_{IL} \leq 0.2$ V
Standby power supply current: DC	I_{SB}	—	1	3	mA	$\overline{CS} = V_{IH}$
Standby power supply current (1): DC	I_{SB1}	—	2 ^{*2}	100 ^{*2}	μA	$V_{in} \geq 0$ V, $\overline{CS} \geq V_{CC} - 0.2$ V
		—	2 ^{*3}	50 ^{*3}	μA	
		—	2 ^{*4}	20 ^{*4}	μA	
Output low voltage	V_{OL}	—	—	0.4	V	$I_{OL} = 2.1$ mA
Output high voltage	V_{OH}	2.4	—	—	V	$I_{OH} = -1.0$ mA

Notes: 1. Typical values are at $V_{CC} = 5.0$ V, $T_a = +25$ °C and specified loading, and not guaranteed.
2. This characteristics is guaranteed only for L version.
3. This characteristics is guaranteed only for L-SL version.

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4.This characteristics is guaranteed only for L-UL version.

Capacitance (Ta = +25°C, f = 1 MHz)

Parameter	Symbol	Typ	Max	Unit	Test conditions
Input capacitance*1	C _{in}	—	8	pF	V _{in} = 0 V
Input/output capacitance*1	C _{I/O}	—	10	pF	V _{I/O} = 0 V

Note: 1.This parameter is sampled and not 100% tested.

AC Characteristics (Ta = -20 to +70°C, V_{CC} = 5 V ± 10%, unless otherwise noted.)

Test Conditions

- Input pulse levels: 0.8 V to 2.4 V
- Input rise and fall time: 5 ns
- Input and output timing reference levels: 1.5 V
- Output load: 1 TTL Gate + C_L (100 pF) (HM628512B-7)
1 TTL Gate + C_L (50 pF) (HM628512B-5)
(Including scope & jig)

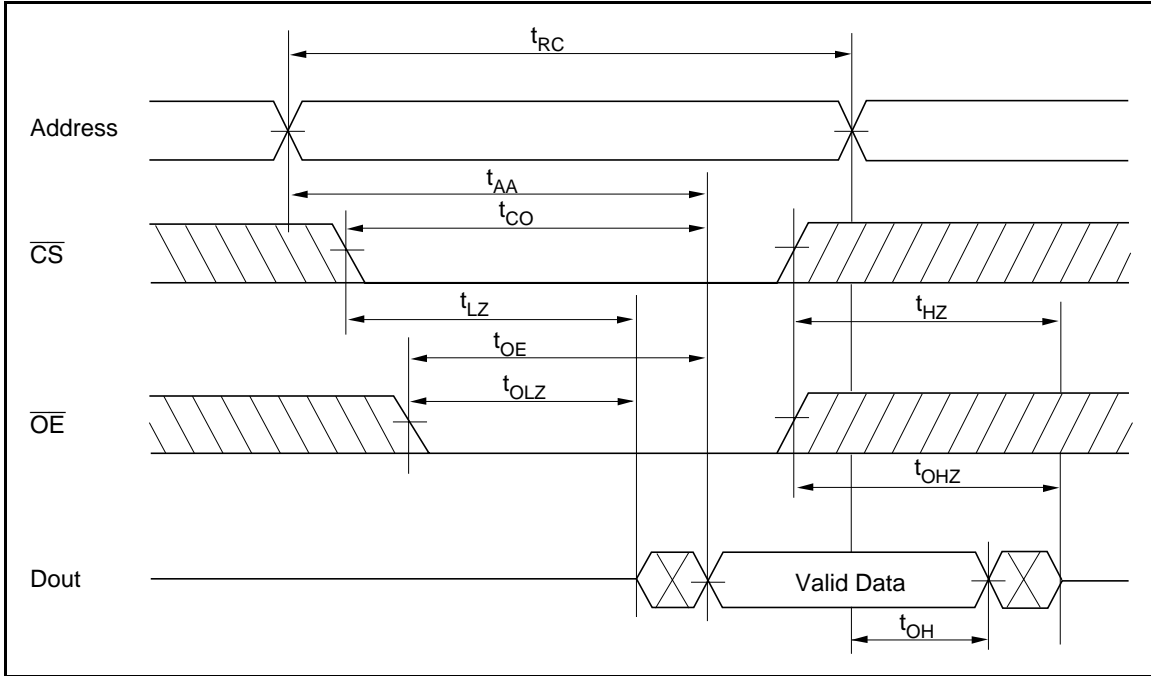
Read Cycle

HM628512B							
		-5		-7			
Parameter	Symbol	Min	Max	Min	Max	Unit	Notes
Read cycle time	t _{RC}	55	—	70	—	ns	
Address access time	t _{AA}	—	55	—	70	ns	
Chip select access time	t _{CO}	—	55	—	70	ns	
Output enable to output valid	t _{OE}	—	25	—	35	ns	
Chip selection to output in low-Z	t _{LZ}	10	—	10	—	ns	2
Output enable to output in low-Z	t _{OLZ}	5	—	5	—	ns	2
Chip deselection to output in high-Z	t _{HZ}	0	20	0	25	ns	1, 2
Output disable to output in high-Z	t _{OHZ}	0	20	0	25	ns	1, 2
Output hold from address change	t _{OH}	10	—	10	—	ns	

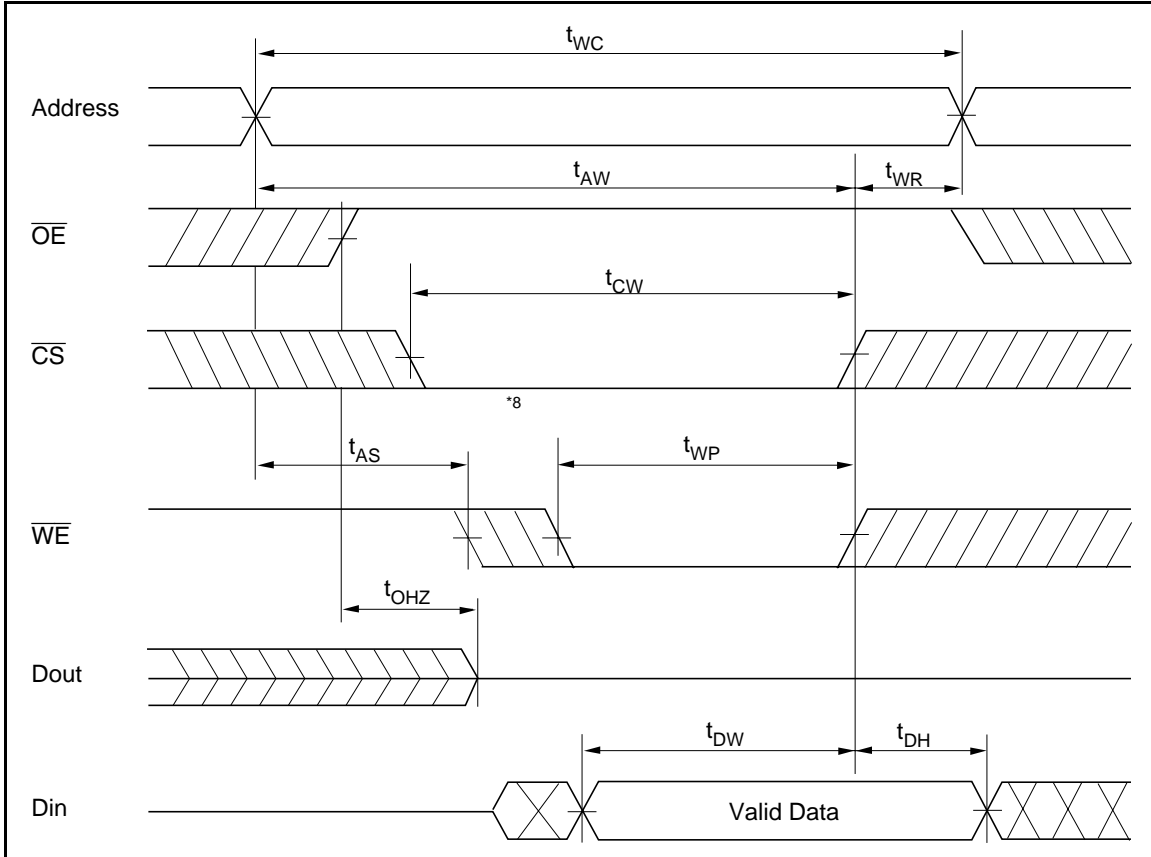
HM628512B Series

Timing Waveforms

Read Timing Waveform ($\overline{WE} = V_{IH}$)

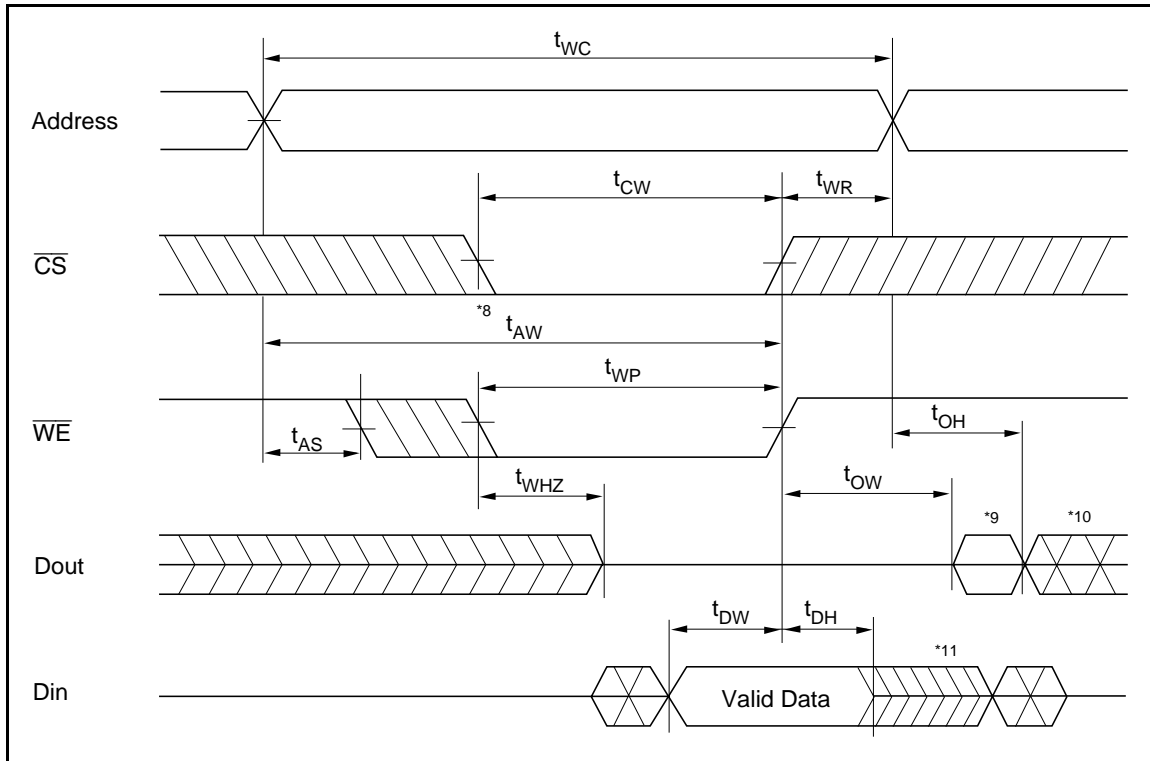


Write Timing Waveform (1) ($\overline{\text{OE}}$ Clock)



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Write Timing Waveform (2) ($\overline{\text{OE}}$ Low Fixed)

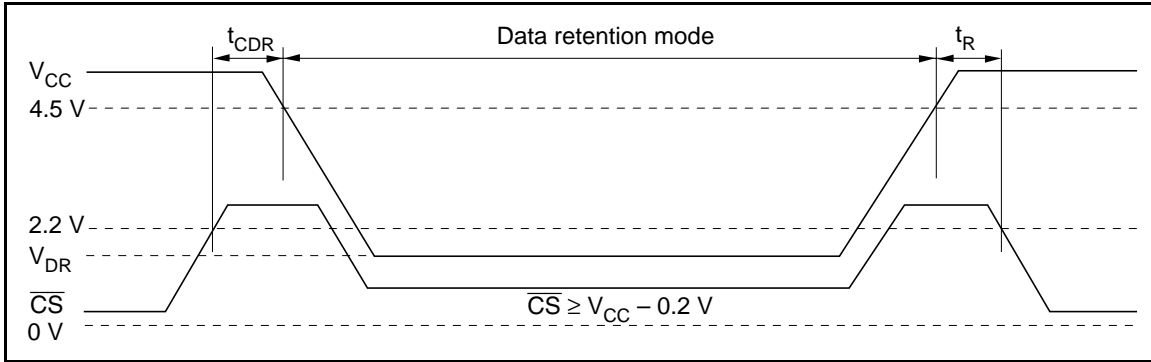


Low V_{CC} Data Retention Characteristics ($T_a = -20$ to $+70^\circ\text{C}$)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions*4
V_{CC} for data retention	V_{DR}	2	—	—	V	$\overline{\text{CS}} \geq V_{CC} - 0.2 \text{ V}$, $V_{in} \geq 0 \text{ V}$
Data retention current	I_{CCDR}	—	1^{*5}	50^{*1}	μA	$V_{CC} = 3.0 \text{ V}$, $V_{in} \geq 0 \text{ V}$
		—	1^{*5}	15^{*2}	μA	$\overline{\text{CS}} \geq V_{CC} - 0.2 \text{ V}$
		—	1^{*5}	10^{*3}	μA	
Chip deselect to data retention time	t_{CDR}	0	—	—	ns	See retention waveform
Operation recovery time	t_R	t_{RC}^{*6}	—	—	ns	

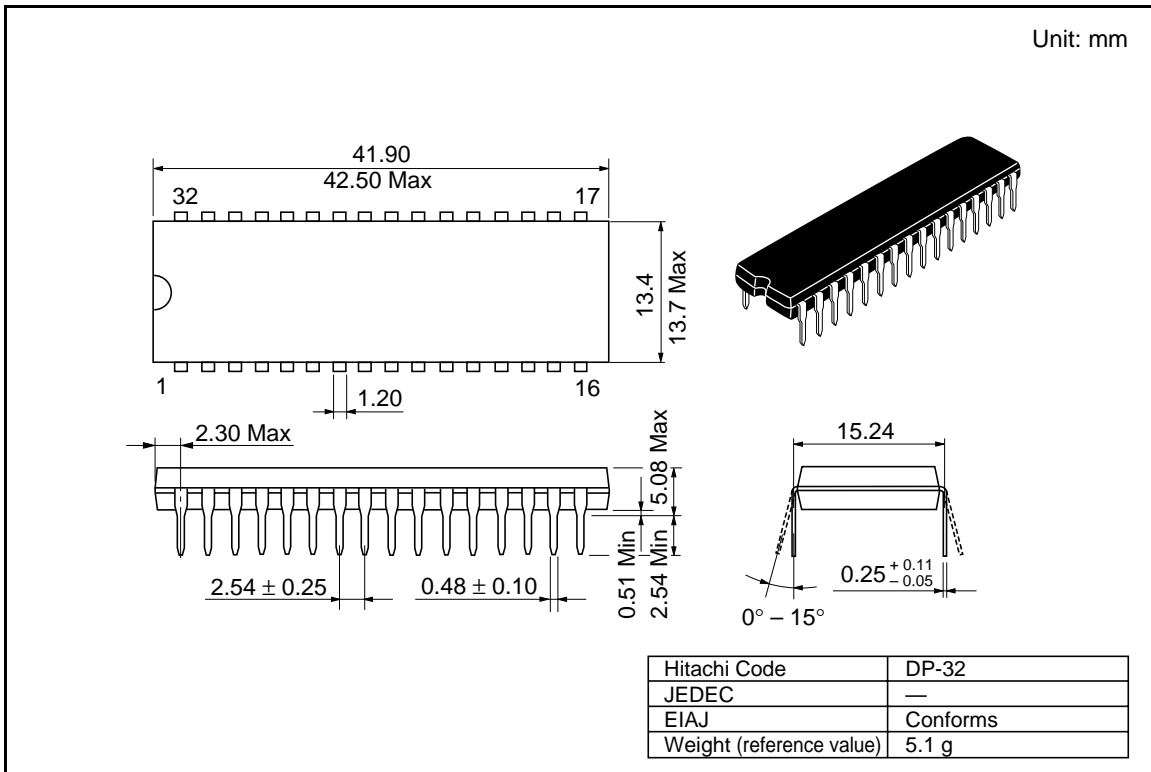
- Notes:
1. For L-version and $20 \mu\text{A}$ (max.) at $T_a = -20$ to $+40^\circ\text{C}$.
 2. For L-SL-version and $3 \mu\text{A}$ (max.) at $T_a = -20$ to $+40^\circ\text{C}$.
 3. For L-UL-version and $3 \mu\text{A}$ (max.) at $T_a = -20$ to $+40^\circ\text{C}$.
 4. $\overline{\text{CS}}$ controls address buffer, $\overline{\text{WE}}$ buffer, $\overline{\text{OE}}$ buffer, and Din buffer. In data retention mode, V_{in} levels (address, $\overline{\text{WE}}$, $\overline{\text{OE}}$, I/O) can be in the high impedance state.
 5. Typical values are at $V_{CC} = 3.0 \text{ V}$, $T_a = +25^\circ\text{C}$ and specified loading, and not guaranteed.
 6. t_{RC} = read cycle time.

Low V_{CC} Data Retention Timing Waveform (\overline{CS} Controlled)



Package Dimensions

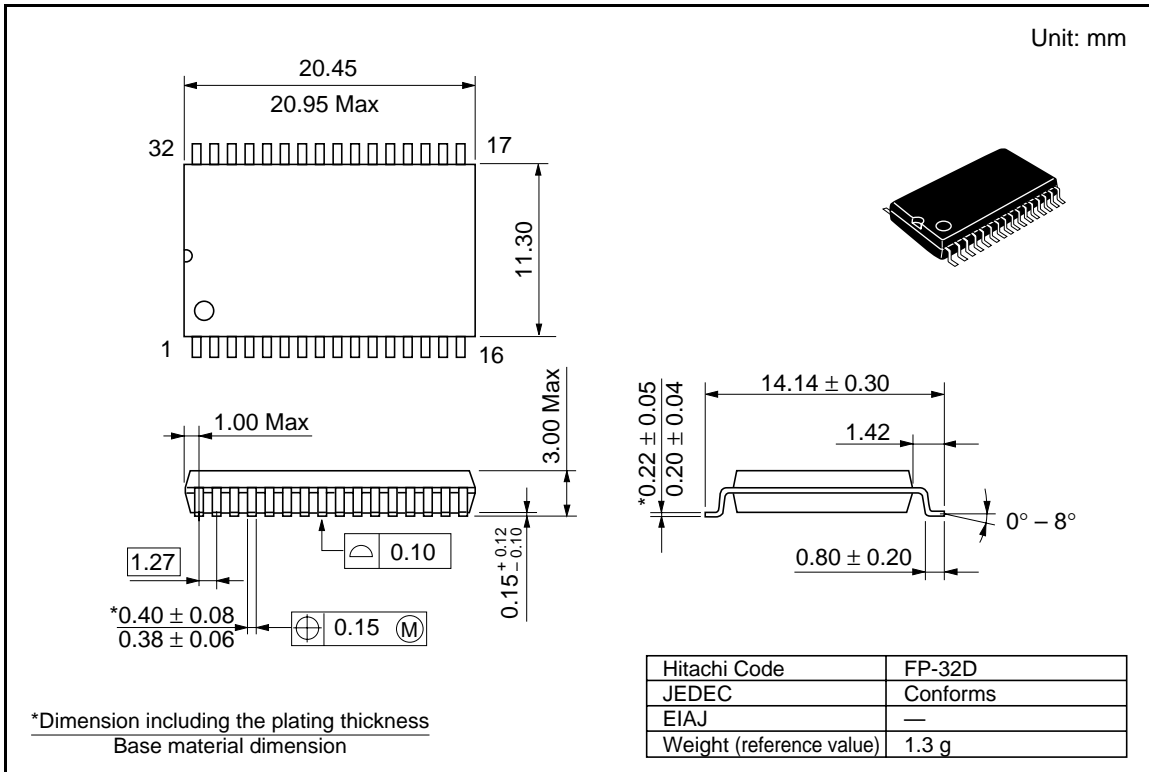
HM628512BLP Series (DP-32)



HM628512B Series

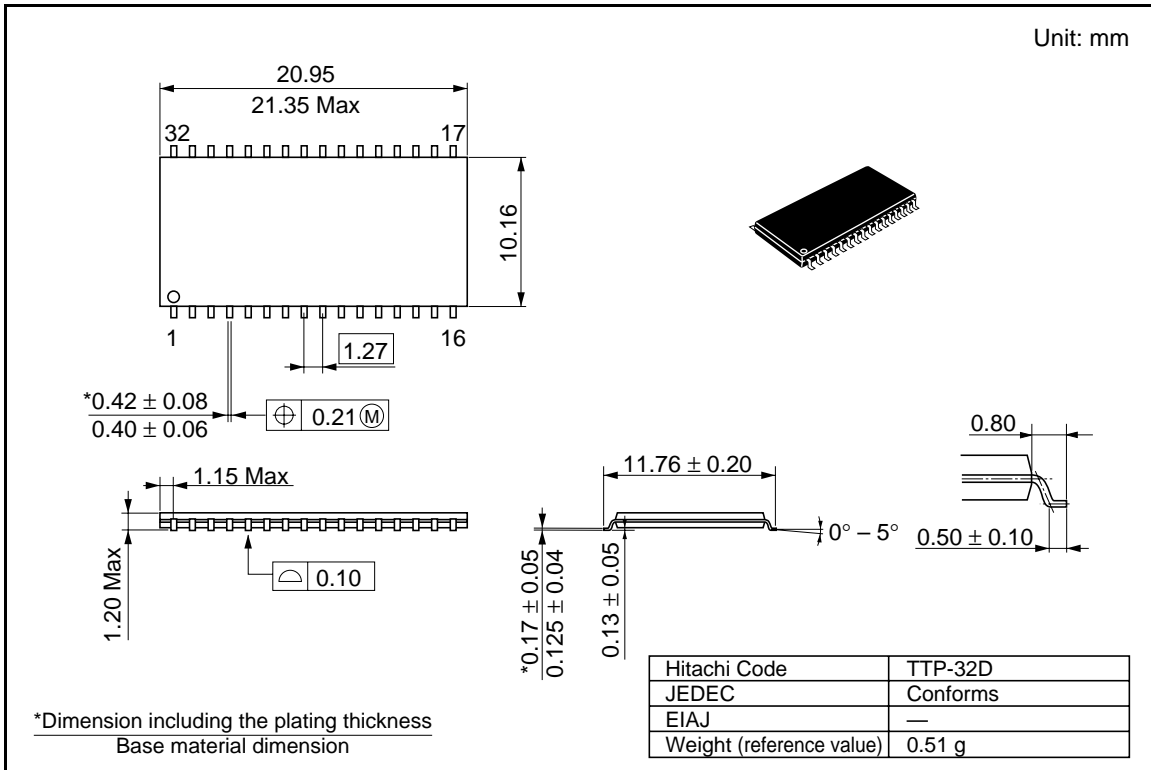
Package Dimensions (cont.)

HM628512BLFP Series (FP-32D)



Package Dimensions (cont.)

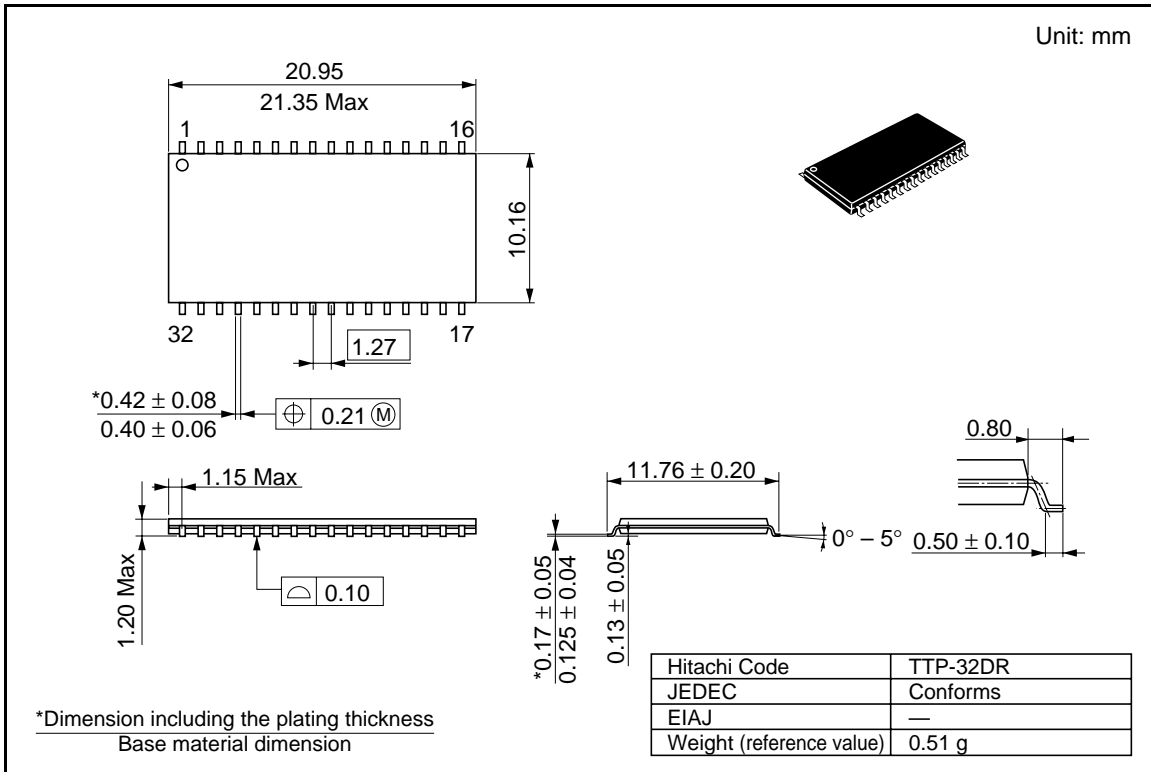
HM628512BLTT Series (TTP-32D)



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Package Dimensions (cont.)

HM628512BLRR Series (TTP-32DR)



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HM628512B Series

Revision Record

Rev.	Date	Contents of Modification	Drawn by	Approved by
0.0	Apr. 24, 1998	Initial issue	M. Higuchi	K. Imato
0.1	Nov. 19, 1998	DC Characteristics I_{SB1} max: 40/20 μ A to 100/50 μ A Low V_{CC} Data Retention Characteristics I_{CCDR} max: 20/10 μ A to 50/15 μ A Change of note1 and 2	S. kunito	K. Imato
1.0	Jan. 13, 1999	Deletion of Preliminary Features Change of Power dissipation Standby: TBD (typ) to 10 μ W (typ) DC Characteristics I_{SB1} typ: TBD/TBD to 2/2 μ A Low V_{CC} Data Retention Characteristics I_{CCDR} typ: TBD/TBD to 1/1 μ A	S. kunito	K. Imato
2.0	Apr. 8, 1999	Addition of L-UL-version DC Characteristics I_{SB1} typ: 2/2 μ A to 2/2/2 μ A I_{SB1} max: 100/50 μ A to 100/50/20 μ A Addition of note4 Low V_{CC} Data Retention Characteristics I_{CCDR} typ: 1/1 μ A to 1/1/1 μ A I_{CCDR} max: 50/15 μ A to 50/15/10 μ A Addition of note3	S. kunito	K. Makuta
3.0	Aug. 24, 1999	Low V_{CC} Data Retention Characteristics Correct error: t_R unit ms to ns		