

FEATURES

- 14V/μs Slew Rate: 10V/μs Min
- 5MHz Gain-Bandwidth Product
- Fast Settling Time: 1.3μs to 0.02%
- 150μV Offset Voltage (LT1057): 450μV Max
- 180μV Offset Voltage (LT1058): 600μV Max
- 2μV/°C V_{OS} Drift: 7μV/°C Max
- 50pA Bias Current at 70°C
- Low Voltage Noise:
 - 13nV/√Hz at 1kHz
 - 26nV/√Hz at 10Hz

APPLICATIONS

- Precision, High Speed Instrumentation
- Fast, Precision Sample-and-Hold
- Logarithmic Amplifiers
- D/A Output Amplifiers
- Photodiode Amplifiers
- Voltage-to-Frequency Converters
- Frequency-to-Voltage Converters

DESCRIPTION

The LT®1057 is a matched JFET input dual op amp in the industry standard 8-pin configuration, featuring a combination of outstanding high speed and precision specifications. It replaces all the popular bipolar and JFET input dual op amps. In particular, the LT1057 upgrades the performance of systems using the LF412A and OP-215 JFET input duals.

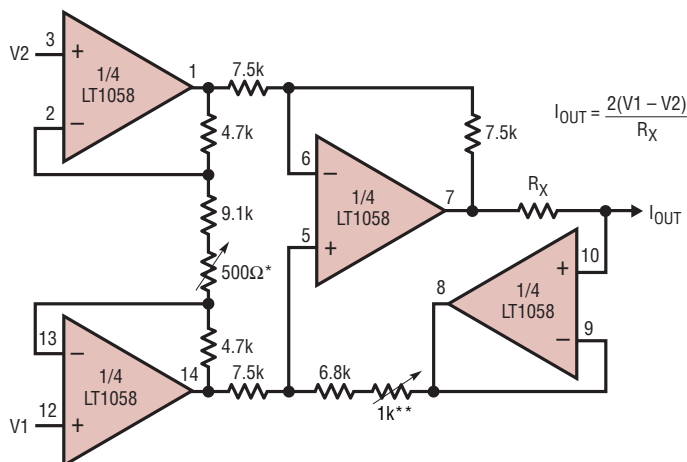
The LT1058 is the lowest offset quad JFET input operational amplifier in the standard 14-pin configuration. It offers significant accuracy improvement over presently available JFET input quad operational amplifiers. The LT1058 can replace four single precision JFET input op amps, while saving board space, power dissipation and cost.

Both the LT1057 and LT1058 are available in the plastic PDIP package and the surface mount SO package.

LT, LT, LTC and LTM are registered trademarks of Linear Technology Corporation. All other trademarks are the property of their respective owners.

TYPICAL APPLICATION

**Current Output, High Speed, High Input Impedance
Instrumentation Amplifier**

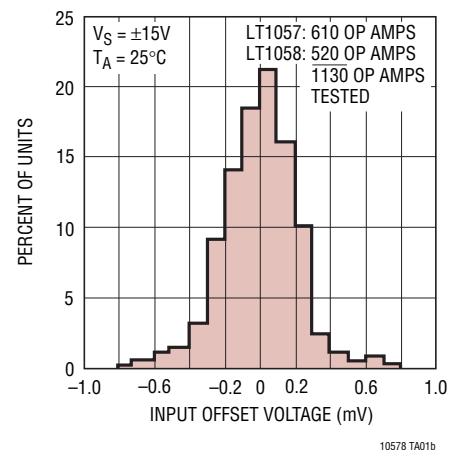


*GAIN ADJUST

**COMMON MODE REJECTION ADJUST
BANDWIDTH ≈ 2MHz

10578 TA01

**Distribution of Offset Voltage
(All Packages, LT1057 and LT1058)**



10578 TA01b

LT1057/LT1058

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage $\pm 20V$
 Differential Input Voltage $\pm 40V$
 Input Voltage $\pm 20V$
 Output Short-Circuit Duration Indefinite
 Storage Temperature Range $-65^{\circ}C$ to $150^{\circ}C$
 Lead Temperature (Soldering, 10 sec) $300^{\circ}C$

Operating Temperature Range

LT1057AM/LT1057M/
 LT1058AM/LT1058M (**OBSOLETE**) $-55^{\circ}C$ to $125^{\circ}C$
 LT1057AC/LT1057C/LT1057S
 LT1058AC/LT1058C/LT1058S $0^{\circ}C$ to $70^{\circ}C$
 LT1057I/LT1058I $-40^{\circ}C \leq T_A \leq 85^{\circ}C$

PACKAGE/ORDER INFORMATION

TOP VIEW SW PACKAGE 16-LEAD PLASTIC (WIDE) SO $T_{JMAX} = 150^{\circ}C$, $\theta_{JA} = 90^{\circ}C/W$	TOP VIEW SW PACKAGE 16-LEAD PLASTIC (WIDE) SO $T_{JMAX} = 150^{\circ}C$, $\theta_{JA} = 90^{\circ}C/W$	TOP VIEW S8 PACKAGE 8-LEAD PLASTIC SO $T_{JMAX} = 150^{\circ}C$, $\theta_{JA} = 200^{\circ}C/W$ Please note that the LT1057S8/LT1057IS8 standard surface mount pin-out differs from that of the LT1057 standard CERPDP/DPID packages.	ORDER PART NUMBER LT1057S8 LT1057IS8 S8 PART MARKING 1057 1057I
ORDER PART NUMBER LT1057SW LT1057ISW	ORDER PART NUMBER LT1058SW LT1058ISW	TOP VIEW H PACKAGE 8-LEAD METAL CAN	ORDER PART NUMBER LT1057AMH LT1057MH LT1057ACH LT1057CH
TOP VIEW N14 PACKAGE 14-LEAD PDIP $T_{JMAX} = 125^{\circ}C$, $\theta_{JA} = 130^{\circ}C/W$ J14 PACKAGE 14-LEAD CERPDP $T_{JMAX} = 150^{\circ}C$, $\theta_{JA} = 100^{\circ}C/W$	ORDER PART NUMBER LT1058ACN LT1058CN LT1058AMJ LT1058MJ LT1058ACJ LT1058CJ	ORDER PART NUMBER LT1057ACN8 LT1057CN8 LT1057ACJ8 LT1057CJ8 LT1057AMJ8 LT1057MJ8	TOP VIEW N8 PACKAGE 8-LEAD PDIP $T_{JMAX} = 125^{\circ}C$, $\theta_{JA} = 130^{\circ}C/W$ J8 PACKAGE 8-LEAD CERPDP $T_{JMAX} = 150^{\circ}C$, $\theta_{JA} = 100^{\circ}C/W$

Order Options Tape and Reel: Add #TR

Lead Free: Add #PBF Lead Free Tape and Reel: Add #TRPBF

Lead Free Part Marking: <http://www.linear.com/leadfree/>

Consult LTC Marketing for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS $V_S = \pm 15V$, $T_A = 25^\circ C$, $V_{CM} = 0V$ unless otherwise noted. (Note 2)

SYMBOL	PARAMETER	CONDITIONS	LT1057AM/LT1058AM LT1057AC/LT1058AC			LT1057M/LT1058M LT1057C/LT1058C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{OS}	Input Offset Voltage	LT1057 LT1057 (S8 Package) LT1058		150 180	450 600		200 220 250	800 1200 1000	μV μV μV
I_{OS}	Input Offset Current	Fully Warmed Up		3	40		4	50	pA
I_B	Input Bias Current	Fully Warmed Up		± 5	± 50		± 7	± 75	pA
	Input Resistance	Differential Common Mode $V_{CM} = -11V$ to $8V$ Common Mode $V_{CM} = 8V$ to $11V$		10^{12} 10^{12} 10^{11}			10^{12} 10^{12} 10^{11}		Ω Ω Ω
	Input Capacitance			4			4		pF
e_n	Input Noise Voltage	0.1Hz to 10Hz LT1057 LT1058			2.0 2.4			2.1 2.5	μV_{P-P} μV_{P-P}
e_n	Input Noise Voltage Density	$f_0 = 10Hz$ $f_0 = 1kHz$ (Note 3)		26 13	22		28 14	24	$nV/\sqrt{Hz}$ $nV/\sqrt{Hz}$
i_n	Input Noise Current Density	$f_0 = 10Hz, 1kHz$ (Note 4)		1.5	4		1.8	6	$fA/\sqrt{Hz}$
A_{VOL}	Large-Signal Voltage Gain	$V_0 = \pm 10V$, $R_L = 2k$ $V_0 = \pm 10V$, $R_L = 1k$	150 120	350 250		100 80	300 220		V/mV V/mV
	Input Voltage Range		± 10.5	14.3 -11.5		± 10.5	14.3 -11.5		V V
CMRR	Common Mode Rejection Ratio	LT1057 LT1058	86 84	100 98		82 80	98 96		dB dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 10V$ to $\pm 18V$	88	103		86	102		dB
V_{OUT}	Output Voltage Swing	$R_L = 2k$	± 12	± 13		± 12	± 13		V
SR	Slew Rate		10	14		8	13		V/ μs
GBW	Gain-Bandwidth Product	$f = 1MHz$ (Note 6)	3.5	5		3	5		MHz
I_S	Supply Current Per Amplifier			1.6	2.5		1.7	2.8	mA
	Channel Separation	DC to 5kHz, $V_{IN} = \pm 10V$		132			130		dB

(LT1057/LT1058 SW Package Only), $V_S = \pm 15V$, $T_A = 25^\circ C$, $V_{CM} = 0V$ unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	LT1057 LT1058		0.3 0.35	2 2.5	mV
I_{OS}	Input Offset Current	Fully Warmed Up		5	50	pA
I_B	Input Bias Current	Fully Warmed Up		± 10	± 100	pA
	Input Resistance –Differential –Common Mode	$V_{CM} = -11V$ to $8V$ $V_{CM} = 8V$ to $11V$		0.4 0.4 0.05		$T\Omega$
	Input Capacitance			4		pF
e_n	Input Noise Voltage	0.1Hz to 10Hz LT1057 LT1058		2.1 2.5		μV_{P-P}
e_n	Input Noise Voltage Density	$f_0 = 10Hz$ $f_0 = 1kHz$		26 13		$nV/\sqrt{Hz}$

LT1057/LT1058

ELECTRICAL CHARACTERISTICS (LT1057/LT1058 SW Package Only), $V_S = \pm 15V$, $T_A = 25^\circ C$, $V_{CM} = 0V$ unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
i_n	Input Noise Current Density	$f_0 = 10Hz, 1kHz$		1.8		$fA/\sqrt{Hz}$
A_{VOL}	Large-Signal Voltage Gain	$V_0 = \pm 10V$ $R_L = 2k$ $R_L = 1k$	100 50	300 220		V/mV
	Input Voltage Range		± 10.5	14.3 -11.5		V
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm 15V$ LT1057 LT1058	82 80	98 98		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 10V$ to $\pm 18V$	86	102		dB
V_{OUT}	Output Voltage Swing	$R_L = 2k$	± 12	± 13		V
SR	Slew Rate		8	13		V/ μs
GBW	Gain-Bandwidth Product	$f = 1MHz$ (Note 6)	3	5		MHz
I_S	Supply Current Per Amplifier			1.7	2.8	mA
	Channel Separation	DC to 5kHz, $V_{IN} = \pm 10V$		130		dB

The ● denotes the specifications which apply over the temperature range of $0^\circ C \leq T_A \leq 70^\circ C$ or $-40^\circ C \leq T_A \leq 85^\circ C$ (LT1057IS8), otherwise specifications are $T_A = 25^\circ C$. $V_S = \pm 15V$, $V_{CM} = 0V$, unless noted.

SYMBOL	PARAMETER	CONDITIONS		LT1057AC LT1058AC			LT1057C LT1058C			UNITS
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{OS}	Input Offset Voltage	LT1057 LT1057IS8 LT1057S8 LT1058	● ● ● ●		250	800		330 500 400 400	1400 2300 1900 1800	μV μV μV μV
	Average Temperature Coefficient of Input (Offset Voltage)	LT1057 H/J8 Package N8 Package LT1057S8 (Note 5) LT1057IS8 (Note 5) LT1058 J Package (Note 5) N Package (Note 5)	● ● ● ● ● ●		1.8 3	7 10		2.3 4 4 4.5 3 5	12 16 16 16 15 22	$\mu V/^\circ C$ $\mu V/^\circ C$ $\mu V/^\circ C$ $\mu V/^\circ C$ $\mu V/^\circ C$ $\mu V/^\circ C$
I_{OS}	Input Offset Current	Warmed Up, $T_A = 70^\circ C$ LT1057IS8	●		18	150		20 35	250 600	pA
I_B	Input Bias Current	Warmed Up, $T_A = 70^\circ C$ LT1057IS8	●		± 50	± 250		± 60 ± 100	± 350 ± 900	pA
A_{VOL}	Large-Signal Voltage Gain	$V_0 = \pm 10V$, $R_L = 2k$	●	70	220		50	200		V/mV
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm 10.4V$	●	85	98		80	96		dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 10V$ to $\pm 18V$	●	87	102		84	100		dB
V_{OUT}	Output Voltage Swing	$R_L = 2k$	●	± 12	± 12.8		± 12	± 12.8		V
I_S	Supply Current Per Amplifier	$T_A = 70^\circ C$	●			2.8			3.2	mA mA
					14			1.5		

ELECTRICAL CHARACTERISTICS (LT1057/LT1058 SW Package Only). The ● denotes specifications which apply over the temperature range of $V_S = \pm 15V$, $V_{CM} = 0V$, $0^\circ C \leq T_A \leq 70^\circ C$ (LT1057SW, LT1058SW) or $-40^\circ C \leq T_A \leq 85^\circ C$ (LT1057ISW, LT1058ISW), unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS			MIN	TYP	MAX	UNITS
V _{OS}	Input Offset Voltage	LT1057 LT1058S LT1058IS	● ● ●			0.5 0.6 0.7	2.5 3.0 4.0	mV
	Average Temperature Coefficient of Input Offset Voltage		●			5		μV/°C
I _{OS}	Input Offset Current	Warmed Up, T _A = 70°C Warmed Up, T _A = 85°C				20 35	250 400	pA
I _B	Input Bias Current	Warmed Up, T _A = 70°C Warmed Up, T _A = 85°C				±60 ±100	±400 ±700	pA
A _{VOL}	Large-Signal Voltage Gain	V _O = ±10V, R _L = 2k	LT1057 LT1058	● ●	50 40	200 200		mV
CMRR	Common Mode Rejection Ratio	V _{CM} = ±10.5V	LT1057 LT1058	● ●	80 78	96 96		dB
PSRR	Power Supply Rejection Ratio	V _S = ±10V to ±18V	LT1057 LT1058	● ●	84 82	100 100		dB
V _{OUT}	Output Voltage Swing	R _L = 2k		●	±12	±12.8		V

The ● denotes the specifications which apply over the temperature range of $-55^\circ C \leq T_A \leq 125^\circ C$, $V_S = \pm 15V$, $V_{CM} = 0V$, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	LT1057AM LT1058AM			LT1057M LT1058M			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{OS}	Input Offset Voltage	LT1057 LT1058	● ●	300 380	1100 1600		400 550	2000 2500	μV μV
	Average Temperature Coefficient of Input Offset Voltage	LT1057 LT1058 (Note 5)	● ●	2.0 2.5	7 10		2.5 3	12 15	$\mu V/^\circ C$ $\mu V/^\circ C$
I_{OS}	Input Offset Current	Warmed Up, $T_A = 125^\circ C$		0.15	2		0.2	3	nA
I_B	Input Bias Current	Warmed Up, $T_A = 125^\circ C$		± 0.6	± 4.5		± 0.7	± 6	nA
A_{VOL}	Large-Signal Voltage Gain	$V_O = \pm 10V$, $R_L = 2k$	●	40	120		30	110	V/mV
CMRR	Common Mode Rejection Ratio	$V_{CM} = \pm 10.4V$	●	84	97		80	95	dB
PSRR	Power Supply Rejection Ratio	$V_S = \pm 10V$ to $\pm 17V$	●	86	100		83	98	dB
V_{OUT}	Output Voltage Swing	$R_L = 2k$	●	± 12	± 12.7		± 12	± 12.6	V
I_S	Supply Current Per Amplifier	$T_A = 125^\circ C$		1.25	1.9		1.3	2.2	mA

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: Typical parameters are defined as the 60% yield of distributions of individual amplifiers; (i.e., out of 100 LT1058s or 100 LT1057s, typically 240 op amps, or 120 for the LT1057, will be better than the indicated specification).

Note 3: This parameter is tested on a sample basis only.

Note 4: Current noise is calculated from the formula:

$$i_n = (2qI_b)^{1/2}$$

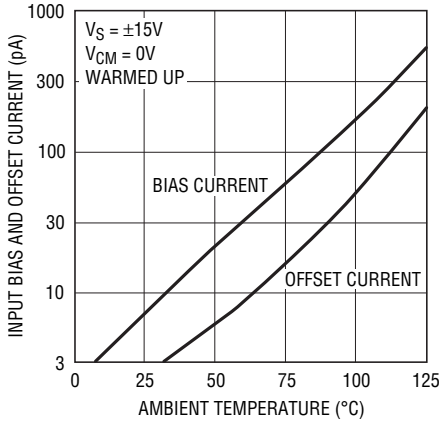
where $q = 1.6 \cdot 10^{-19}$ coulomb. The noise of source resistors up to 1G swamps the contribution of current noise.

Note 5: This parameter is not 100% tested.

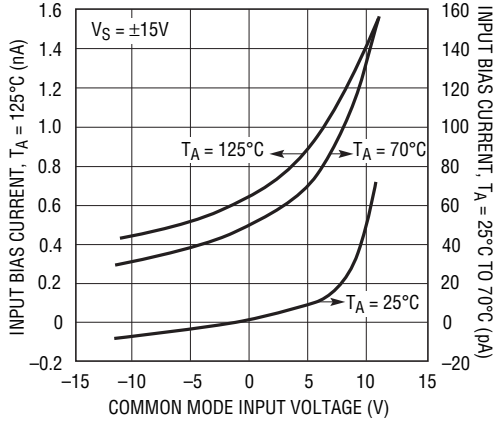
Note 6: Gain-bandwidth product is not tested. It is guaranteed by design and by inference from the slew rate measurement.

TYPICAL PERFORMANCE CHARACTERISTICS

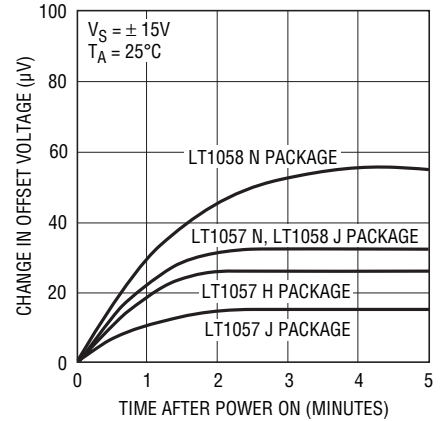
Input Bias and Offset Currents vs Temperature



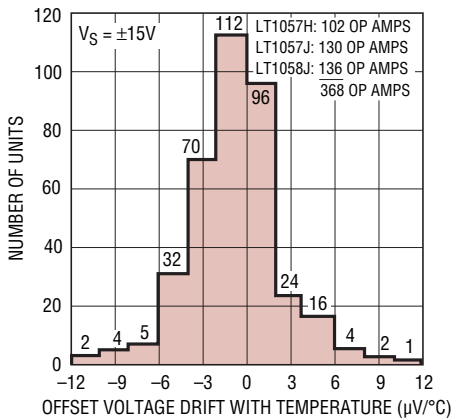
Input Bias Current Over the Common-Mode Range



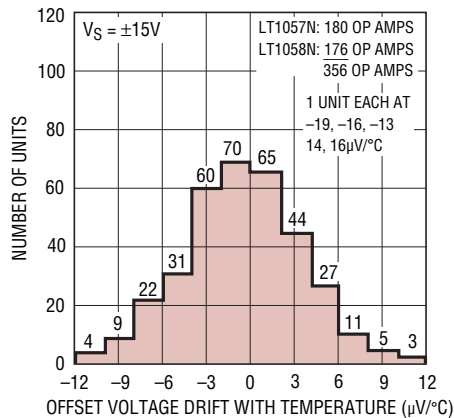
Warm-Up Drift



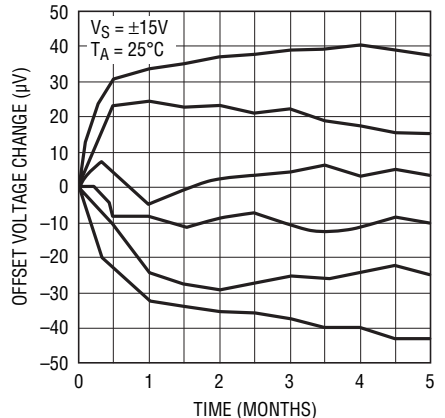
Distribution of Offset Voltage Drift with Temperature (H and J Package)



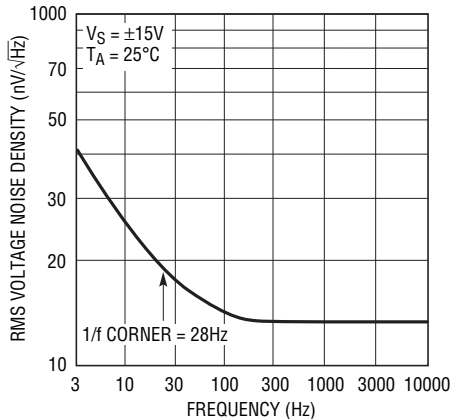
Distribution of Offset Voltage Drift with Temperature (Plastic N Package)



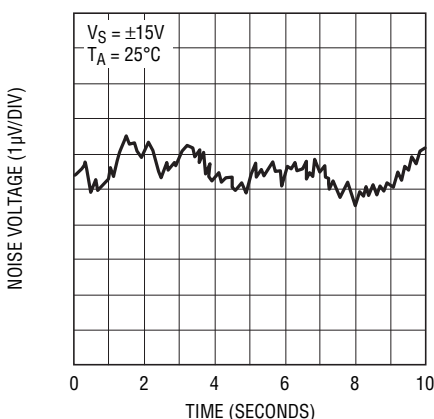
Long-Term Drift of Representative Units



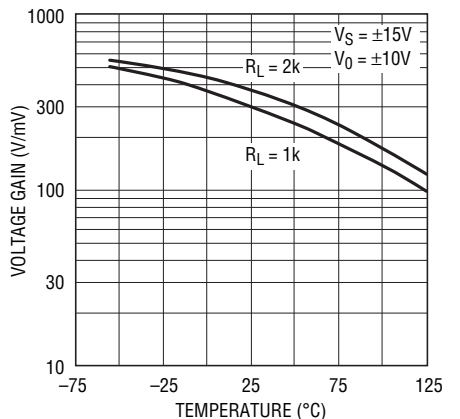
Voltage Noise vs Frequency



0.1Hz to 10Hz Noise

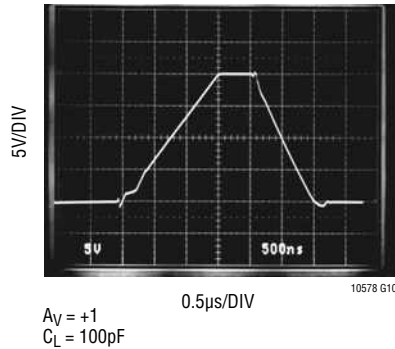


Voltage Gain vs Temperature

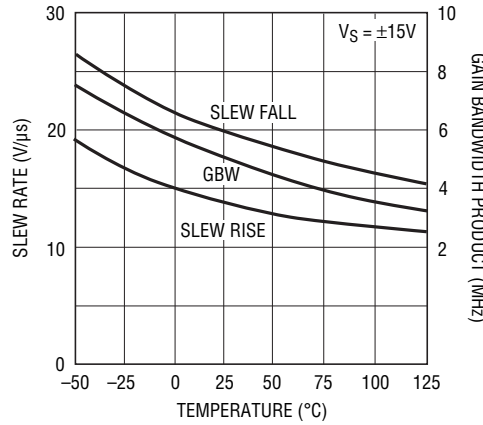


TYPICAL PERFORMANCE CHARACTERISTICS

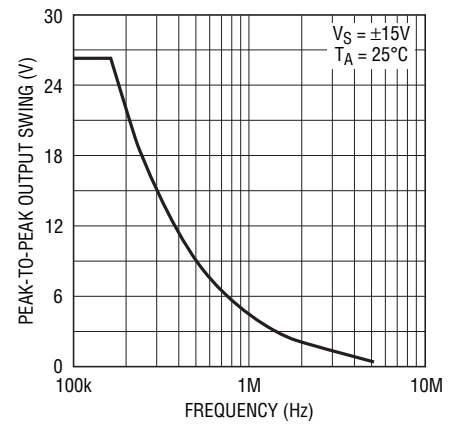
Large-Signal Response



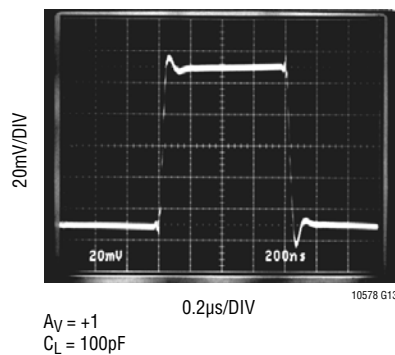
Slew Rate, Gain-Bandwidth Product vs Temperature



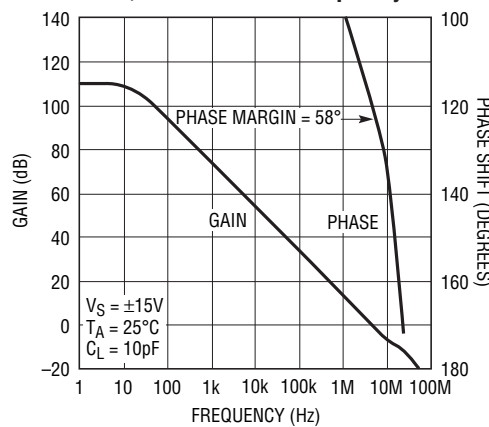
Undistorted Output Swing vs Frequency



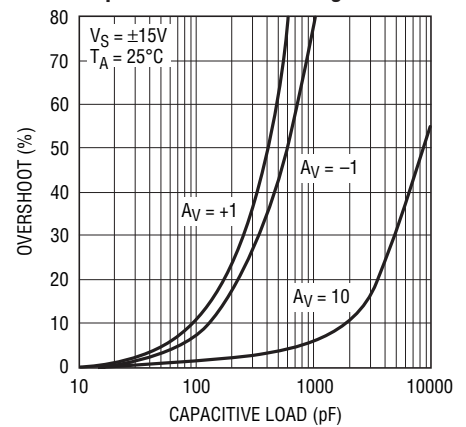
Small-Signal Response



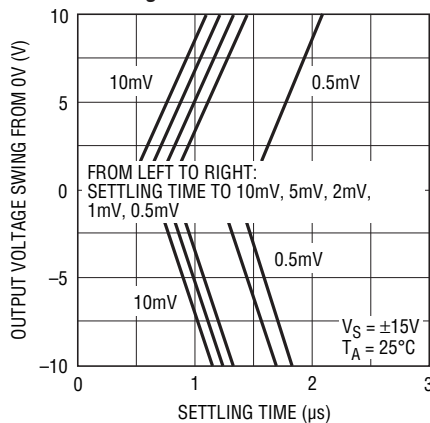
Gain, Phase Shift vs Frequency



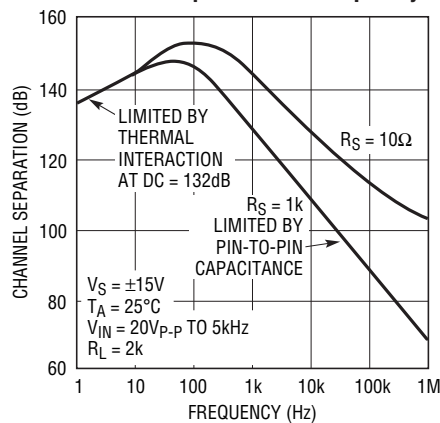
Capacitive Load Handling



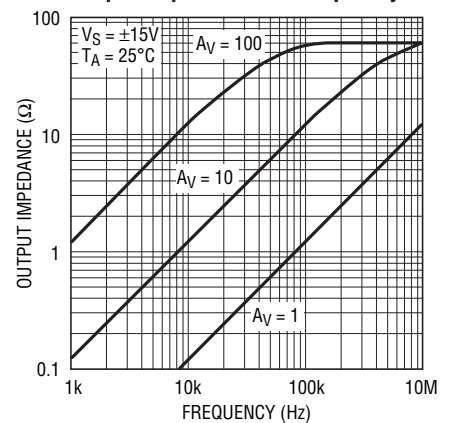
Settling Time



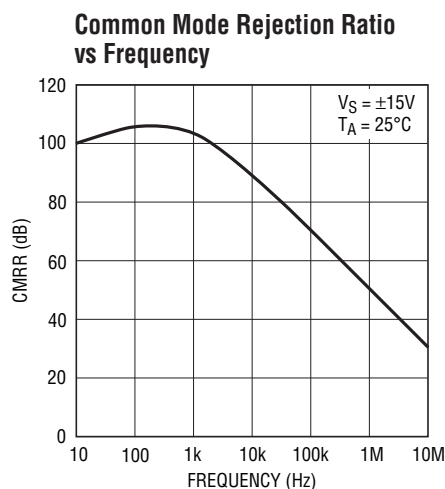
Channel Separation vs Frequency



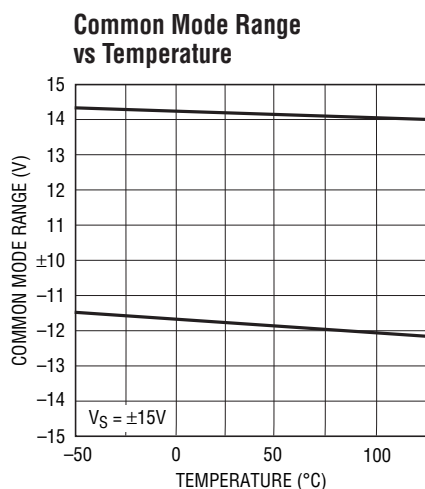
Output Impedance vs Frequency



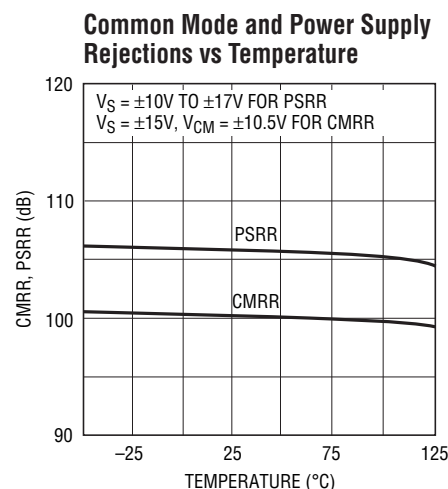
TYPICAL PERFORMANCE CHARACTERISTICS



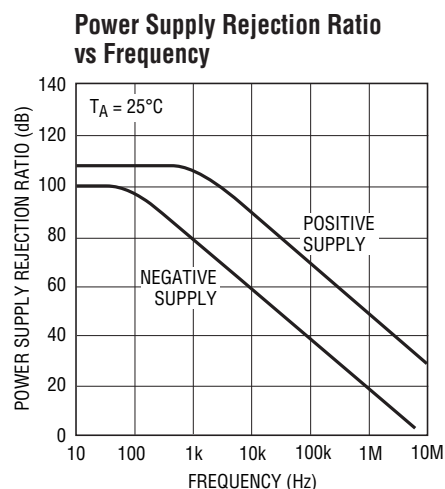
10578 G19



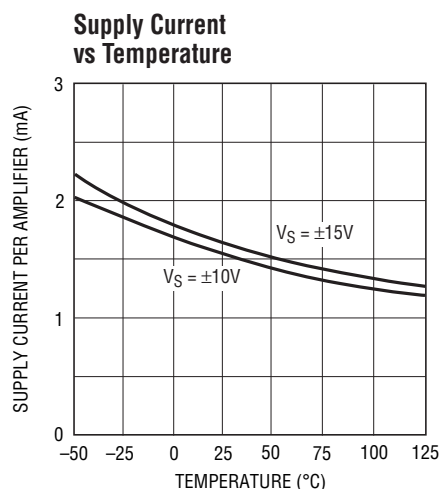
10578 G20



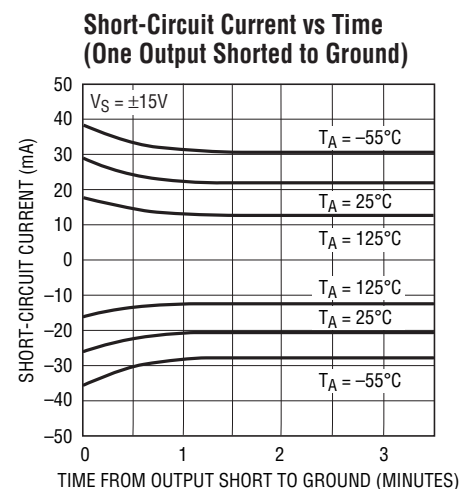
10578 G21



10578 G22



10578 G23



10578 G24

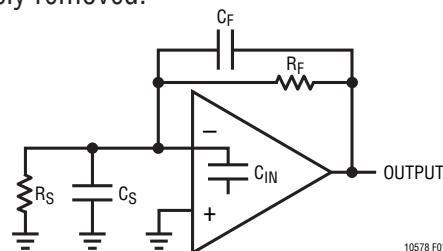
APPLICATIONS INFORMATION

The LT1057 may be inserted directly in LF353, LF412, LF442, TL072, TL082 and OP-215 sockets. The LT1058 plugs into LF347, LF444, TL074 and TL084 sockets. Of course, all standard dual and quad bipolar op amps can also be replaced by these devices.

High Speed Operation

When the feedback around the op amp is resistive (R_F) a pole will be created with R_F , the source resistance and capacitance (R_S , C_S), and the amplifier input capacitance ($C_{IN} \approx 4pF$). In low closed loop gain configurations and

with R_S and R_F in the kilohm range, this pole can create excess phase shift and even oscillation. A small capacitor (C_F) in parallel with R_F eliminates this problem. With $R_S(C_S + C_{IN}) = R_F C_F$, the effect of the feedback pole is completely removed.



10578 F01

10578fd

APPLICATIONS INFORMATION

Settling time is measured in a test circuit which can be found in the LT1055/LT1056 data sheet and in Application Note 10.

Achieving Picoampere/Microvolt Performance

In order to realize the picoampere/microvolt level accuracy of the LT1057/LT1058, proper care must be exercised. For example, leakage currents in circuitry external to the op amp can significantly degrade performance. High quality insulation should be used (e.g., Teflon™, Kel-F); cleaning of all insulating surfaces to remove fluxes and other residues will probably be required. Surface coating may be necessary to provide a moisture barrier in high humidity environments.

Board leakage can be minimized by encircling the input circuitry with a guard ring operated at a potential close to that of the inputs; in inverting configurations, the guard ring should be tied to ground, in noninverting connections, to the inverting input. Guarding both sides of the printed circuit board is required. Bulk leakage reduction depends on the guard ring width.

The LT1057/LT1058 have the lowest offset voltage of any dual and quad JFET input op amps available today. However, the offset voltage and its drift with time and temperature are still not as good as on the best bipolar amplifiers (because the transconductance of FETs is considerably lower than that of bipolar transistors). Conversely, this lower transconductance is the main cause of the significantly faster speed performance of FET input op amps.

Offset voltage also changes somewhat with temperature cycling. The AM grades show a typical 40 μ V hysteresis (50 μ V on the M grades) when cycled over the -55°C to 125°C temperature range. Temperature cycling from 0°C to 70°C has a negligible (less than 20 μ V) hysteresis effect.

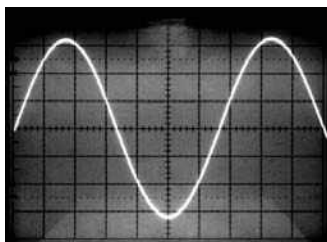
The offset voltage and drift performance are also affected by packaging. In the plastic N package, the molding compound is in direct contact with the chip, exerting pressure on the surface. While NPN input transistors are largely unaffected by this pressure, JFET device drift is degraded. Consequently for best drift performance, as shown in the Typical Performance Characteristics distribution plots, the J or H packages are recommended.

In applications where speed and picoampere bias currents are not necessary, Linear Technology offers the bipolar input, pin compatible LT1013 and LT1014 dual and quad op amps. These devices have significantly better DC specifications than any JFET input device.

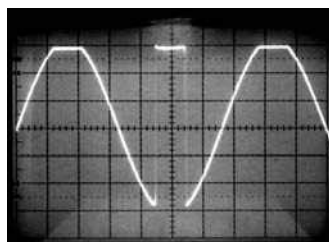
Phase Reversal Protection

Most industry standard JFET input single, dual and quad op amps (e.g., LF156, LF351, LF353, LF411, LF412, OP-15, OP-16, OP-215, TL084) exhibit phase reversal at the output when the negative common mode limit at the input is exceeded (i.e., below -12V with $\pm 15\text{V}$ supplies). The photos below show a $\pm 16\text{V}$ sine wave input (A), the response of an LF412A in the unity gain follower mode (B), and the response of the LT1057/LT1058 (C).

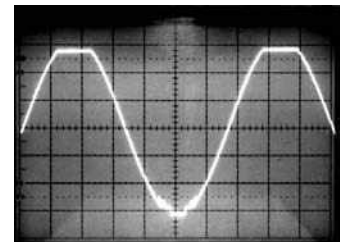
The phase reversal of photo (B) can cause lock-up in servo systems. The LT1057/LT1058 does not phase-reverse due to a unique phase reversal protection circuit.



(A) $\pm 16\text{V}$ Sine Wave Input



(B) LF412A Output



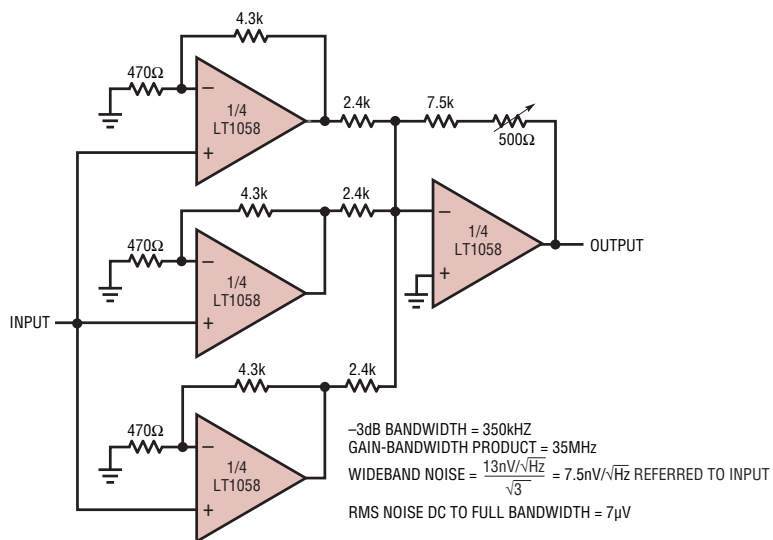
(C) LT1057/LT1058 Output

All Photos 5V/Div Vertical Scale, 50 μ s/Div Horizontal Scale

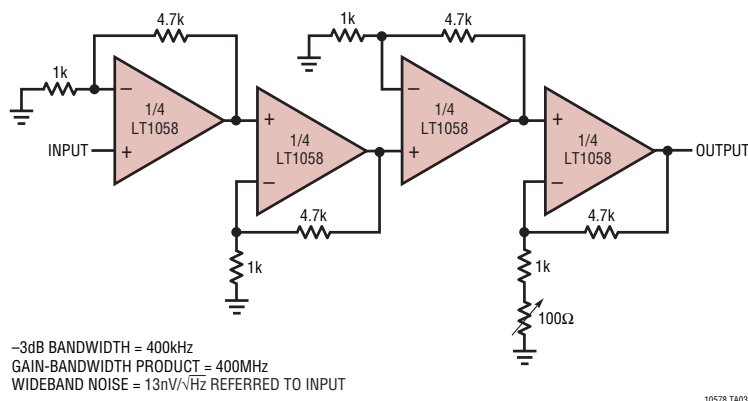
Teflon is a trademark of DuPont.

TYPICAL APPLICATIONS

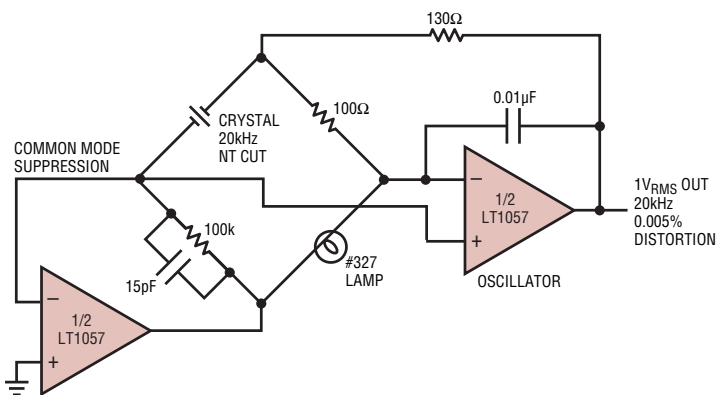
Low Noise, Wideband, Gain = 100 Amplifier with High Input Impedance



Wideband, High Input Impedance, Gain = 1000 Amplifier

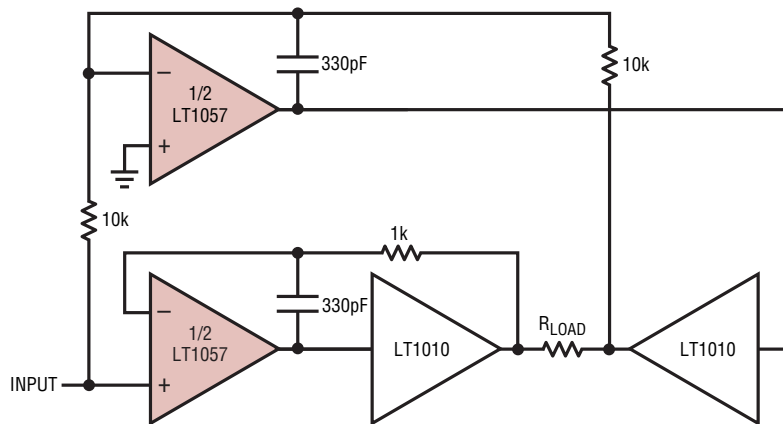


Low Distortion, Crystal Stabilized Oscillator



TYPICAL APPLICATIONS

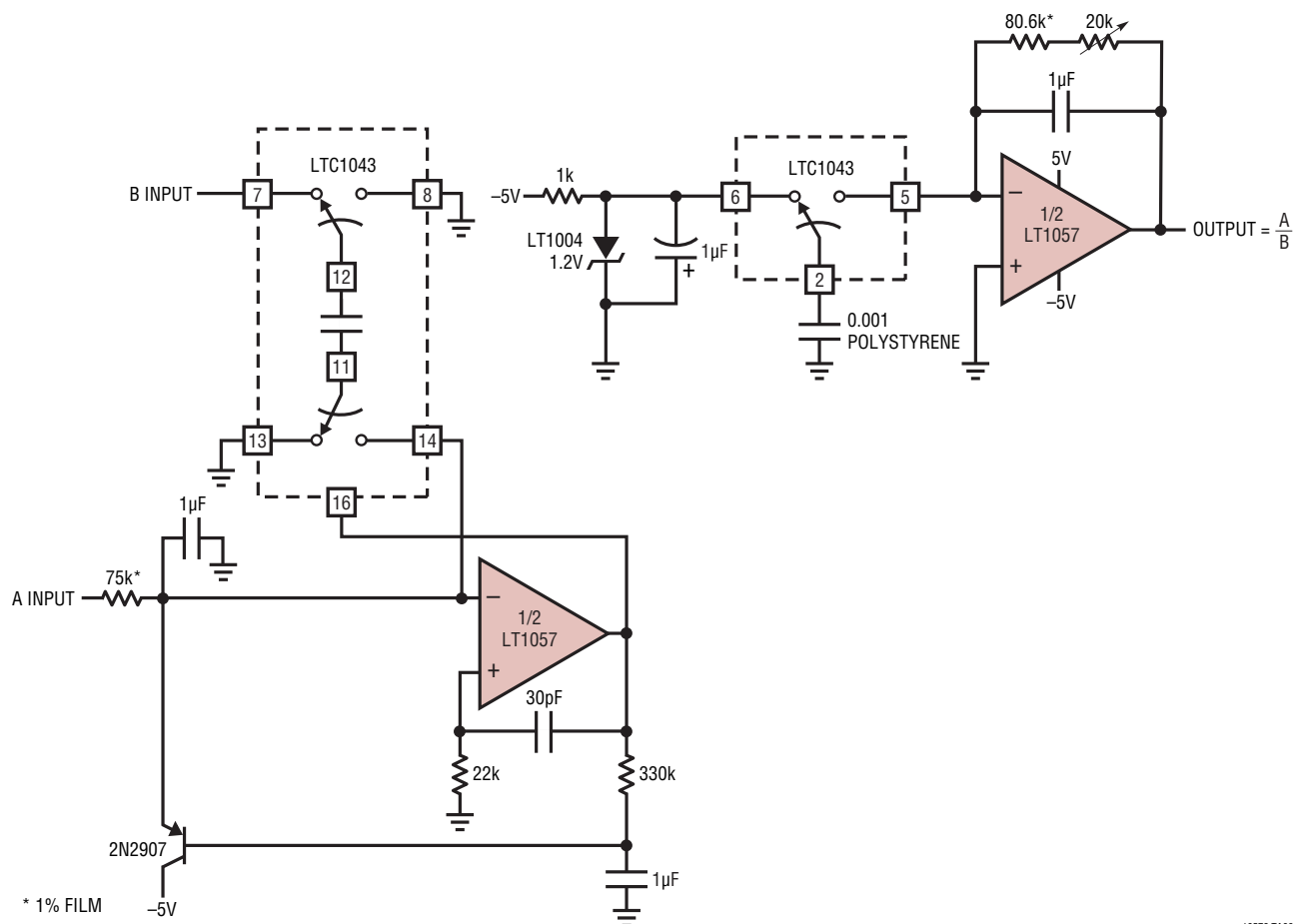
Fast, Precision Bridge Amplifier



SLEW RATE = 14V/ μ s
 OUTPUT CURRENT TO LOAD = 150mA
 LOAD CAPACITANCE: UP TO 1 μ F

10578 TA05

Analog Divider



* 1% FILM

10578 TA06
 10578fd

The circuit diagram illustrates a 1000 Hz sine wave generator. It features an input stage with a 36.5k* resistor and a 10k resistor, connected to an LT1058 op-amp. The output of this op-amp is connected to a 5V supply and a 1μF capacitor. The circuit also includes a 2N3906 transistor, a 10k resistor, and a 0.1μF capacitor. The output of the transistor is connected to a 1M* resistor and a 1μF capacitor. The final output stage consists of two LT1058 op-amps, one configured as a buffer and the other as a sine wave generator, with a 22k resistor and a 150pF capacitor. The output is labeled "DATA OUTPUT 0kHz TO 1kHz".

*1% FILM MATCH 1M RESISTORS TO 0.05%

10578 TA07

The circuit diagram illustrates a 10-bit digital-to-analog converter (DAC) using the R-2R ladder technique. The circuit is powered by a 5V supply and a -15V supply.

Key Components and Blocks:

- INTEGRATOR:** A 1/4 LT1058 op-amp configured as an integrator. Its non-inverting input (+) is grounded. The inverting input (-) is connected to the input E_{IN} through a 100k resistor and to the output through a feedback capacitor of 0.01μF. The output is connected to pin 2 of the 74C74 flip-flop.
- FLIP-FLOP:** A 74C74 15V flip-flop. Pin 14 is connected to 5V, and pin 7 is connected to ground. The output of the integrator (pin 2) is connected to pin 1. The output of the flip-flop (pin 3) is connected to the clock input of the 1/4 LT1058 op-amp in the output gate block.
- CURRENT SWITCH:** An LTC1043 current switch. Its inputs (pins 4, 16, 15, 18) are connected to the -15V supply. The output (pin 3) is connected to the non-inverting input (+) of the 1/4 LT1058 op-amp in the output gate block.
- LEVEL SHIFT:** A 2N4393 NPN transistor. Its base is connected to the output of the flip-flop (pin 3) through a 68pF capacitor. The emitter is connected to ground through an 820Ω resistor. The collector is connected to the inverting input (-) of the 1/4 LT1058 op-amp in the output gate block.
- OUTPUT GATE:** A 1/4 LT1058 op-amp configured as a buffer. Its non-inverting input (+) is connected to the output of the current switch. The inverting input (-) is connected to the collector of the 2N4393 transistor. The output is connected to the output A_{OUT} through a 10k resistor. The output is also connected to the output B_{OUT} through a 2k resistor.

Resistor Values and Connections:

- 100k resistor: Input E_{IN} to the integrator.
- 0.01μF capacitor: Feedback capacitor of the integrator.
- 5V and -15V: Power supply rails.
- 6.8k resistor: Connected to the base of the 2N4393 transistor.
- 180pF capacitor: Connected to the base of the 2N4393 transistor.
- 10k resistor: Connected to the base of the 2N4393 transistor.
- 820Ω resistor: Emitter resistor of the 2N4393 transistor.
- 10k resistor: Connected to the output A_{OUT} .
- 2k resistor: Connected to the output B_{OUT} .
- 95k resistor: Connected to the output A_{OUT} .
- 10k resistor: Connected to the output A_{OUT} .

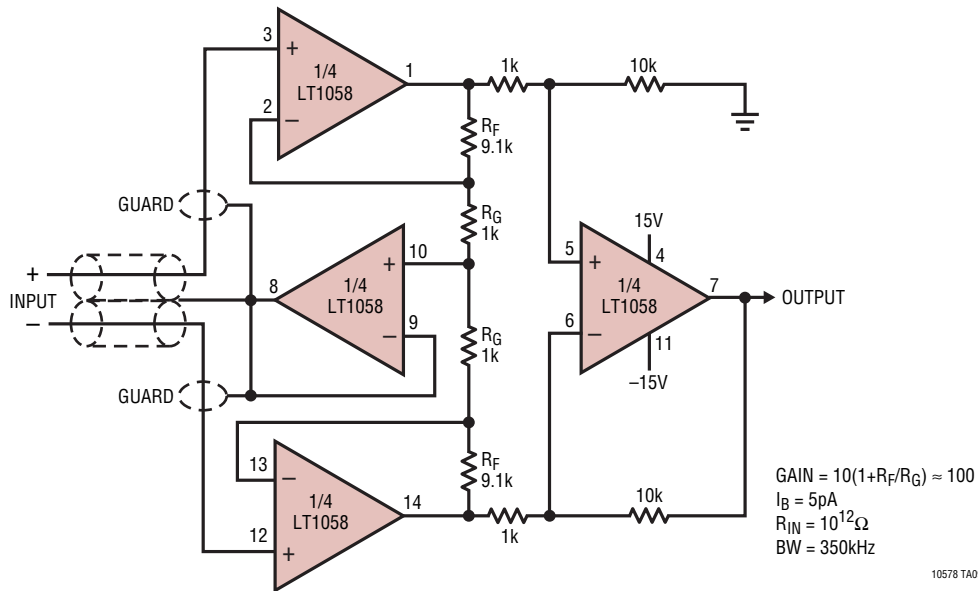
Equation and Notes:

DATA OUTPUT = $\frac{A_{OUT}}{B_{OUT}}$

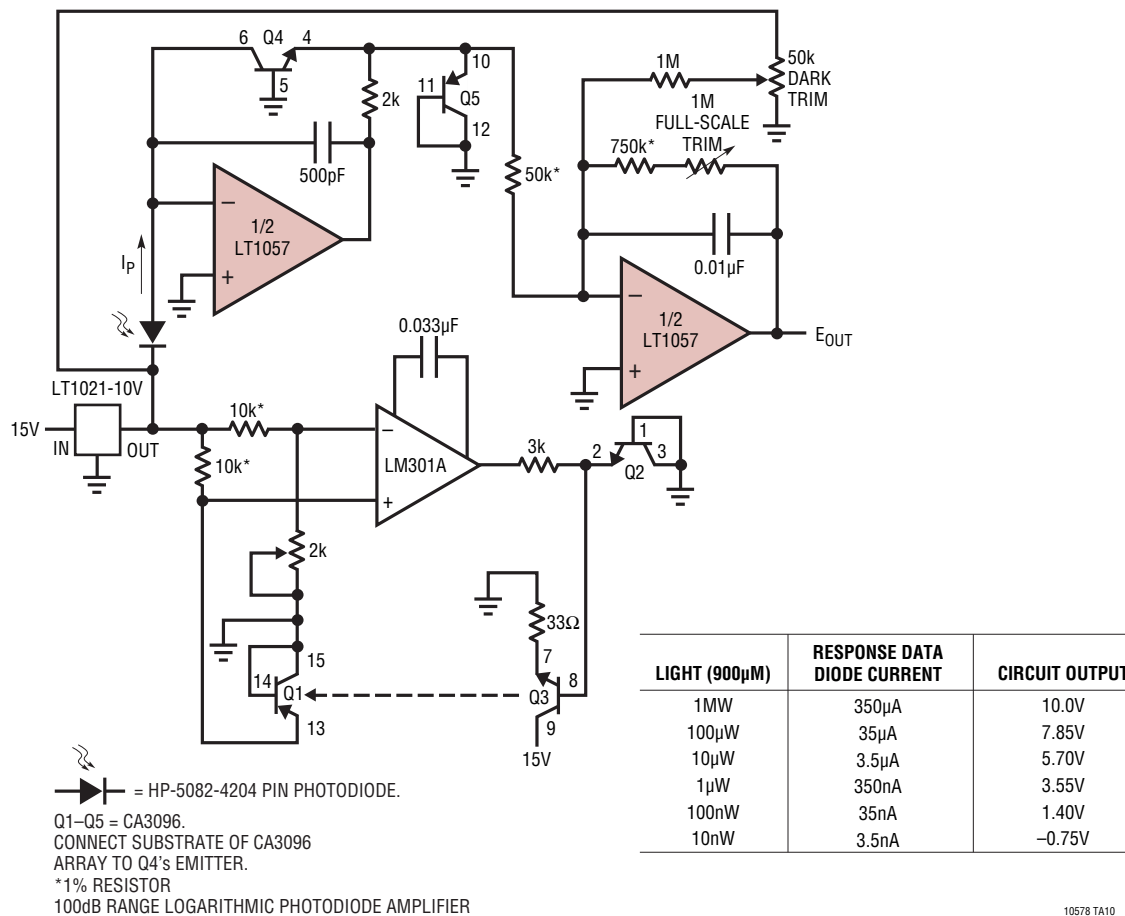
*VISHAY S-102 RESISTOR

TYPICAL APPLICATIONS

Instrumentation Amplifier with Shield Driver



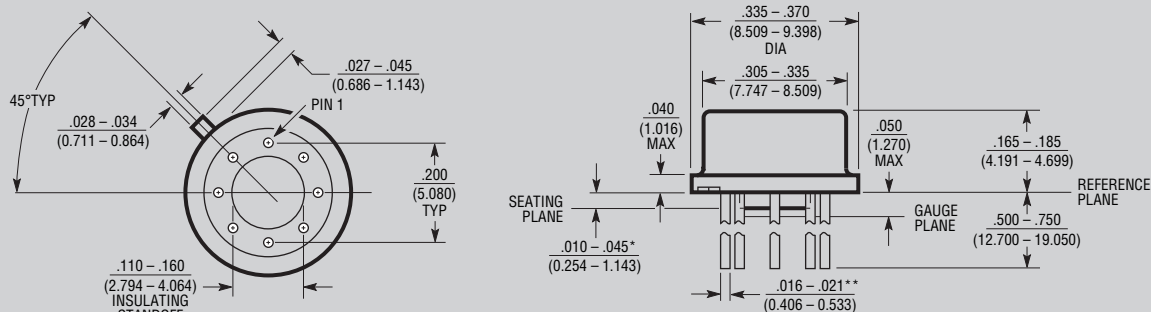
100dB Range Logarithmic Photodiode Amplifier



10578fd

PACKAGE DESCRIPTION

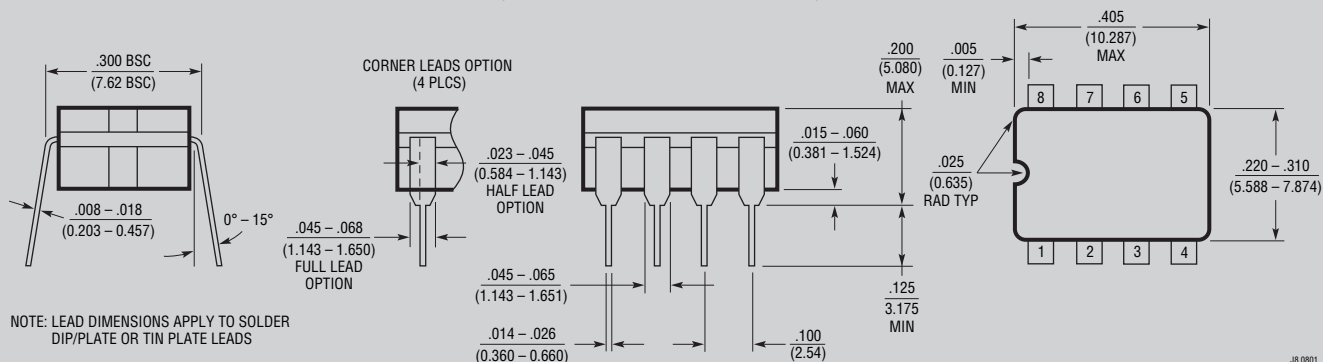
H Package 8-Lead TO-5 Metal Can (.200 Inch PCD) (Reference LTC DWG # 05-08-1320)



* LEAD DIAMETER IS UNCONTROLLED BETWEEN THE REFERENCE PLANE AND THE SEATING PLANE

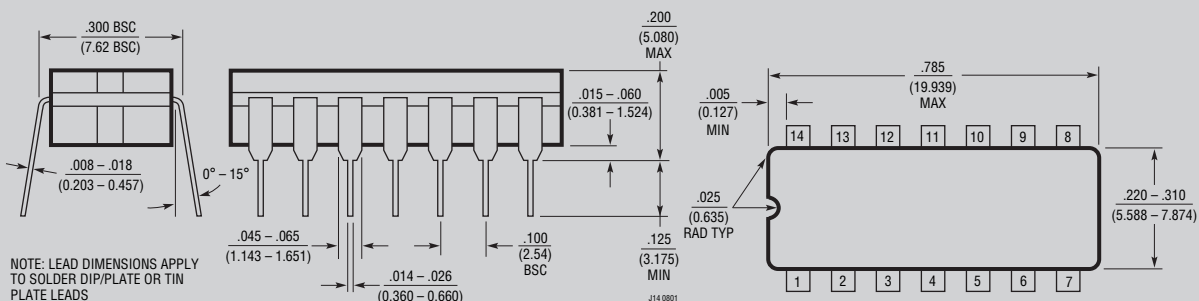
** FOR SOLDER DIP LEAD FINISH, LEAD DIAMETER IS .016-.024 (0.406-.0610) HB(TO-5) 0.200 PCD 0801

J8 Package 8-Lead Cerdip (Narrow .300 Inch, Hermetic) (Reference LTC DWG # 05-08-1110)



NOTE: LEAD DIMENSIONS APPLY TO SOLDER DIP/PLATE OR TIN PLATE LEADS

J Package 14-Lead Cerdip (Narrow .300 Inch, Hermetic) (Reference LTC DWG # 05-08-1110)

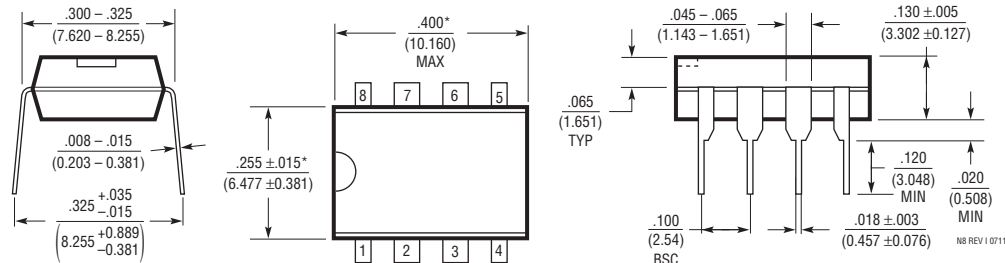


NOTE: LEAD DIMENSIONS APPLY TO SOLDER DIP/PLATE OR TIN PLATE LEADS

OBSOLETE PACKAGES

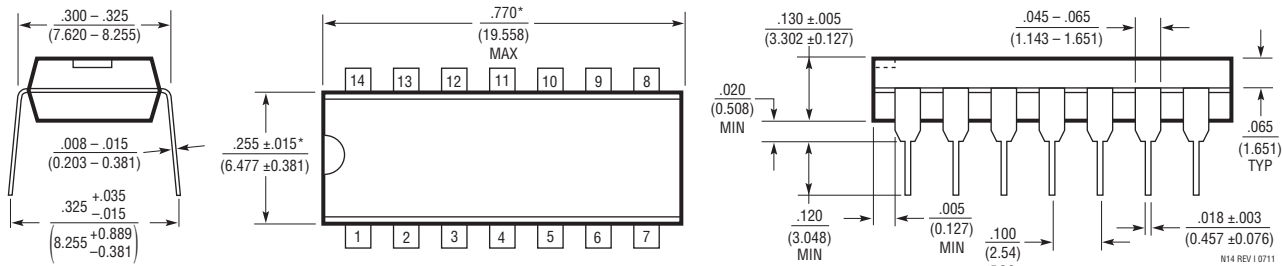
PACKAGE DESCRIPTION

N Package 8-Lead PDIP (Narrow .300 Inch) (Reference LTC DWG # 05-08-1510 Rev I)



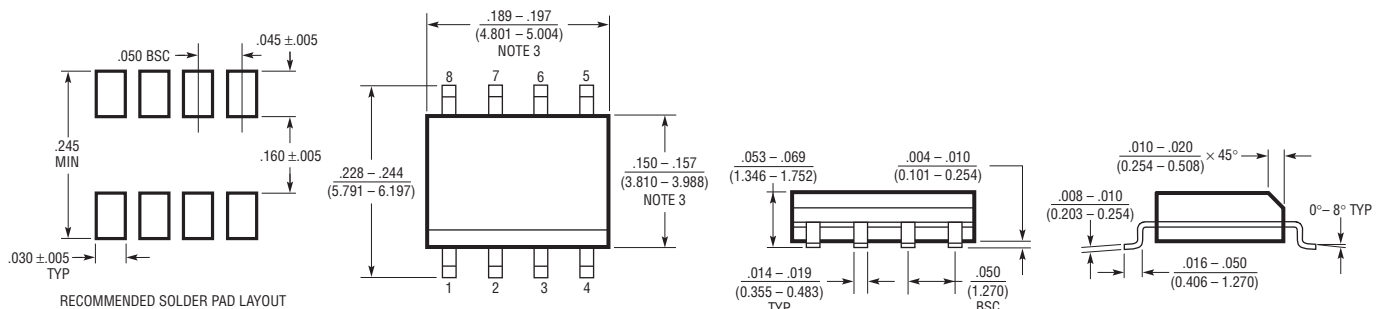
NOTE:
1. DIMENSIONS ARE $\frac{\text{INCHES}}{\text{MILLIMETERS}}$
*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 INCH (0.254mm)

N Package 14-Lead PDIP (Narrow .300 Inch) (Reference LTC DWG # 05-08-1510 Rev I)



NOTE:
1. DIMENSIONS ARE $\frac{\text{INCHES}}{\text{MILLIMETERS}}$
*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 INCH (0.254mm)

S8 Package 8-Lead Plastic Small Outline (Narrow .150 Inch) (Reference LTC DWG # 05-08-1610 Rev G)

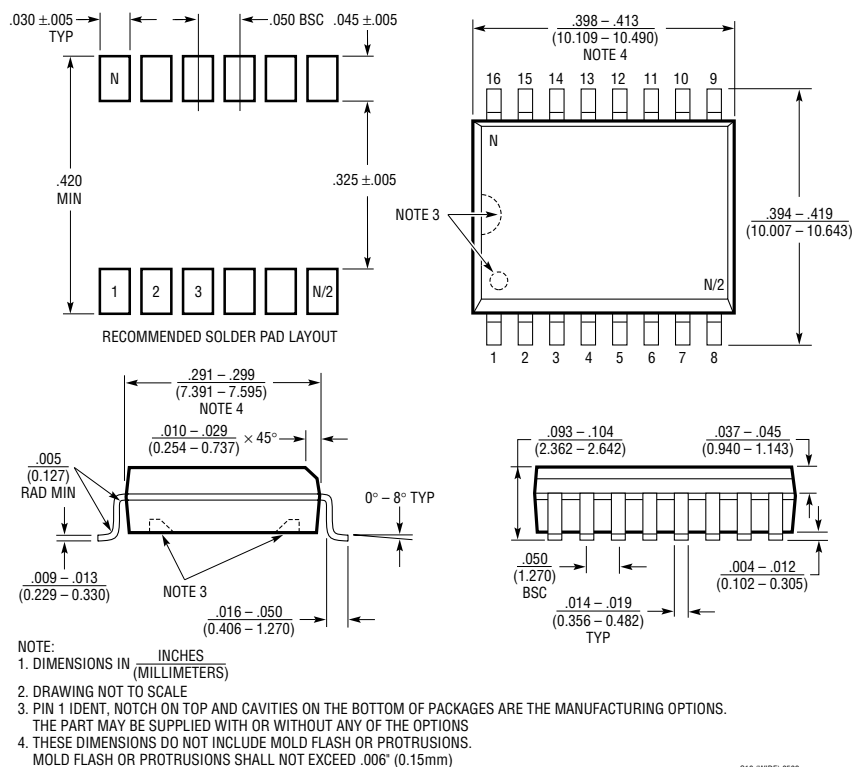


NOTE:
1. DIMENSIONS IN $\frac{\text{INCHES}}{\text{MILLIMETERS}}$
2. DRAWING NOT TO SCALE
3. THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .006" (0.15mm)
4. PIN 1 CAN BE BEVEL EDGE OR A DIMPLE

S08 REV G 0212

TYPICAL APPLICATION

SW Package 16-Lead Plastic Small Outline (Wide .300 Inch) (Reference LTC DWG # 05-08-1620)



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1055/6	Precision, High Speed, JFET Input Operational Amplifiers	12V/ μ s Slew Rate, 5.5MHz Bandwidth
LT1880	SOT-23, Rail-to-Rail Output, Picoamp Input Precision Op Amps	150 μ V Max Offset Voltage, 900pA Max Input Bias Current
LT1881/2	Dual and Quad Rail-to-Rail Output, Picoamp Input Precision Op Amps	50 μ V Max Offset Voltage, 200pA Max Input Bias Current
LT1884/5	Dual/Quad Rail-to-Rail Output, Picoamp Input Precision Op Amps	50 μ V Max Offset Voltage, 400pA Max Input Bias Current
LT6010	135 μ A, 14nV/rHz, Rail-to-Rail Output, Precision Low Power Op Amp with Shutdown	35 μ V Max Offset Voltage, 300pA Max Input Bias Current
LT6011/12	Dual/Quad 135 μ A, 14nV/rHz, Rail-to-Rail Output Precision Low Power Op Amp	60 μ V Max Offset Voltage, 300pA Max Input Bias Current
LTC6078/9	Micropower Precision, Dual/Quad CMOS Rail-to-Rail Input/Output Amplifiers	Maximum Offset Drift: 0.7 μ V/ $^\circ$ C
LTC6241/2	Dual/Quad 18MHz, Low Noise, Rail-to-Rail CMOS Op Amps	0.1Hz to 10Hz Noise: 550n Vpp