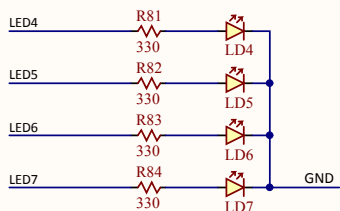
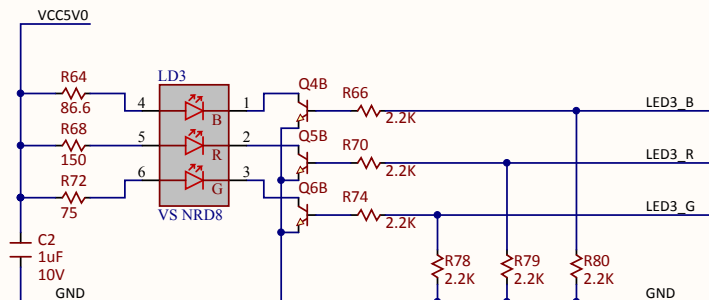
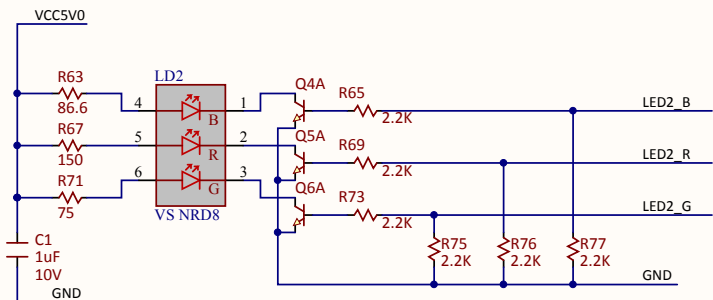
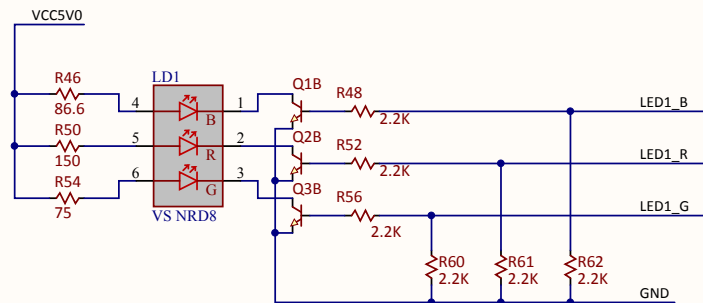
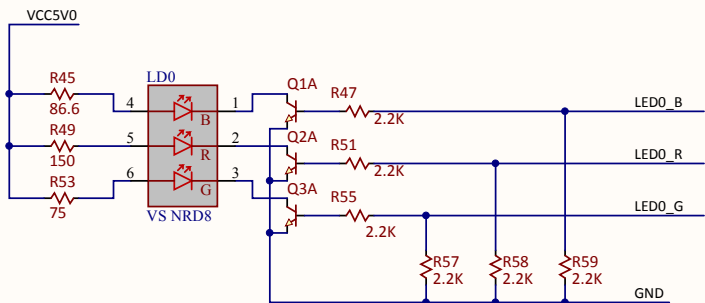


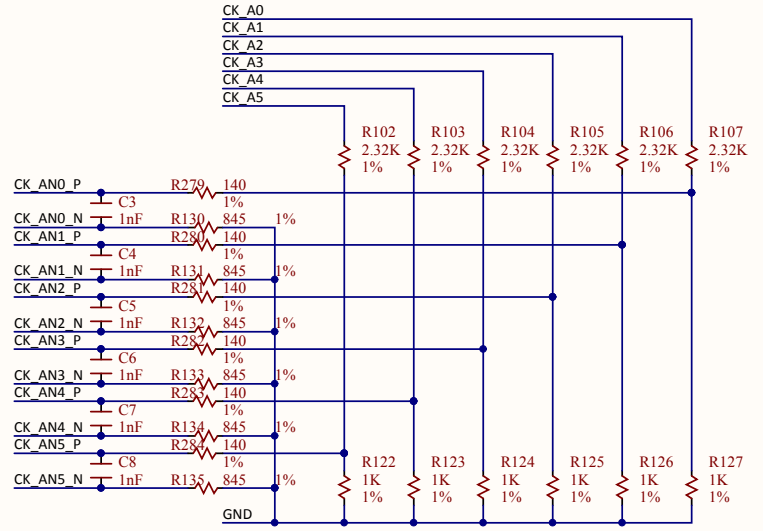
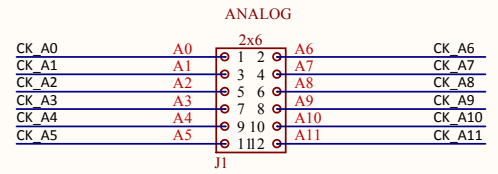
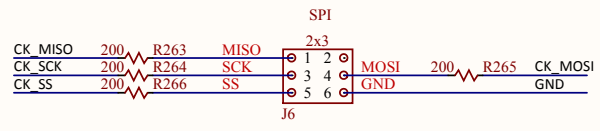
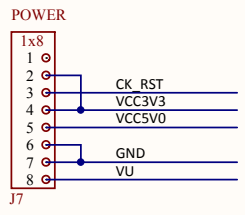
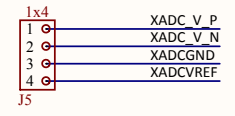
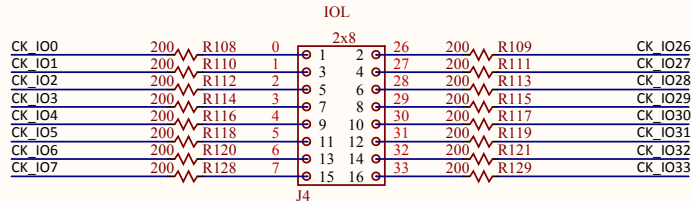
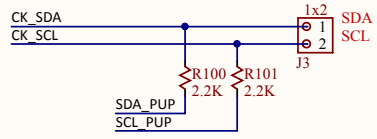
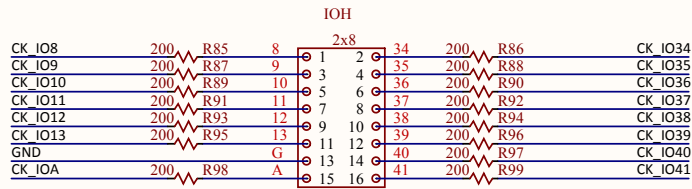
- Foot
- F1
- Foot
- F2
- Foot
- F3
- Foot
- F4

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<h1>Arty</h1>		<h1>C.1</h1>	
		Copyright 2015	
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MTA		GMA	
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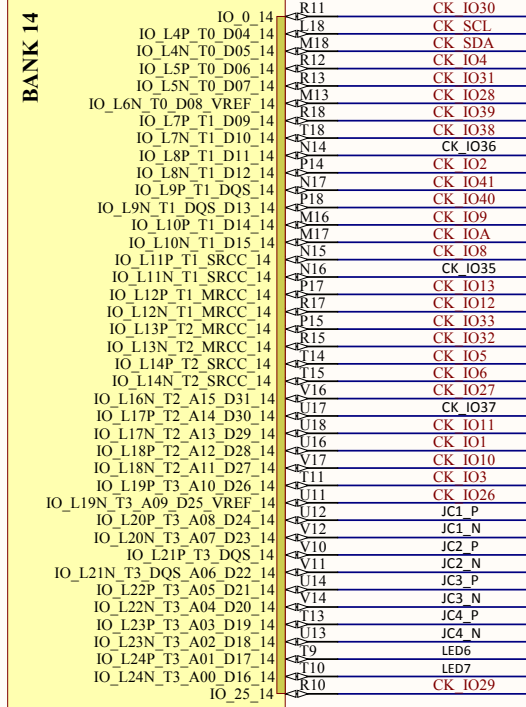
Title		Rev	
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Author	GMA		
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Note: Terminate N signals next to Analog Header

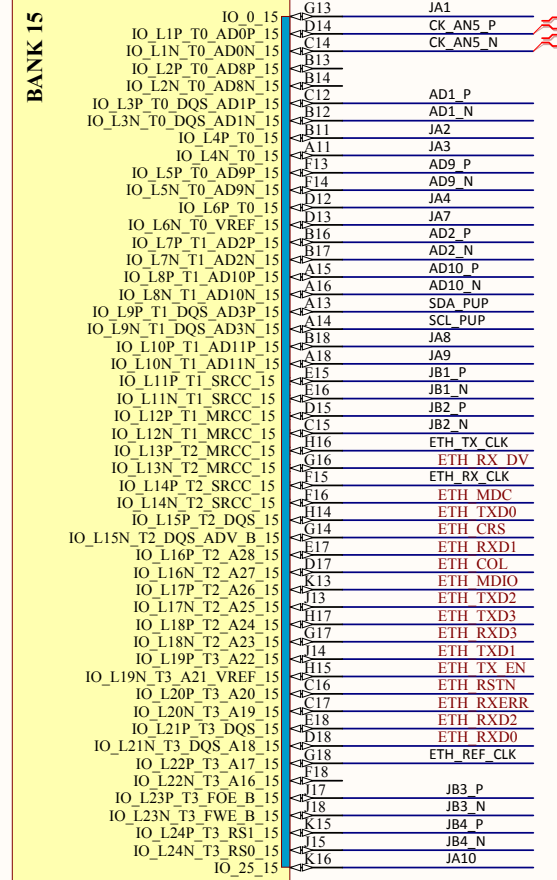
Title		Rev
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Author	GMA	
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IC1A



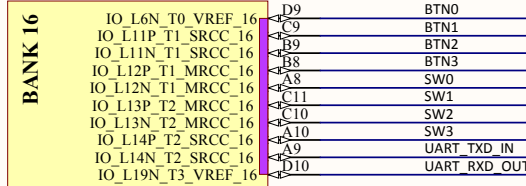
XC7A35T-L1CSG324I

IC1B

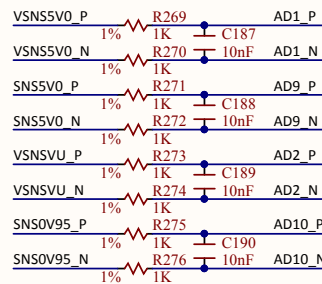


XC7A35T-L1CSG324I

IC1C



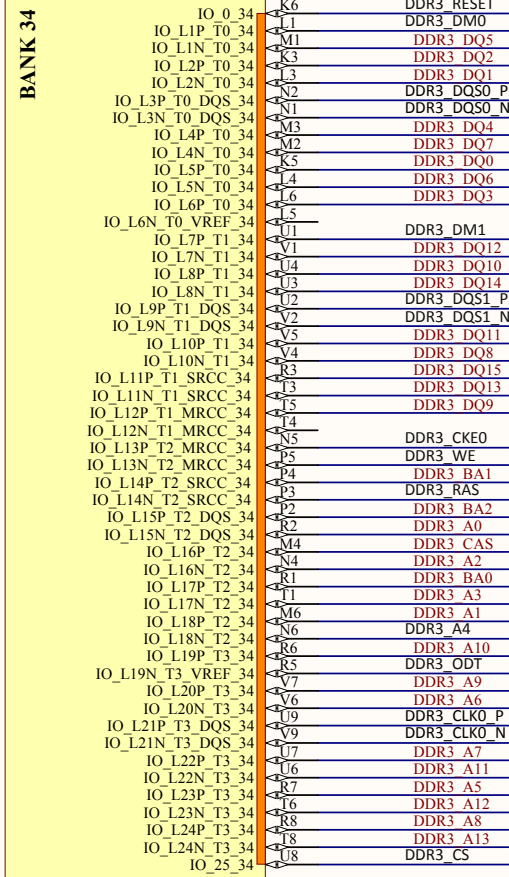
XC7A35T-L1CSG324I



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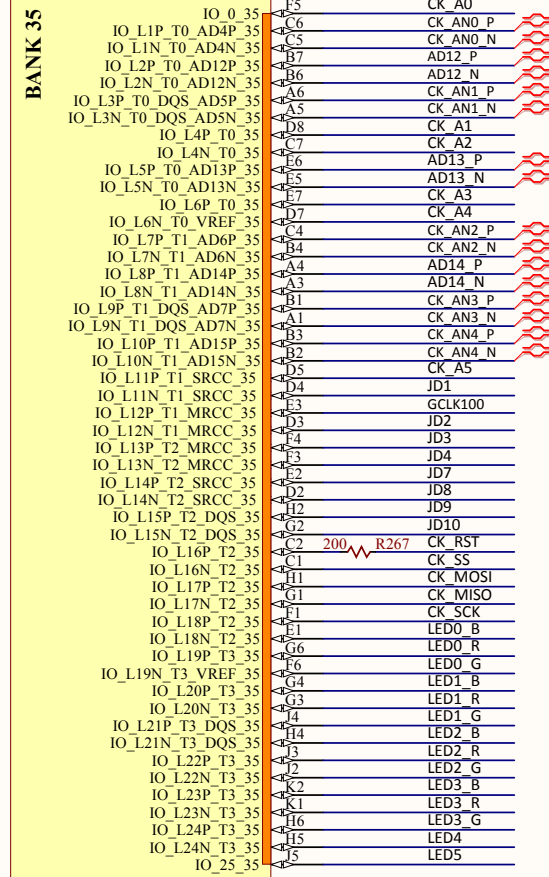


IC1D

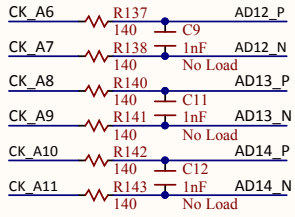
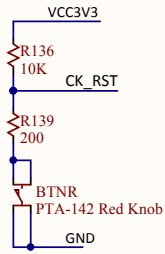
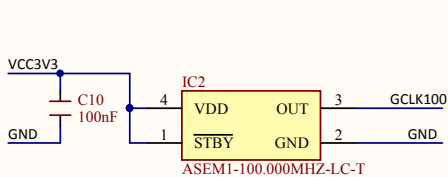


XC7A35T-L1CSG324I


IC1E



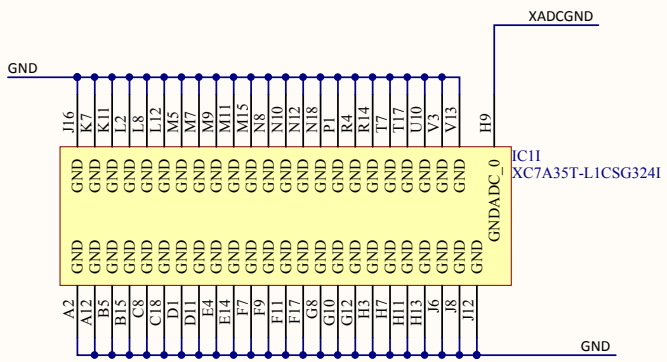
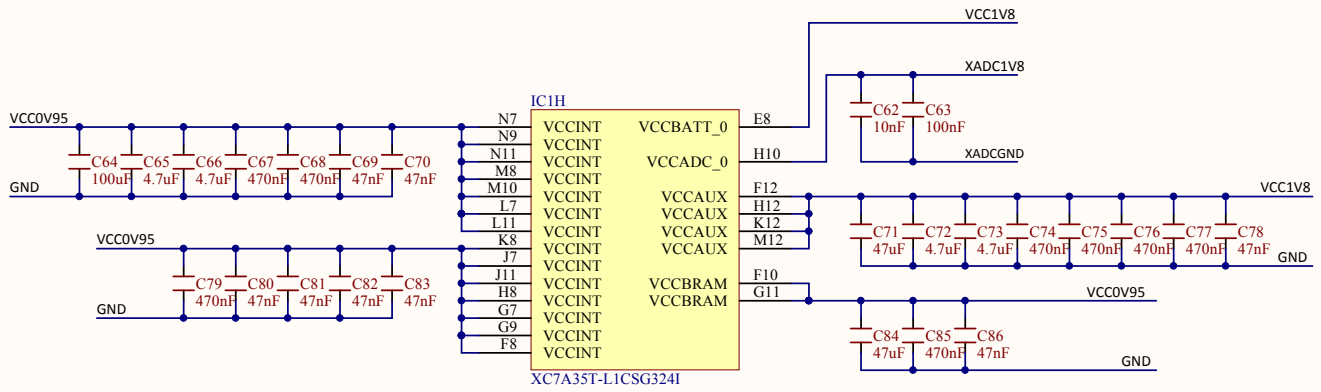
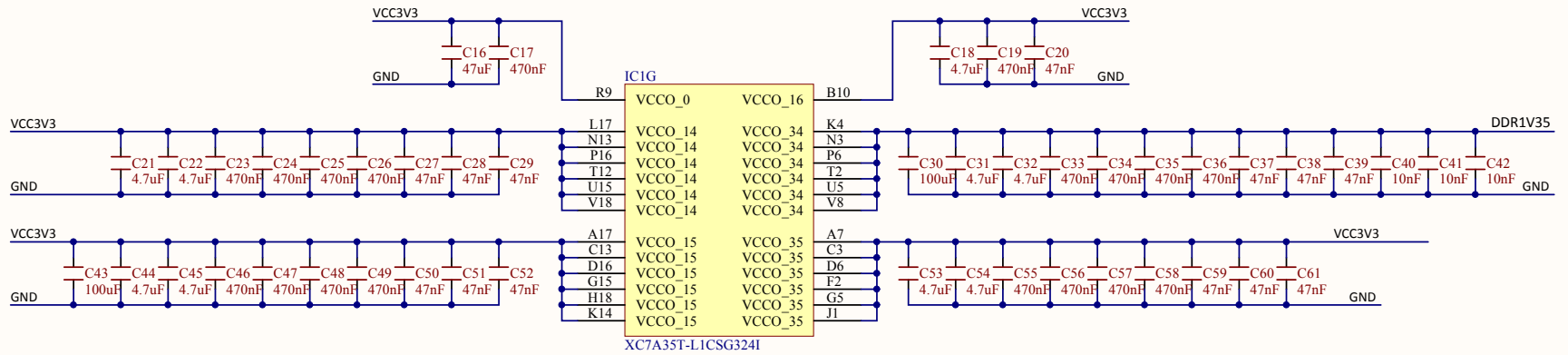
XC7A35T-L1CSG324I




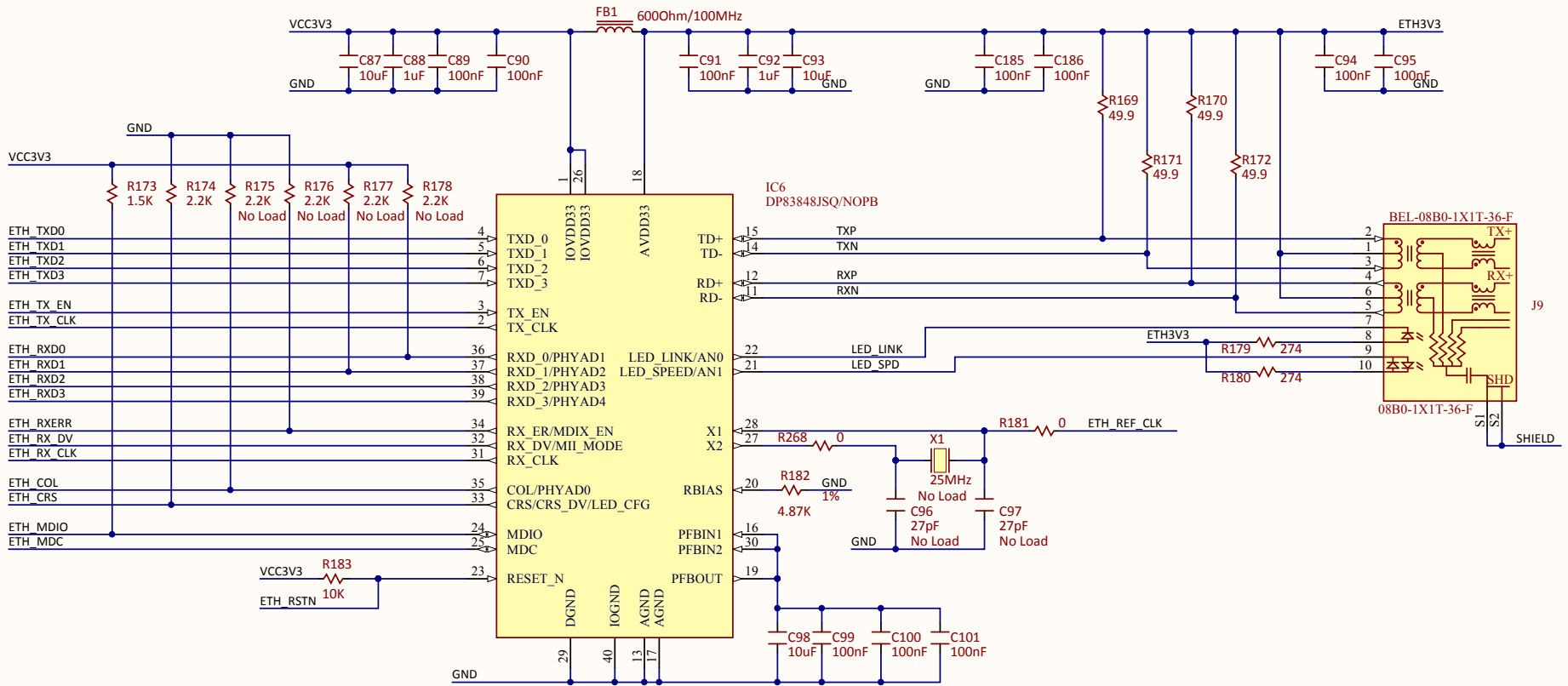
Title		Rev
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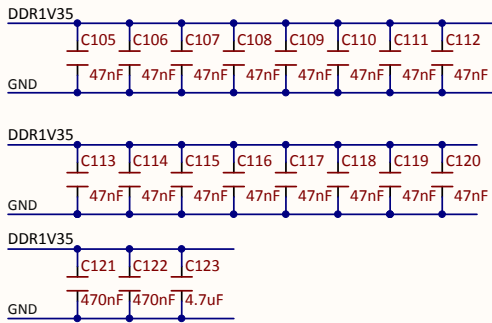
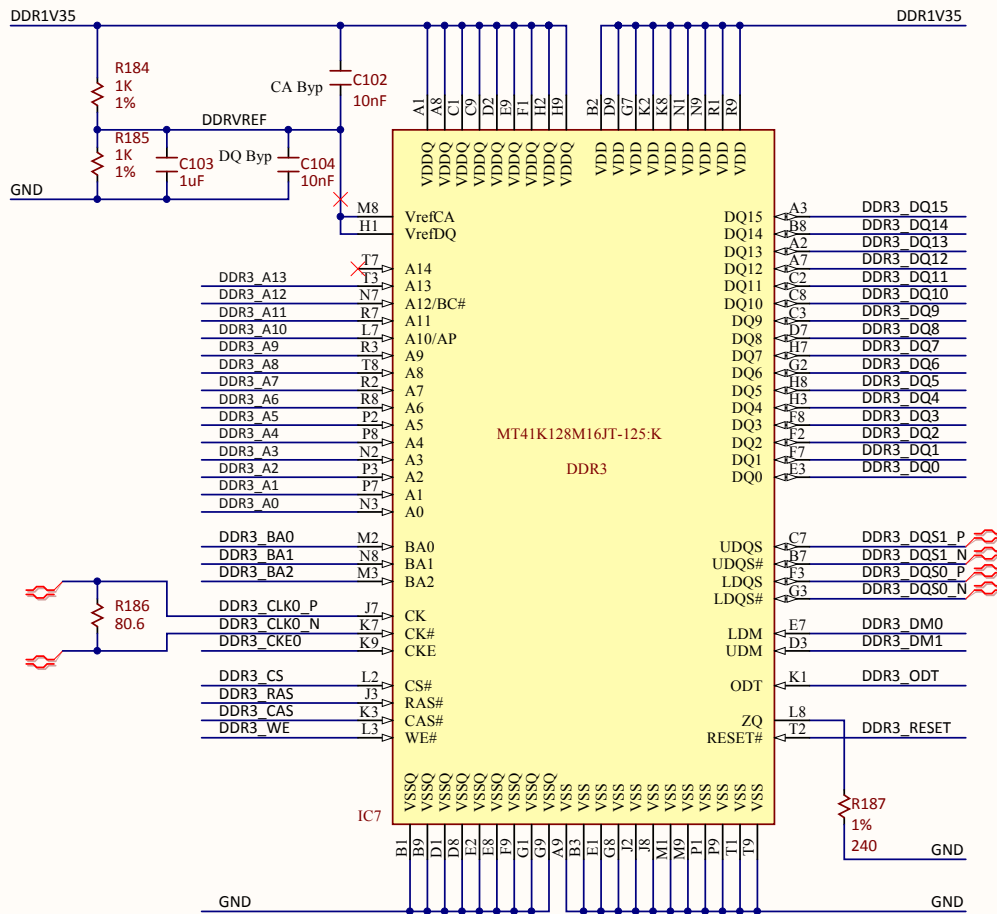
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NOTE: REF_CLK In Mode (ETH_REF_CLK = 25MHz)

NOTE: PHY MDIO Address = 00001

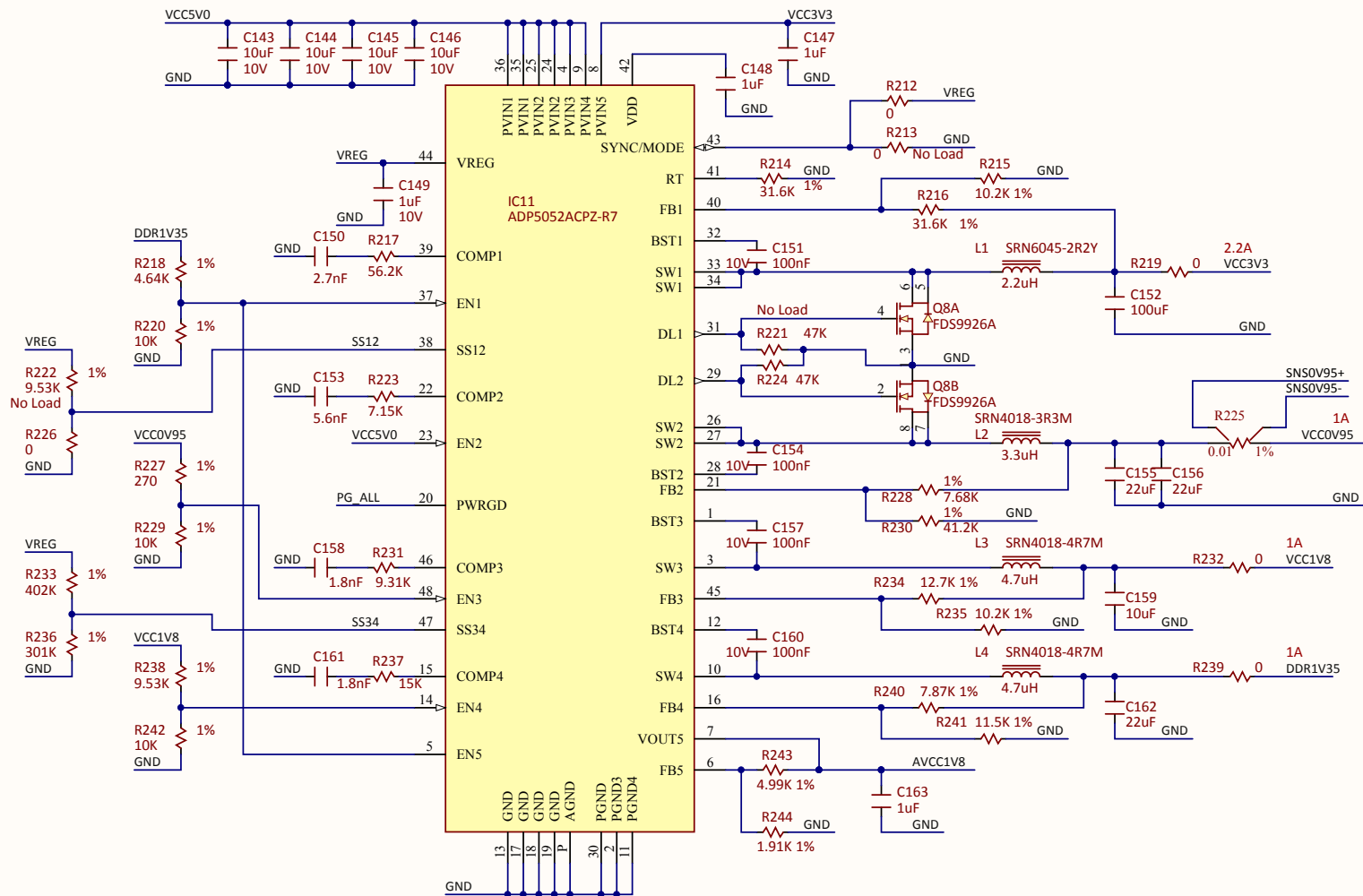
Title Arty		Rev C.1 Copyright 2015
Circuit ETHERNET		 DIGILENT BEYOND THEORY
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Author GMA		
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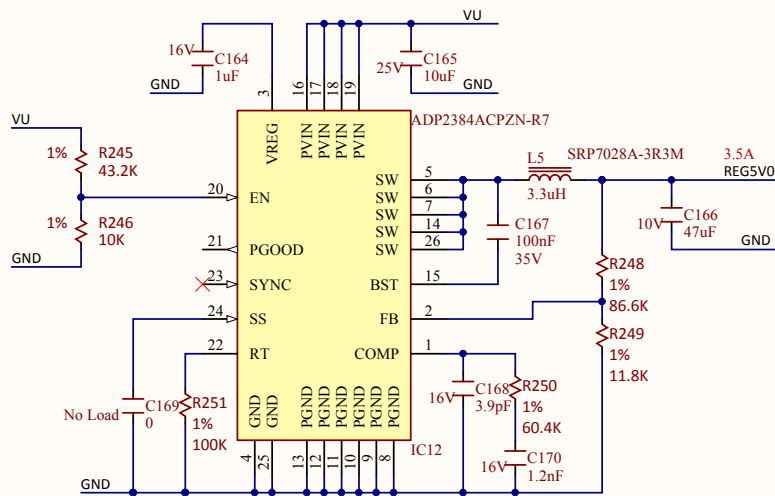
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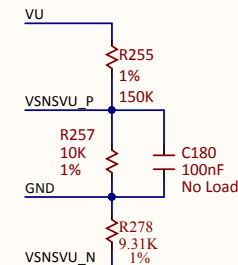
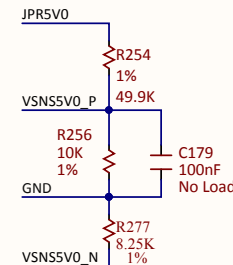
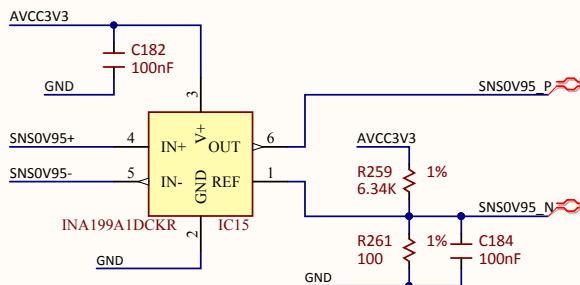
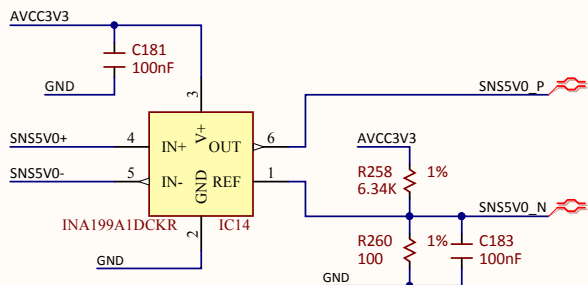
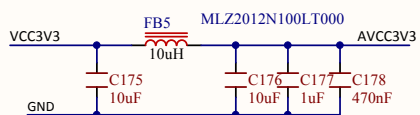
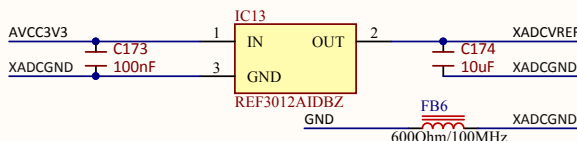
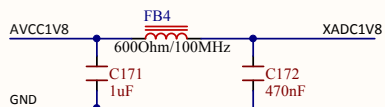
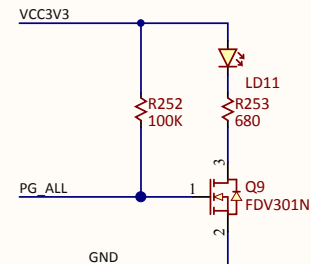
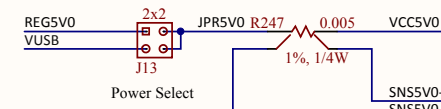
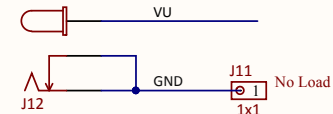
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<h1>Arty</h1>		<h1>C.1</h1>	
		Copyright 2015	
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Note: Input Voltage 7-15V.



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