

SN55451B, SN55452B, SN55453B, SN55454B SN75451B, SN75452B, SN75453B, SN75454B DUAL PERIPHERAL DRIVERS

SLRS021B – DECEMBER 1976 – REVISED SEPTEMBER 1999

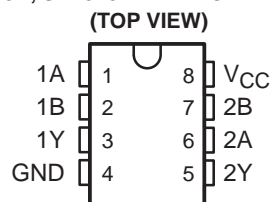
PERIPHERAL DRIVERS FOR HIGH-CURRENT SWITCHING AT VERY HIGH SPEEDS

- Characterized for Use to 300 mA
- High-Voltage Outputs
- No Output Latch-Up at 20 V (After Conducting 300 mA)
- High-Speed Switching
- Circuit Flexibility for Varied Applications
- TTL-Compatible Diode-Clamped Inputs
- Standard Supply Voltages
- Plastic DIP (P) With Copper Lead Frame Provides Cooler Operation and Improved Reliability
- Package Options Include Plastic Small-Outline Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs

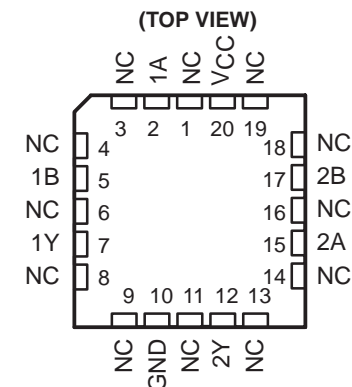
SUMMARY OF DEVICES

DEVICE	LOGIC OF COMPLETE CIRCUIT	PACKAGES
SN55451B	AND	FK, JG
SN55452B	NAND	JG
SN55453B	OR	FK, JG
SN55454B	NOR	JG
SN75451B	AND	D, P
SN75452B	NAND	D, P
SN75453B	OR	D, P
SN75454B	NOR	D, P

SN55451B, SN55452B,
SN55453B, SN55454B . . . JG PACKAGE
SN75451B, SN75452B,
SN75453B, SN75454B . . . D OR P PACKAGE



SN55451B, SN55452B
SN55453B, SN55454B . . . FK PACKAGE



NC – No internal connection

description

The SN55451B through SN55454B and SN75451B through SN75454B are dual peripheral drivers designed for use in systems that employ TTL logic. This family is functionally interchangeable with and replaces the SN75450 family and the SN75450A family devices manufactured previously. The speed of the devices is equal to that of the SN75450 family, and the parts are designed to ensure freedom from latch-up. Diode-clamped inputs simplify circuit design. Typical applications include high-speed logic buffers, power drivers, relay drivers, lamp drivers, MOS drivers, line drivers, and memory drivers.

The SN55451B/SN75451B, SN55452B/SN75452B, SN55453B/SN75453B, and SN55454B/SN75454B are dual peripheral AND, NAND, OR, and NOR drivers, respectively (assuming positive logic), with the output of the logic gates internally connected to the bases of the npn output transistors.

The SN55' drivers are characterized for operation over the full military range of -55°C to 125°C . The SN75' drivers are characterized for operation from 0°C to 70°C .

**SN55451B, SN55452B, SN55453B, SN55454B
SN75451B, SN75452B, SN75453B, SN75454B
DUAL PERIPHERAL DRIVERS**

SLRS021B – DECEMBER 1976 – REVISED SEPTEMBER 1999

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

	SN55'	SN75'	UNIT
Supply voltage, V_{CC} (see Note 1)	7	7	V
Input voltage, V_I	5.5	5.5	V
Inter-emitter voltage (see Note 2)	5.5	5.5	V
Off-state output voltage, V_O	30	30	V
Continuous collector or output current, I_{OK} (see Note 3)	400	400	mA
Peak collector or output current, I_I ($t_W \leq 10$ ms, duty cycle $\leq 50\%$, see Note 4)	500	500	mA
Continuous total power dissipation	See Dissipation Rating Table		
Operating free-air temperature range, T_A	-55 to 125	0 to 70	°C
Storage temperature range, T_{stg}	-65 to 150	-65 to 150	°C
Case temperature for 60 seconds	FK package	260	°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds	JG package	300	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	D or P package		260 °C

- NOTES: 1. Voltage values are with respect to network GND, unless otherwise specified.
 2. This is the voltage between two emitters of a multiple-emitter transistor.
 3. This value applies when the base-emitter resistance (R_{BE}) is equal to or less than 500 Ω .
 4. Both halves of these dual circuits may conduct rated current simultaneously; however, power dissipation averaged over a short time interval must fall within the continuous dissipation rating.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$	$T_A = 70^\circ\text{C}$ POWER RATING	$T_A = 125^\circ\text{C}$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	—
FK	1375 mW	11.0 mW/°C	880 mW	275 mW
JG	1050 mW	8.4 mW/°C	672 mW	210 mW
P	1000 mW	8.0 mW/°C	640 mW	—

recommended operating conditions

	SN55'			SN75'			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level input voltage, V_{IH}	2			2			V
Low-level input voltage, V_{IL}	0.8			0.8			V
Operating free-air temperature, T_A	-55 125			0 70			°C



SN55451B, SN55452B, SN55453B, SN55454B SN75451B, SN75452B, SN75453B, SN75454B DUAL PERIPHERAL DRIVERS

SLRS021B – DECEMBER 1976 – REVISED SEPTEMBER 1999

logic symbol†



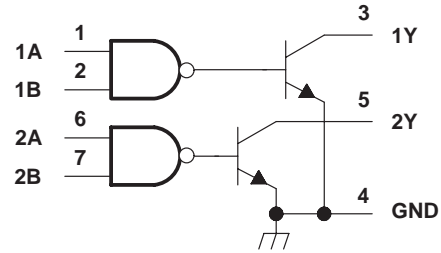
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC publication 617-12.
Pin numbers shown are for the D, JG, and P packages.

FUNCTION TABLE
(each driver)

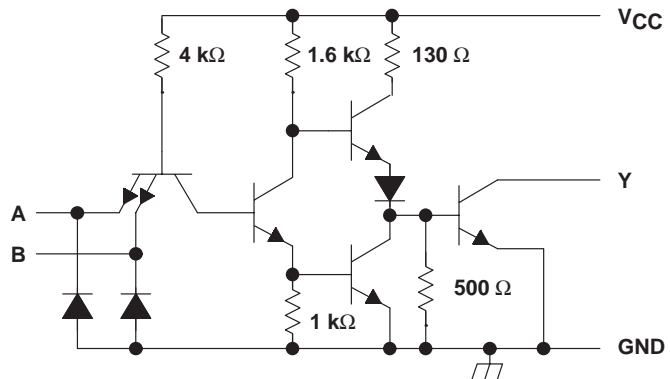
A	B	Y
L	L	L (on state)
L	H	L (on state)
H	L	L (on state)
H	H	H (off state)

positive logic:
 $Y = AB$ or $\overline{A+B}$

logic diagram (positive logic)



schematic (each driver)



Resistor values shown are nominal.

electrical characteristics over recommended operating free-air temperature range

PARAMETER	TEST CONDITIONS‡	SN55451B			SN75451B			UNIT
		MIN	TYP§	MAX	MIN	TYP§	MAX	
V_{IK} Input clamp voltage	$V_{CC} = \text{MIN}$, $I_I = -12 \text{ mA}$	-1.2	-1.5		-1.2	-1.5		V
V_{OL} Low-level output voltage	$V_{CC} = \text{MIN}$, $V_{IL} = 0.8 \text{ V}$, $I_{OL} = 100 \text{ mA}$	0.25	0.5		0.25	0.4		V
	$V_{CC} = \text{MIN}$, $V_{IL} = 0.8 \text{ V}$, $I_{OL} = 300 \text{ mA}$	0.5	0.8		0.5	0.7		
I_{OH} High-level output current	$V_{CC} = \text{MIN}$, $V_{IH} = \text{MIN}$, $V_{OH} = 30 \text{ V}$			300			100	μA
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}$, $V_I = 5.5 \text{ V}$			1			1	mA
I_{IH} High-level input current	$V_{CC} = \text{MAX}$, $V_I = 2.4 \text{ V}$			40			40	μA
I_{IL} Low-level input current	$V_{CC} = \text{MAX}$, $V_I = 0.4 \text{ V}$	-1	-1.6		-1	-1.6		mA
I_{CCH} Supply current, outputs high	$V_{CC} = \text{MAX}$, $V_I = 5 \text{ V}$	7	11		7	11		mA
I_{CCL} Supply current, outputs low	$V_{CC} = \text{MAX}$, $V_I = 0$	52	65		52	65		mA

‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

§ All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.

switching characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH} Propagation delay time, low-to-high-level output	$I_O \approx 200 \text{ mA}$, $C_L = 15 \text{ pF}$, $R_L = 50 \Omega$, See Figure 1		18	25	ns
t_{PHL} Propagation delay time, high-to-low-level output			18	25	
t_{TLH} Transition time, low-to-high-level output			5	8	
t_{THL} Transition time, high-to-low-level output			7	12	
V_{OH} High-level output voltage after switching	SN55451B	$V_S - 6.5$			mV
	SN75451B	$V_S - 6.5$			

SN55451B, SN55452B, SN55453B, SN55454B SN75451B, SN75452B, SN75453B, SN75454B DUAL PERIPHERAL DRIVERS

SLRS021B – DECEMBER 1976 – REVISED SEPTEMBER 1999

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC publication 617-12.

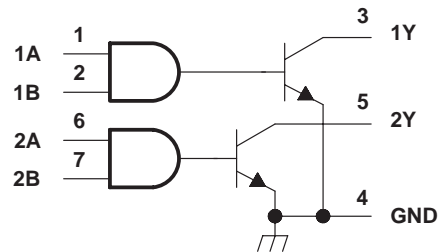
Pin numbers shown are for the D, JG, and P packages.

FUNCTION TABLE
(each driver)

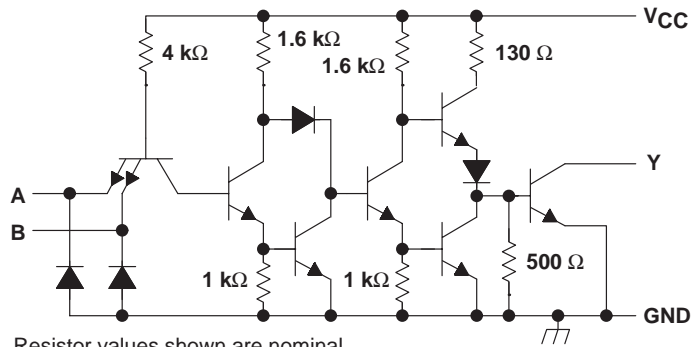
A	B	Y
L	L	H (off state)
L	H	H (off state)
H	L	H (off state)
H	H	L (on state)

positive logic:
 $Y = \overline{AB}$ or $\overline{A+B}$

logic diagram (positive logic)



schematic (each driver)



Resistor values shown are nominal.

electrical characteristics over recommended operating free-air temperature range

PARAMETER	TEST CONDITIONS‡	SN55452B			SN75452B			UNIT	
		MIN	TYP§	MAX	MIN	TYP§	MAX		
V_{IK} Input clamp voltage	$V_{CC} = \text{MIN}$, $I_I = -12 \text{ mA}$	-1.2	-1.5		-1.2	-1.5		V	
V_{OL} Low-level output voltage	$V_{CC} = \text{MIN}$, $V_{IH} = \text{MIN}$, $I_{OL} = 100 \text{ mA}$		0.25	0.5		0.25	0.4	V	
	$V_{CC} = \text{MIN}$, $V_{IH} = \text{MIN}$, $I_{OL} = 300 \text{ mA}$		0.5	0.8		0.5	0.7		
I_{OH} High-level output current	$V_{CC} = \text{MIN}$, $V_{IL} = 0.8 \text{ V}$, $V_{OH} = 30 \text{ V}$			300			100	μA	
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}$, $V_I = 5.5 \text{ V}$			1			1	mA	
I_{IH} High-level input current	$V_{CC} = \text{MAX}$, $V_I = 2.4 \text{ V}$			40			40	μA	
I_{IL} Low-level input current	$V_{CC} = \text{MAX}$, $V_I = 0.4 \text{ V}$			-1.1			-1.1	-1.6	mA
I_{CCH} Supply current, outputs high	$V_{CC} = \text{MAX}$, $V_I = 0$			11			11	14	mA
I_{CCL} Supply current, outputs low	$V_{CC} = \text{MAX}$, $V_I = 5 \text{ V}$			56			56	71	mA

‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

§ All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.

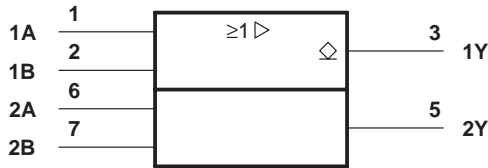
switching characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH} Propagation delay time, low-to-high-level output	$I_O \approx 200 \text{ mA}$, $C_L = 15 \text{ pF}$, $R_L = 50 \Omega$, See Figure 1		26	35	ns
t_{PHL} Propagation delay time, high-to-low-level output			24	35	
t_{TLH} Transition time, low-to-high-level output			5	8	
t_{THL} Transition time, high-to-low-level output			7	12	
V_{OH} High-level output voltage after switching	SN55452B	$V_S - 6.5$			mV
	SN75452B	$V_S - 6.5$			

SN55451B, SN55452B, SN55453B, SN55454B SN75451B, SN75452B, SN75453B, SN75454B DUAL PERIPHERAL DRIVERS

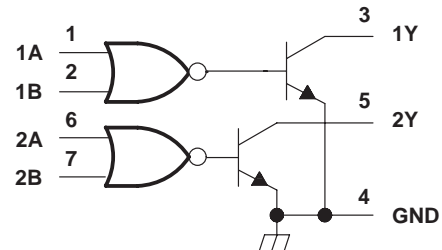
SLRS021B – DECEMBER 1976 – REVISED SEPTEMBER 1999

logic symbol†

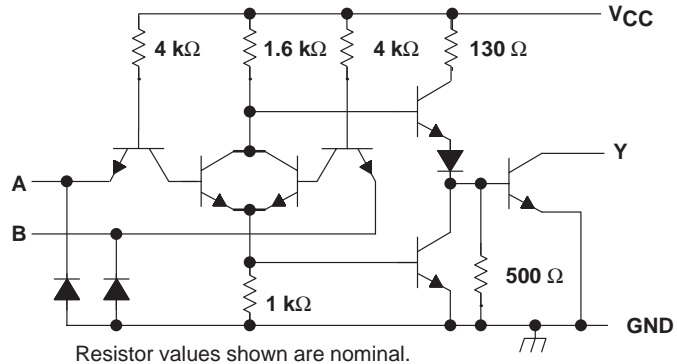


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC publication 617-12. Pin numbers shown are for the D, JG, and P packages.

logic diagram (positive logic)



schematic (each driver)



FUNCTION TABLE
(each driver)

A	B	Y
L	L	L (on state)
L	H	H (off state)
H	L	H (off state)
H	H	H (off state)

positive logic:
 $Y = A+B$ or $\overline{A} \overline{B}$

electrical characteristics over recommended operating free-air temperature range

PARAMETER	TEST CONDITIONS‡	SN55453B		SN75453B		UNIT		
		MIN	TYP§	MAX	MIN		TYP§	MAX
V_{IK} Input clamp voltage	$V_{CC} = \text{MIN}$, $I_I = -12 \text{ mA}$	-1.2		-1.5	-1.2		-1.5	V
V_{OL} Low-level output voltage	$V_{CC} = \text{MIN}$, $V_{IL} = 0.8 \text{ V}$, $I_{OL} = 100 \text{ mA}$	0.25		0.5	0.25		0.4	V
	$V_{CC} = \text{MIN}$, $V_{IL} = 0.8 \text{ V}$, $I_{OL} = 300 \text{ mA}$	0.5		0.8	0.5		0.7	
I_{OH} High-level output current	$V_{CC} = \text{MIN}$, $V_{IH} = \text{MIN}$, $V_{OH} = 30 \text{ V}$			300			100	μA
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}$, $V_I = 5.5 \text{ V}$			1			1	mA
I_{IH} High-level input current	$V_{CC} = \text{MAX}$, $V_I = 2.4 \text{ V}$			40			40	μA
I_{IL} Low-level input current	$V_{CC} = \text{MAX}$, $V_I = 0.4 \text{ V}$	-1		-1.6	-1		-1.6	mA
I_{CCH} Supply current, outputs high	$V_{CC} = \text{MAX}$, $V_I = 5 \text{ V}$	8		11	8		11	mA
I_{CCL} Supply current, outputs low	$V_{CC} = \text{MAX}$, $V_I = 0$	54		68	54		68	mA

‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

§ All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.

switching characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH} Propagation delay time, low-to-high-level output	$I_O \approx 200 \text{ mA}$, $C_L = 15 \text{ pF}$, $R_L = 50 \Omega$, See Figure 1		18	25	ns
t_{PHL} Propagation delay time, high-to-low-level output			18	25	
t_{TLH} Transition time, low-to-high-level output			5	8	
t_{THL} Transition time, high-to-low-level output			7	12	
V_{OH} High-level output voltage after switching	SN55453B	$V_S - 6.5$			mV
	SN75453B	$V_S - 6.5$			

SN55451B, SN55452B, SN55453B, SN55454B SN75451B, SN75452B, SN75453B, SN75454B DUAL PERIPHERAL DRIVERS

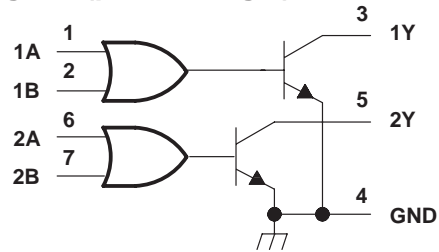
SLRS021B – DECEMBER 1976 – REVISED SEPTEMBER 1999

logic symbol†

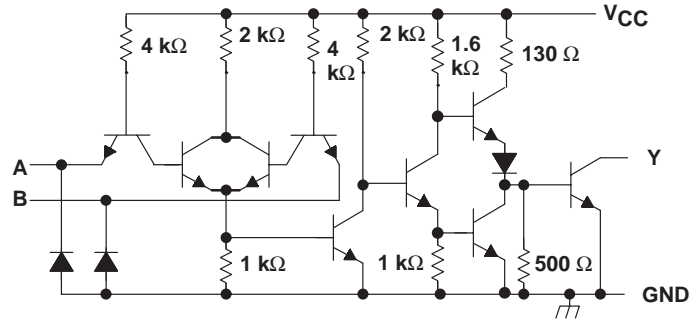


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC publication 617-12. Pin numbers shown are for the D, JG, and P packages.

logic diagram (positive logic)



schematic (each driver)



Resistor values shown are nominal.

FUNCTION TABLE
(each driver)

A	B	Y
L	L	H (off state)
L	H	L (on state)
H	L	L (on state)
H	H	L (on state)

positive logic:
 $Y = A+B$ or \overline{AB}

electrical characteristics over recommended operating free-air temperature range

PARAMETER	TEST CONDITIONS‡	SN55454B			SN75454B			UNIT
		MIN	TYP§	MAX	MIN	TYP§	MAX	
V_{IK} Input clamp voltage	$V_{CC} = \text{MIN}$, $I_I = -12 \text{ mA}$	-1.2	-1.5		-1.2	-1.5		V
V_{OL} Low-level output voltage	$V_{CC} = \text{MIN}$, $V_{IH} = \text{MIN}$, $I_{OL} = 100 \text{ mA}$	0.25	0.5		0.25	0.4		V
	$V_{CC} = \text{MIN}$, $V_{IH} = \text{MIN}$, $I_{OL} = 300 \text{ mA}$	0.5	0.8		0.5	0.7		
I_{OH} High-level output current	$V_{CC} = \text{MIN}$, $V_{OH} = 30 \text{ V}$, $V_{IL} = 0.8 \text{ V}$			300			100	μA
I_I Input current at maximum input voltage	$V_{CC} = \text{MAX}$, $V_I = 5.5 \text{ V}$			1			1	mA
I_{IH} High-level input current	$V_{CC} = \text{MAX}$, $V_I = 2.4 \text{ V}$			40			40	μA
I_{IL} Low-level input current	$V_{CC} = \text{MAX}$, $V_I = 0.4 \text{ V}$	-1	-1.6		-1	-1.6		mA
I_{CCH} Supply current, outputs high	$V_{CC} = \text{MAX}$, $V_I = 0$	13	17		13	17		mA
I_{CCL} Supply current, outputs low	$V_{CC} = \text{MAX}$, $V_I = 5 \text{ V}$	61	79		61	79		mA

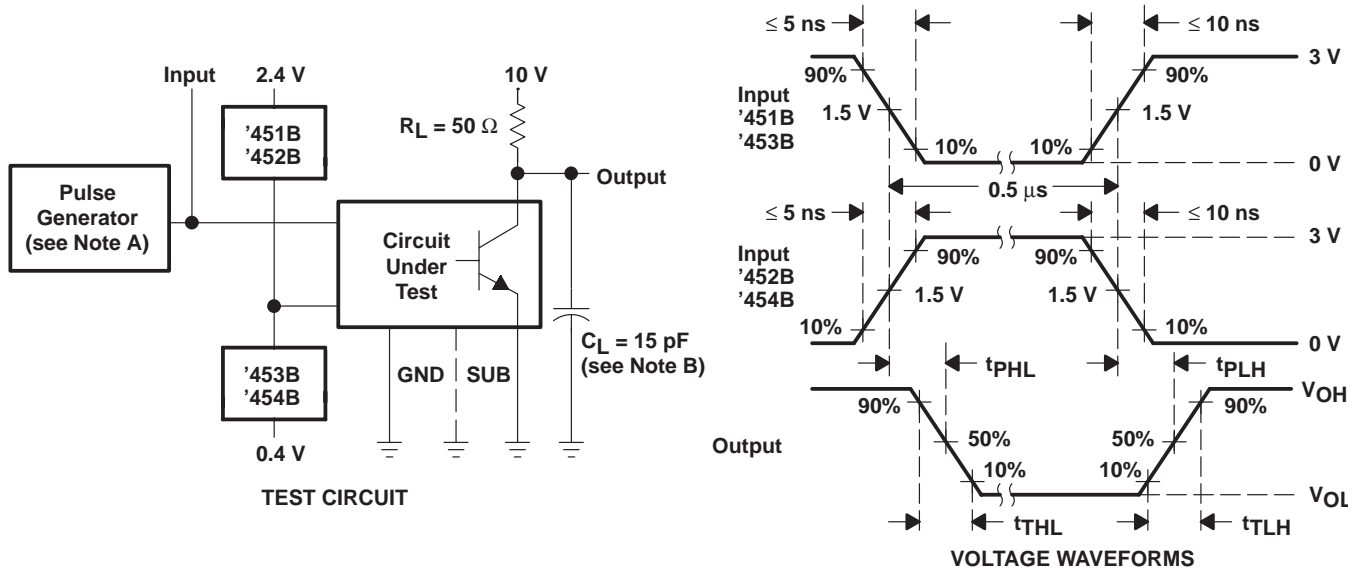
‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

§ All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.

switching characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$

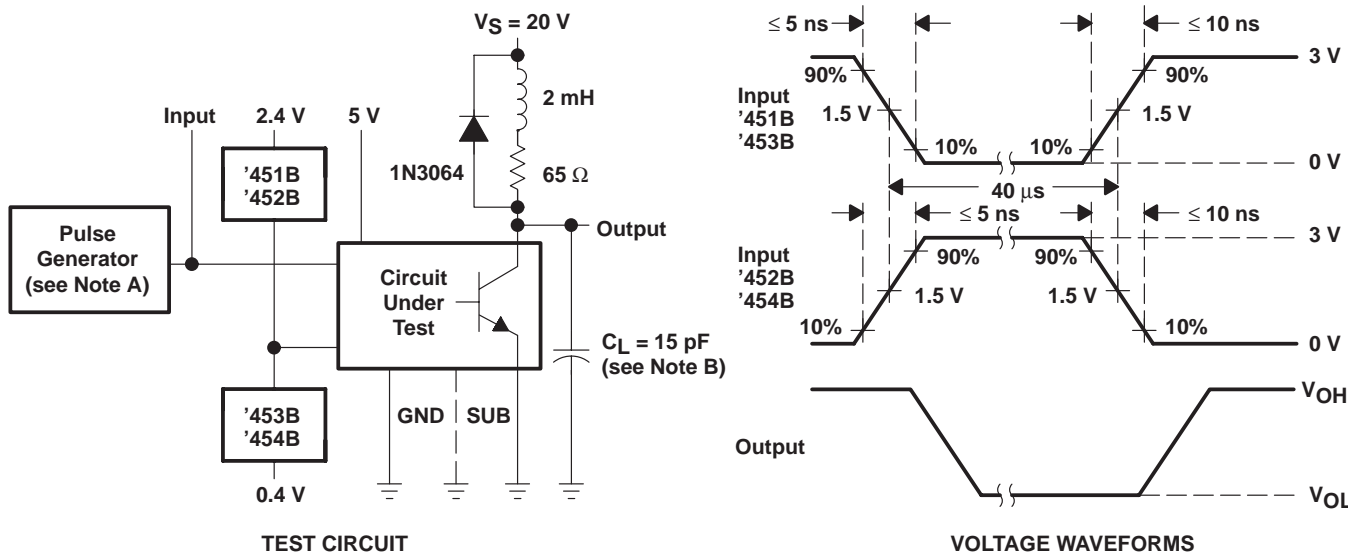
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
t_{PLH} Propagation delay time, low-to-high-level output	$I_O \approx 200 \text{ mA}$, $C_L = 15 \text{ pF}$, $R_L = 50 \Omega$, See Figure 1		27	35	ns	
t_{PHL} Propagation delay time, high-to-low-level output			24	35		
t_{TLH} Transition time, low-to-high-level output			5	8		
t_{THL} Transition time, high-to-low-level output			7	12		
V_{OH} High-level output voltage after switching	SN55454B	$V_S = 20 \text{ V}$, $I_O \approx 300 \text{ mA}$, See Figure 2			$V_S - 6.5$	mV
	SN75454B				$V_S - 6.5$	

PARAMETER MEASUREMENT INFORMATION



NOTES: A. The pulse generator has the following characteristics: PRR \leq 1 MHz, $Z_O = 50 \Omega$.
 B. C_L includes probe and jig capacitance.

Figure 1. Test Circuit and Voltage Waveforms, Complete Drivers

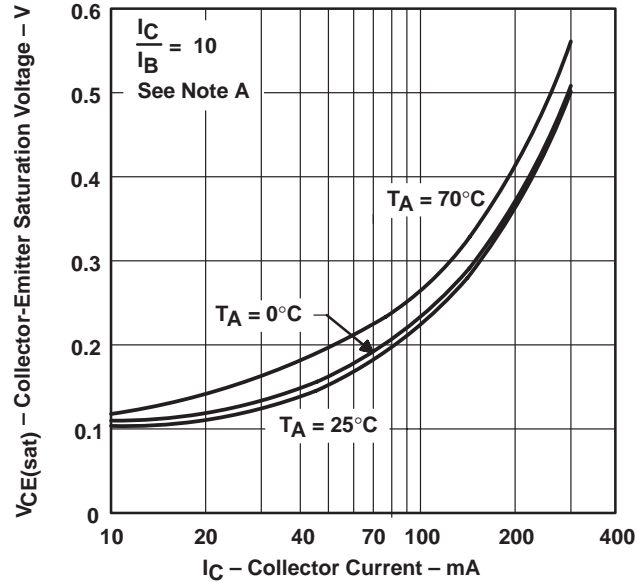


NOTES: A. The pulse generator has the following characteristics: PRR \leq 12.5 kHz, $Z_O = 50 \Omega$.
 B. C_L includes probe and jig capacitance.

Figure 2. Test Circuit and Voltage Waveforms for Latch-Up Test of Complete Drivers

TYPICAL CHARACTERISTICS

TRANSISTOR
COLLECTOR-EMITTER SATURATION VOLTAGE
vs
COLLECTOR CURRENT



NOTE A: These parameters must be measured using pulse techniques, $t_w = 300 \mu\text{s}$, duty cycle $\leq 2\%$.

Figure 3

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-9563301Q2A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962- 9563301Q2A SNJ55 453BFK	Samples
5962-9563301QPA	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	9563301QPA SNJ55453B	Samples
77049012A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	77049012A SNJ55 452BFK	Samples
7704901PA	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	7704901PA SNJ55452B	Samples
77049022A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	77049022A SNJ55 451BFK	Samples
7704902PA	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	7704902PA SNJ55451B	Samples
JM38510/12902BPA	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510 /12902BPA	Samples
JM38510/12903BPA	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510 /12903BPA	Samples
JM38510/12905BPA	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510 /12905BPA	Samples
M38510/12902BPA	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510 /12902BPA	Samples
M38510/12903BPA	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510 /12903BPA	Samples
M38510/12905BPA	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510 /12905BPA	Samples
SN55451BJG	ACTIVE	CDIP	JG	8	50	TBD	A42	N / A for Pkg Type	-55 to 125	SN55451BJG	Samples
SN55452BJG	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	SN55452BJG	Samples
SN55453BJG	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	SN55453BJG	Samples
SN55454BJG	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	SN55454BJG	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN75451BD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	75451B	Samples
SN75451BDE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	75451B	Samples
SN75451BDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	75451B	Samples
SN75451BDRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	75451B	Samples
SN75451BDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	75451B	Samples
SN75451BP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN75451BP	Samples
SN75451BPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN75451BP	Samples
SN75451BPSR	ACTIVE	SO	PS	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	A451B	Samples
SN75452BD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	75452B	Samples
SN75452BDE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	75452B	Samples
SN75452BDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	75452B	Samples
SN75452BDRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	75452B	Samples
SN75452BDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	75452B	Samples
SN75452BP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN75452BP	Samples
SN75452BPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN75452BP	Samples
SN75452BPSR	ACTIVE	SO	PS	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	A452B	Samples
SN75452BPSRE4	ACTIVE	SO	PS	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	A452B	Samples
SN75452BPSRG4	ACTIVE	SO	PS	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	A452B	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN75453BD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	75453B	Samples
SN75453BDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	75453B	Samples
SN75453BDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	75453B	Samples
SN75453BDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	75453B	Samples
SN75453BP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN75453BP	Samples
SN75453BPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN75453BP	Samples
SN75453BPSR	ACTIVE	SO	PS	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	A453B	Samples
SN75454BD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	75454B	Samples
SN75454BDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	75454B	Samples
SN75454BP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN75454BP	Samples
SN75454BPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN75454BP	Samples
SN75454BPSR	ACTIVE	SO	PS	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	A454B	Samples
SNJ55451BFK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	77049022A SNJ55 451BFK	Samples
SNJ55451BJG	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	7704902PA SNJ55451B	Samples
SNJ55452BFK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	77049012A SNJ55 452BFK	Samples
SNJ55452BJG	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	7704901PA SNJ55452B	Samples
SNJ55453BFK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962- 9563301Q2A SNJ55	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
										453BFBK	
SNJ55453BJG	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	9563301QPA SNJ55453B	Samples
SNJ55454BFBK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	SNJ55 454BFBK	Samples
SNJ55454BJG	ACTIVE	CDIP	JG	8	1	TBD	A42	N / A for Pkg Type	-55 to 125	SNJ55 454BJG	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN55451B, SN55452B, SN55453B, SN55454B, SN75451B, SN75452B, SN75453B, SN75454B :

- Catalog: [SN75451B](#), [SN75452B](#), [SN75453B](#), [SN75454B](#)
- Military: [SN55451B](#), [SN55452B](#), [SN55453B](#), [SN55454B](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION
REEL DIMENSIONS

TAPE DIMENSIONS


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN75451BDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN75451BPSR	SO	PS	8	2000	330.0	16.4	8.2	6.6	2.5	12.0	16.0	Q1
SN75452BDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN75452BPSR	SO	PS	8	2000	330.0	16.4	8.2	6.6	2.5	12.0	16.0	Q1
SN75453BDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN75453BPSR	SO	PS	8	2000	330.0	16.4	8.2	6.6	2.5	12.0	16.0	Q1
SN75454BDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN75454BPSR	SO	PS	8	2000	330.0	16.4	8.2	6.6	2.5	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN75451BDR	SOIC	D	8	2500	340.5	338.1	20.6
SN75451BPSR	SO	PS	8	2000	367.0	367.0	38.0
SN75452BDR	SOIC	D	8	2500	340.5	338.1	20.6
SN75452BPSR	SO	PS	8	2000	367.0	367.0	38.0
SN75453BDR	SOIC	D	8	2500	340.5	338.1	20.6
SN75453BPSR	SO	PS	8	2000	367.0	367.0	38.0
SN75454BDR	SOIC	D	8	2500	340.5	338.1	20.6
SN75454BPSR	SO	PS	8	2000	367.0	367.0	38.0

JG (R-GDIP-T8)

CERAMIC DUAL-IN-LINE



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. This package can be hermetically sealed with a ceramic lid using glass frit.
 D. Index point is provided on cap for terminal identification.
 E. Falls within MIL STD 1835 GDIP1-T8

FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



4040140/D 01/11

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package can be hermetically sealed with a metal lid.
 - Falls within JEDEC MS-004

P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Falls within JEDEC MS-001 variation BA.

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



4211283-2/E 08/12

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

MECHANICAL DATA

PS (R-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

PS (R-PDSO-G8)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as "components") are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI's terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers' products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers' products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI's goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or "enhanced plastic" are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have **not** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products

Audio	www.ti.com/audio
Amplifiers	amplifier.ti.com
Data Converters	dataconverter.ti.com
DLP® Products	www.dlp.com
DSP	dsp.ti.com
Clocks and Timers	www.ti.com/clocks
Interface	interface.ti.com
Logic	logic.ti.com
Power Mgmt	power.ti.com
Microcontrollers	microcontroller.ti.com
RFID	www.ti-rfid.com
OMAP Applications Processors	www.ti.com/omap
Wireless Connectivity	www.ti.com/wirelessconnectivity

Applications

Automotive and Transportation	www.ti.com/automotive
Communications and Telecom	www.ti.com/communications
Computers and Peripherals	www.ti.com/computers
Consumer Electronics	www.ti.com/consumer-apps
Energy and Lighting	www.ti.com/energy
Industrial	www.ti.com/industrial
Medical	www.ti.com/medical
Security	www.ti.com/security
Space, Avionics and Defense	www.ti.com/space-avionics-defense
Video and Imaging	www.ti.com/video

TI E2E Community

e2e.ti.com