MRF24J40MC Data Sheet

2.4 GHz IEEE Std. 802.15.4™ RF Transceiver Module with PA/LNA and External Antenna Connector

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ISBN: 978-1-61341-006-6

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MRF24J40MC

2.4 GHz IEEE Std. 802.15.4™ RF Transceiver Module with PA/LNA and External Antenna Connector

Features:

- IEEE Std. 802.15.4™ Compliant RF Transceiver
- Supports ZigBee®, MiWi™ Development Environment Proprietary Wireless Networking Protocols
- 4-Wire Serial Peripheral Interface (SPI) with Interrupt
- Small size: 0.9" x 1.3" (22.9 mm x 33.0 mm), Surface Mountable : Pin Compatible with MRF24J40MB
- Integrated Crystal, Internal Voltage Regulator, Matching Circuitry, Power Amplifier, Low Noise Amplifier
- External Antenna Connector : Ultra Miniature Coaxial (U.FL), 50Ω
- Easy Integration into Final Product : Minimize Product Development, Quicker Time to Market
- Radio Regulation Certified for United States (FCC), Canada (IC), Europe (ETSI) and Australia/New Zealand (C-TICK)
- Compatible with Microchip microcontroller families (PIC16, PIC18, PIC24, dsPIC33 and PIC32)
- Range up to 4000 ft

Operational:

- Operating Voltage: 2.7V – 3.6V (3.3V typical)
- Temperature Range: -40°C to +85°C Industrial
- Low-Current Consumption:
  - Rx Mode: 25 mA (typical)
 - Tx Mode: 120 mA (typical)
  - Sleep: 12 µA (typical)

RF/Analog Features:

- ISM Band 2.405 GHz – 2.475 GHz Operation
- Data Rate: 250 kbps
- -108 dBm Typical Sensitivity with -23 dBm Maximum Input Level
- +19 dBm Typical Output Power with 45 dB Tx Power Control Range
- Integrated Low Phase Noise VCO, Frequency Synthesizer and PLL Loop Filter
- Digital VCO and Filter Calibration
- Integrated RSSI ADC and I/Q DACs
- Integrated LDO
- High Receiver RSSI Dynamic Range

MAC/Baseband Features:

- Hardware CSMA-CA Mechanism, Automatic ACK Response and FCS Check
- Independent Beacon, Transmit and GTS FIFO
- Supports all CCA modes and RSS/LQI
- Automatic Packet Retransmit Capable
- Hardware Security Engine (AES-128) with CTR, CCM and CBC-MAC modes
- Supports Encryption and Decryption for MAC Sub layer and Upper Layer

Pin Diagram:

GND	1	
RESET	2	
WAKE	3	
INT	4	
SDI	5	
SCK	6	

	12	GND
	11	GND
	10	V$_{IN}$
	9	NC
	8	CS
	7	SDO
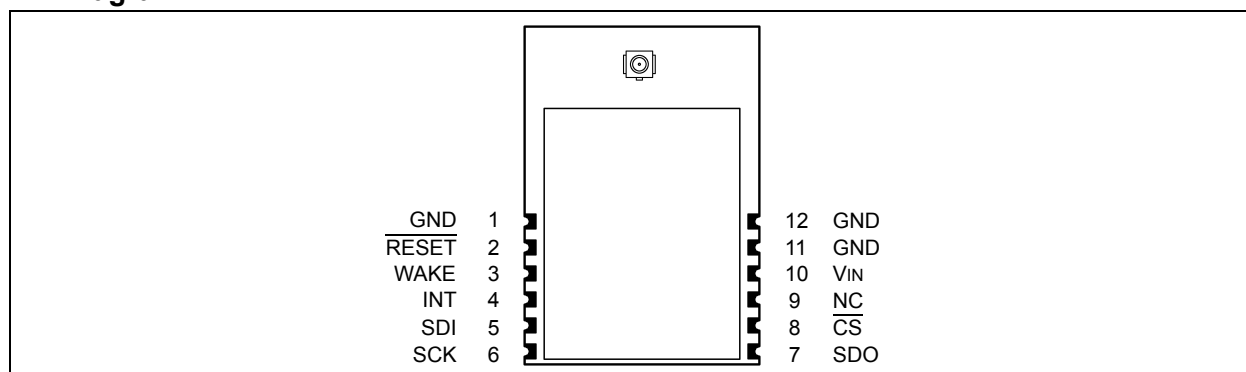
1.0   DEVICE OVERVIEW

The MRF24J40MC is a 2.4 GHz IEEE Std. 802.15.4™ compliant, surface mount module with integrated crystal, internal voltage regulator, matching circuitry, Power Amplifier (PA), Low Noise Amplifier (LNA) with 50Ω external antenna connector. The MRF24J40MC module operates in the non-licensed 2.4 GHz frequency band. The integrated module design frees the integrator from extensive RF and antenna design, and regulatory compliance testing allowing quicker time to market.

The MRF24J40MC module is compatible with Microchip's ZigBee®, and MiWi™ Development Environment software stacks. The MiWi Development Environment software stack including the source code is available as a free download, from the Microchip web site: http://www.microchip.com/wireless.

The MRF24J40MC module has received regulatory approvals for modular devices in the United States (FCC) and Canada (IC). Modular approval removes the need for expensive RF and antenna design, and allows the end user to place the MRF24J40MC module inside a finished product and does not require regulatory testing for an intentional radiator (RF transmitter). To maintain conformance, refer to module settings in **Section 3.1.1 "MRF24J40MC Settings"** for the United States and **Section 3.2.1 "MRF24J40MC Settings"** for Canada.

The MRF24J40MC module has been tested and conforms to ETS EN 300 328 V1.7.1 (2006-10) European Standards. The module tests can be applied toward final product certification and Declaration of Conformity (DoC). To maintain conformance for Europe, refer to module settings in **Section 3.3.1 "MRF24J40MC Settings"**. Additional testing may be required depending on the end application.

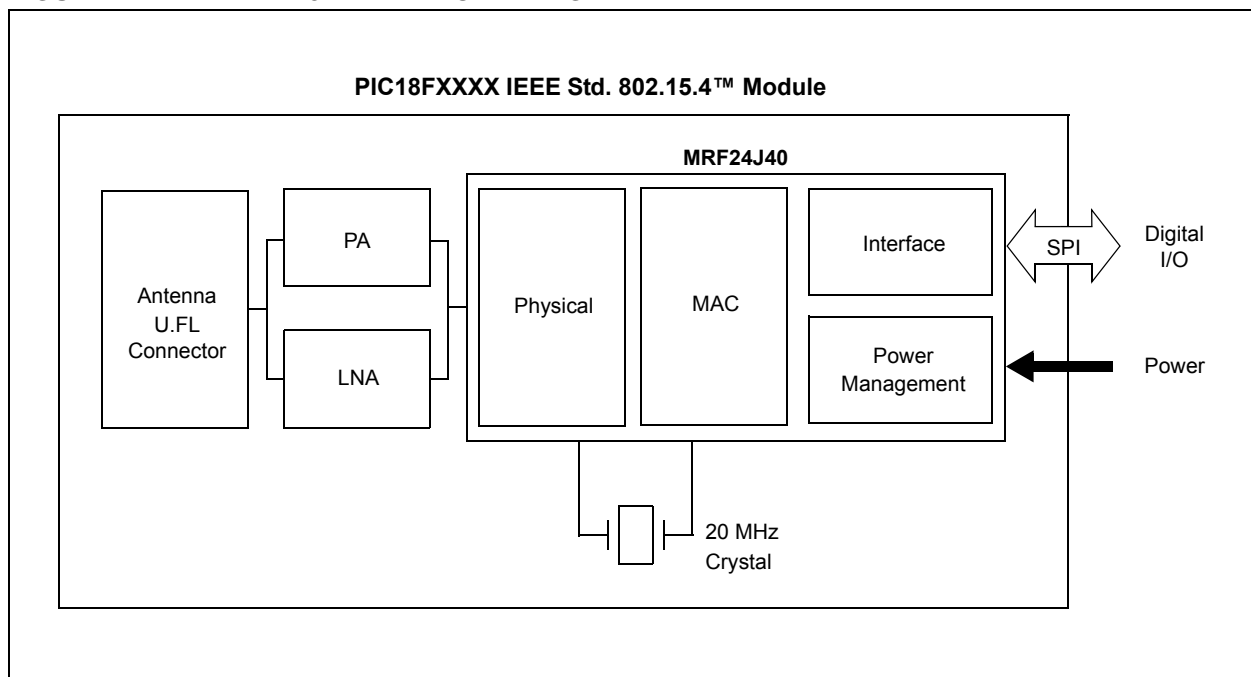### 1.1   Interface Description

Figure 1-1 shows a simplified block diagram of the MRF24J40MC module. The module is based on the Microchip Technology MRF24J40 IEEE 802.15.4™ 2.4 GHz RF Transceiver IC. The module interfaces to many popular Microchip PIC® microcontrollers through a 4-wire SPI interface, interrupt, wake, reset, power and ground, as shown in Figure 1-2. Table 1-1 provides the pin descriptions.

Serial communication and module configuration for the MRF24J40MC module are documented in the *"MRF24J40 Data Sheet"* (DS39776). Refer to the datasheet for specific serial interface protocol and register definitions.

Also, see **Section 1.3 "Operation"** for specific register settings that are unique to the MRF24J40MC module.
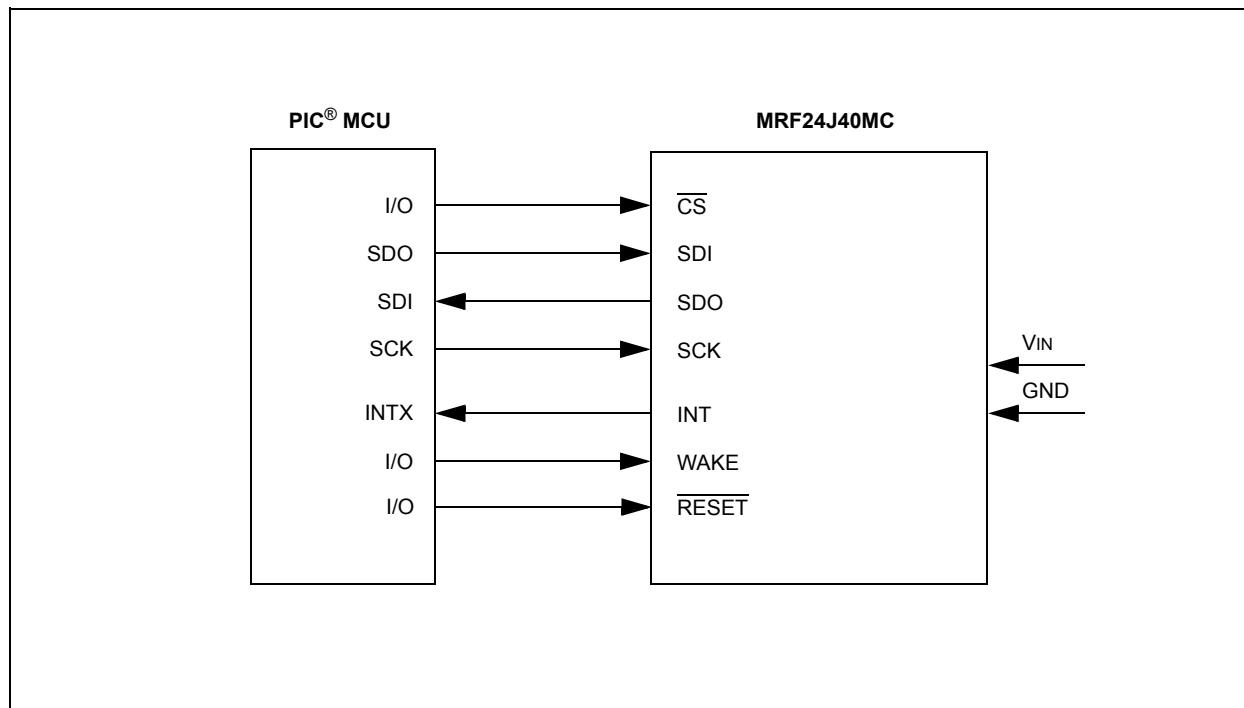
FIGURE 1-1:   PIC18FXXXX BLOCK DIAGRAM

MRF24J40MC

TABLE 1-1: PIN DESCRIPTION

Pin	Symbol	Type	Description
1	GND	Ground	Ground
2	$\overline{\text{RESET}}$	DI	Global hardware Reset pin
3	WAKE	DI	External wake-up trigger
4	INT	DO	Interrupt pin to microcontroller
5	SDI	DI	Serial interface data input
6	SCK	DI	Serial interface clock
7	SDO	DO	Serial interface data output from MRF24J40
8	$\overline{\text{CS}}$	DI	Serial interface enable
9	NC	—	No connection
10	V$_{IN}$	Power	Power supply
11	GND	Ground	Ground
12	GND	Ground	Ground

Legend: Pin type abbreviation: D = Digital, I = Input, O = Output

FIGURE 1-2: MICROCONTROLLER TO MRF24J40MC INTERFACE

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1.2 Mounting Details

The MRF24J40MC is a surface mountable module. Module dimensions are shown in Figure 1-3. The module Printed Circuit Board (PCB) is 0.032" thick with castellated mounting points on the edge. Figure 1-4 is a recommended host PCB footprint for the MRF24J40MC .

The MRF24J40MC has 50Ω ultra miniature coaxial (U.FL) connector.

Caution: The U.FL connector is fragile and can only tolerate very limited number of insertions.

FIGURE 1-3:   MODULE DETAILS

FIGURE 1-4:   RECOMMENDED PCB FOOTPRINT

MRF24J40MC

1.3 Operation

The MRF24J40MC module is based on the Microchip Technology MRF24J40 2.4 GHz IEEE 802.15.4 RF Transceiver IC. Serial communication and configuration are documented in the "*MRF24J40 Data Sheet*" (DS39776).

This section emphasizes operational settings that are unique to the MRF24J40MC module design that must be followed for proper operation.

1.3.1 PA/LNA CONTROL

Operation of the PA U3 and LNA U2 is controlled by the MRF24J40 internal RF state machine through RF switches, U1 and U4, and the GPIO1 and GPIO2 pins on the MRF24J40. Figure 1-5 shows the PA/LNA block diagram. Figure 2-2 is the schematic diagram for the module.

The internal RF state machine is configured for the PA/LNA Mode by setting TESTMODE (0x22<2:0>) = 111. Pins GPIO1 and GPIO2 control the RF switches, PA and LNA automatically when the MRF24J40 receives and transmits data.

> **Note:** A complete explanation of the operation of the PA/LNA control is documented in the "*MRF24J40 Data Sheet*" (DS39776), Section 4.2 "External PA/LNA Control".

Voltage regulator U5 supplies a regulated 2.2V to the PA. This provides a stable voltage to the PA over the V_{IN} voltage range of the module. U5 is enabled or shutdown from GPIO3. Ensure that the GPIO3 direction has been set to output (TRISGP3 (0x34<3>) = 1). Setting a logic high (GPIO3(0x33<3>) = 1) enables the voltage regulator and supplies voltage to the PA. Setting a logic low (GPIO3 (0x33<3>) = 0) will shutdown the voltage regulator, disabling the PA, and provides the lowest shutdown current.

FIGURE 1-5:   PA/LNA BLOCK DIAGRAM
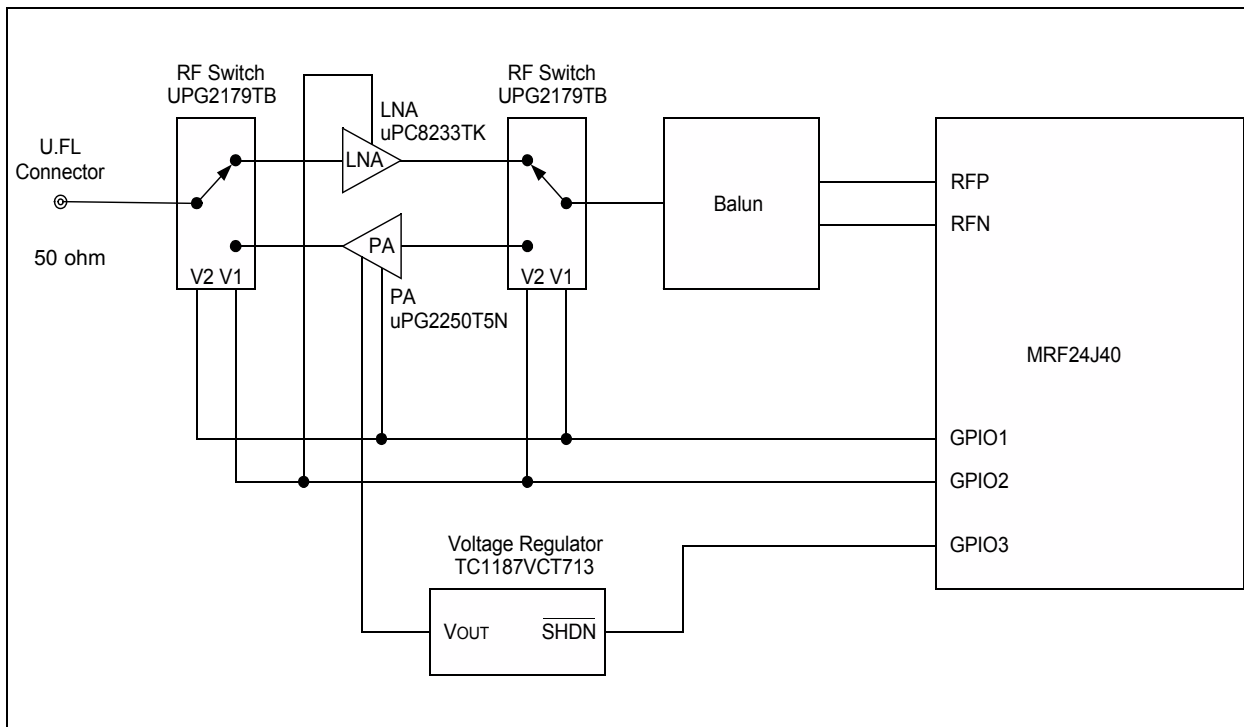
1.3.2 ENERGY DETECTION (ED)

Before performing an energy detection (see Section 3.6.1 "RSSI Firmware Request (RSSI Mode 1)" in the *"MRF24J40 Data Sheet"* (DS39776)), perform the following steps:

1. Configure the internal RF state machine to normal operation (TESTMODE (0x22F<2:0>) = 000).

2. Configure GPIO2 and GPIO1 direction for output (TRISGP2 (0x34<2>) = 1 and TRISGP1 (0x34<1>) = 1).

3. Set GPIO2 (0x33<2>) = 1 and GPIO1 (0x32<1>) = 0. This enables the LNA and disables the PA.

4. Perform the energy detection following the steps in Section 3.6.1 "RSSI Firmware Request (RSSI Mode 1)" in the *"MRF24J40 Data Sheet"* (DS39776).

> **Note:** The LNA will amplify the received signal. The RSSI value will include the receive signal strength plus the LNA amplification.

1.3.3 SLEEP

To get the lowest power consumption from the MRF24J40MC module during Sleep, it is necessary to disable the PA, PA voltage regulator and LNA. To do this, perform the following steps:

1. Configure the internal RF state machine to normal operation (TESTMODE (0x22F<2:0>) = 000).

2. Configure the GPIO3, GPIO2 and GPIO1 direction for output (TRISGP3 (0x34<3>) = 1, TRISGP2 (0x34<2>) = 1 and TRISGP1 (0x34<1>) = 1).

3. Set GPIO2 (0x33<2>) = 0 and GPIO1 (0x32<1>) = 0. This disables the LNA and the PA.

4. Set GPIO3 (0x33<3>) = 0. This shuts down the voltage regulator U5 that supplies 2.2 volts to the PA.

5. Put the MRF24J40 to Sleep following the steps in the *"MRF24J40 Data Sheet"* (DS39776).

When waking the module, re-enable the PA/LNA Mode.