

N-Channel 45 V (D-S) MOSFET



PRODUCT SUMMARY	
V_{DS} (V)	45
$R_{DS(on)}$ max. (Ω) at $V_{GS} = 10$ V	0.00120
$R_{DS(on)}$ max. (Ω) at $V_{GS} = 4.5$ V	0.00180
Q_g typ. (nC)	50.5
I_D (A) ^a	208
Configuration	Single

FEATURES

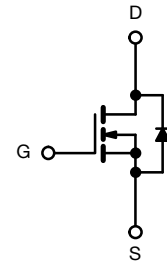
- TrenchFET® Gen IV power MOSFET
- 45 V Drain-source break-down voltage
- Tuned for low Q_g and Q_{oss}
- 100 % R_g and UIS tested
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912



RoHS
COMPLIANT
HALOGEN
FREE

APPLICATIONS

- Synchronous rectification
- High power density DC/DC
- Motor drive control



N-Channel MOSFET

ORDERING INFORMATION	
Package	PowerPAK SO-8
Lead (Pb)-free and halogen-free	SiR608DP-T1-RE3

ABSOLUTE MAXIMUM RATINGS ($T_A = 25$ °C, unless otherwise noted)				
PARAMETER	SYMBOL	LIMIT	UNIT	
Drain-source voltage	V_{DS}	45	V	
Gate-source voltage	V_{GS}	+20, -16		
Continuous drain current ($T_J = 150$ °C)	I_D	$T_C = 25$ °C	208	A
		$T_C = 70$ °C	166	
		$T_A = 25$ °C	51 ^{b, c}	
		$T_A = 70$ °C	40.8 ^{b, c}	
Pulsed drain current ($t = 100$ μ s)	I_{DM}	400		
Continuous source-drain diode current	I_S	$T_C = 25$ °C	94.5	
		$T_A = 25$ °C	5.6 ^{b, c}	
Single pulse avalanche current	I_{AS}	50		
Single pulse avalanche Energy	E_{AS}	125	mJ	
Maximum power dissipation	P_D	$T_C = 25$ °C	104	W
		$T_C = 70$ °C	66.6	
		$T_A = 25$ °C	6.25 ^{b, c}	
		$T_A = 70$ °C	4 ^{b, c}	
Operating junction and storage temperature range	T_J, T_{stg}	-55 to +150	°C	
Soldering recommendations (peak temperature) ^{d, e}		260		

THERMAL RESISTANCE RATINGS					
PARAMETER	SYMBOL	TYPICAL	MAXIMUM	UNIT	
Maximum junction-to-ambient ^{b, f}	R_{thJA}	15	20	°C/W	
Maximum junction-to-case (drain)	R_{thJC}	0.9	1.2		

Notes

- Based on $T_C = 25$ °C
- Surface mounted on 1" x 1" FR4 board
- $t = 10$ s
- See solder profile (www.vishay.com/doc?73257). The PowerPAK SO-8 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection
- Rework conditions: manual soldering with a soldering iron is not recommended for leadless components
- Maximum under steady state conditions is 54 °C/W
- Package limited



SPECIFICATIONS ($T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static						
Drain-source breakdown voltage	V_{DS}	$V_{GS} = 0\text{ V}$, $I_D = 250\text{ }\mu\text{A}$	45	-	-	V
V_{DS} temperature coefficient	$\Delta V_{DS}/T_J$	$I_D = 10\text{ mA}$	-	29	-	mV/ $^\circ\text{C}$
$V_{GS(th)}$ temperature coefficient	$\Delta V_{GS(th)}/T_J$	$I_D = 250\text{ }\mu\text{A}$	-	-5.8	-	
Gate-source threshold voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$	1.1	-	2.3	V
Gate-source leakage	I_{GSS}	$V_{DS} = 0\text{ V}$, $V_{GS} = +20, -16\text{ V}$	-	-	± 100	nA
Zero gate voltage drain current	I_{DSS}	$V_{DS} = 45\text{ V}$, $V_{GS} = 0\text{ V}$	-	-	1	μA
		$V_{DS} = 45\text{ V}$, $V_{GS} = 0\text{ V}$, $T_J = 55\text{ }^\circ\text{C}$	-	-	10	
On-state drain current ^a	$I_{D(on)}$	$V_{DS} \geq 5\text{ V}$, $V_{GS} = 10\text{ V}$	50	-	-	A
Drain-source on-state resistance ^a	$R_{DS(on)}$	$V_{GS} = 10\text{ V}$, $I_D = 20\text{ A}$	-	0.00100	0.00120	Ω
		$V_{GS} = 4.5\text{ V}$, $I_D = 20\text{ A}$	-	0.00136	0.00180	
Forward transconductance ^a	g_{fs}	$V_{DS} = 10\text{ V}$, $I_D = 20\text{ A}$	-	120	-	S
Dynamic ^b						
Input capacitance	C_{iss}	$V_{DS} = 20\text{ V}$, $V_{GS} = 0\text{ V}$, $f = 1\text{ MHz}$	-	8900	-	pF
Output capacitance	C_{oss}		-	1244	-	
Reverse transfer capacitance	C_{rss}		-	120	-	
C_{rss}/C_{iss} ratio			-	0.0135	0.0270	
Total gate charge	Q_g	$V_{DS} = 20\text{ V}$, $V_{GS} = 10\text{ V}$, $I_D = 20\text{ A}$	-	111	167	nC
Gate-source charge	Q_{gs}	$V_{DS} = 20\text{ V}$, $V_{GS} = 4.5\text{ V}$, $I_D = 20\text{ A}$	-	50.5	76	
Gate-drain charge	Q_{gd}		-	26	-	
Output charge	Q_{oss}		$V_{DS} = 20\text{ V}$, $V_{GS} = 0\text{ V}$	-	59	
Gate resistance	R_g	$f = 1\text{ MHz}$	0.3	0.88	1.5	Ω
Turn-on delay time	$t_{d(on)}$	$V_{DD} = 20\text{ V}$, $R_L = 1\text{ }\Omega$ $I_D \cong 20\text{ A}$, $V_{GEN} = 10\text{ V}$, $R_g = 1\text{ }\Omega$	-	19	38	ns
Rise time	t_r		-	10	20	
Turn-off delay time	$t_{d(off)}$		-	50	100	
Fall time	t_f		-	8	16	
Turn-on delay time	$t_{d(on)}$	$V_{DD} = 20\text{ V}$, $R_L = 1\text{ }\Omega$ $I_D \cong 20\text{ A}$, $V_{GEN} = 4.5\text{ V}$, $R_g = 1\text{ }\Omega$	-	52	104	
Rise time	t_r		-	86	172	
Turn-off delay time	$t_{d(off)}$		-	50	100	
Fall time	t_f		-	25	50	
Drain-Source Body Diode Characteristics						
Continuous source-drain diode current	I_S	$T_C = 25\text{ }^\circ\text{C}$	-	-	94.5	A
Pulse diode forward current ($t_p = 100\text{ }\mu\text{s}$)	I_{SM}		-	-	400	
Body diode voltage	V_{SD}	$I_S = 10\text{ A}$	-	0.7	1.1	V
Body diode reverse recovery time	t_{rr}	$I_F = 10\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $T_J = 25\text{ }^\circ\text{C}$	-	52	104	ns
Body diode reverse recovery charge	Q_{rr}		-	71	142	nC
Reverse recovery fall time	t_a		-	32	-	ns
Reverse recovery rise time	t_b		-	20	-	

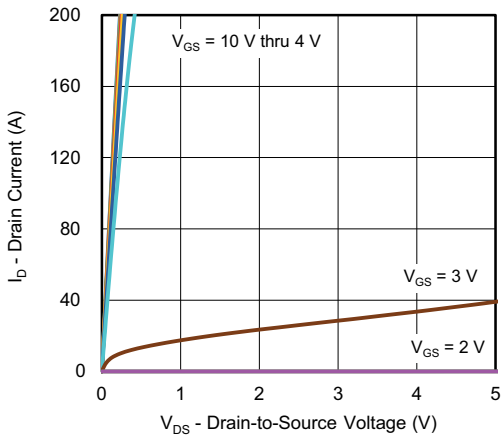
Notes

- a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$
b. Guaranteed by design, not subject to production testing

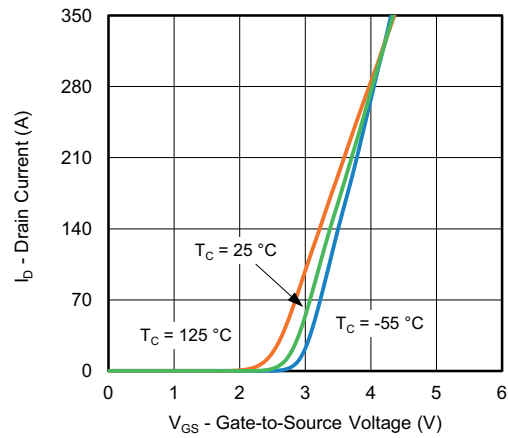
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



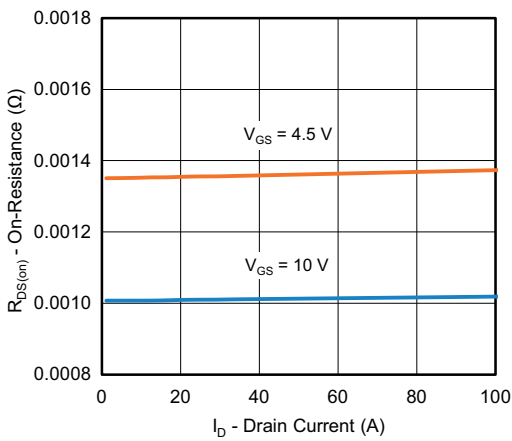
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



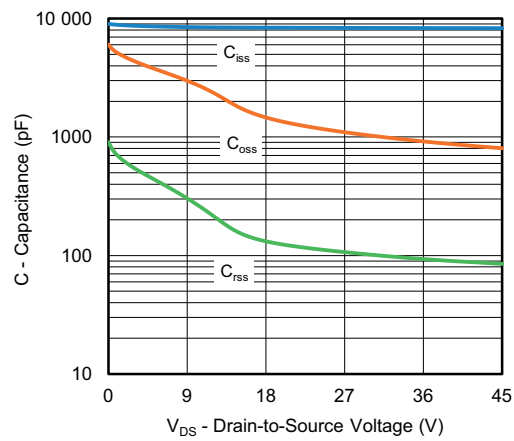
Output Characteristics



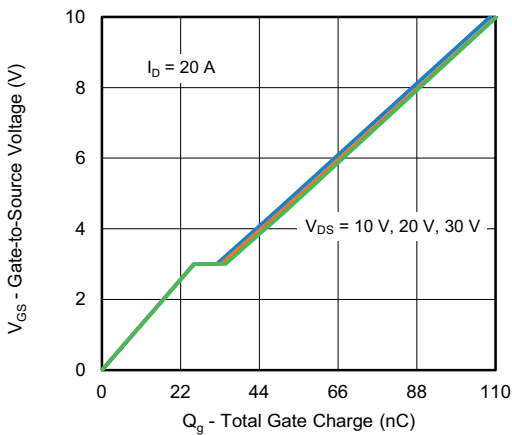
Transfer Characteristics



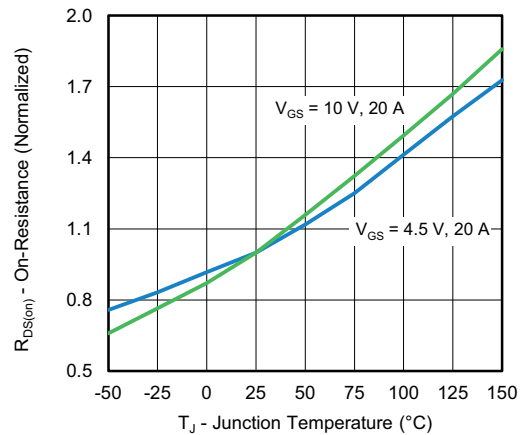
On-Resistance vs. Drain Current



Capacitance



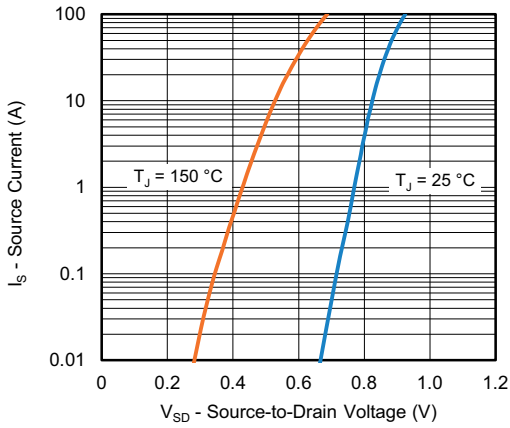
Gate Charge



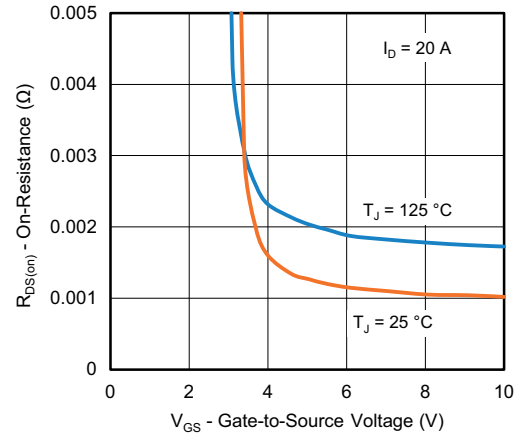
On-Resistance vs. Junction Temperature



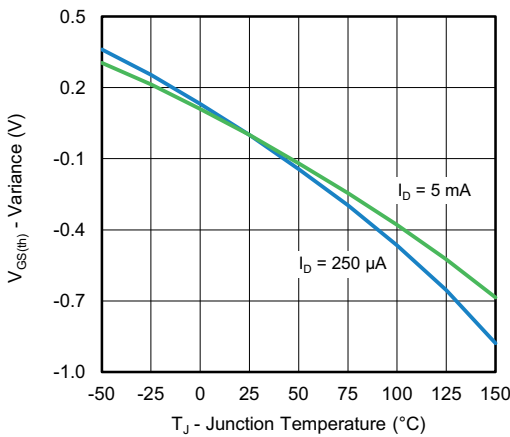
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



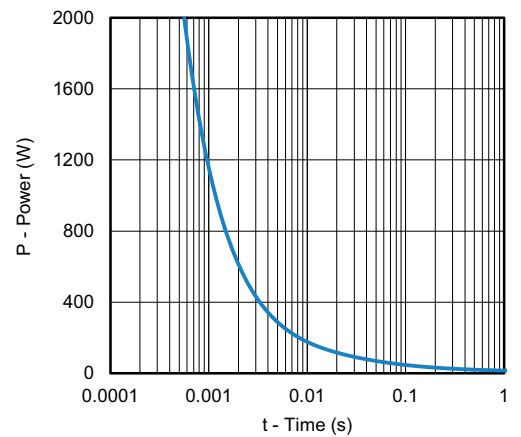
Source-Drain Diode Forward Voltage



On-Resistance vs. Gate-to-Source Voltage



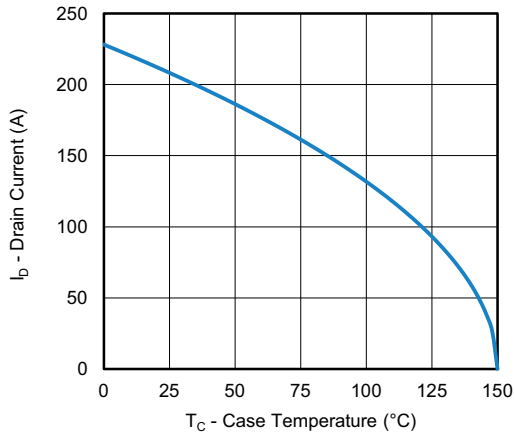
Threshold Voltage



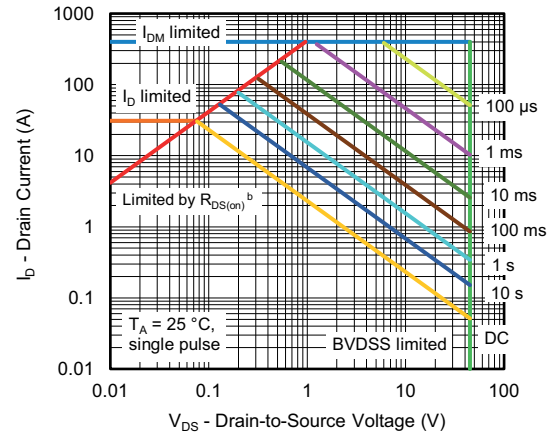
Single Pulse Power, Junction-to-Ambient



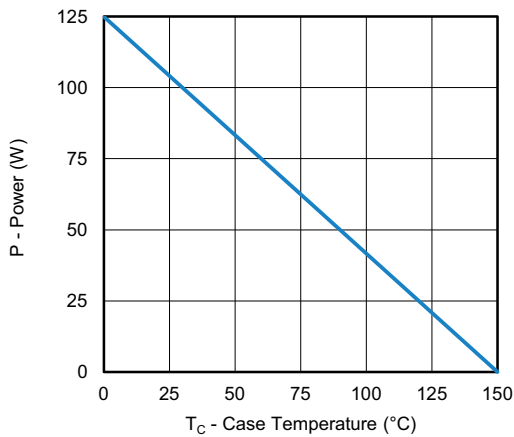
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



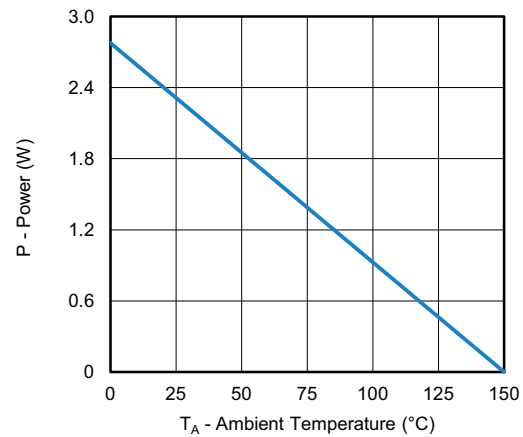
Current Derating ^a



Safe Operating Area



Power, Junction-to-Case



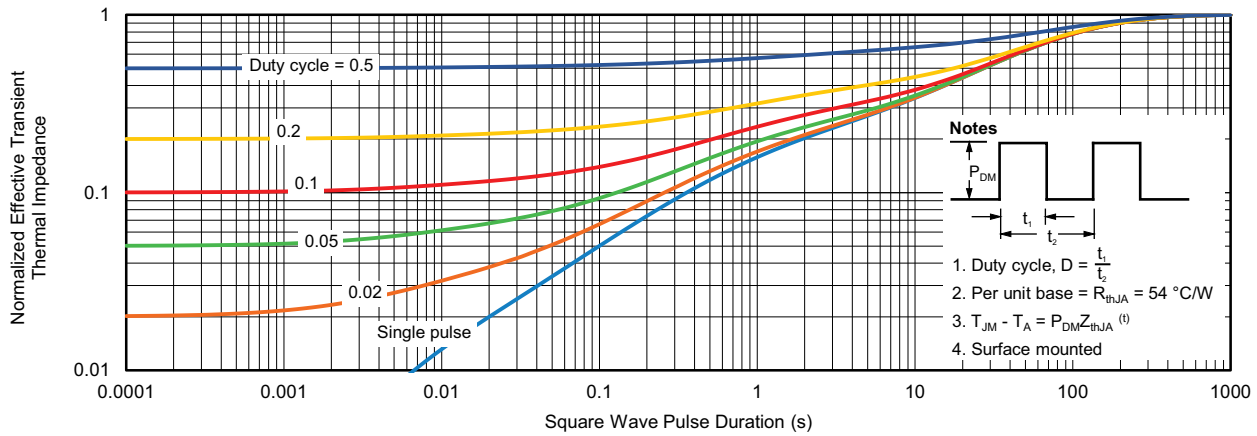
Power, Junction-to-Ambient

Notes

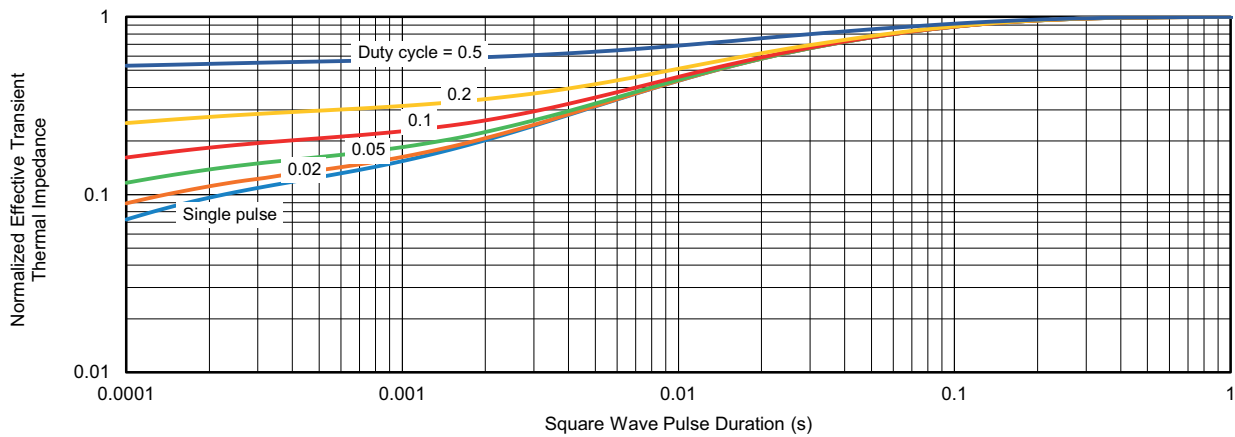
- a. The power dissipation P_D is based on T_J max. = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.
- b. $V_{GS} >$ minimum V_{GS} at which $R_{DS(on)}$ is specified



TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

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