MP3435

19A, 600kHz, 22V Output Range, Synchronous Boost Converter with Input Disconnect Function

DESCRIPTION

The MP3435 is a 600kHz, fixed frequency, high-efficiency, highly integrated boost converter that operates across a wide input voltage (V_{IN}) range, with optional input disconnect and an input average current limit function. The input disconnect feature provides additional protection by isolating the input from the output during an output short or shutdown. For battery-operated applications, this feature also helps prevent battery depletion. With a configurable input average current limit, the MP3435 supports a wide range of applications.

The MP3435 features a 10mΩ low-side MOSFET (LS-FET) and a 15mΩ synchronous high-side MOSFET (HS-FET) for high efficiency and low BOM cost. An external compensation pin allows flexibility in setting loop dynamics and obtaining optimal transient performance under all conditions.

The MP3435 includes under-voltage lockout (UVLO), switching current limiting, and thermal shutdown to prevent damage in the event of an output overload.

The MP3435 is available in a low-profile QFN-20 (3mmx4mm) package.

FEATURES

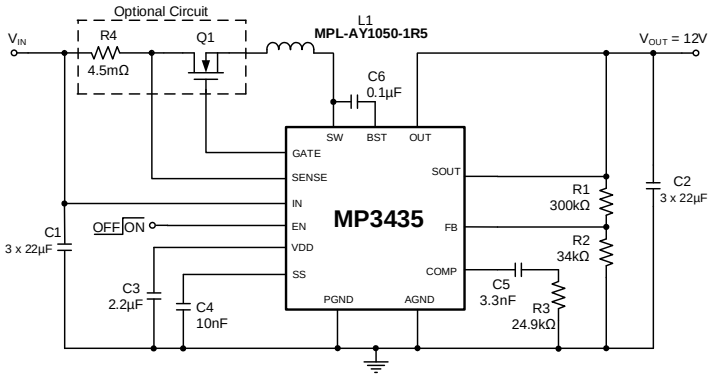
- 3V to 20V Wide Input Voltage (V_{IN}) Range
- Up to 22V Output Voltage (V_{OUT})
- Integrated 10mΩ and 15mΩ MOSFET
- 19A Internal Switch Current Limit or External Configurable Input Current Limit
- Input Disconnect and Output Short-Circuit Protection (SCP)
- Configurable Under-Voltage Lockout (UVLO) and Hysteresis
- <1μA Shutdown Current
- Thermal Shutdown at 150°C
- Available in QFN-20 (3mmx4mm) Package

MPL Optimized Performance with MPS Inductor MPL-AY1050 Series

APPLICATIONS

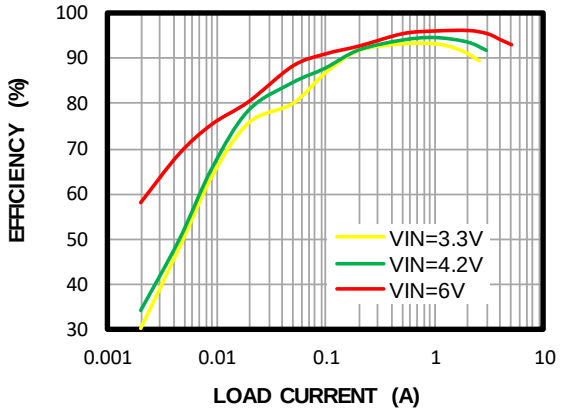
- Thunderbolt Interfaces
- Notebooks and Tablets
- Bluetooth Audio
- Power Banks
- Fuel Cells
- Point-of-Sale (POS) Systems

TYPICAL APPLICATION



Efficiency vs. Load Current

V_{OUT} = 12V, without input MOSFET, GATE = GND



ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MP3435GL	QFN-20 (3mmx4mm)	*See Below*	1

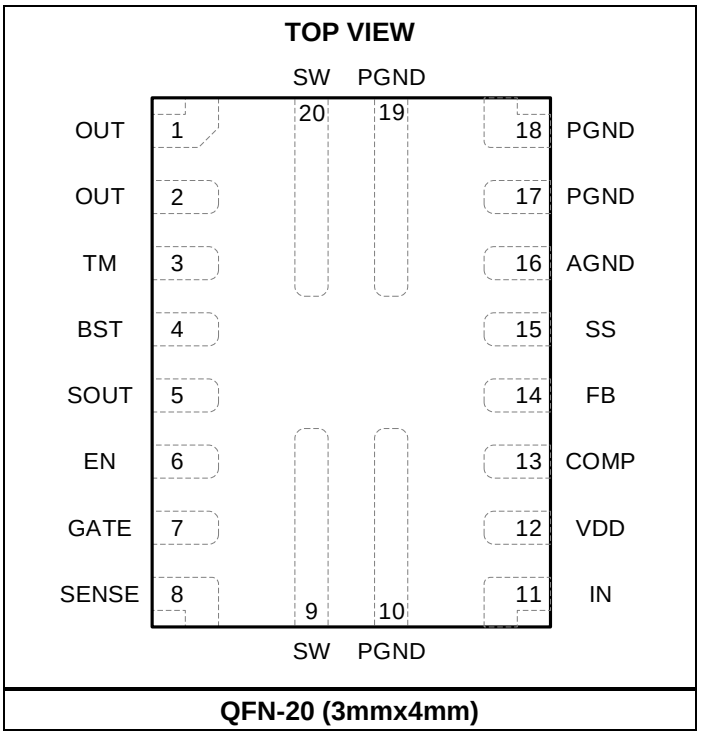
* For Tape & Reel, add suffix -Z (e.g. MP3435GL-Z).

TOP MARKING

MPYW
3435
LLL

MP: MPS prefix
Y: Year code
W: Week code
3435: Part number
LLL: Lot number

PACKAGE REFERENCE



QFN-20 (3mmx4mm)

PIN FUNCTIONS

Pin #	Name	Description
1, 2	OUT	**Power output.** Connect OUT to the high-side MOSFET (HS-FET)'s drain.
3	TM	**Internal test pin.** Only use in product test mode. Float TM in application.
4	BST	**Bootstrap.** BST powers the HS-FET driver.
5	SOUT	**Samples the output voltage and charges the BST capacitor**. VDD is powered from SOUT when V_{SOUT} exceeds V_{IN}.
6	EN	**Regulator on/off control input**. Pull this pin high to turn on the internal regulator circuit; pull it low to turn off the regulator circuit. An input above the EN turn-on threshold enables the IC to start switching. When the EN pin is not used, connect EN to the input source (through a 100kΩ pull-up resistor if V_{IN} > 5.5V) for automatic start-up. This pin can also configure V_{IN} UVLO. Do not leave EN floating.
7	GATE	**Driver for the input disconnect MOSFET.** If this pin is floating or connected to the input MOSFET gate, an external current-sense resistor is required. Connect GATE to ground to use the internal current-sense circuit. Do not pull GATE down to ground through a resistor.
8	SENSE	**Voltage sense.** The voltage sensed between SENSE and IN determines the external current-sense signal. Connect SENSE to IN if the internal current-sense function is selected.
9, 20	SW	**Power switch.** Connect SW to the internal low-side MOSFET (LS-FET)'s drain and the internal, synchronous HS-FET source. Connect the power inductor to SW.
10, 17, 18, 19	PGND	**Power ground.**
11	IN	**Input supply.** IN must be locally bypassed.
12	VDD	**Internal bias supply.** Decouple the VDD pin with a 2.2µF ceramic capacitor, placed as close to VDD as possible.
13	COMP	**Compensation.** Connect a capacitor and resistor in series to the analog ground for loop stability.
14	FB	**Feedback input.** The reference voltage (V_{REF}) is 1.225V. Connect a resistor divider from output to FB.
15	SS	**Soft-start control.** Connect a soft-start capacitor (C_{SS}) to SS. C_{SS} is charged with a constant current. Leave SS disconnected if soft start is not used.
16	AGND	**Analog ground.**

ABSOLUTE MAXIMUM RATINGS (1)

SW.....-0.3V (-3.5V for <10ns) to
……+24V (28V for <10ns)
IN, SENSE, OUT, SOUT..... -0.3V to +24V
GATE.....-0.3V to IN +5.5V
BST, TM ..... -0.3V to V_{SW} +5.5V
All other pins..... -0.3V to +5.5V
EN sinking current 0.5mA (2)
Continuous power dissipation (T_A = 25°C) (3)
.....4.6W (5)
Junction temperature .....150°C
Lead temperature .....260°C
Storage temperature.....-65°C to +150°C

ESD Ratings

Human body model (HBM) 2000V
Charged device model (CDM).....1500V

Recommended Operating Conditions (4)

Supply voltage (V_{IN}) ..... 3V to 20V
Output voltage (V_{OUT})..... V_{IN} to 22V
EN sinking curent.....0mA to 0.3mA (2)
Operating junction temp (T_J) .... -40°C to +125°C

Thermal Resistance θ_{JA} θ_{JC}

QFN-20 (3mmx4mm)			
EVL3435-L-00A (5)	27	4	°C/W
JESD51-7 (6)	48	11	°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) Refer to the Enable (EN) and Configurable UVLO section on page 17.
3) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX) - T_A) / θ_{JA}. Exceeding the maximum allowable power dissipation can generate an excessive die temperature, which may cause the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
4) The device is not guaranteed to function outside of its operating conditions.
5) Measured on the EVL3435-L-00A, a 4-layer, 2oz PCB (63mmx63mm).
6) The value of θ_{JA} given in this table is only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD51-7, and simulated on a specified JEDEC board. They do not represent the performance obtained in an actual application.

ELECTRICAL CHARACTERISTICS

V_{IN} = V_{EN} = 3.3V, T_J = -40°C to +125°C [7], typical values are tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Operating input voltage	V_{IN}		3		20	V
Input under-voltage lockout (UVLO)	IN_{UVLO-R}	V_{IN} rising	2.6	2.68	2.76	V
Input UVLO hysteresis	$IN_{UVLO-HYS}$			250		mV
Operating VDD voltage	V_{DD}	V_{IN} = 12V		5		V
Shutdown current	I_{SD}	V_{EN} = 0V, measured on IN, T_J = 25°C			1	µA
Quiescent current	I_{Q-SOUT}	V_{FB} = 1.35V, no switching, V_{OUT} = 12V, measured on SOUT		650	750	µA
	I_{Q-IN}	V_{FB} = 1.35V, no switching, V_{OUT} = 12V, measured on IN		110	150	
Switching frequency	f_{SW}	T_J = 25°C	510	600	690	kHz
		T_J = -40°C to +125°C	450		690	
Minimum off time [8]	$t_{MIN-OFF}$	V_{FB} = 0V		190		ns
Minimum on time [8]	t_{MIN-ON}			200		ns
EN turn-on threshold	V_{EN-ON}	V_{EN} rising (switching)	1.26	1.33	1.39	V
EN high threshold	V_{EN-H}	V_{EN} rising (micro power)			1	V
EN low threshold	V_{EN-L}	V_{EN} falling (micro power)	0.4			V
EN turn-on hysteresis current	I_{EN-HYS}	1V < EN < 1.4V	3	4.5	6	µA
EN input bias current	I_{EN}	V_{EN} = 0V, 3.3V		0		µA
Soft-start (SS) charge current	I_{SS}		5	7	9	µA
FB reference voltage	V_{FB}	T_J = 25°C	1.212	1.225	1.238	V
		T_J = -40°C to +125°C	1.207	1.225	1.243	
FB input bias current	I_{FB}	V_{FB} = 1V	-50			nA
Error amplifier transconductance	G_{EA}			160		µA/V
Error amplifier max output current	$I_{EA(MAX)}$	V_{FB} = 1V or 1.5V		39		µA
Current to COMP gain	G_{CS}	V_{GATE} = GND		32		A/V
Sense to COMP gain	G_{XCS}	Float GATE, ΔV_{SENSE} / ΔV_{COMP}		103		mV/V
COMP switching threshold [8]	V_{PSM}			0.5		V
COMP high clamp	V_{COMP_HIGH}			2		V
Low-side (LS) switch on resistance	R_{ON-L}			10		mΩ

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = V_{EN} = 3.3V, T_J = -40°C to +125°C (7), typical values are tested at T_J = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
High-side (HS) switch on resistance	R_{ON-H}			15		mΩ
SW current limit	I_{LIMT}	V_{GATE} = GND, T_J = 25°C, duty cycle = 40%	19	25	29	A
External sense average current limit	V_{CL}	Float GATE	45	54	63	mV
Linear charge start-up short-circuit protection (SCP) blanking time	t_{CL}	Float GATE		0.5		ms
Thermal shutdown (8)	T_{SD}			150		°C
Thermal shutdown hysteresis (8)	T_{SD-HYS}			25		°C

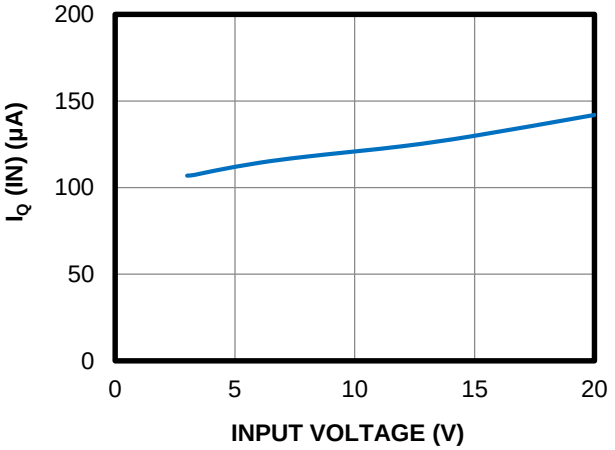
Notes:

7) Guaranteed by over-temperature correlation. Not tested in production.
8) Guaranteed by characterization. Not tested in production.

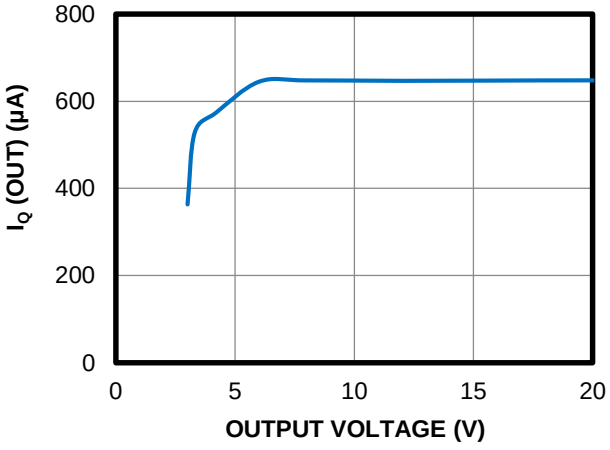
TYPICAL CHARACTERISTICS

V_{IN} = V_{EN} = 3.3V, V_{OUT} = 12V, L = 1.5µH, T_A = 25°C, unless otherwise noted.

I_Q (IN) vs. Input Voltage

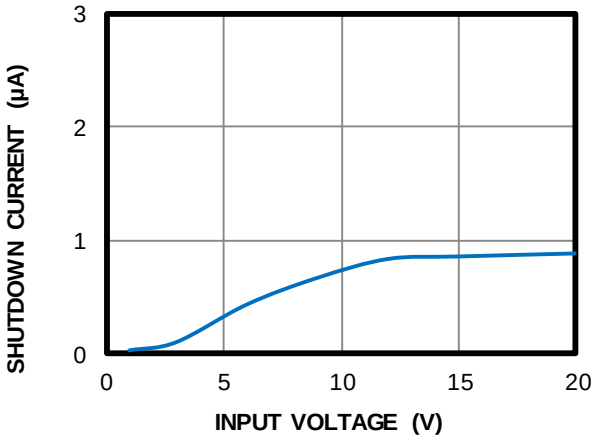


I_Q (OUT) vs. Output Voltage



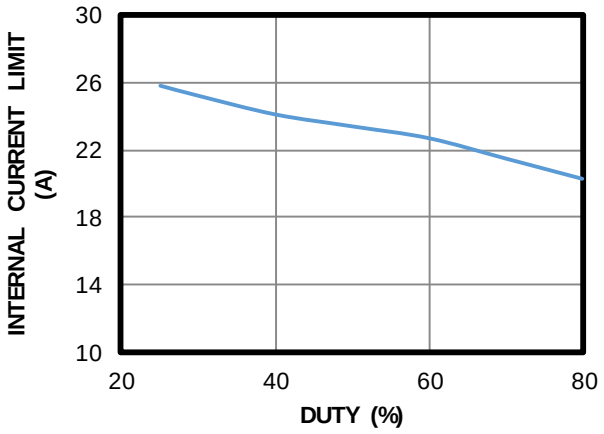
Shutdown Current vs. V_{IN}

EN = low

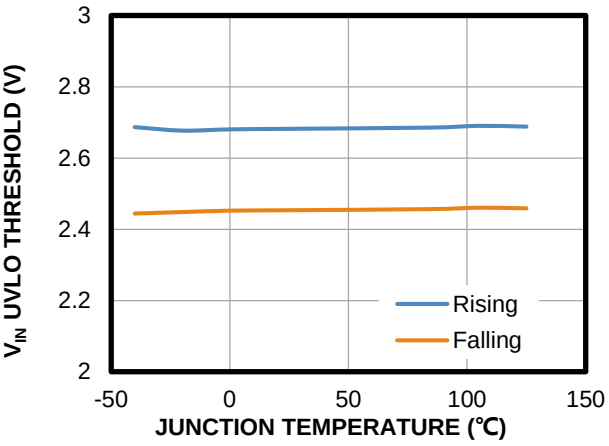


Internal Current Limit vs. Duty Cycle

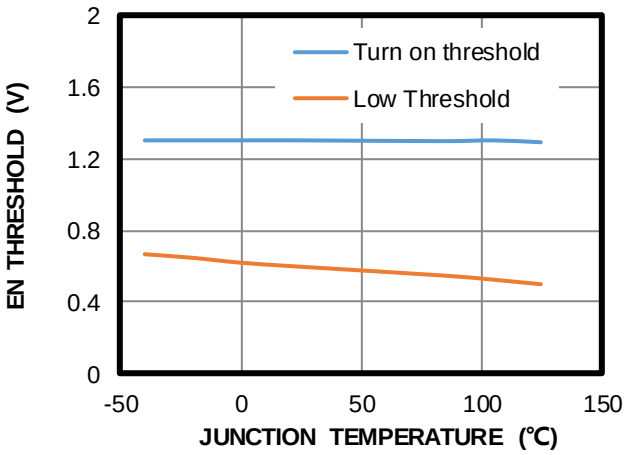
GATE = GND



V_{IN} UVLO Threshold vs. Temperature



EN Threshold vs. Temperature

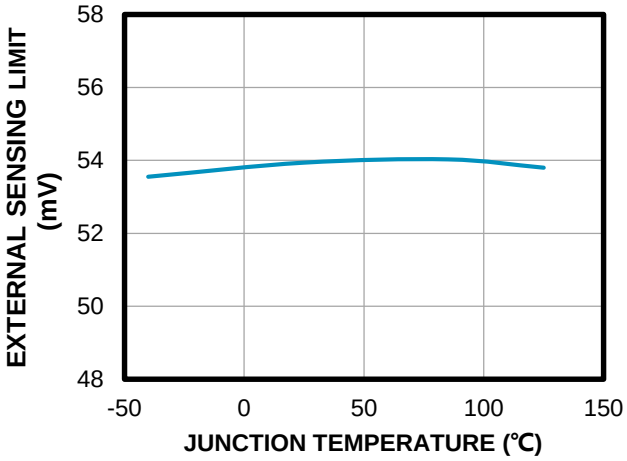


TYPICAL CHARACTERISTICS *(continued)*

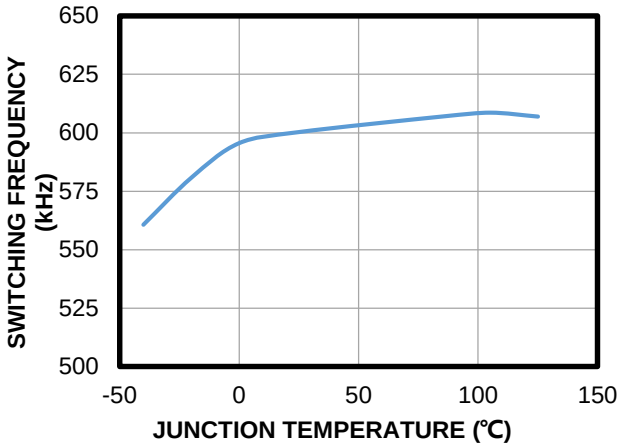
V_{IN} = V_{EN} = 3.3V, V_{OUT} = 12V, L = 1.5µH, T_A = 25°C, unless otherwise noted.

External Sense Average Current Limit vs. Temperature

GATE = Float

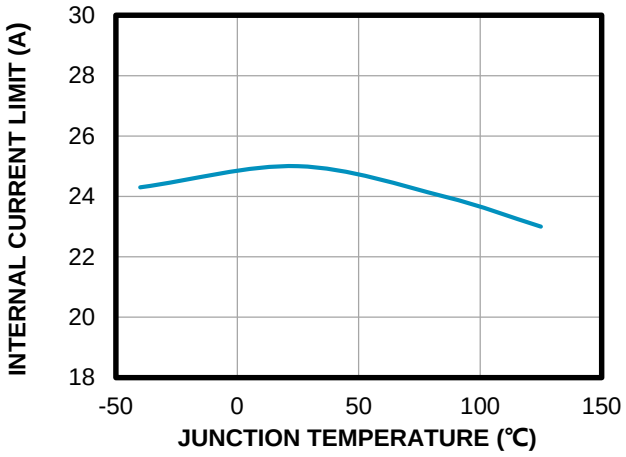


Switching Frequency vs. Temperature



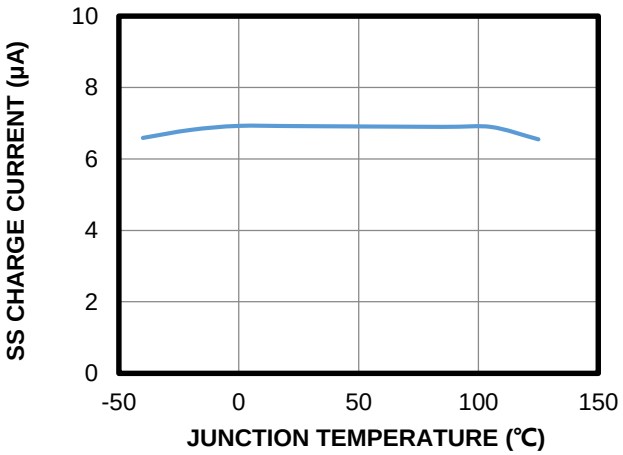
Internal Current Limit vs. Temperature

GATE = GND, duty = 40%



SS Charge Current vs. Temperature

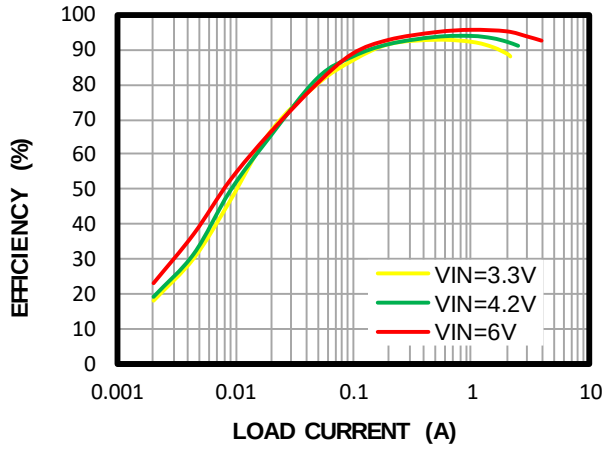
V_{SS} = 0V



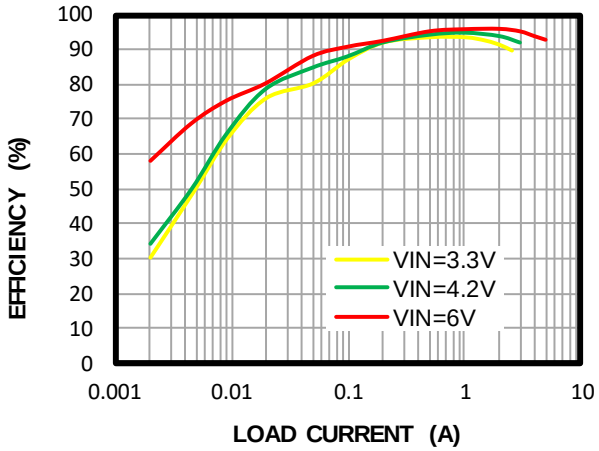
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 3.3V, V_{OUT} = 12V, L = 1.5µH, I_{OUT} = 2A, C_{OUT} = 3 x 22µF, R_{SENSE} = 4.5mΩ, add an input disconnect MOSFET, T_A = 25°C, unless otherwise noted.

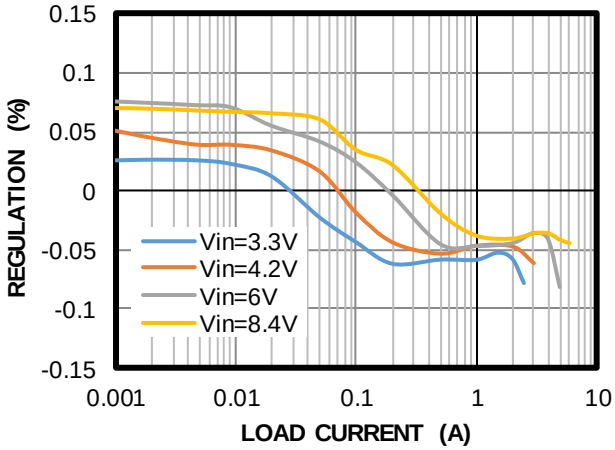
Efficiency vs. Load Current
With an input MOSFET



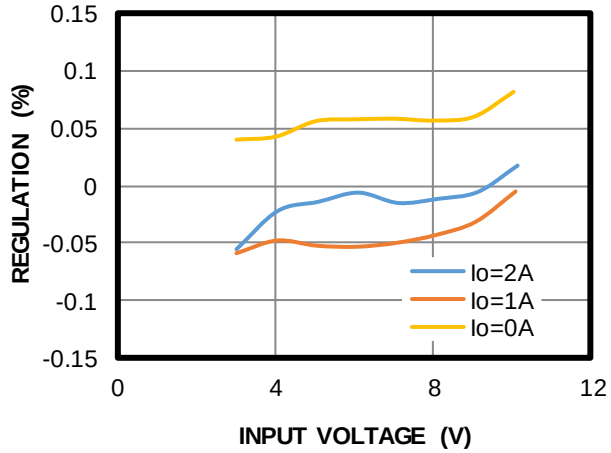
Efficiency vs. Load Current
Without an input MOSFET, GATE = GND



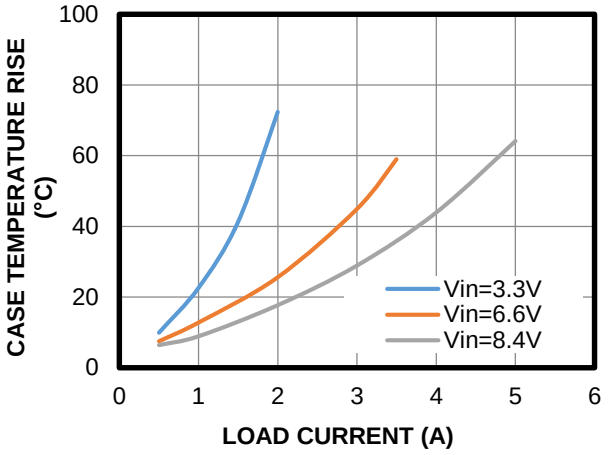
Load Regulation



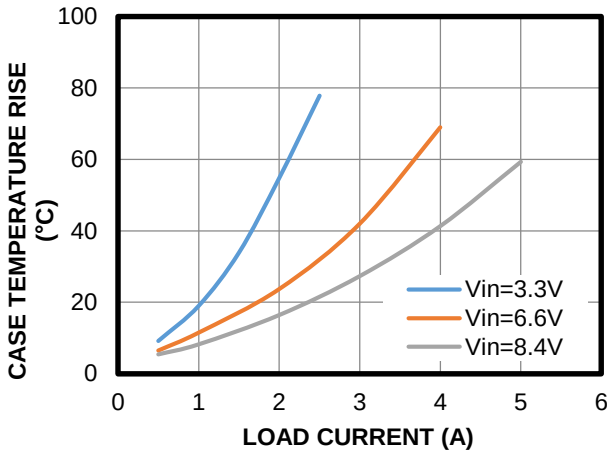
Line Regulation



Case Temperature Rise
With input MOSFET



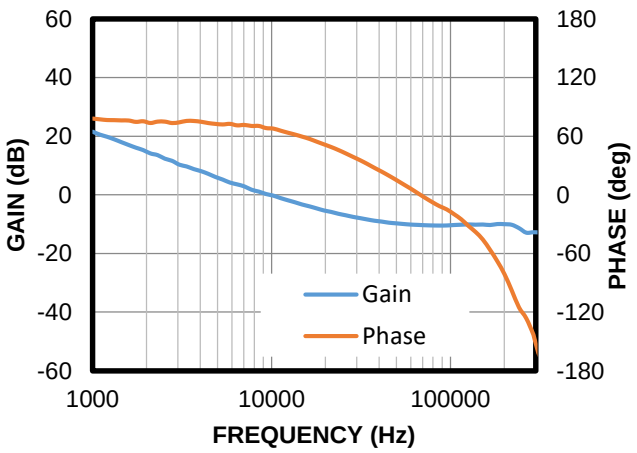
Case Temperature Rise
Without input MOSFET, GATE = GND



TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 3.3V, V_{OUT} = 12V, L = 1.5µH, I_{OUT} = 2A, C_{OUT} = 3 x 22µF, R_{SENSE} = 4.5mΩ, add an input disconnect MOSFET, T_A = 25°C, unless otherwise noted.

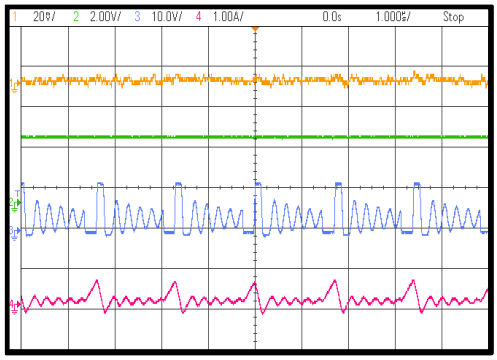
Bode Plot



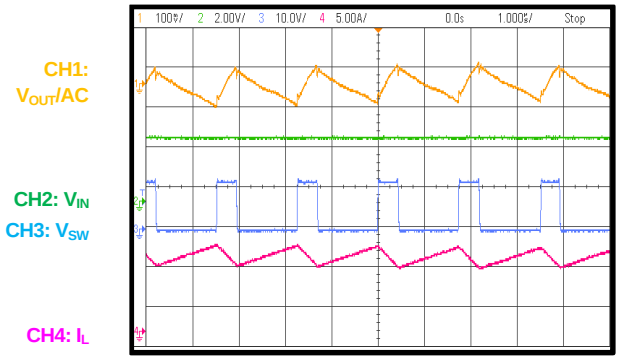
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 3.3V, V_{OUT} = 12V, L = 1.5µH, I_{OUT} = 2A, C_{OUT} = 3 x 22µF, R_{SENSE} = 4.5mΩ, add an input disconnect MOSFET, T_A = 25°C, unless otherwise noted.

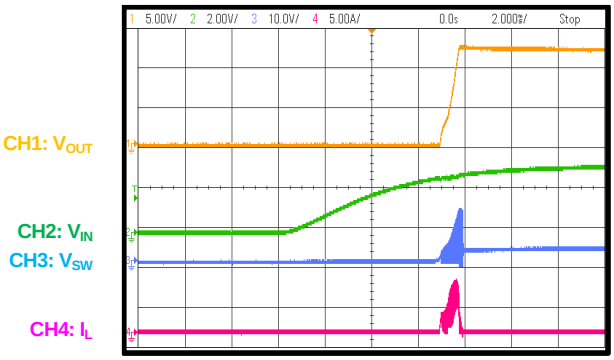
Steady State
I_{OUT} = 0A



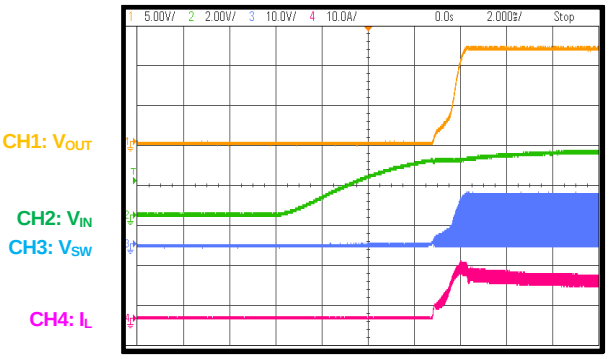
Steady State
I_{OUT} = 2A



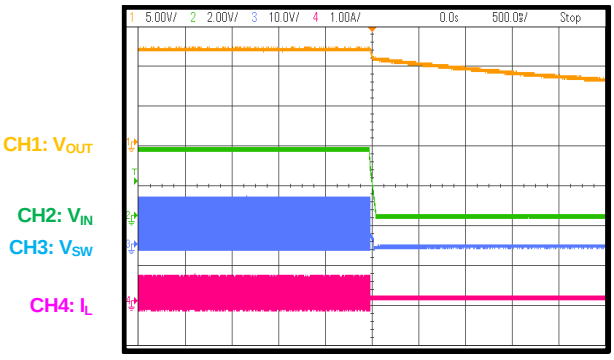
Start-Up through IN
I_{OUT} = 0A



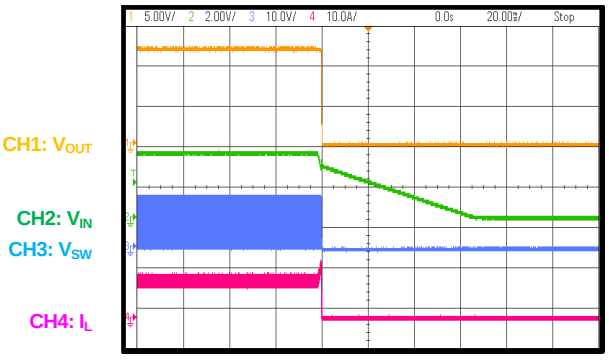
Start-Up through IN
I_{OUT} = 2A



Shutdown through IN
I_{OUT} = 0A



Shutdown through IN
I_{OUT} = 2A

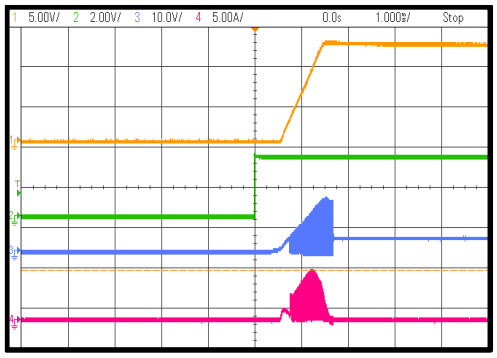


TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 3.3V, V_{OUT} = 12V, L = 1.5µH, I_{OUT} = 2A, C_{OUT} = 3 x 22µF, R_{SENSE} = 4.5mΩ, add an input disconnect MOSFET, T_A = 25°C, unless otherwise noted.

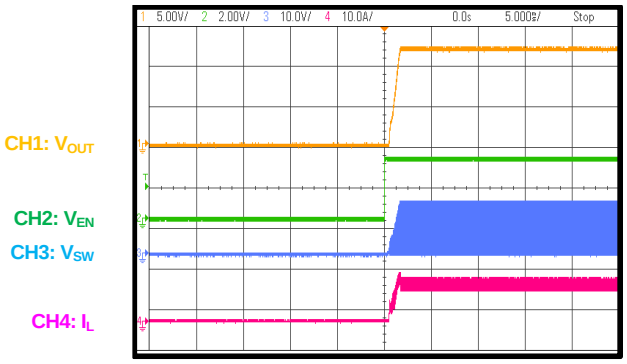
Start-Up through EN

I_{OUT} = 0A



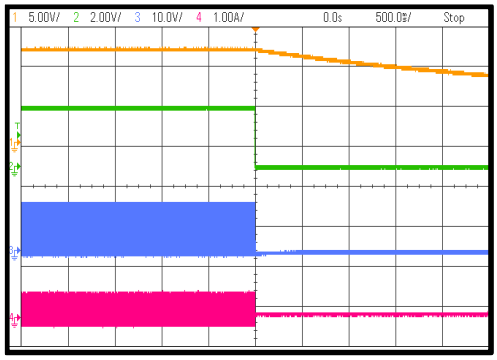
Start-Up through EN

I_{OUT} = 2A



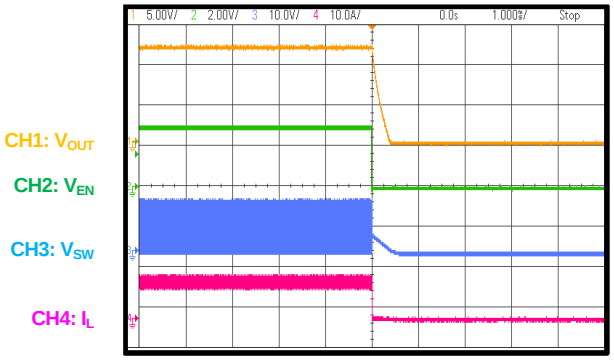
Shutdown through EN

I_{OUT} = 0A



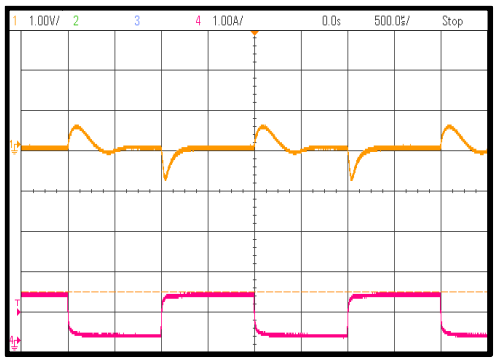
Shutdown through EN

I_{OUT} = 2A



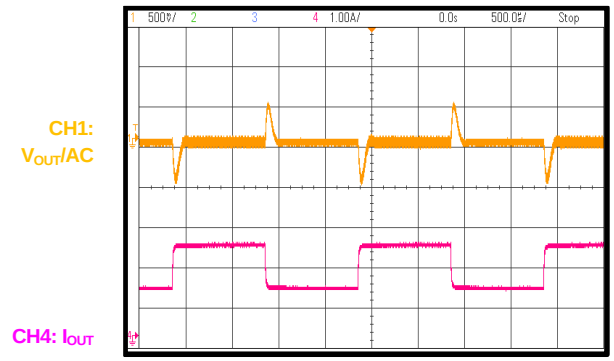
Load Transient

I_{OUT} = 0A to 1A, I_{RAMP} = 25mA/µs



Load Transient

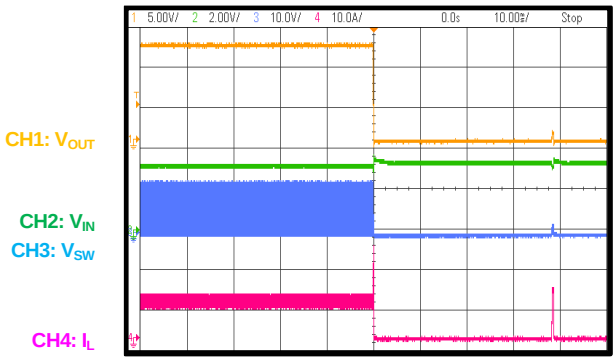
I_{OUT} = 1A to 2A, I_{RAMP} = 25mA/µs



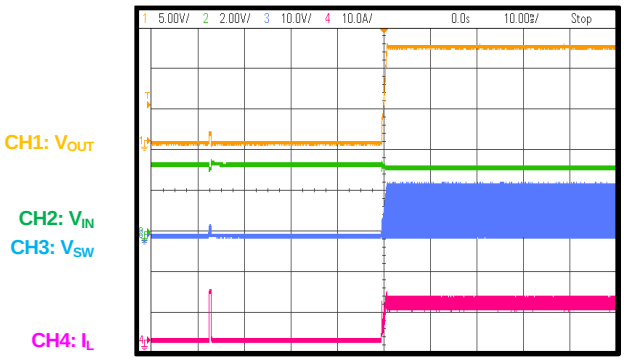
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 3.3V, V_{OUT} = 12V, L = 1.5µH, I_{OUT} = 2A, C_{OUT} = 3 x 22µF, R_{SENSE} = 4.5mΩ, add an input disconnect MOSFET, T_A = 25°C, unless otherwise noted.

SCP Entry



SCP Recovery



FUNCTIONAL BLOCK DIAGRAM

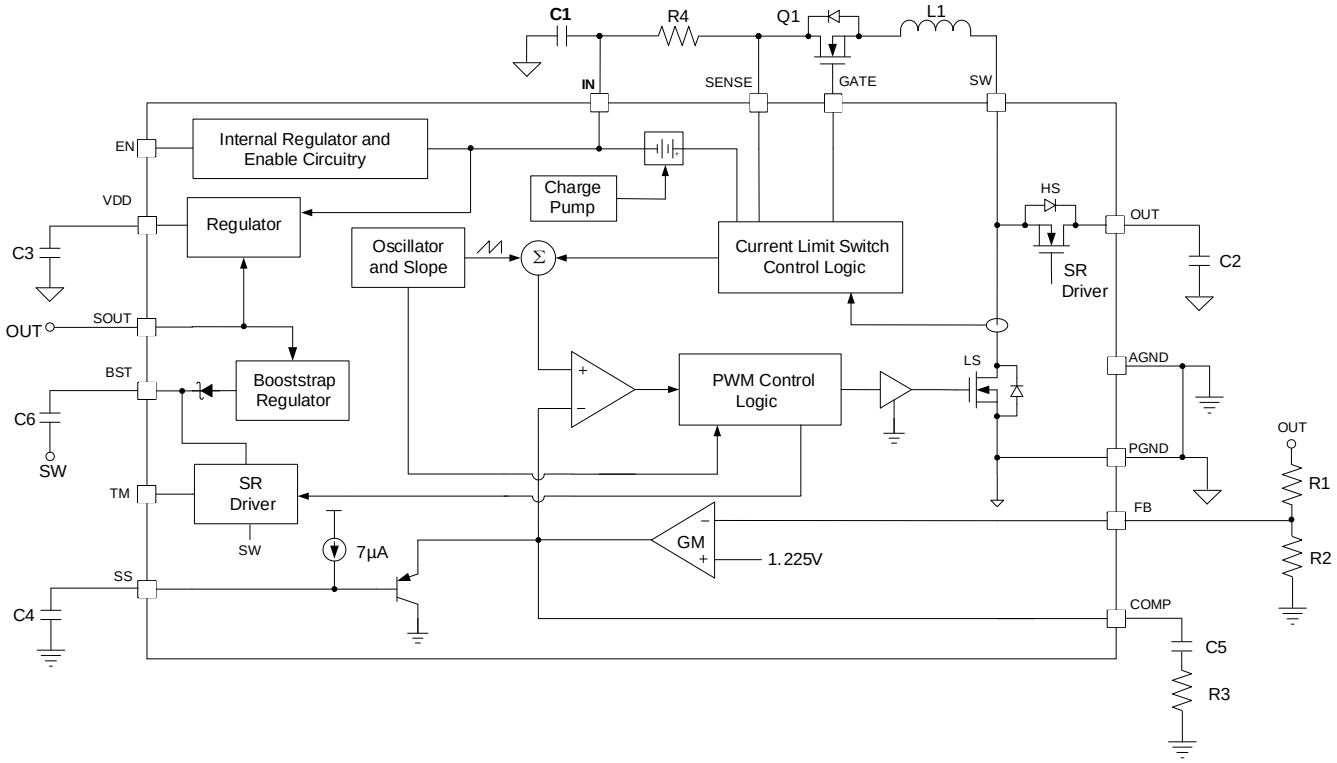


Figure 1: Functional Block Diagram

OPERATION

Boost Function

The MP3435 uses a constant frequency, peak current mode, boost regulation architecture to regulate the output voltage (V_{OUT}).

At the beginning of each cycle, the low-side MOSFET (LS-FET) turns on, forcing the inductor current (I_L) to rise. The current flowing through the LS-FET is externally measured (or internally measured when GATE is connected to GND) and converted to a voltage by the current amplifier. This voltage is compared with the internal transconductance error amplifier (COMP) error voltage, which is a buffer voltage from the external COMP pin during normal operation. The external COMP voltage (V_{COMP}) is an amplified version of the difference between the 1.225V reference voltage (V_{REF}) and the feedback (FB) voltage. When the sensed voltage is equal to V_{COMP}, the pulse-width modulation (PWM) comparator turns off the LS-FET. The stored inductor current charges the output capacitor (C_{OUT}) through the internal high-side MOSFET (HS-FET), and I_L drops. The peak inductor current ($I_{L(MAX)}$) is controlled by the voltage, which in turn is controlled by V_{OUT}. Thus, V_{OUT} is regulated by I_L to satisfy the load. Current mode regulation improves the transient response and control loop stability.

VDD Power

The MP3435 internal circuit is powered by VDD. A ceramic capacitor (minimum 2.2μF) is required to decouple VDD. During start-up, VDD power is regulated by IN. Once V_{OUT} exceeds the input voltage (V_{IN}), VDD is powered from V_{OUT} instead of V_{IN}. This allows the MP3435 to maintain a low MOSFET on resistance (R_{ON}) and high efficiency even with a low V_{IN}.

Soft Start (SS)

The MP3435 uses one external soft start (SS) capacitor to control the switching frequency (f_{SW}) during start-up. The operation frequency is initially 1/4 of the normal frequency. As the soft-start capacitor (C_{SS}) charges (which occurs after the MP3435 runs in boost operation), the frequency continually increases. When the SS voltage (V_{SS}) exceeds 0.65V, the frequency switches to a normal frequency. In addition, V_{COMP} is clamped within V_{SS} + 0.7V. This means that during start-up, V_{COMP} quickly reaches 0.7V, then rises at the same rate as V_{SS}. These two mechanisms prevent a high inrush current from the input power supply.

Bootstrap (BST) Function

The HS-FET driver is powered from BST, and the BST voltage (V_{BST}) is powered from SOUT. If V_{OUT} or the duty cycle is too low, V_{BST} may not be regulated to 5V, triggering BST under-voltage lockout (UVLO). It is recommended to connect a Schottky diode from an external, 5V source to BST. Otherwise, the HS-FET driver signal may be lost.

Current-Sense Configuration

The MP3435 offers the option of using an internal circuit or an external resistor to sense I_L. When using an internal current-sense circuit, GATE must be directly connected to ground before start-up, and SENSE should be connected to IN. Under this condition, the internally sensed current is compared to both V_{COMP} and the peak inductor current limit to generate the duty cycle.

When GATE is connected to the input MOSFET gate or is left floating before start-up, I_L is sensed by an external resistor between IN and SENSE. Under this configuration, the externally sensed current is compared with COMP for LS-FET on/off control. The overload protection (OLP) or disconnect function is achieved by monitoring the average input current through the external sensing resistor (see the Protection and Input Disconnect Function section below for additional details).

Protection and Input Disconnect Function

The MP3435 features excellent over-current protection (OCP) and short-circuit protection (SCP).

During start-up, the MP3435 monitors the GATE voltage (V_{GATE}) to determine if there is in internal or external current sense. Connect GATE to an external MOSFET gate or leave it floating to select an external sensing resistor; directly connect GATE to ground to select an internal current-sense circuit.

If internal current sensing is selected, OCP is achieved by limiting $I_{L(MAX)}$ in every switching cycle (without hiccup mode), unless V_{OUT} is pulled below V_{IN}. After V_{SS} exceeds about 0.7V, the MP3435 can work in hiccup mode if it detects that V_{OUT} is below V_{IN}. This prevents the MP3435 from damage, even if there is no input disconnect MOSFET under a heavy-load condition.

If external current sensing is selected, GATE is charged by a typical 13µA current from the internal charge pump. Once V_{GATE} reaches the MOSFET threshold (V_{TH}), the input current (I_{IN}) is generated, and the output capacitors are charged. V_{OUT} follows V_{GATE} with a V_{TH} difference. The MP3435 has a current feedback loop to control V_{GATE} and V_{COMP}, so I_{IN} does not exceed V_{CL} (mV) / R_{SENSE} (mΩ).

During start-up with external current sensing (if V_{GATE} is below V_{IN} + 1.6V), the linear charge current limit works with the V_{CL} / R_{SENSE} limitation, and V_{GATE} is regulated to limit the current. The MP3435 shuts down if the linear charge current limit is triggered for over 0.5ms by pulling GATE down to ground. The MP3435 waits for 20ms to 70ms (the hiccup time depends on V_{IN} and V_{OUT}) to restart if it is not reset by V_{IN} or EN. A normal load does not lead to hiccup protection during start-up.

If V_{GATE} exceeds V_{IN} + 1.6V, boost switching is enabled. SS is charged, and the power MOSFET periodically turns on and off to regulate V_{OUT} following the SS signal. When the MP3435 starts switching and V_{OUT} is below V_{IN}, both the linear charge current limit (regulated by V_{GATE}) and the boost input average current limit (regulated by V_{COMP}) begin to work. Both control loops work with the V_{CL} / R_{SENSE} limit.

After V_{OUT} is charged above V_{IN} in boost mode, only the boost input average current limit works (regulated by V_{COMP}). The MP3435 does not trigger hiccup OCP unless V_{SS} exceeds 0.7V, and V_{OUT} drops below V_{IN}. If hiccup protection is triggered in switching mode, the switching stops, and GATE is pulled low. It will restart after 20ms to 70ms, depending on V_{IN} and V_{OUT}. The recovery process is the same as the start-up process.

Table 1 shows the detailed OCP mode when using an external current-sense resistor.

Table 1: OCP Modes with an External Current-Sense Resistor

Condition	Work Mode	OCP Action
$V_{GATE} < V_{IN}$ + 1.6V	Linear charge mode, no boost switching	The linear charge current limit works when: 1. V_{GATE} is regulated down to keep I_{IN} at V_{CL} / R_{SENSE}. 2. If the linear charge OCP lasts 0.5ms, the MP3435 triggers hiccup protection. The boost input average current limit does not work.
$V_{GATE} \geq V_{IN}$ + 1.6V (9) $V_{OUT} \leq V_{IN}$ $V_{SS} \leq$ 0.7V	Boost switching	The linear charge current limit works when: 1. V_{GATE} is regulated down to keep I_{IN} at V_{CL} / R_{SENSE}. 2. If the linear charge OCP lasts 0.5ms, the MP3435 triggers hiccup protection. The boost input average current limit works when V_{COMP} is regulated to keep the input average current at V_{CL} / R_{SENSE}.
$V_{GATE} \geq V_{IN}$ + 1.6V (9) $V_{OUT} \leq V_{IN}$ $V_{SS} >$ 0.7V	Boost switching	Enters hiccup protection without a delay.
$V_{GATE} \geq V_{IN}$ + 1.6V (9) $V_{OUT} > V_{IN}$	Boost switching	The linear charge current limit does not work, while V_{GATE} remains high. The boost input average current limit works when V_{COMP} is regulated to keep the input average current at V_{CL} / R_{SENSE}. There is no hiccup mode.

Note:

9) After start-up, the $V_{GATE} \geq V_{IN}$ + 1.6V condition is registered if V_{GATE} exceeds V_{IN} + 1.6V one time. This means the MP3435 treats the condition as $V_{GATE} \geq V_{IN}$ + 1.6V, even if V_{GATE} falls below V_{IN} + 1.6V again in protection mode (unless the device turns off due to hiccup mode or if the power is cycled.

If I_L quickly ramps and $I_{L(MAX)}$ exceeds 100(mV) / R_{SENSE} (mΩ), the MP3435 immediately shuts down, entering SCP hiccup mode. This fast protection allows the MP3435 to survive all SCP events.

When the MP3435 is shut down by EN or V_{IN}, GATE is pulled down to GND, so input and output are well isolated by the input MOSFET. This is the V_{IN} to V_{OUT} disconnect function.

Light-Load Operation

To optimize efficiency at light loads, the MP3435 employs frequency foldback and pulse-skipping mechanisms. When the load becomes lighter, V_{COMP} decreases, causing the MP3435 to enter fold-back operation (the lighter the load, the lower the frequency). However, if the load becomes exceedingly low, the MP3435 enters pulse-skip mode (PSM). PSM operation is optimized so that only one switching pulse is launched in every burst cycle.

Enable (EN) and Configurable UVLO

EN enables and disables the MP3435. When a voltage exceeding V_{EN_H} (about 1V) is applied, the MP3435 starts up some of the internal circuits (micro-power mode). If the EN voltage continues to rise above V_{EN_ON} (about 1.33V), the MP3435 enables all functions and begins boost operation. Boost operation is disabled if the EN voltage is below V_{EN_ON}. To shut down the MP3435 completely, a voltage below V_{EN_L} (about 0.4V) is required on EN. After shutdown, the MP3435 sinks a current below 1μA from the input power.

The maximum recommended voltage on EN is 5.5V. If the EN control signal comes from a voltage above 5.5V, a resistor should be added between EN and the control source. An internal Zener diode on EN clamps the EN voltage to prevent runaway.

Ensure the Zener-clamped current flowing into EN is below 0.3mA. EN configures the V_{IN} UVLO threshold (see the Under-Voltage Lockout (UVLO) Hysteresis section on page 18 for additional details).

Output Over-Voltage Protection (OVP)

Except for controlling the COMP signal to regulate V_{OUT}, the MP3435 also provides OVP. If the FB voltage exceeds 108% of V_{REF}, boost switching stops. When the FB voltage drops below 104% of V_{REF}, the device resumes switching automatically.

Thermal Shutdown

The device has an internal temperature monitor. If the die temperature exceeds 150°C, the converter shuts down. Once the temperature drops below 125°C, the converter turns on again.

APPLICATION INFORMATION

Selecting the Current Limit Resistor

The MP3435 features an average current limit when the external sensing resistor is used. R_{SENSE} is the resistor connected between IN and SENSE, and it sets the current limit (I_{CL}). I_{CL} can be calculated using Equation (1):

$$I_{CL} = V_{CL} / R_{SENSE} \quad (1)$$

Where V_{CL} is typically 54mV, I_{CL} is in A, and R_{SENSE} is in mΩ.

Considering the parasitic inductance on the sense resistor, a small package resistor (e.g., 0805 package) is recommended. Add several parallel resistors if the power rating is lower than requested. To reduce parasitic resistance and noise, a minimum 4mΩ current-sense resistor is recommended.

Under-Voltage Lockout (UVLO) Hysteresis

The MP3435 features a configurable UVLO hysteresis. During start-up, EN sinks a 4.5μA current from the upper resistor, R_{TOP} (see Figure 2).

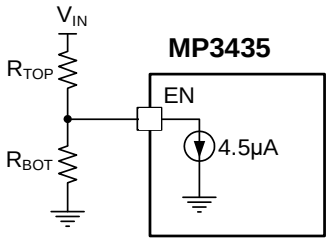


Figure 2: Configurable V_{IN} UVLO

V_{IN} must increase to overcome the current sink. The V_{IN} start-up threshold (V_{IN-ON}) can be estimated with Equation (2):

$$V_{IN-ON} = V_{EN-ON} \times (1 + \frac{R_{TOP}}{R_{BOT}}) + 4.5\mu A \times R_{TOP} \quad (2)$$

Where V_{EN-ON} is the EN turn-on threshold (typically 1.33V).

Once the EN voltage reaches V_{EN-ON}, the 4.5μA sink current turns off to create a reverse hysteresis for the V_{IN} falling threshold ($V_{IN-UVLO-HYS}$). $V_{IN-UVLO-HYS}$ can be calculated with Equation (3):

$$V_{IN-UVLO-HYS} = 4.5\mu A \times R_{TOP} \quad (3)$$

Selecting the Soft-Start Capacitor (C_{SS})

The MP3435 includes a SS circuit that limits V_{COMP} during start-up to prevent excessive I_{IN}. This prevents premature termination of the source voltage at start-up due to I_{IN} overshoot. When power is applied to the MP3435 and EN asserts, a 7μA internal current source charges the external C_{SS}. V_{SS} clamps V_{COMP} (as well as $I_{L(MAX)}$) until the output is close to regulation, or until V_{COMP} reaches 2V. For most applications, a 10nF C_{SS} is sufficient. If the output capacitance is large or the front power supply cannot withstand the huge inrush current, use a larger-value capacitor.

Setting the Output Voltage (V_{OUT})

V_{OUT} is fed back through two sense resistors placed in series. The FB reference voltage (V_{FB}) is typically 1.225V. V_{OUT} can be estimated with Equation (4):

$$V_{OUT} = V_{REF} \times (1 + \frac{R1}{R2}) \quad (4)$$

Where R1 is the top FB resistor, R2 is the bottom FB resistor, and V_{REF} is the reference voltage (typically 1.225V).

Choose the FB resistors in the 10kΩ range (or higher) for good efficiency.

Selecting the Input Capacitor

An input capacitor is required to supply the AC ripple current to the inductor while limiting noise at the input source. A low-ESR capacitor is required to minimize noise. Ceramic capacitors are recommended, but tantalum or low ESR electrolytic capacitors are sufficient.

For loop stability, at least two 22μF capacitors are recommended for high-power applications,. The capacitor can be electrolytic, tantalum, or ceramic. Since the capacitor absorbs the input switching current, it requires an adequate ripple current rating. Use a capacitor with an RMS current rating exceeding the inductor ripple current (see the Selecting the Inductor section on page 19 to determine the inductor ripple current).

To ensure stable operation, place the input capacitor as close to the IC as possible. Alternately, a smaller, high-quality, 0.1µF ceramic capacitor can be placed close to the IC, while a larger-value capacitor is placed further away. If using this technique, an electrolytic or tantalum capacitor is recommended for the larger-value capacitor. All ceramic capacitors should be placed close to the MP3435's input.

Selecting the Output Capacitor

The output capacitor is required to maintain the DC V_{OUT}. Low-ESR capacitors are recommended to minimize the output voltage ripple (V_{RIPPLE}). The characteristics of the output capacitor affect regulation and control system stability. Ceramic, tantalum, or low-ESR electrolytic capacitors are recommended. If using ceramic capacitors, the impedance of the capacitor at f_{SW} is dominated by the capacitance, so V_{RIPPLE} is independent of the ESR. V_{RIPPLE} can be calculated with Equation (5):

$$V_{RIPPLE} = \frac{(1-\frac{V_{IN}}{V_{OUT}})\times I_{LOAD}}{C_{OUT}\times f_{SW}} \quad (5)$$

Where V_{IN} and V_{OUT} are the DC input and output voltages, respectively, I_{LOAD} is the load current, f_{SW} is the fixed 600kHz switching frequency, and C_{OUT} is the output capacitor's capacitance.

If using tantalum or low-ESR electrolytic capacitors, the ESR dominates the impedance at f_{SW}, so V_{RIPPLE} can be estimated using Equation (6):

$$V_{RIPPLE} = \frac{(1-\frac{V_{IN}}{V_{OUT}})\times I_{LOAD}}{C_{OUT}\times f_{SW}} + \frac{I_{LOAD}\times R_{ESR}\times V_{OUT}}{V_{IN}} \quad (6)$$

Where R_{ESR} is the equivalent series resistance of the output capacitors.

Choose an output capacitor to satisfy the V_{RIPPLE} and load transient design requirements. Capacitance de-rating should be taken into consideration when designing high V_{OUT} applications. Three 22µF ceramic capacitors are suitable for most applications.

Selecting the Inductor

MPL **Optimized Performance with MPS Inductor MPL-AY1050 Series**

The inductor is required to force a higher V_{OUT} while being driven by V_{IN}. A larger-value inductor has less ripple current, resulting in a lower $I_{L(MAX)}$. This reduces stress on the internal N-channel switch and enhances efficiency. However, a larger-value inductor has a larger physical size, a higher series resistance, and a lower saturation current.

A good rule of thumb is to allow the peak-to-peak ripple current to be approximately 30% to 40% of the maximum input current ($I_{IN(MAX)}$). Make sure that $I_{L(MAX)}$ is below 75% of I_{CL} at the operating duty cycle to prevent regulation loss due to I_{CL}. Additionally, make sure that the inductor does not saturate under the worst-case load transient and start-up conditions. The required inductance value (L) can be estimated with Equation (7):

$$L = \frac{V_{IN}\times(V_{OUT}-V_{IN})}{V_{OUT}\times f_{SW}\times \Delta I} \quad (7)$$

$I_{IN(MAX)}$ can be calculated with Equation (8):

$$I_{IN(MAX)} = \frac{V_{OUT}\times I_{LOAD(MAX)}}{V_{IN}\times \eta} \quad (8)$$

Where $I_{LOAD(MAX)}$ is the maximum load current, ΔI is the peak-to-peak inductor ripple current, ΔI = (30% to 40%) x $I_{IN(MAX)}$, and η is the efficiency.

MPS inductors are optimized and tested for use with our complete line of integrated circuits.

Table 2 lists the MPS power inductor recommendations, where the part numbers can be selected based on the design requirements.

Table 2: Power Inductor Selection

Part Number	Inductor Value	Manufacturer
MPL-AY	0.47µH to 10µH	MPS
MPL-AY1050-1R5	1.5µH	MPS
MPL-AY1050-1R0	1µH	MPS
MPL-AY1050-2R2	2.2µH	MPS

For more information, visit the Inductors page on the MPS website.

BST Charger for Low Output Applications

In some low output applications (e.g. a 5V output), the voltage across C_{BST} may be insufficient. In this case, a Schottky diode should be connected from the output port to BST, conducting the current into C_{BST} when SW goes low (see Figure 3).

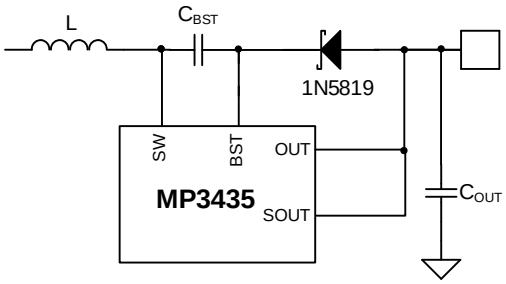


Figure 3: BST Charger for Low Output Applications

Selecting the Input MOSFET

The MP3435 integrates one GATE pin to drive an external N-channel MOSFET, which disconnects the input power or limits I_{IN}. The parameters to select the input disconnect MOSFET are described in greater detail below.

1. Drain-to-source voltage rating: This value should exceed V_{IN}.
2. Drain-to-source current rating: $I_{IN(MAX)}$ is the maximum current through the input disconnect MOSFET. This occurs when V_{IN} is at a minimum, and the load power is at a maximum.
3. Safe operating area (SOA): When conduction a current, the MOSFET should be able to support a current pulse that has a high level of V_{CL} (mV) / R_{SENSE} (mΩ) and lasts for C_{SS} (nF) x 0.7V / 7μA + 0.5ms.
4. Gate-to-source voltage rating: The positive gate-to-source voltage rating should exceed 5.5V, while the negative voltage rating should exceed V_{OUT}. If V_{OUT} is too high and the MOSFET gate-to-source rating cannot meet the requirement, placing a diode between the source and disconnecting MOSFET gate is recommended (see Figure 4).

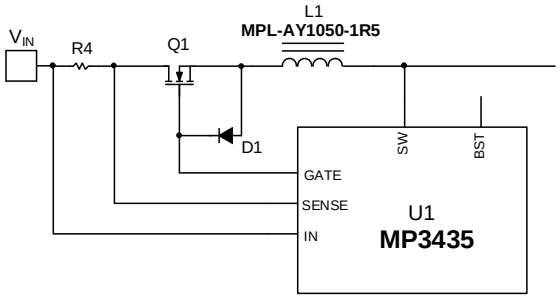


Figure 4: Gate Protection Diode for High Output Voltage Condition

5. Gate-to-source threshold voltage: The threshold should be below 1.5V. A 1V to 1.2V range across the overall temperature range is recommended.
6. On resistance (R_{DS_ON}): This value should be small for high conversion efficiency.
7. Low leakage current: This value should be low for better isolation.

In addition to the parameters listed above, consider the size and thermal temperature.

Compensation

The output of COMP compensates the regulation control system. The system uses two poles (F_{P1} and F_{P2}) and one zero to stabilize the control loop.

F_{P1} is set by the output capacitor (C_{OUT}) and the load resistance (R_{LOAD}), and F_{P2} starts from the origin. The zero (F_{Z1}) is set by the compensation capacitor (C_{COMP}) and the compensation resistor (R_{COMP}). F_{P1} and F_{Z1} can be calculated with Equation (9) and Equation (10), respectively:

$$F_{P1} = \frac{1}{2 \times \pi \times R_{LOAD} \times C_{OUT}} (Hz) \quad (9)$$

$$F_{Z1} = \frac{1}{2 \times \pi \times R_{COMP} \times C_{COMP}} (Hz) \quad (10)$$

The DC loop gain can be calculated using Equation (11):

$$A_{VDC} = \frac{A_{VEA} \times V_{IN} \times R_{LOAD} \times V_{FB} \times G_{CS} \times R_{COMP}}{2 \times V_{OUT}^2} (V/V) \quad (11)$$

Where G_{CS} is the compensation voltage to the I_L gain, A_{VEA} is the error amplifier voltage gain, and V_{FB} is the feedback regulation threshold.

There is also a right half-plane zero (F_{RHPZ}) that exists in continuous conduction mode (CCM), where I_L does not drop to zero in each cycle. F_{RHPZ} can be calculated using Equation (12):

$$F_{RHPZ} = \frac{R_{LOAD}}{2 \times \pi \times L} \times (\frac{V_{IN}}{V_{OUT}})^2 (Hz) \quad (12)$$

F_{RHPZ} increases the gain and reduces the phase simultaneously, resulting in a smaller phase and gain margin. The worst-case condition occurs when V_{IN} is at its minimum and the output power is at its maximum. See the Typical Application Circuits section on page 23 for compensation recommendations.

Design Example

Table 3 shows a design example following the application guidelines for the specifications below.

Table 3: Design Example

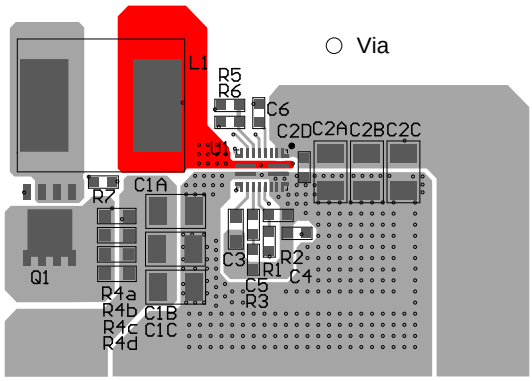
V_{IN}	V_{OUT}	I_{OUT}
3V to 10V	12V	0A to 2A

The maximum output current is determined by the allowable temperature rise, I_{CL}, and V_{IN}. Figure 6 and Figure 7 on page 23 show the detailed application schematics. The typical performance and circuit waveforms are shown in the Typical Performance Characteristics section on page 9. For more device applications, refer to the related evaluation board datasheet.

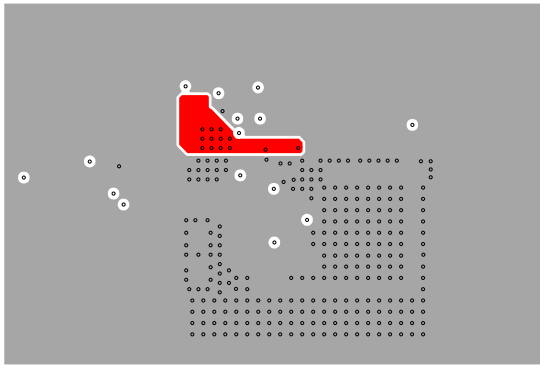
PCB Layout Guidelines

Efficient PCB layout is critical for high-frequency switching power supplies. A poor layout can result in reduced performance, excessive EMI, resistive loss, and system instability. Use a 4-layer PCB for high-power applications. For the best results, refer to Figure 5 and follow the guidelines below:

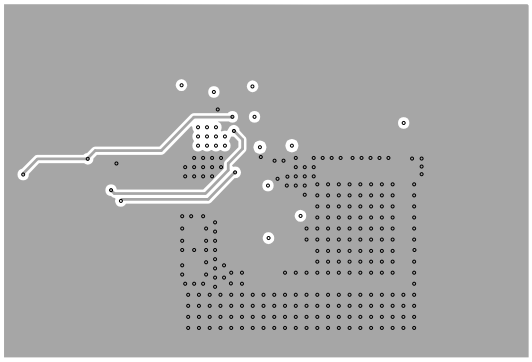
1. Keep the output loop (OUT, PGND, and C2) as small as possible.
2. Place a 0.1µF capacitor (C2D) close to the IC to reduce the PCB parasitical inductance.
3. Connect SW to Mid-Layer 1 through two vias on the right side of SW to enhance the current capability (shown as the red connections in the Top Layer and Mid-Layer 1 on Figure 5).
4. Place the FB dividers (R1 and R2) as close as possible to FB.
5. Route the sensing traces (SENSE and IN) closely in parallel with a small, closed area.
6. Use a 0805 package for the sensing resistor (R4) to reduce parasitic inductance.
7. Connect the VOUT feedback wire close to the output capacitor (C2C).
8. Connect the compensation components, C_{SS}, and VDD capacitor to AGND with a short loop.
9. Keep the input loop (C1, R4, Q1, L1, SW, and PGND) as small as possible.
10. Make the BST path as short as possible.
11. Float the TM pin in application.
12. Place enough GND vias close to the MP3435 for good thermal dissipation.
13. Place wide copper or vias associated with the input MOSFET's drain pin for thermal dissipation.



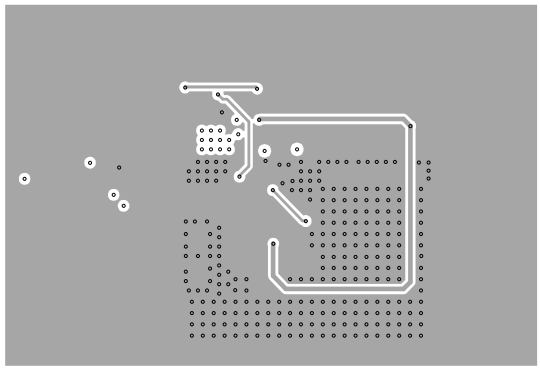
Top Layer



Mid-Layer 1



Mid-Layer 2



Bottom Layer

Figure 5: Recommended PCB Layout

TYPICAL APPLICATION CIRCUITS

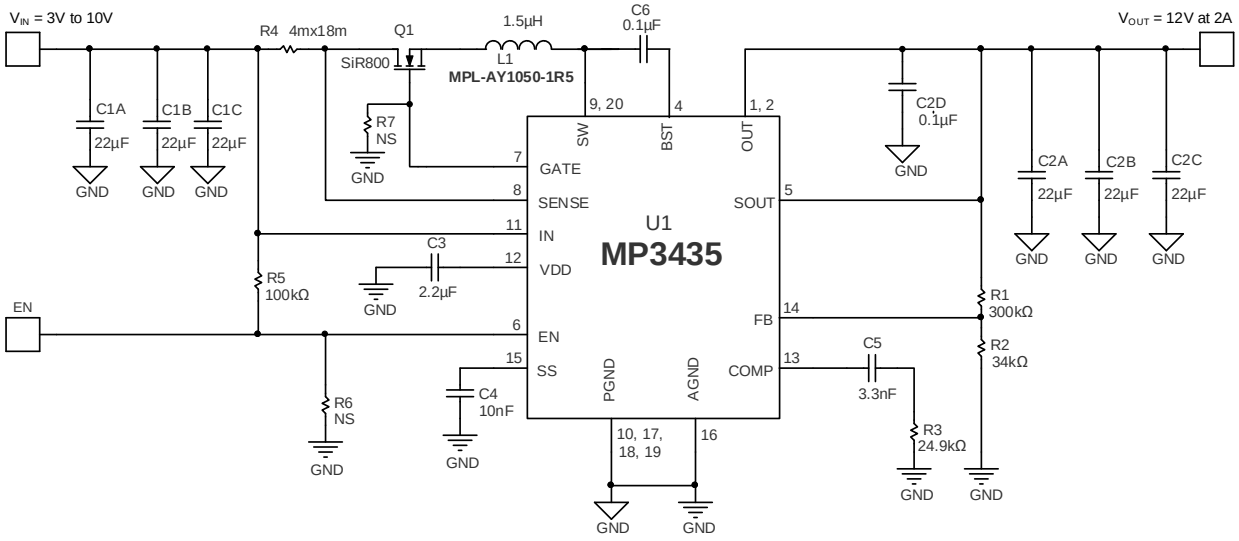


Figure 6: 12V Output Solution with Input Disconnect Function

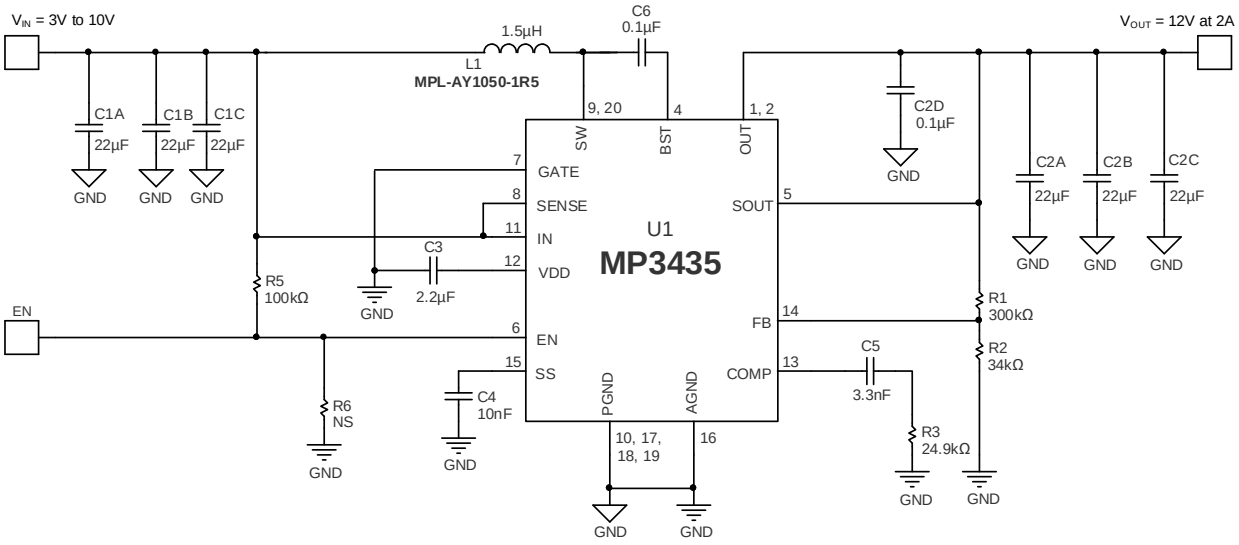
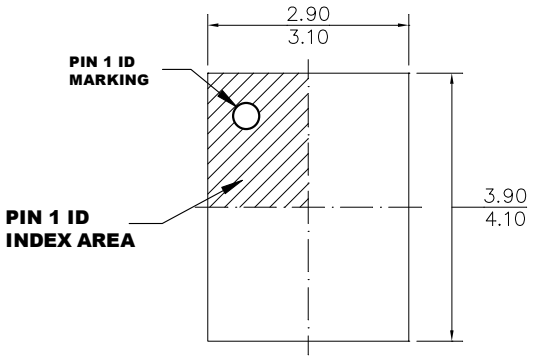


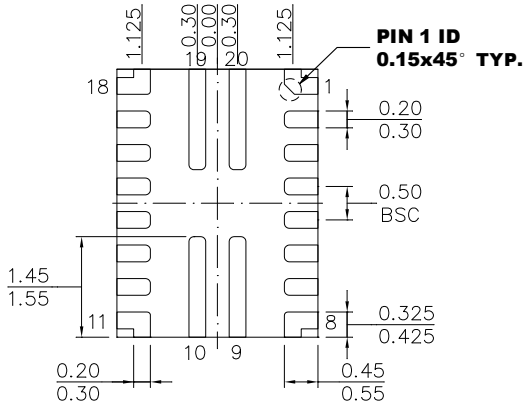
Figure 7: 12V Output Solution without Input Disconnect Function

PACKAGE INFORMATION

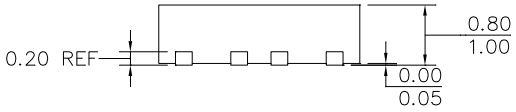
QFN-20 (3mmx4mm)



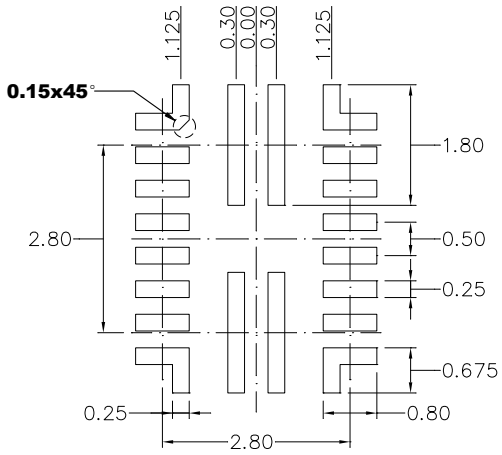
TOP VIEW



BOTTOM VIEW



SIDE VIEW

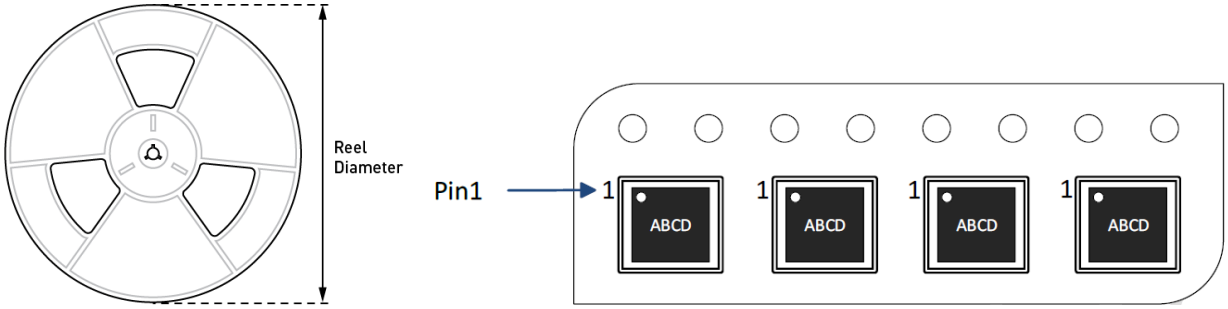


RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) LEAD COPLANARITY SHALL BE 0.08 MILLIMETERS MAX.
3) JEDEC REFERENCE IS MO-220.
4) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP3435GL-Z	QFN-20 (3mmx4mm)	5000	N/A	N/A	13in	12mm	8mm

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	11/30/2021	Initial Release	-