NX20P5090

High Voltage USB PD Power Switch

Rev. 1 — 22 October 2015 Product data sheet

1. General description

The NX20P5090 is an advanced 5A uni-directional power switch for USB PD. It includes under voltage lockout, over voltage lockout, reverse current protection and over-temperature protection circuits, it is designed to automatically isolate the power switch terminals when a fault condition occurs. Both VBUS and VINT pin have 29V tolerance in shutdown mode, two chips of NX20P5090 can be used in parallel to support dual power inputs connecting to same charging circuit.

The device has a default 23V over voltage protection threshold, and the OVP threshold can be adjusted by using external resistor divider on OVLO pin. A 15ms de-bounce time is deployed every time before the device is switched ON, following by a soft start to limit the inrush current.

Designed for operation from 2.5 V to 20.0 V, it is used in USB PD power control applications to offer essential protection and enhance system reliability.

NX20P5090 is offered in a small 15-bump 1.54 x 2.56 mm, 0.5mm pitch WLCSP package.

2. Features and benefits

- Wide supply voltage range from 2.5 V to 20.0 V
- I_{SW} maximum 5A continuous current
- 29 V tolerance on both VBUS and VINT pin
- 30 mΩ (typical) Low ON resistance
- Adjustable VBUS over voltage protection
- Built in slew rate control for inrush current limit
- All time two level reverse-current protection
- Protection circuitry
  - Over-Temperature Protection
  - Over-Voltage Protection
  - Under-Voltage Lockout
  - Reverse Current Protection
- Surge protection:
  - IEC61000-4-5 exceeds ±90 V on VBUS without capacitor
  - IEC61000-4-5 exceeds ±100 V on VBUS with 22uF capacitor
- ESD protection
  - IEC61000-4-2 contact discharge exceeds 8 kV on VBUS
  - HBM ANSI/ESDA/JEDEC JS-001 Class 2 exceeds 2 kV
  - CDM AEC standard Q100-01 (JESD22-C101E)
- Specified from –40 °C to +85 °C

3. Applications

- Smart and feature phones
- Tablets, eBooks
- Notebook

4. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
NX20P5090UK	–40 °C to +85 °C	WLCSP15	wafer level chip-scale package, 15bumps; body 1.54 x 2.56mm; 0.5 mm pitch (Backside Coating included)	NX20P5090

5. Marking

Table 2. Marking codes

Type number	Marking code
NX20P5090UK	X20PPD

6. Functional diagram

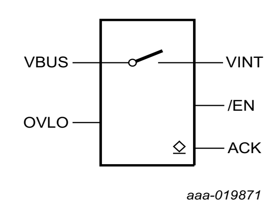


Fig 1. Logic symbol

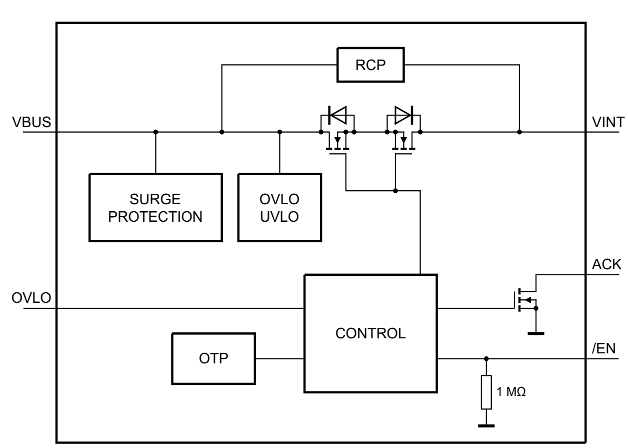


Fig 2. Logic diagram

7. Pinning information

7.1 Pinning

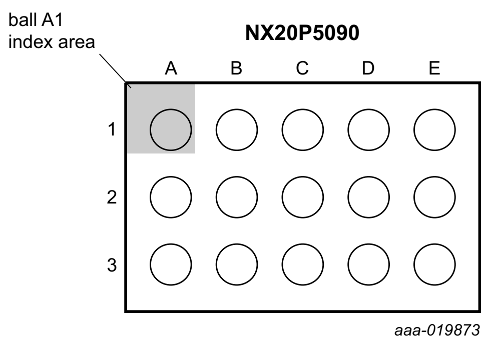


Fig 3. Pin configuration WLCSP15

NX20P5090

	A	B	C	D	E
1	VINT	VINT	VINT	VINT	VBUS
2	ACK	VBUS	VBUS	VBUS	VBUS
3	/EN	OVLO	GND	GND	GND

aaa-019874

Transparent top view

Fig 4. Ball mapping for WLCSP15

7.2 Pin description

Table 3. Pin description

Symbol	Pin	Description
VBUS	B2, C2, D2, E1, E2	VBUS (Power Input)
VINT	A1, B1, C1, D1	VINT (Power Output)
OVLO	B3	V_{OVLO} threshold input
ACK	A2	Power Good Acknowledge (open-drain output)
GND	C3, D3, E3	ground (0 V)
$\overline{EN}$	A3	enable input (active LOW)

8. Functional description

Table 4. Function table[1]

$\overline{EN}$	VBUS	VINT	ACK	Operation mode
L	< 2.5 V	X	Z	Under-voltage lockout; switch open
L	2.5 V < VBUS < V_{OVLO}	X	L	Enabled; switch closed; charging mode
L	X	X	Z	Over-temperature protection; switch open
L	> V_{OVLO}	X	Z	Over-voltage lockout; switch open
H	X	X	Z	Disable; switch open
X	X	VINT>VBUS	Z	Reverse Current Protection; Switch open

[1] H = HIGH voltage level; L = LOW voltage level, Z = high-impedance OFF-state.

8.1 $\overline{EN}$-input

A HIGH on $\overline{EN}$ will disable the channel MOSFET and all protection circuits, putting the device into a low power mode. A LOW on $\overline{EN}$ will enable the protection circuits and the MOSFET. There is an internal 1 MΩ pull-down resistor on the $\overline{EN}$ pin to ensure the power switch conducting in dead-battery situation. A 15ms de-bounce time has been deployed before device turning on. $\overline{EN}$ pin has 29V voltage tolerance.

8.2 Under-voltage lockout

When $\overline{EN}$ is LOW and VBUS < V_{UVLO}, the under-voltage lockout (UVLO) circuits disable the power MOSFET. Once VBUS exceeds V_{UVLO} and no other protection circuit is active, the state of the channel MOSFET is controlled by the $\overline{EN}$ pin.

8.3 Over-voltage lockout

When $\overline{EN}$ is LOW and VBUS > V_{OVLO}, the over-voltage lockout (OVLO) circuit will disable the power MOSFET. Once VBUS drops below V_{OVLO} and no other protection circuit is active, the power MOSFET will resume operation.

OVLO pin is used to set the over voltage threshold. the default over voltage threshold is 23V when OVLO pin is short to GND. By connecting a resistor divider to the OVLO pin (see Figure 5), the over voltage threshold is adjustable from 4V to 23V with below equation

$$Vovlo = Vth(ovlo) \times (R1 + R2)/(R2)$$

When the voltage on OVLO pin is below 0.1V, the device will use default 23V OVP threshold.

8.4 Over-temperature protection

When $\overline{EN}$ is LOW and the device temperature exceeds 140 °C the over-temperature protection (OTP) circuit will disable the power MOSFET and set the ACK output Hi-Z. Once the device temperature decreases below 115 °C and no other protection circuit is active, the state of the N-channel MOSFET is controlled by the $\overline{EN}$ pin again.

8.5 ACK output

The ACK output is an open-drain output that requires an external pull-up resistor. ACK pin indicates the state of the power switch, when no fault is detected and power switch is conducting, ACK will output low, otherwise it will stay at high impedance. The pull up resistor value is recommend to be 10KΩ to 200KΩ.

8.6 Reverse Current Protection

NX20P5090 has all time reverse current protection regardless the $\overline{EN}$ logic level. Once the voltage on VINT is higher than VBUS for 45mV, RCP circuit will be triggered after a 3.7ms de-glitch time. If the voltage gap is greater than 120mV, RCP will be triggered right away to switch off the power MOSFET.

During the start up de-glitch time, if the device detects the VINT voltage is higher than VBUS by 45mV, the power MOSFET will not be turned on.

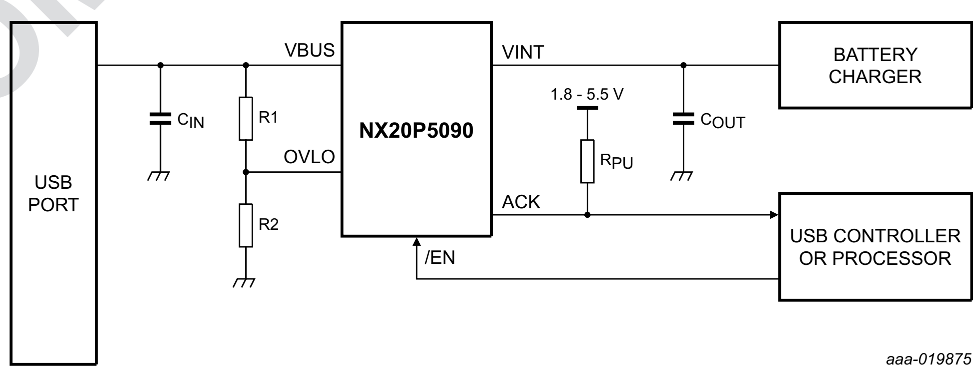
The RCP circuit benefits the system design by providing the capability of parallel connecting two USB charging port to single charger input without the backward leakage.

9. Application diagram

The NX20P5090 is typically used on a USB port charging path in a portable, battery operated device. The ACK signal requires an additional external pull-up resistor which should be connected to a supply voltage matching the logic input pin supply level that it is connected to.

When the default 23V OVP threshold is used, the OVLO pin shall be short to GND. While if an adjustable OVP threshold is needed, a resister divider shall be connected to the OVLO pin.

For the best performance, it is recommended to keep input and output trace short and capacitors as close to the device as possible. Regarding to the thermal performance, it is recommended to increasing the PCB area around VINT and VBUS pins.

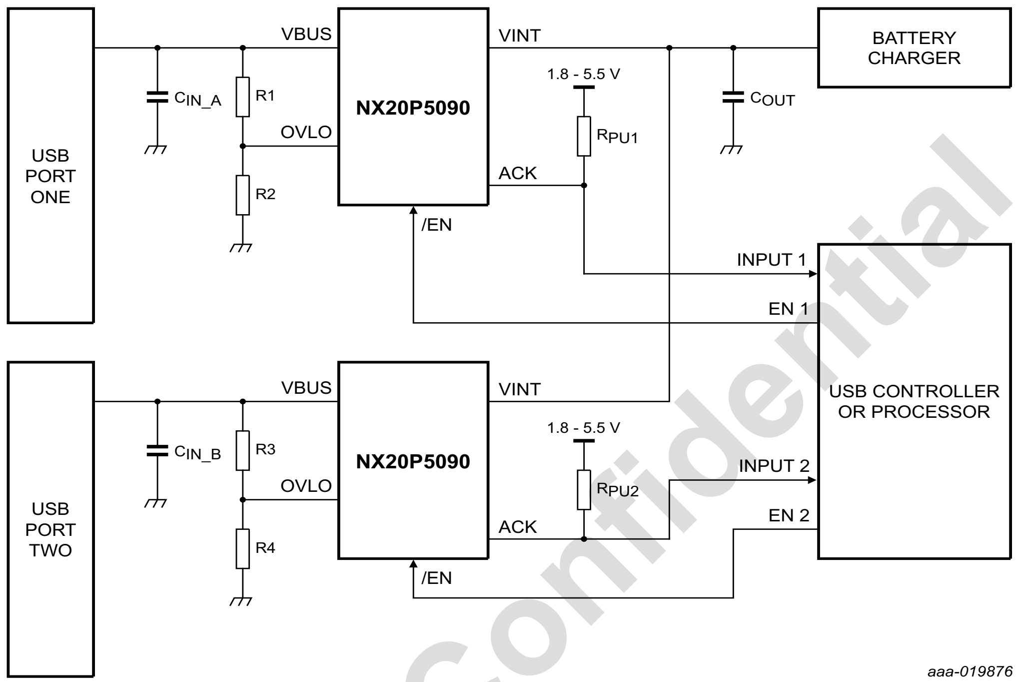


R1 and R2 are only needed for adjustable V_{OVLO}; To use default V_{OVLO} threshold, connect OVLO to GND

R1 is recommended to use minimum 1MΩ Resistor

C_{OUT} minimum is recommended to be 1uF;

Fig 5. NX20P5090 application with one charging input



R1, R2, R3 and R4 are only needed for adjustable V_{OVLO}; To use default V_{OVLO} threshold, connect OVLO to GND

R1 and R3 are recommended to use minimum 1MΩ Resistor

C_{OUT} minimum is recommended to be 1uF

Fig 6. NX20P5090 application with two charging inputs

10. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V_I	input voltage	VBUS	[1]	–0.5	+29	V
		VINT	[1]	–0.5	+29	V
		OVLO		–0.5	VBUS	V
		$\overline{\text{EN}}$	[2]	–0.5	+29	V
V_O	output voltage	ACK		–0.5	+6.0	V
I_{IK}	input clamping current	$\overline{\text{EN}}$: $V_I < -0.5$ V		–50	-	mA
I_{SK}	switch clamping current	VBUS; VINT; $V_I < -0.5$ V		–50	-	mA
I_{SW}	continuous switch current	T_{amb} = 85 °C		-	5	A
		T_{amb} = 105 °C		-	3.5	A
	peak switch current	100μs pulse, 2% duty cycle		-	10	A
T_{stg}	storage temperature			–65	+150	°C
P_{tot}	total power dissipation	T_{amb} = 25 °C		-	1.45	W

[1] The minimum and maximum switch voltage ratings may be exceeded if the switch clamping current rating is observed.

[2] The minimum input voltage rating may be exceeded if the input current rating is observed.

11. Recommended operating conditions

Table 6. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_I	input voltage	VBUS	2.5	20	V
		VINT	2.5	20	V
		$\overline{EN}$	0	20	V
V_O	output voltage	ACK	0	5.5	V
$T_{j(max)}$	maximum junction temperature		–40	+125	°C
T_{amb}	ambient temperature		–40	+85	°C

12. Thermal characteristics

Table 7. Thermal characteristics

Symbol	Parameter	Conditions		Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient		[1][2]	67.2	K/W

[1] The overall Rth(j-a) can vary depending on the board layout. To minimize the effective Rth(j-a), all pins must have a solid connection to larger Cu layer areas e.g. to the power and ground layer. In multi-layer PCB applications, the second layer should be used to create a large heat spreader area right below the device. If this layer is either ground or power, it should be connected with several vias to the top layer connecting to the device ground or supply.Try not to use any solder-stop varnish under the chip.

[2] This Rth(j-a) is calculated based on JEDEX2S2P board. The actual Rth(j-a) value may vary in applications using different layer stacks and layouts.

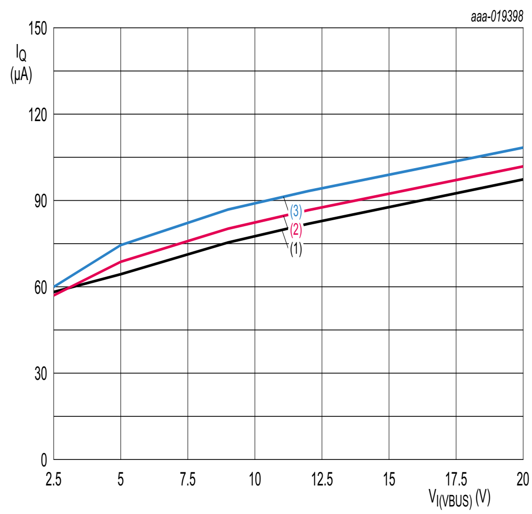
13. Static characteristics

Table 8. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	T_{amb} = 25 °C			T_{amb} = −40 °C to +85 °C		Unit
			Min	Typ	Max	Min	Max	
V_{IH}	HIGH-level input voltage	$\overline{EN}$ pin; $V_{I(VBUS)}$ = 2.5V to 20V	1.2	-	-	1.2	-	V
V_{IL}	LOW-level input voltage	$\overline{EN}$ pin; $V_{I(VBUS)}$ = 2.5V to 20V	-	-	0.4	-	0.4	V
V_{OL}	LOW-level output voltage	ACK; I_O = 8 mA; $V_{I(VBUS)}$ = 2.5V to 20V	-	-	0.5	-	0.5	V
R_{pd}	pull-down resistance	$\overline{EN}$	-	1	-	-	-	MΩ
I_q	VBUS quiescent current	$\overline{EN}$ = 0 V; $V_{I(VBUS)}$ = 5.0 V; I_O = 0 A;	-	70	-	-	95	µA
		$\overline{EN}$ = 0 V; $V_{I(VBUS)}$ = 20 V; I_O = 0 A;	-	100	-	-	140	µA
		$\overline{EN}$ = 5.0 V; $V_{I(VBUS)}$ = 5.0 V; I_O = 0 A;	-	5	-	-	10	µA
		$\overline{EN}$ = 5.0 V; $V_{I(VBUS)}$ = 20 V; I_O = 0 A;	-	15	-	-	30	µA
$I_{S(OFF)}$	VBUS OFF-state leakage current	$\overline{EN}$ = 5.0 V; $V_{I(VBUS)}$ = 5.0V; VINT = 0 V	-	5	-	-	10	µA
		$\overline{EN}$ = 5.0 V; $V_{I(VBUS)}$ = 20 V; VINT = 0 V	-	15	-	-	30	µA
	VINT OFF-state Leakage current	$\overline{EN}$ = 5.0 V; $V_{I(VINT)}$ = 5.0V; VBUS = 0V	-	1	-	-	5	µA
		$\overline{EN}$ = 5.0 V; $V_{I(VINT)}$ = 20 V; VBUS = 0V	-	4	-	-	16	µA
$I_{S(ON)}$	RCP leakage current	$\overline{EN}$ = 0 V; $V_{I(VINT)}$ = 5V; $V_{(VBUS)}$ = 0V	-	1	-	-	5	µA
I_I	OVLO input leakage Current	V_{OVLO}=$V_{th(OVLO)}$	-	-	-	-	50	nA
V_{UVLO}	under-voltage lockout release voltage	VBUS Rising; $\overline{EN}$ = 0 V	-	2.37	-	2.24	2.5	V
$V_{hys(UVLO)}$	under-voltage lockout hysteresis voltage	VBUS Falling;	-	100	-	-	-	mV
V_{OVLO}	Default overvoltage lockout voltage	VBUS Rising; $\overline{EN}$ = 0 V; OVLO short to GND	-	23	-	-	-	V
		VBUS Falling; $\overline{EN}$ = 0 V; OVLO short to GND	-	22.5	-	-	-	V
$V_{th(OVLO)}$	external OVLO set threshold voltage	$V_{I(VBUS)}$ = 2.5V to 20V; $\overline{EN}$ = 0 V	-	1.227	-	1.164	1.287	V
V_{trig}	RCP trigger voltage	V_{trig} = $V_{(VINT)}$ - $V_{(VBUS)}$	-	45	-	10	80	mV
C_I	input capacitance	$\overline{EN}$ pin; $V_{I(VBUS)}$ = 5V	-	4.5	-	-	-	pF

13.1 Graphs



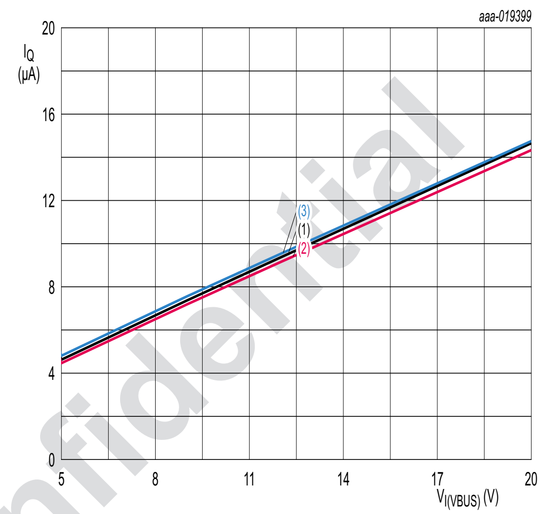
$\overline{EN}$ = 0V; I_O = 0 A

(1) T_{amb} = +85 °C.

(2) T_{amb} = +25 °C.

(3) T_{amb} = –40 °C.

Fig 7. On-state quiescent current versus input voltage



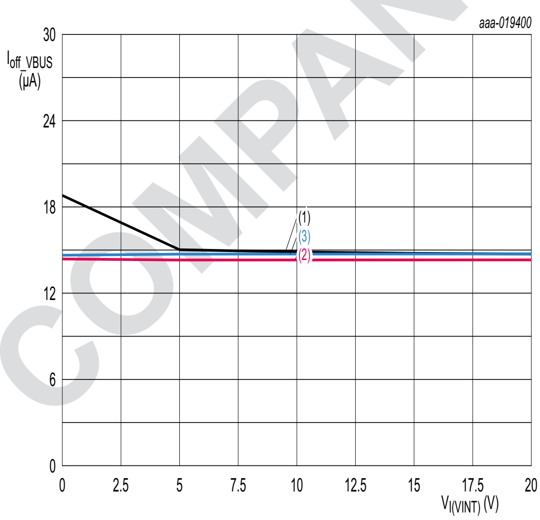
$\overline{EN}$ = 5V; I_O = 0 A

(1) T_{amb} = +85 °C.

(2) T_{amb} = +25 °C.

(3) T_{amb} = –40 °C.

Fig 8. OFF-state quiescent current versus input voltage



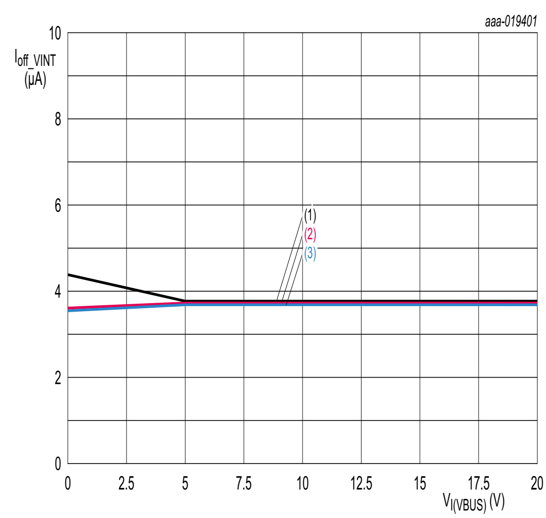
$V_{I(VBUS)}$ = 20V; $\overline{EN}$ = 5V

(1) T_{amb} = +85 °C.

(2) T_{amb} = +25 °C.

(3) T_{amb} = –40 °C.

Fig 9. OFF-state leakage current on VBUS pin



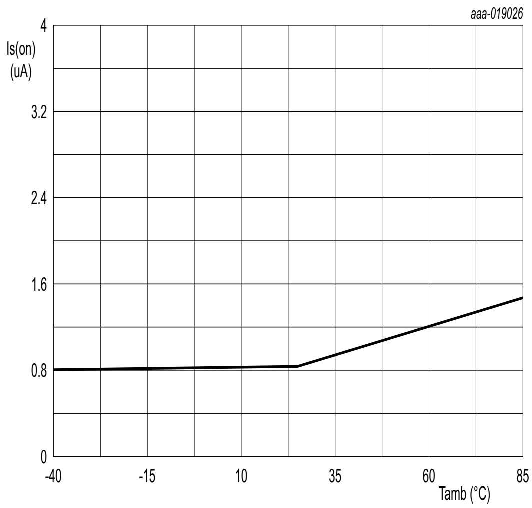
$V_{I(VINT)}$ = 20V; $\overline{EN}$ = 5V

(1) T_{amb} = +85 °C

(2) T_{amb} = +25 °C.

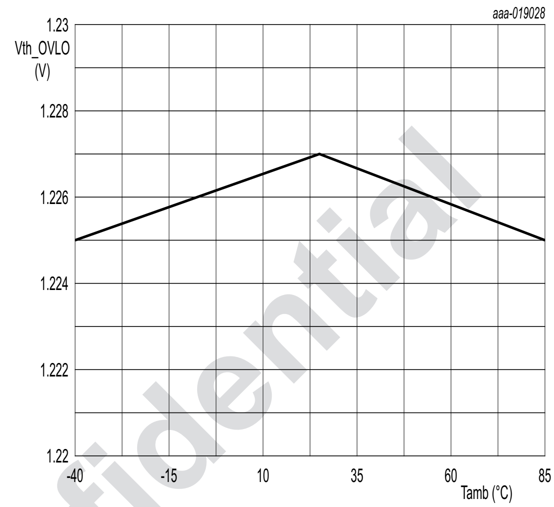
(3) T_{amb} = –40 °C.

Fig 10. OFF-state leakage current on VINT pin



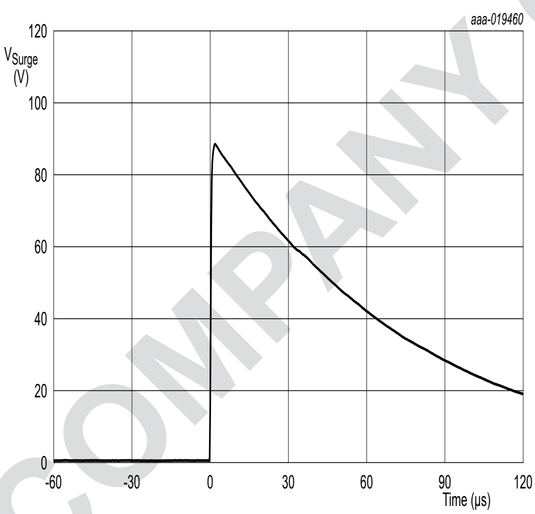
$\overline{EN}$ = 0V; $V_{I(VINT)}$ = 5V; VBUS = 0V

Fig 11. Reverse Leakage Current versus temperature



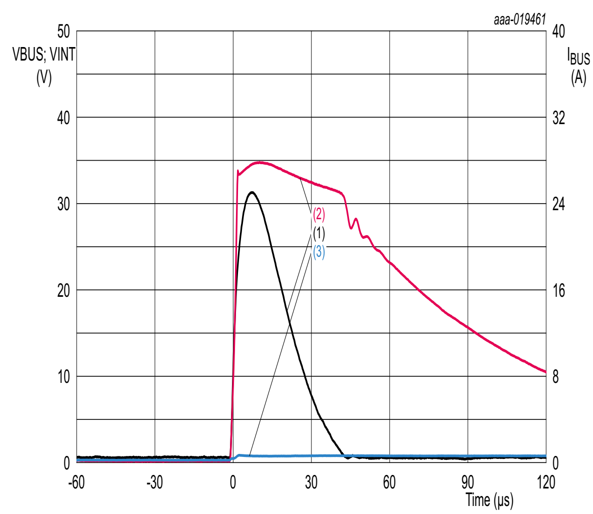
$\overline{EN}$ = 0V; $V_{I(VBUS)}$ = 5V;

Fig 12. external OVLO set threshold versus temperature



IEC61000-4-5 90V

Fig 13. 90V Surge Voltage without Device



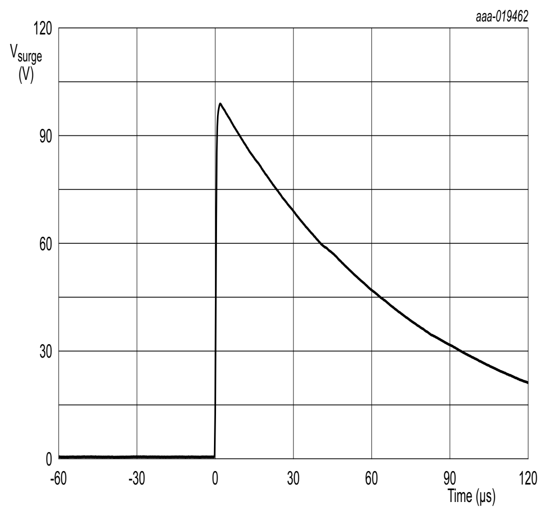
$\overline{EN}$ = 0V; OVLO short to GND; no capacitor on VBUS

(1) $I_{I(VBUS)}$

(2) $V_{I(VBUS)}$

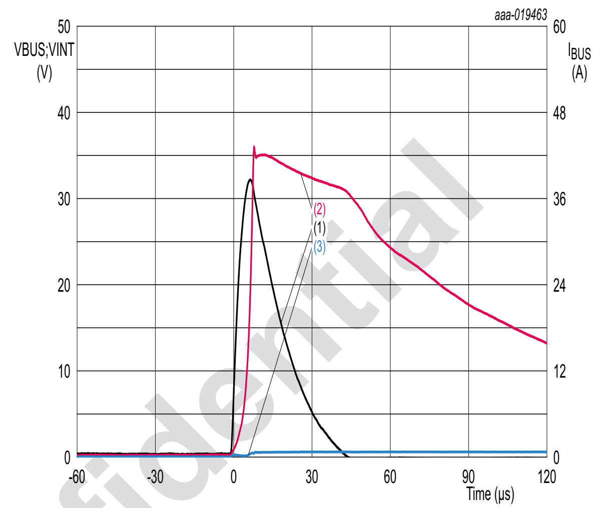
(3) $V_{O(VINT)}$

Fig 14. 90V Surge with Device



IEC61000-4-5 100V

Fig 15. 100V Surge Voltage without Device



$\overline{EN}$ = 0V; OVLO short to GND; 22uF capacitor on VBUS

(1) $I_{I(VBUS)}$

(2) $V_{I(VBUS)}$

(3) $V_{O(VINT)}$

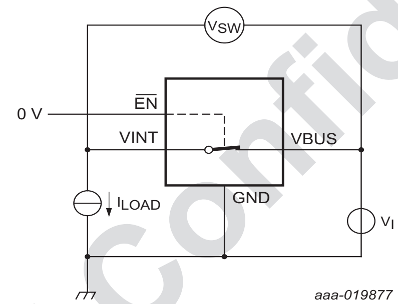
Fig 16. 100V Surge with Device

13.2 ON resistance

Table 9. ON resistance
At recommended operating conditions; voltages are referenced to GND (ground = 0 V)

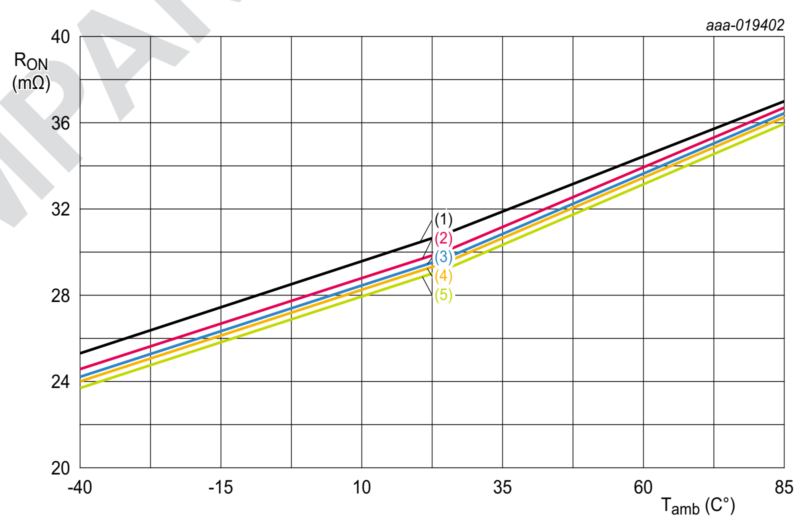
Symbol	Parameter	Conditions	T_{amb} = 25 °C			T_{amb} = −40 °C to +85 °C		Unit
			Min	Typ	Max	Min	Max	
R_{ON}	ON resistance	I_{LOAD} = 1 A						
		$V_{I(VBUS)}$ = 5.0 V	-	30	36	-	43	mΩ
		$V_{I(VBUS)}$ = 20 V	-	30	36	-	43	mΩ

13.3 ON resistance test circuit and graphs



$R_{ON} = V_{SW} / I_{LOAD}$

Fig 17. Test circuit for measuring ON resistance



(1) $V_{I(VBUS)}$ = 2.5 V
(2) $V_{I(VBUS)}$ = 5.0 V
(3) $V_{I(VBUS)}$ = 9.0 V
(4) $V_{I(VBUS)}$ = 12.0 V
(5) $V_{I(VBUS)}$ = 20.0 V

Fig 18. ON resistance versus temperature

14. Dynamic characteristics

Table 10. Dynamic characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V); for test circuit see Figure 20.

Symbol	Parameter	Conditions	T_{amb} = 25 °C			T_{amb} = –40 °C to +85 °C		Unit
			Min	Typ	Max	Min	Max	
t_{en}	Enable Time	From $\overline{EN}$ to $V_{(VINT)}$ = 10% of $V_{(VBUS)}$; (Including 15ms debounce time); $V_{I(VBUS)}$ = 5V; C_{Load} = 100μF; R_{Load} = 100Ω	-	21.9	-	-	-	ms
t_{TLH}	VINT rise time	$V_{(VINT)}$ from 10% to 90% $V_{(VBUS)}$; C_{Load} = 100μF; R_{Load} = 100Ω						
		$V_{I(VBUS)}$ = 5V	-	3.4	-	-	-	ms
		$V_{I(VBUS)}$ = 20V	-	6.9	-	-	-	ms
$t_{dis(OVP)}$	OVP turn off time	From $V_{(VBUS)}$>V_{ovlo} to $V_{(VINT)}$ = 80% of $V_{(VBUS)}$; R_{load} = 100Ω,; C_{load} = 0 μF; $V_{I(VBUS)}$ = 20V; OVLO pin short to GND	-	122	-	-	-	ns
t_{degl}	RCP de-glitch time	From $V_{(VINT)}$>$V_{(VBUS)}$+45mV to switch off	-	3.7	-	2.6	4.8	ms
$t_{dis(RCP)}$	RCP turn off time	From $V_{(VINT)}$>$V_{(VBUS)}$+120mV to switch off [1]	-	10	-	-	-	us
t_{on}	turn-on time	$\overline{EN}$ to $V_{(VINT)}$ = 90% $V_{(VBUS)}$						
		$V_{I(VBUS)}$ = 5.0 V	-	25.3	-	-	-	ms
		$V_{I(VBUS)}$ = 20 V	-	29.2	-	-	-	ms
t_{off}	turn-off time	$\overline{EN}$ to $V_{(VINT)}$ = 10% $V_{(VBUS)}$						
		$V_{I(VBUS)}$ = 5.0 V; C_{Load} = 100μF; R_{Load} = 100Ω	-	23	-	-	-	ms
		$V_{I(VBUS)}$ = 20V; C_{Load} = 100μF; R_{Load} = 100Ω	-	23	-	-	-	ms

[1] Guaranteed by design

14.1 Waveforms and test circuit

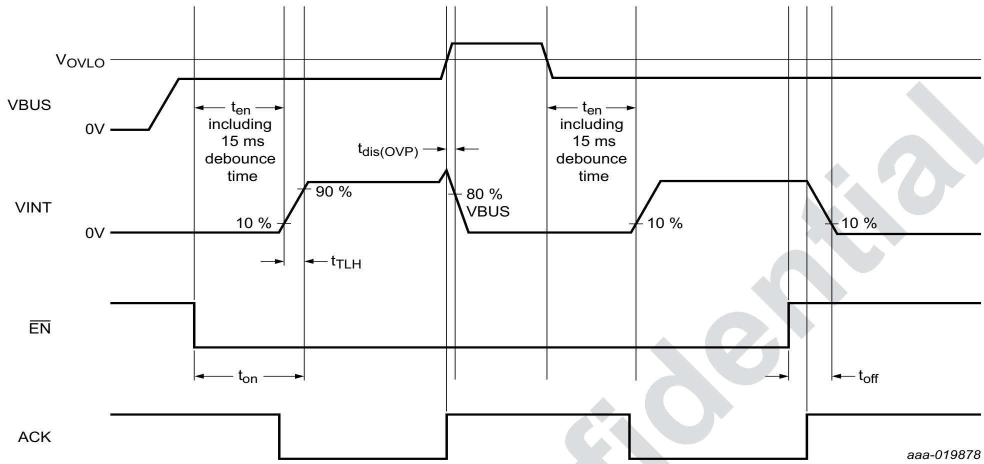
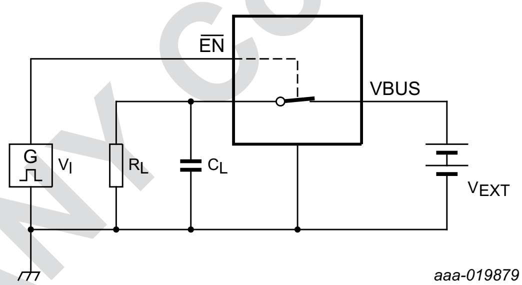


Fig 19. Switching times



Test Condition is given in Table 11

R_L = Load resistance.

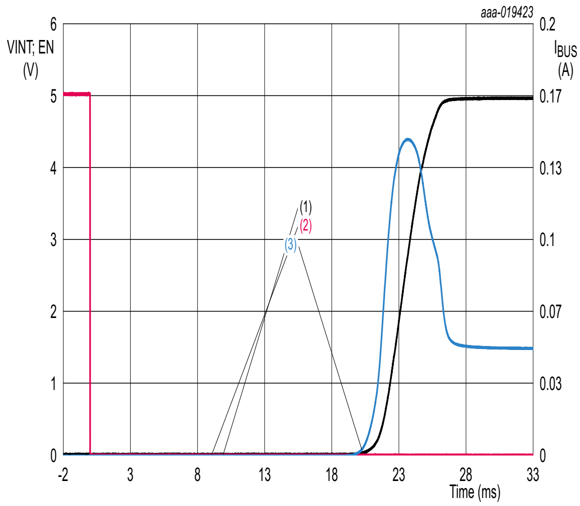
C_L = Load capacitance including jig and probe capacitance.

V_{EXT} = External voltage for measuring switching times.

Fig 20. Test circuit for measuring switching times

Table 11. Test Condition

Supply voltage V_{EXT}	Load	
VBUS	C_L	R_L
2.5 V to 20V	100 μF	100 Ω



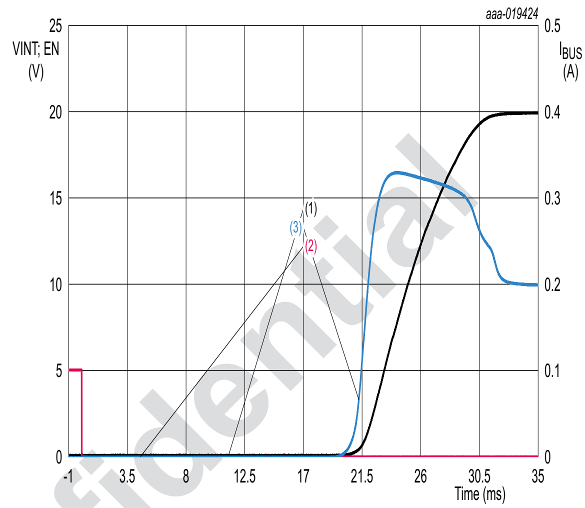
$V_{I(VBUS)}$ = 5.0 V; R_L = 100 Ω; C_L = 100 μF

(1) VINT

(2) $\overline{EN}$

(3) $I_{I(VBUS)}$

Fig 21. Turn on time and in-rush current at 5V



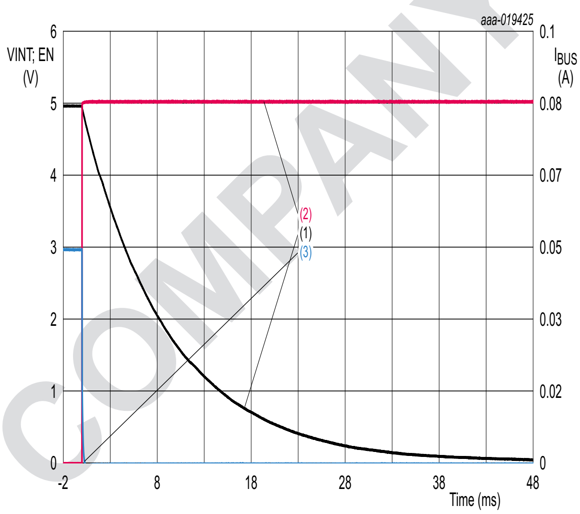
$V_{I(VBUS)}$ = 20.0 V; R_L = 100 Ω; C_L = 100 μF

(1) VINT

(2) $\overline{EN}$

(3) $I_{I(VBUS)}$

Fig 22. Turn on time and in-rush current at 20V



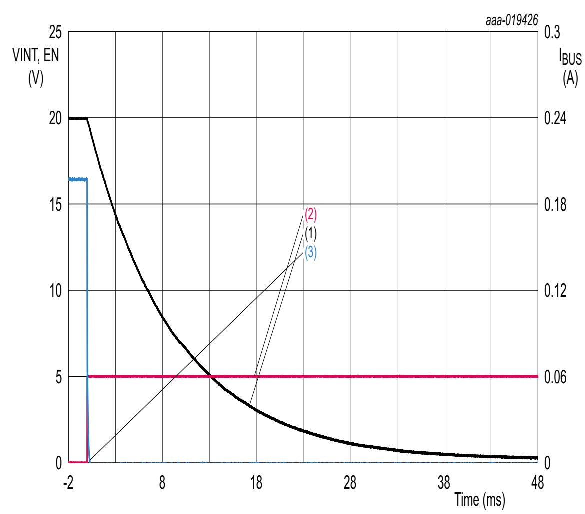
$V_{I(VBUS)}$ = 5.0 V; R_L = 100 Ω; C_L = 100 μF

(1) VINT

(2) $\overline{EN}$

(3) $I_{I(VBUS)}$

Fig 23. Turn off time at 5V



$V_{I(VBUS)}$ = 20.0 V; R_L = 100 Ω; C_L = 100 μF

(1) VINT

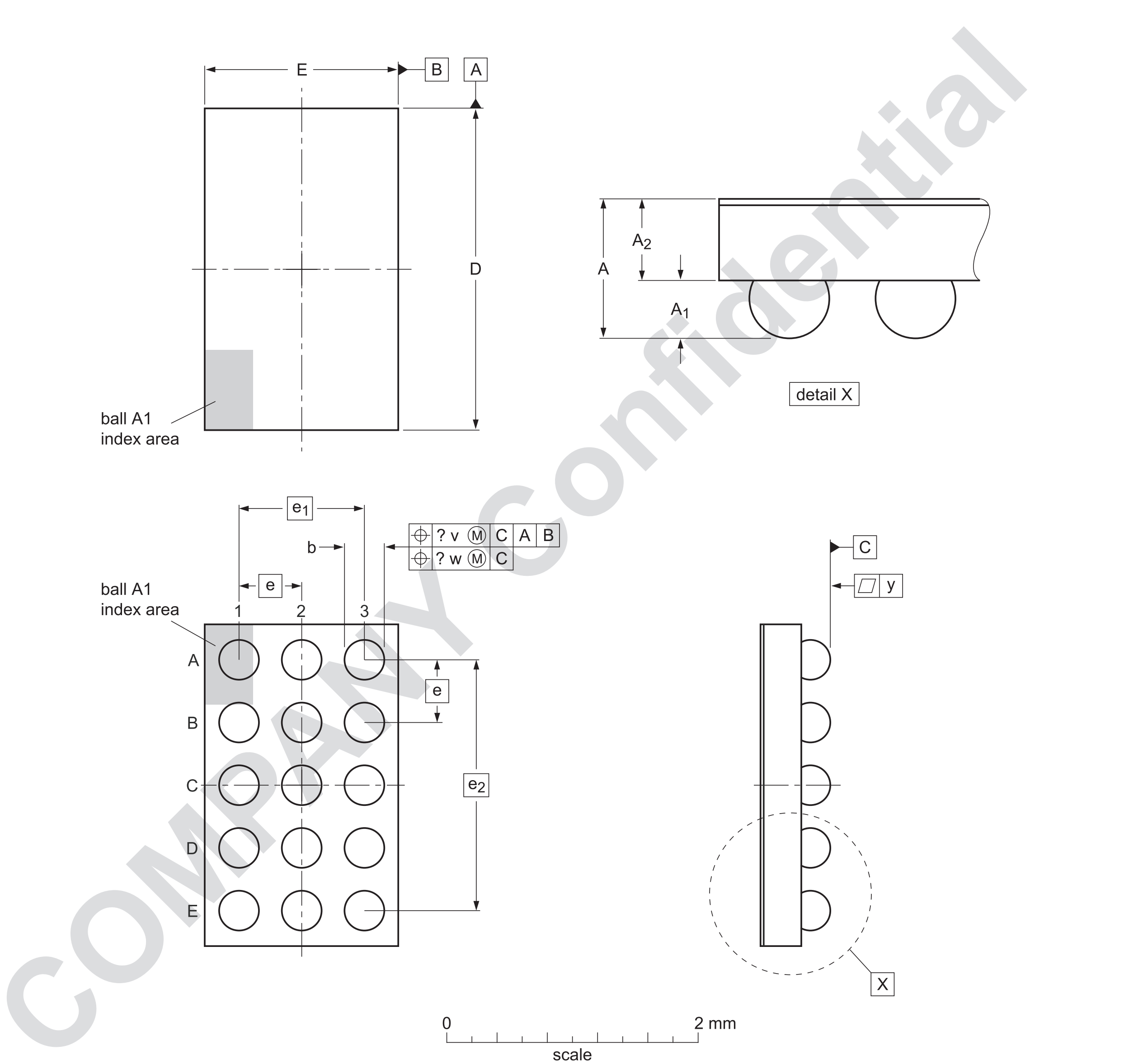
(2) $\overline{EN}$

(3) $I_{I(VBUS)}$

Fig 24. Turn off time at 20V

15. Package outline

WLCSP15: wafer level chip-scale package; 15 bumps; 2.56 x 1.54 x 0.555 mm (Backside coating included) **SOT1392-1**



Dimensions (mm are the original dimensions)

Unit		A	A_1	A_2	b	D	E	e	e_1	e_2	v	w	y
mm	max	0.595	0.260	0.350	0.35	2.59	1.57						
	nom	0.555	0.230	0.325	0.32	2.56	1.54	0.5	1.0	2.0	0.05	0.015	0.03
	min	0.515	0.200	0.290	0.29	2.53	1.51						

Note: Backside coating 25 祄

sot1392-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
sot1392-1		- - -				~~15-08-11~~ 15-09-14

Fig 25. Package outline SOT1392-1 (WLCSP 15)

16. Packing information

16.1 Packing method

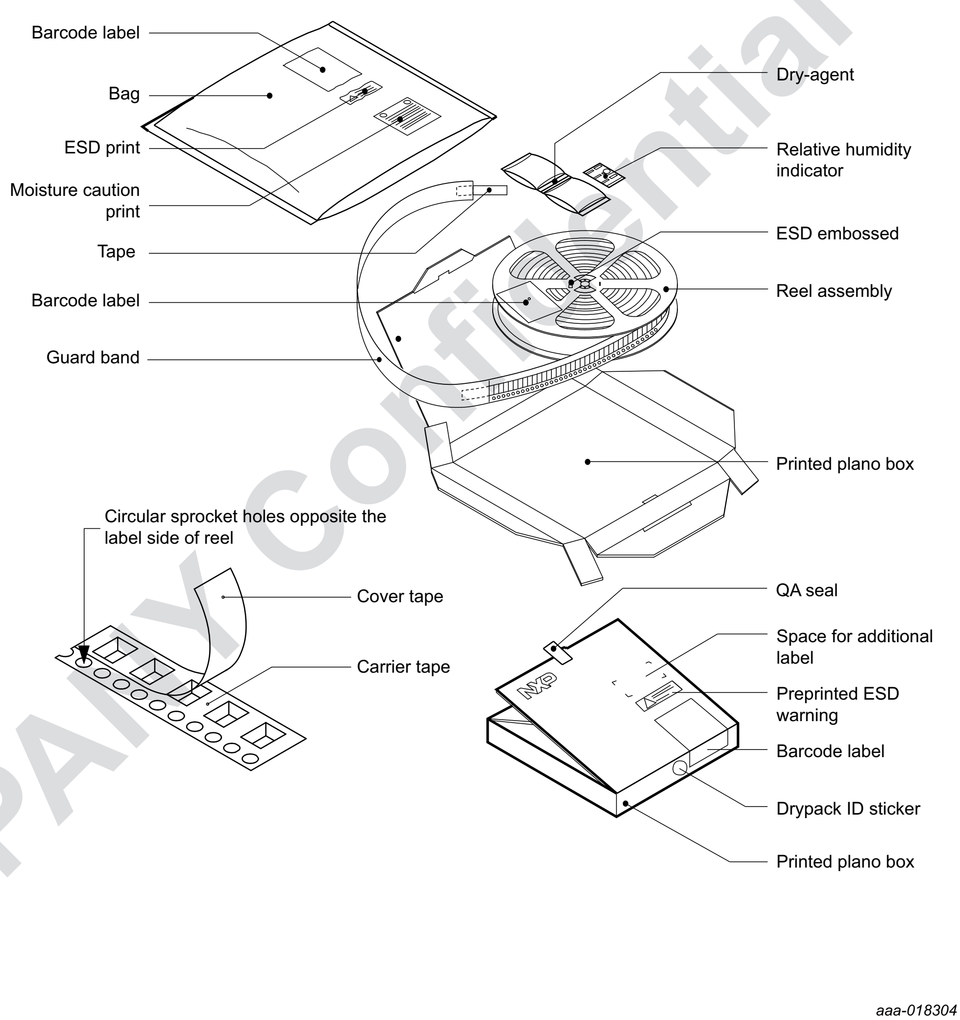


Fig 26. Reel dry pack for SMD: single set of carrier tape sprocket holes

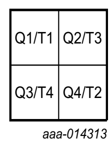
Table 12. Dimensions and quantities

Reel dimensions d × w (mm) [1]	SPQ/PQ (pcs) [2]	Reels per box	Outer box dimensions l × w × h (mm)
180 × 12	3000	1	209 × 206 × 37

[1] d = reel diameter; w = tape width.

[2] Packing quantity dependent on specific product type.
View ordering and availability details at NXP order portal, or contact your local NXP representative.

16.2 Product orientation



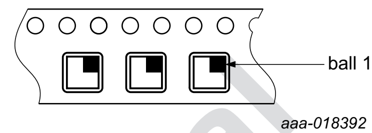


Fig 27. Product orientation in carrier tape

16.3 Carrier tape dimensions

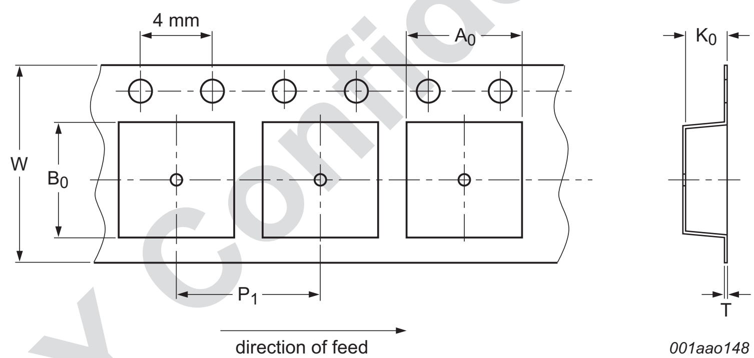


Fig 28. Carrier tape dimensions

Table 13. Carrier tape dimensions

In accordance with IEC 60286-3.

A_0 (mm)	B_0 (mm)	K_0 (mm)	T (mm)	P_1 (mm)	W (mm)
1.67 ± 0.05	2.69 ± 0.05	0.70 ± 0.05	0.25 ± 0.02	4.0 ± 0.1	12 + 0.3 / – 0.1

16.4 Reel dimensions

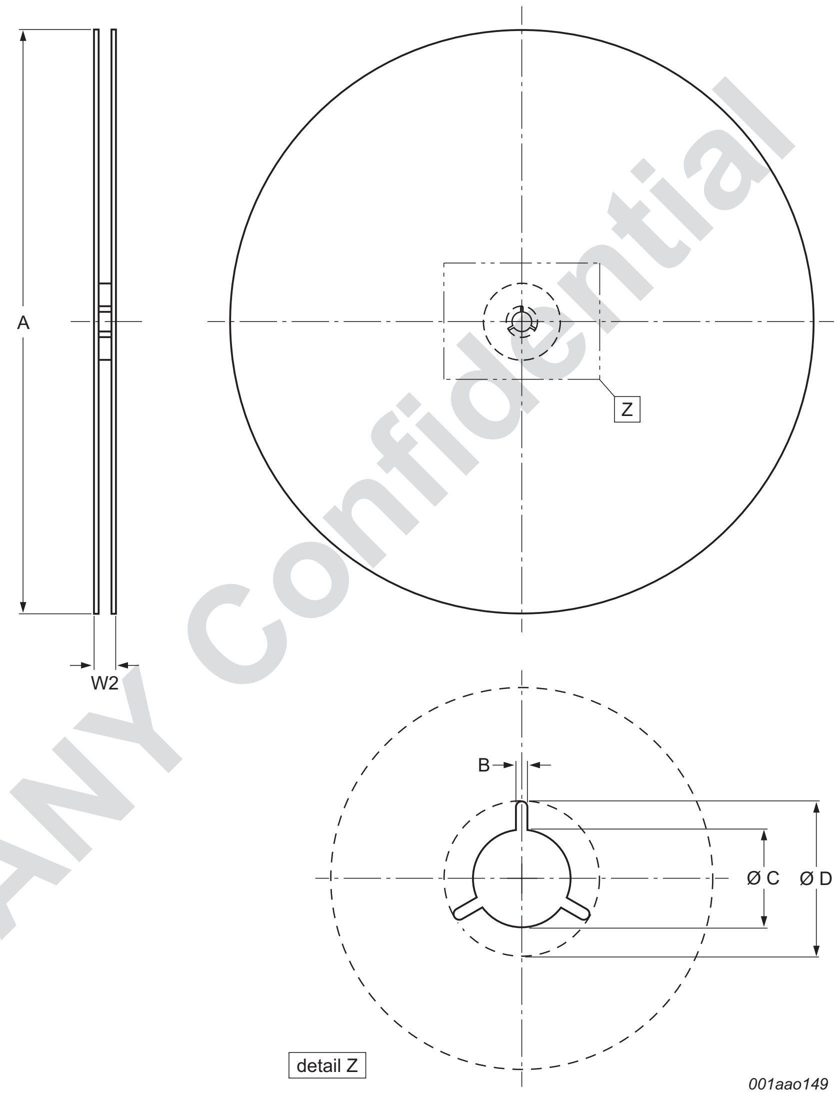


Fig 29. Schematic view of reel

Table 14. Reel dimensions

In accordance with IEC 60286-3.

A [nom] (mm)	W2 [max] (mm)	B [min] (mm)	C [min] (mm)	D [min] (mm)
180	18.4	1.5	12.8	20.2

16.5 Barcode label

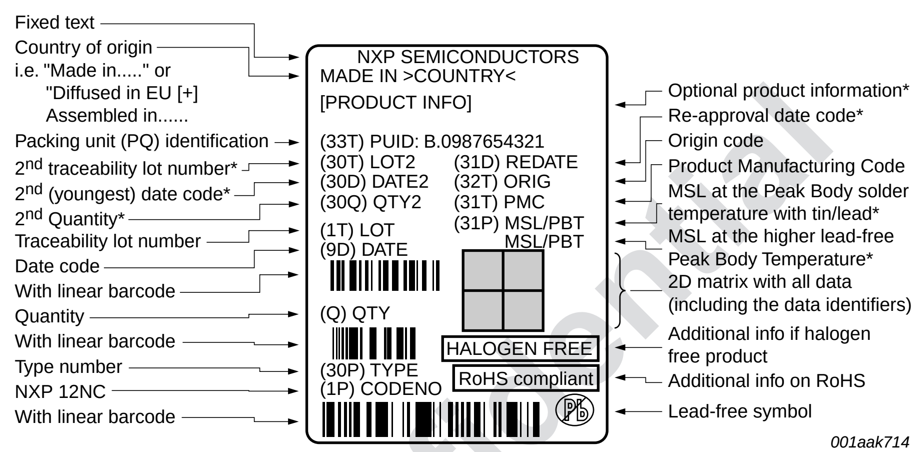


Fig 30. Example of typical box and reel information barcode label

Table 15. Barcode label dimensions

Box barcode label l × w (mm)	Reel barcode label l × w (mm)
100 × 75	100 × 75

17. Soldering of WLCSP packages

17.1 Introduction to soldering WLCSP packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering WLCSP (Wafer Level Chip-Size Packages) can be found in application note *AN10439 “Wafer Level Chip Scale Package”* and in application note *AN10365 “Surface mount reflow soldering description”*.

Wave soldering is not suitable for this package.

All NXP WLCSP packages are lead-free.

17.2 Board mounting

Board mounting of a WLCSP requires several steps:

1. Solder paste printing on the PCB
2. Component placement with a pick and place machine
3. The reflow soldering itself

17.3 Reflow soldering

Key characteristics in reflow soldering are:

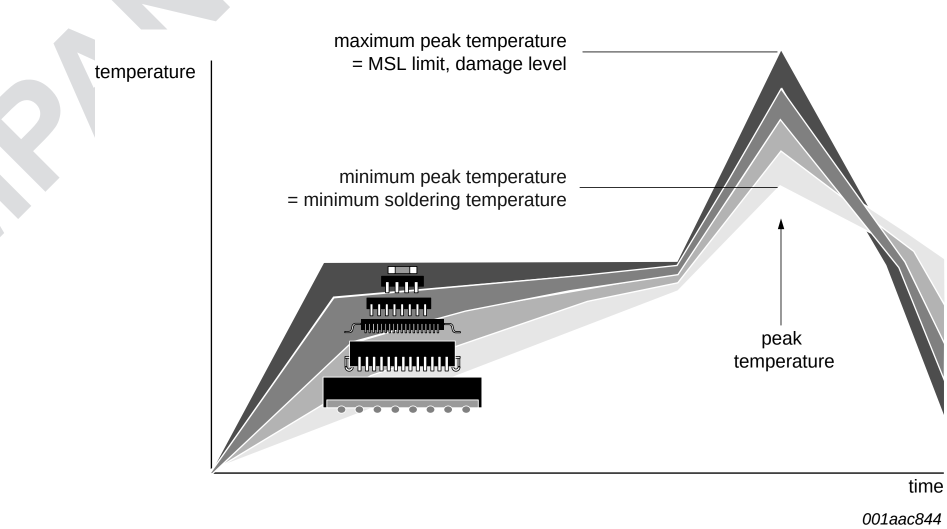
- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 31) than a SnPb process, thus reducing the process window
- Solder paste printing issues, such as smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature), and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic) while being low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 16.

Table 16. Lead-free process (from J-STD-020D)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm³)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 31.



MSL: Moisture Sensitivity Level

Fig 31. Temperature profiles for large and small components

For further information on temperature profiles, refer to application note *AN10365 “Surface mount reflow soldering description”*.

17.3.1 Stand off

The stand off between the substrate and the chip is determined by:

- The amount of printed solder on the substrate
- The size of the solder land on the substrate
- The bump height on the chip

The higher the stand off, the better the stresses are released due to TEC (Thermal Expansion Coefficient) differences between substrate and chip.

17.3.2 Quality of solder joint

A flip-chip joint is considered to be a good joint when the entire solder land has been wetted by the solder from the bump. The surface of the joint should be smooth and the shape symmetrical. The soldered joints on a chip should be uniform. Voids in the bumps after reflow can occur during the reflow process in bumps with high ratio of bump diameter to bump height, i.e. low bumps with large diameter. No failures have been found to be related to these voids. Solder joint inspection after reflow can be done with X-ray to monitor defects such as bridging, open circuits and voids.

17.3.3 Rework

In general, rework is not recommended. By rework we mean the process of removing the chip from the substrate and replacing it with a new chip. If a chip is removed from the substrate, most solder balls of the chip will be damaged. In that case it is recommended not to re-use the chip again.

Device removal can be done when the substrate is heated until it is certain that all solder joints are molten. The chip can then be carefully removed from the substrate without damaging the tracks and solder lands on the substrate. Removing the device must be done using plastic tweezers, because metal tweezers can damage the silicon. The surface of the substrate should be carefully cleaned and all solder and flux residues and/or underfill removed. When a new chip is placed on the substrate, use the flux process instead of solder on the solder lands. Apply flux on the bumps at the chip side as well as on the solder pads on the substrate. Place and align the new chip while viewing with a microscope. To reflow the solder, use the solder profile shown in application note *AN10365 “Surface mount reflow soldering description”*.

17.3.4 Cleaning

Cleaning can be done after reflow soldering.

18. Revision history

Table 17. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
NX20P5090 v1.0	<tbd>	Product data sheet	-	-

19. Legal information

19.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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