256Mb SEMPER™ Nano Flash

Quad SPI, 1.8 V

Device overview

- **Architecture**
  - Infineon 45-nm MIRRORBIT™ technology that stores two data bits in each memory array cell
  - Sector architecture
    - Uniform 128 KB (2bpc) sectors
    - Uniform 64 KB (1bpc) sectors
    - Configurable sector architecture options for 128 KB (2bpc) and 64 KB (1bpc) sectors
  - Page programming buffer of 256 or 512 bytes
  - OTP secure silicon array of 1024 bytes (32 × 32 bytes)
- **Interface**
  - SPI
    - Supports 1S-1S-1S protocols
    - Runs up to 13 MBps (104 MHz clock speed)
  - Quad
    - Supports 1S-1S-4S, 1S-4S-4S protocols
    - Runs up to 52 MBps (104 MHz clock speed)
- **Highlights**
  - Built-in error correcting code (ECC) corrects single-bit error and detects 2-bit error on memory array data
  - Ready Busy (RD/BY# = LOW) indicates that an internal event is ongoing
  - Hardware reset through CS# signaling method (JEDEC) or individual RESET# pin
- **Identification**
  - Serial flash discoverable parameters (SFDP) describing device functions and features
  - Device identification, manufacturer identification, and unique identification
- **Data integrity (100% ECC protection)**
  - Program-erase cycles
    - 1bpc sectors minimum 100K cycles
    - 2bpc sectors minimum 5K cycles
  - Data retention
    - 1bpc sector end of life minimum 0.28 year retention
    - 2bpc sector end of life minimum 25 years retention
- **Supply voltage**
  - 1.7-V to 2.0-V
- **Grade/temperature range**
  - Commercial (0°C to +70°C)
  - Industrial (–40°C to +85°C)
- **Packages**
  - Known good wafer (KGW) (Contact Sales)
  - 24-ball BGA 6 × 8 mm
  - Wafer level chip scale package (WLCSP)

Performance summary

Maximum read rates

Transaction	Clock rate (MHz)	MBps
SPI read	50	6.25
SPI fast read	80	10
	104	13
Quad output read	80	20
	104	52
Quad read SDR	80	20
	104	52

Typical program and erase rates

Operation	KBps
256B page programming	433
512B page programming	610
Sector erase (128 KB 2bpc) / (64 KB 1bpc)	194 / 91

Typical current consumption

Operation	Current (mA)
Read 80 MHz	17
Read 104 MHz	19
Program	29
Erase	27
Standby	0.005
Deep power down (DPD)	0.001

Data integrity

Program / erase (PE) endurance - Commercial (0°C to +70°C) Multi-pass Programming disabled[1]

Sectors size and configuration	Minimum PE cycles	Minimum retention time	Unit
128 KB 2bpc	5,000	25	Years
64 KB 1bpc	60,000	2	
	72,000	1	
	100,000	0.28	

Note
1. Data integrity is for use case with 100% ECC protection for the entire memory array, CFR3N[3] = 1 (Factory Default).

Program / erase (PE) endurance - Industrial (–40°C to +85°C) Multi-pass Programming disabled[2]

Sectors size and configuration	Minimum PE cycles	Minimum retention time	Unit
128 KB 2bpc	500	25	Years
	5,000	5	
64 KB 1bpc	10,000	5	
	50,000	0.5	
	100,000	0.05	

Program / erase (PE) endurance - Commercial (0°C to +70°C) Multi-pass Programming enabled[2]

Sectors size and configuration	Minimum PE cycles	Minimum retention time	Unit
128 KB 2bpc	1,000	25	Years
	5,000	1	
64 KB 1bpc	10,000	5	
	37,500	0.5	

Program / erase (PE) endurance - Industrial (–40°C to +85°C) Multi-pass Programming enabled[2]

Sectors size and configuration	Minimum PE cycles	Minimum retention time	Unit
128 KB 2bpc	500	10	Years
	5,000	0.5	
64 KB 1bpc	10,000	2	
	37,500	0.02	

Program / erase endurance non-volatile register array

Flash memory type	Minimum cycles	Minimum retention time	Unit
Non-volatile register array **Note** Each write transaction to a non-volatile register causes a PE cycle on the entire non-volatile register array.	500	25	Years

Note
2. Data integrity is for use case with <5% ECC protection is off for the entire memory array, CFR3N[3] = 0.

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1 Pinout

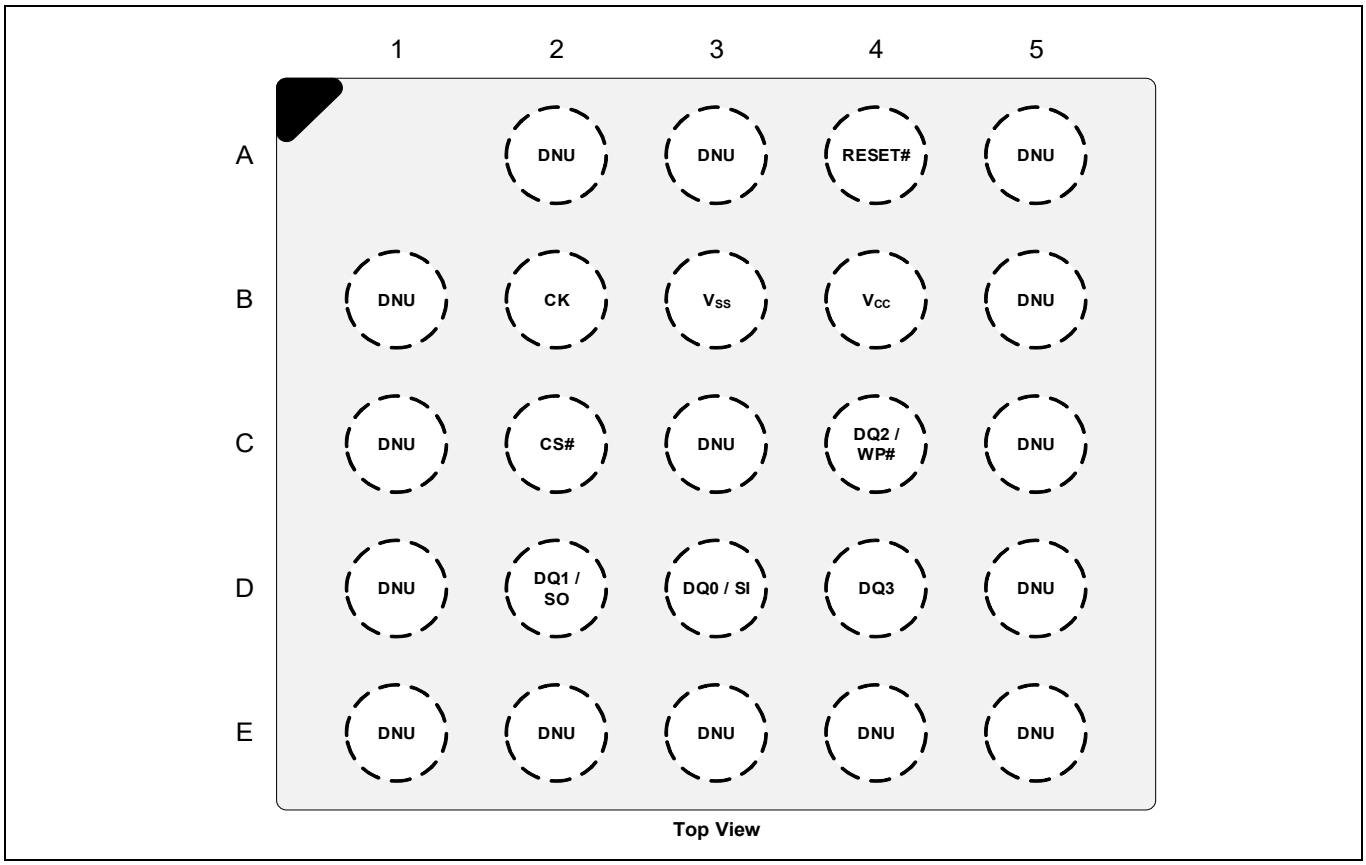


Figure 1 24-ball BGA pinout configuration[1, 2]

Notes
1. Flash memory devices in BGA packages can be damaged if exposed to ultrasonic cleaning methods.
2. The package, data integrity, or both may be compromised if the package body is exposed to temperatures above 150°C for prolonged periods of time.

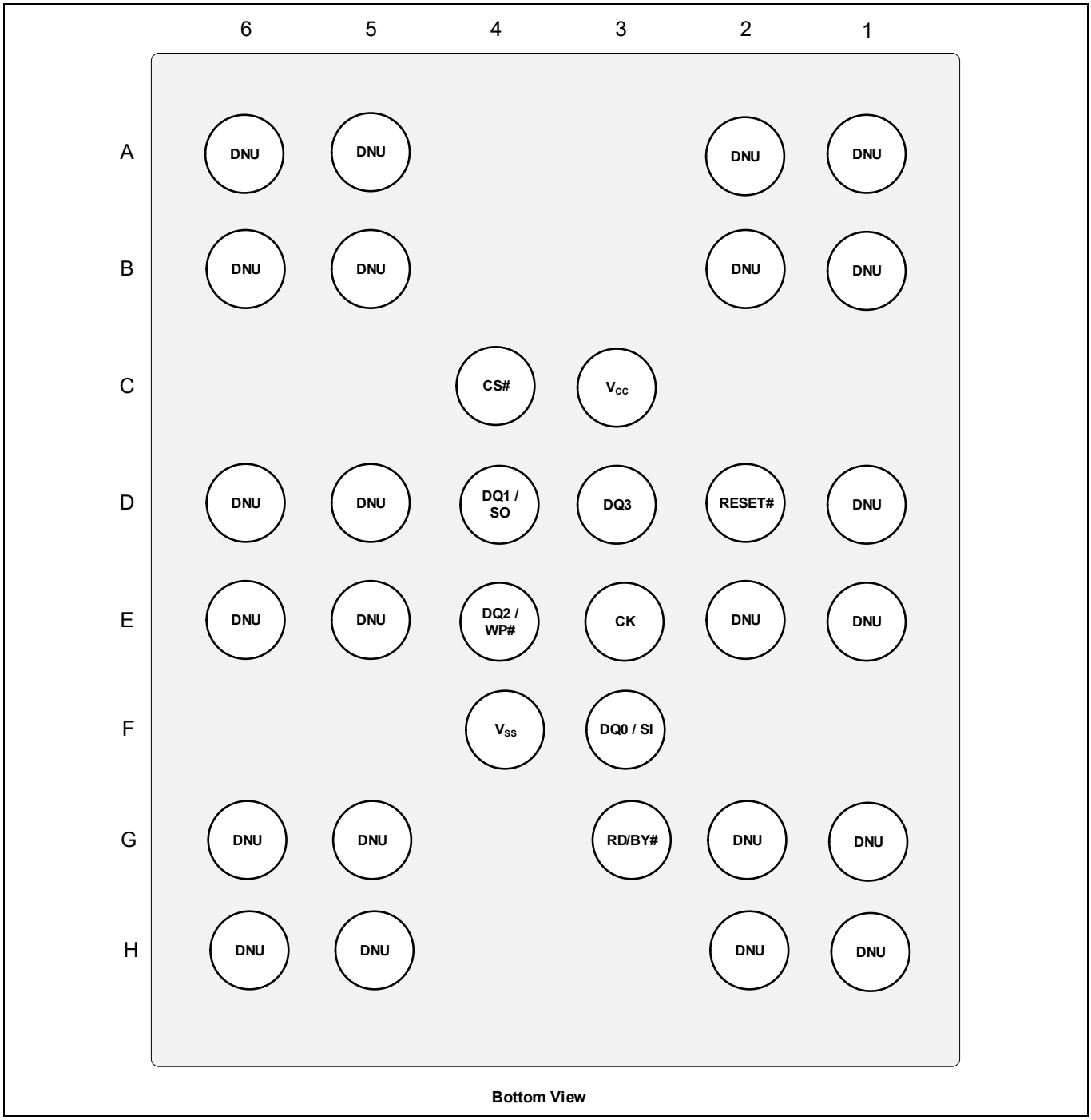


Figure 2 Wafer level chip scale package (WLCSP) pinout configuration[3]

Note
3. All DNU balls maybe connected to V_{SS} on PCB board.

2 Signal description

Table 1 Signal description

Symbol	Type	Mandatory / optional	Description
CS#	Input	Mandatory	**Chip Select (CS#)**. All bus transactions are initiated with a HIGH to LOW transition on CS# and terminated with a LOW to HIGH transition on CS#. Driving CS# LOW enables the device, placing it in the active mode. When CS# is driven HIGH, the device enters standby mode, unless an internal embedded operation is in progress. All other input pins are ignored and the output pins are put in high impedance state. On parts where the pin configuration offers a dedicated RESET# pin, it remains active when CS# is HIGH.
CK			**Clock (CK)**. Clock provides the timing of the serial interface. Transactions are latched on the rising edge of the clock. In SDR protocol, command, address and data inputs are latched on the rising edge of the clock, while data is output on the falling edge of the clock.
DQ0 / SI	Input / Output		Serial Input (SI) for single SPI protocol **DQ0 Input / Output** for Quad protocol
DQ1 / SO			Serial Output (SO) for single SPI protocol **DQ1 Input /Output** Quad protocol
DQ2 / WP#	Input / Output (Weak pull-up)		**Write Protect (WP#)** for single SPI protocol **DQ2 Input / Output** for Quad protocol The signal has an internal pull-up resistor and can be left unconnected in the host system if not used in Quad mode or write protection. If write protection is enabled, the host system is required to drive WP# HIGH or LOW during write register transactions.
DQ3	Input / Output		**DQ3 Input / Output** for Quad protocol
RESET#	Input (Weak pull-up)	Optional	**Hardware Reset (RESET#)**. When LOW, the device will self initialize and return to the array read state. DQ[3:0] are placed into the high impedance state when RESET# is LOW. RESET# includes a weak pull-up, meaning, if RESET# is left unconnected it will be pulled up to the HIGH state on its own.
RD/BY#	Output		Ready Busy (RD/BY# = LOW) indicates that an internal event is ongoing, RD/BY# is only supported on the WLCSP and KGD packages.
V_{CC}	Power Supply	Mandatory	Core power supply
V_{SS}	Ground Supply		Core ground
DNU	–	–	**Do Not Use**

3 Interface overview

3.1 General description

The S25FS256T device is CMOS, MIRRORBIT™ NOR Flash devices that support traditional SPI single-bit serial input and output, as well as four-bit wide Quad Output protocols. Read transactions use a linear burst reading the whole memory array.

The erased state of each memory bit is a logic 1. Programming changes a logic 1 (HIGH) to a logic 0 (LOW). Only an erase operation can change a memory bit from a 0 to a 1. An erase operation must be performed on a complete sector (64 KBs or 128 KBs).

The Page Programming Buffer used during a single programming operation is configurable to either 256 bytes or 512 bytes. The 512 byte option provides the highest programming throughput.

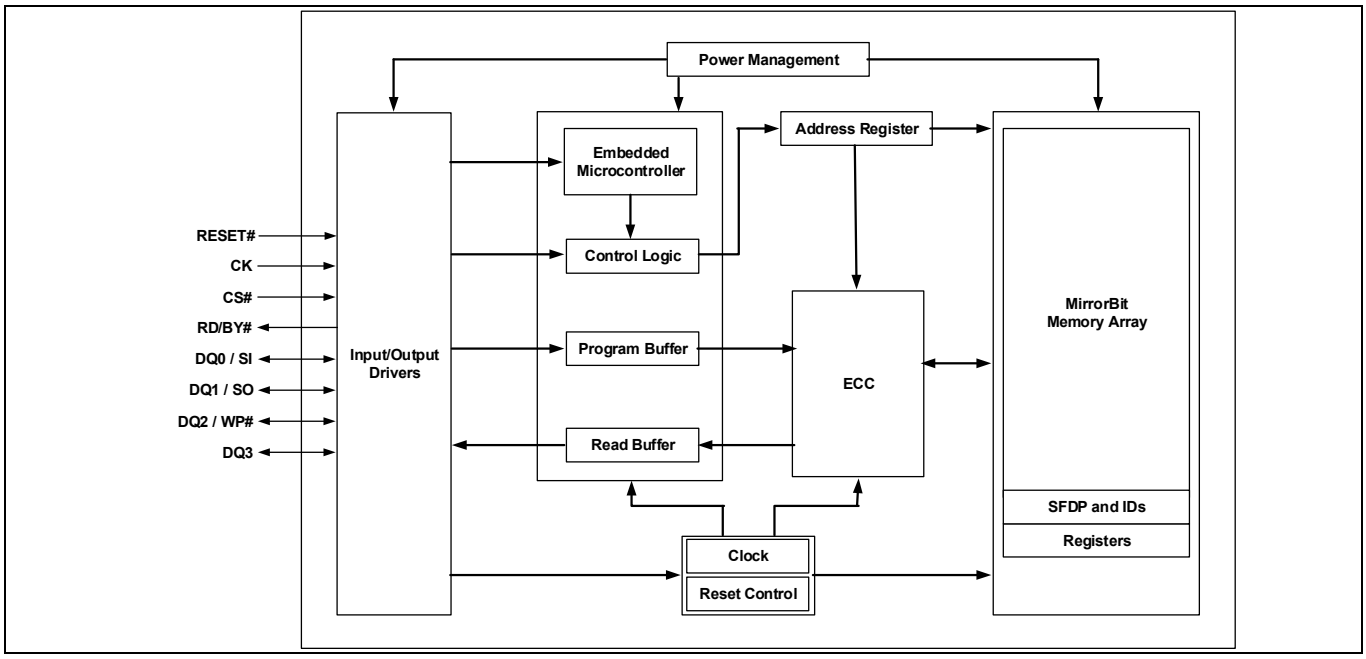


Figure 3 Logic block diagram

The device control logic is subdivided into two parallel operating sections: the Host Interface Controller (HIC) and the Embedded Algorithm Controller (EAC). The HIC monitors signal levels on the device inputs and drives outputs as needed to complete read, program, and write data transfers with the host system. The HIC delivers data from the currently entered address map on read transfers; places write transfer address and data information into the EAC command memory, and notifies the EAC of power transition, and write transfers. The EAC interrogates the command memory, after a program or write transfer, for legal command sequences and performs the related embedded algorithms.

Changing the non-volatile data in the memory array requires a sequence of operations that are part of embedded algorithms (EA). The algorithms are managed entirely by the internal EAC. The main algorithms perform programming and erase of the main flash array data. The host system writes command codes to the flash device. The EAC receives the command, performs all the necessary steps to complete the transaction, and provides status information during the progress of an EA.

The device supports error detection and correction by generating an embedded Hamming ECC during memory array programming.

The device has built-in diagnostic features providing the host system with the device status.

- Program and erase operation: Reporting of program or erase success, failure and suspend status.
- Error 2-bit detection and 1-bit correction.
- Sector Erase Status: Reporting of erase success or failure status per sector.

3.2 Signal protocols

3.2.1 Clock modes

The S25FS256T device can be driven by an embedded microcontroller (bus master) in either of the following two clocking modes:

- **Mode 0** with Clock Polarity LOW at the fall of CS# and staying LOW until it goes HIGH at capture input.
- **Mode 3** with Clock Polarity HIGH at the fall of CS# then going LOW to HIGH at capture input.

For these two modes, data is latched into the device on the rising edge of the CK signal. The output data is available on the falling edge of the CK clock signal. The difference between the two modes is the clock polarity when the bus master is in Standby mode and not transferring any data.

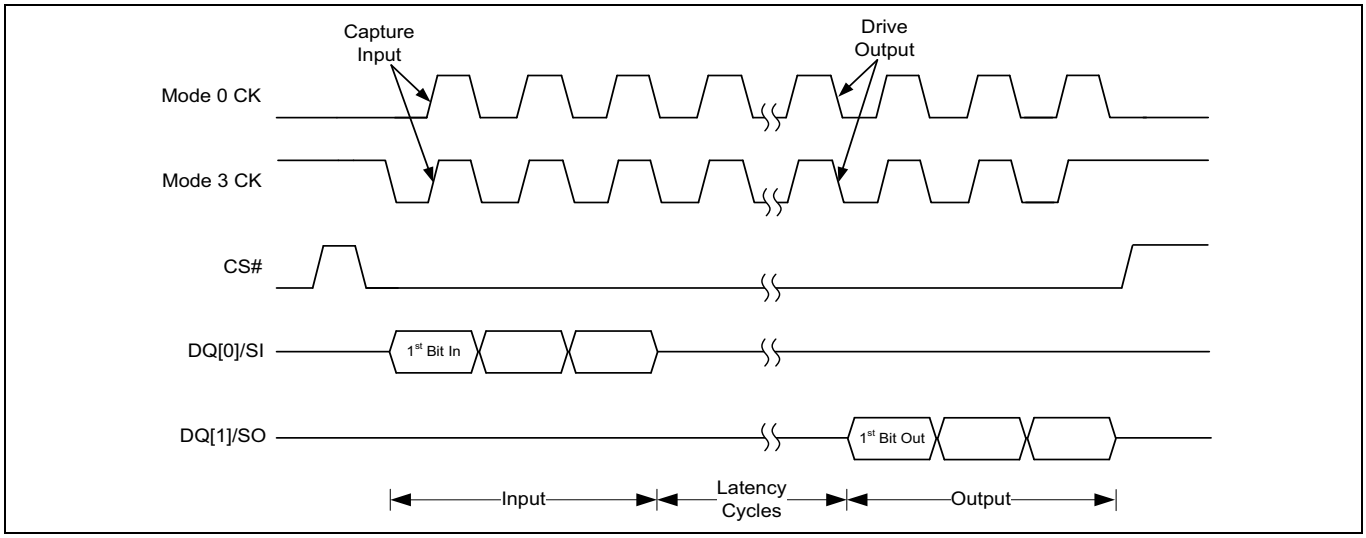


Figure 4 SPI SDR mode support

3.3 Transaction protocol

Transaction

- During the time that CS# is active (LOW) the clock signal (CK) is toggled while command information is first transferred on the data (DQ) signals followed by address and data from the host to the flash device. The clock continues to toggle during the transfer of read data from the flash device to the host or write data from the host to the flash device. When the host has transferred the desired amount of data, the host drives the CS# inactive (HIGH). The period during which CS# is active is called a transaction on the bus.
- While CS# is inactive, the CK is not required to toggle.
- The command transfer occurs at the beginning of every transaction. The address, latency cycles, and data transfer phases are optional and their presence depends on the protocol mode or command transferred.

Transaction capture

- CK marks the transfer of each bit or group of bits between the host and memory. Command, address and write data bits transfer occurs on CK rising edge in SDR transactions.

Note All attempts to read the flash memory array during a program or erase (embedded operations) are ignored. The embedded operation will continue to execute without any effect. A very limited set of commands are accepted during an embedded operation. These are discussed in **"Suspend and resume embedded operation" on page 32**.

Protocol terminology

- The number of DQ signals used during the transaction, depends on the current protocol mode or command transferred. The latency cycles do not use the DQ signals for information transfer. The protocol mode options are described by the data rate and the DQ width (number of DQ signals) used during the command, address, and data phases in the following format:

  WR-WR-WR, where:
  - The first WR is the command bit width and rate.
  - The second WR is the address bit width and rate.
  - The third WR is the data bit width and rate.
- Examples:
  - 1S-1S-1S means that the command is 1 bit wide SDR, the address is 1 bit wide SDR, and the data is one bit wide SDR.
  - 1S-1S-4S means that the command and address are SDR 1 bits wide with data transfers are 4 bits wide SDR.

Protocols definition

- Protocol Modes:

1. 1S-1S-1S: One DQ signal used during command transfer, address transfer, and data transfer. All phases are SDR.
2. 1S-1S-4S: One DQ signal used during command and address transfer, four DQ signals used during data transfer. All phases are SDR.
3. 1S-4S-4S: One DQ signal used during command transfer, four DQ signals used during address transfer, and data transfer. All phases are SDR.

- Each transaction begins with an 8-bit (1-byte) command. The command selects the type of information transfer or device operation to be performed.
- All protocols supports 3 or 4-byte addressing.

1S-1S-1S protocol (single input/output, SIO)

- The 1S-1S-1S mode is the preferred default protocol following Power-on-Reset (POR).
- This protocol uses DQ[0]/SI to transfer information from host to flash device and DQ[1]/SO to transfer information from flash device to host. On each DQ, information is placed on the DQ line in Most Significant bit (MSb) to Least Significant bit (LSb) order within each byte. Sequential address bytes are transferred in highest order to lowest order sequence. Sequential data bytes are transferred in lowest address to highest address order.
- In 1S-1S-1S, DQ[3:2] are not used for data transfer period and will be high impedance.

1S-1S-4S protocol (quad output read, QOR)

- This protocol uses DQ[3:0] signals. The 8-bit command and address placed on the DQ[0] in MSb to LSb order. Sequential data bytes in SDR are transferred in lowest address to highest address order.

1S-4S-4S protocol (quad input/output)

- This protocol uses DQ[3:0] signals. The 8-bit command placed on the DQ[0] in MSb to LSb order. The LSb of address byte is placed on DQ[0] with each higher order bit on the successively higher numbered DQ signals. Sequential address bytes are transferred in highest order to lowest order sequence. Sequential data bytes in SDR are transferred in lowest address to highest address order. **"Serial peripheral interface (SPI, 1S-1S-1S)"** on page 13 through **"QIP SDR program transaction with command, address, and data input"** on page 15 show all transaction formats by protocol mode.

3.3.1 Serial peripheral interface (SPI, 1S-1S-1S)

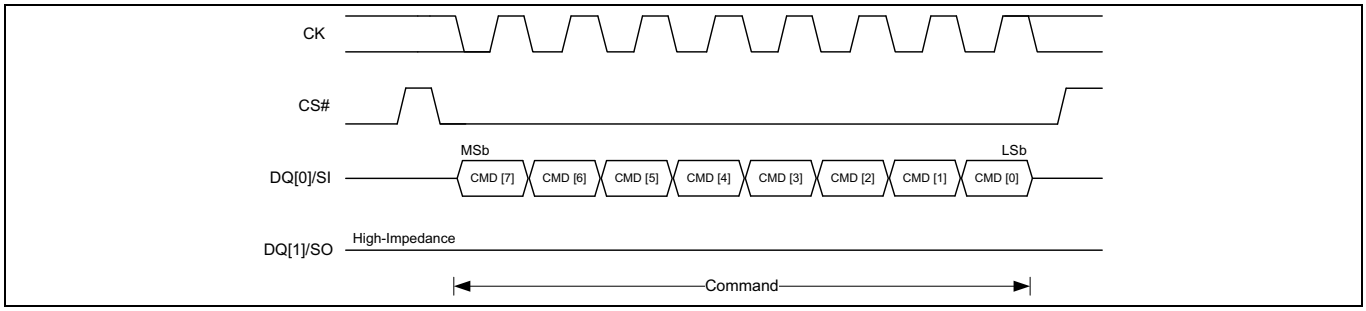


Figure 5 SPI transaction with command input

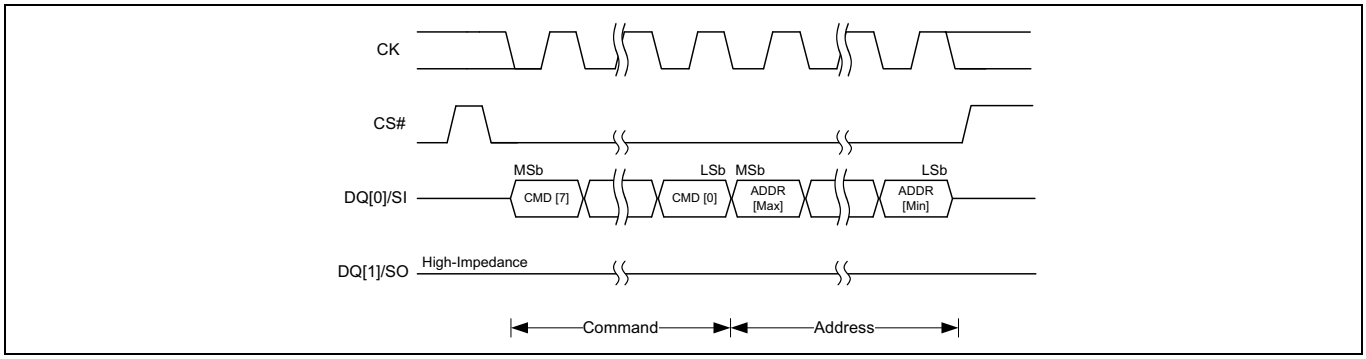


Figure 6 SPI transaction with command and address input

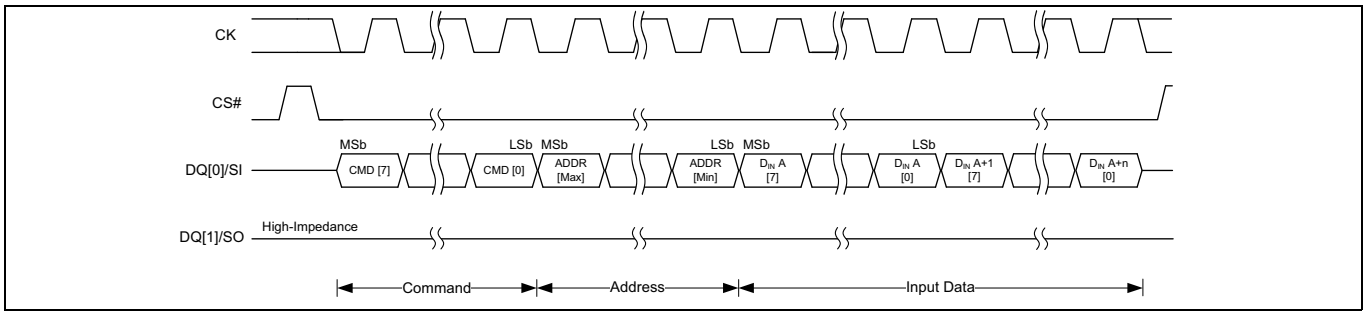


Figure 7 SPI program transaction with command, address, and data input

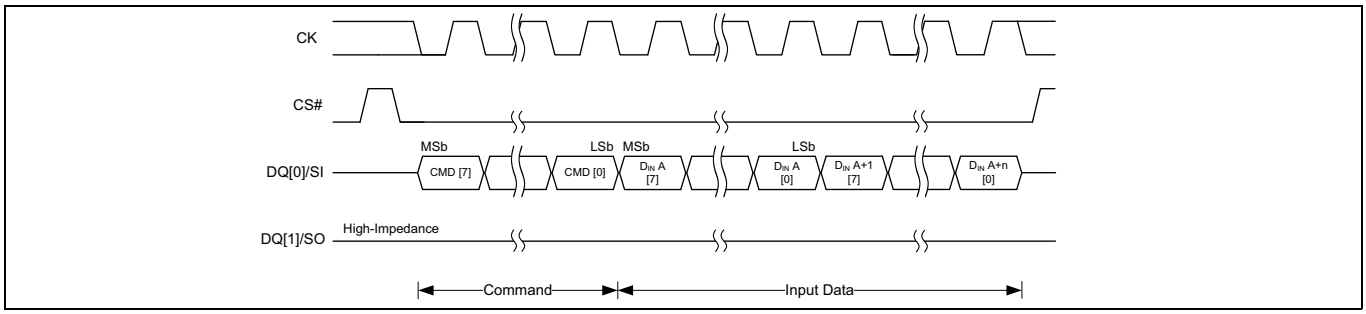


Figure 8 SPI program transaction with command and data input

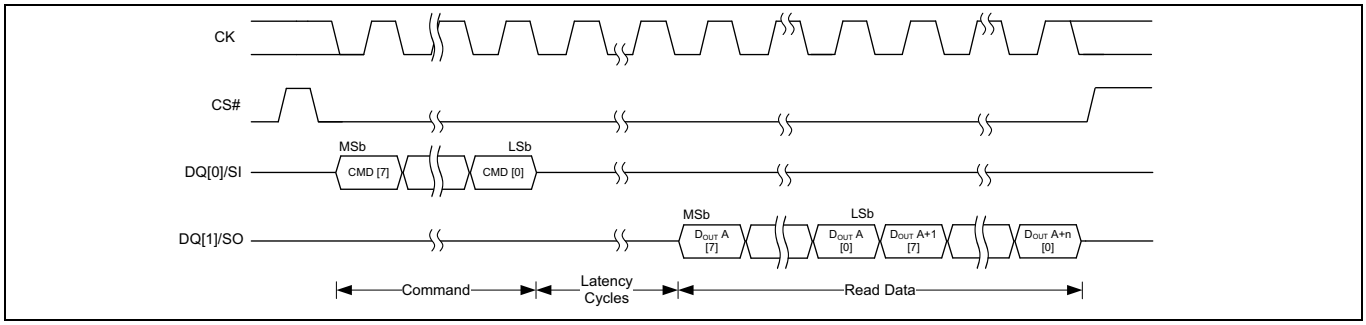


Figure 9 SPI read transaction with command input (Output latency)[4]

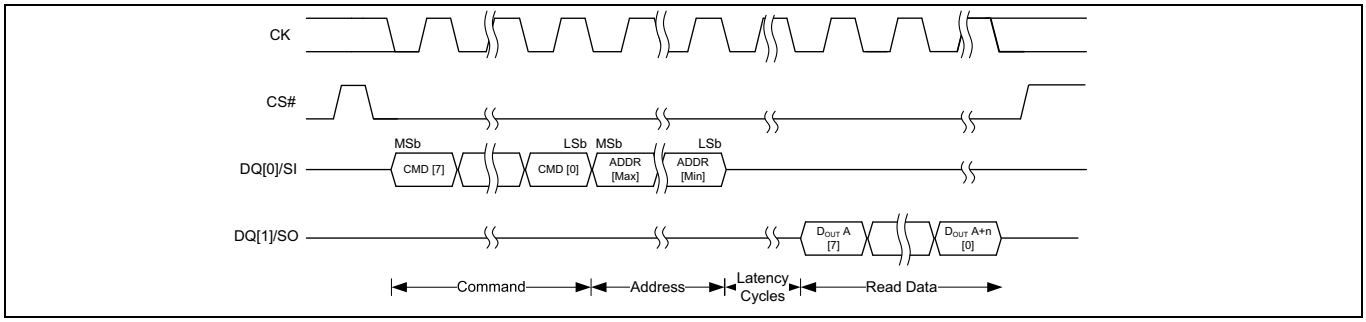


Figure 10 SPI read transaction with command and address input (Output latency)

Note
4. In case of Status Register 1 and 2, Read Byte data out is the updated status.

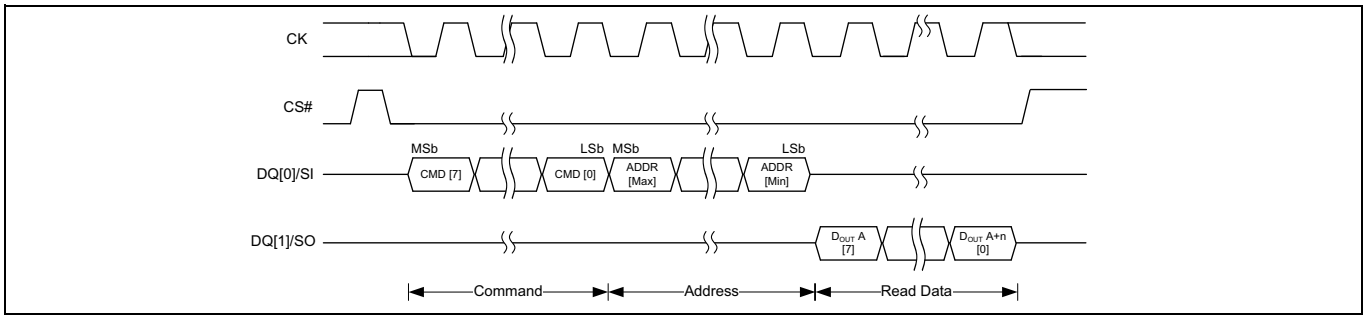


Figure 11 SPI read transaction with command and address input (No output latency)

3.3.2 Quad output read SPI (QOR, 1S-1S-4S)

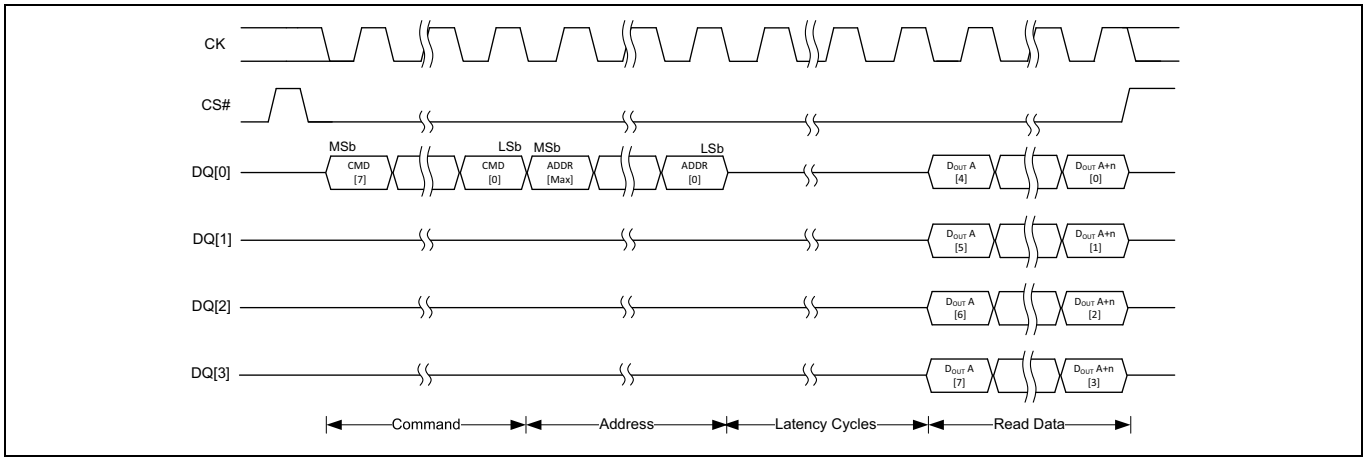


Figure 12 QOR SDR read transaction with command, address input (Output latency)

3.3.3 Quad input program SPI (QIP, 1S-1S-4S)

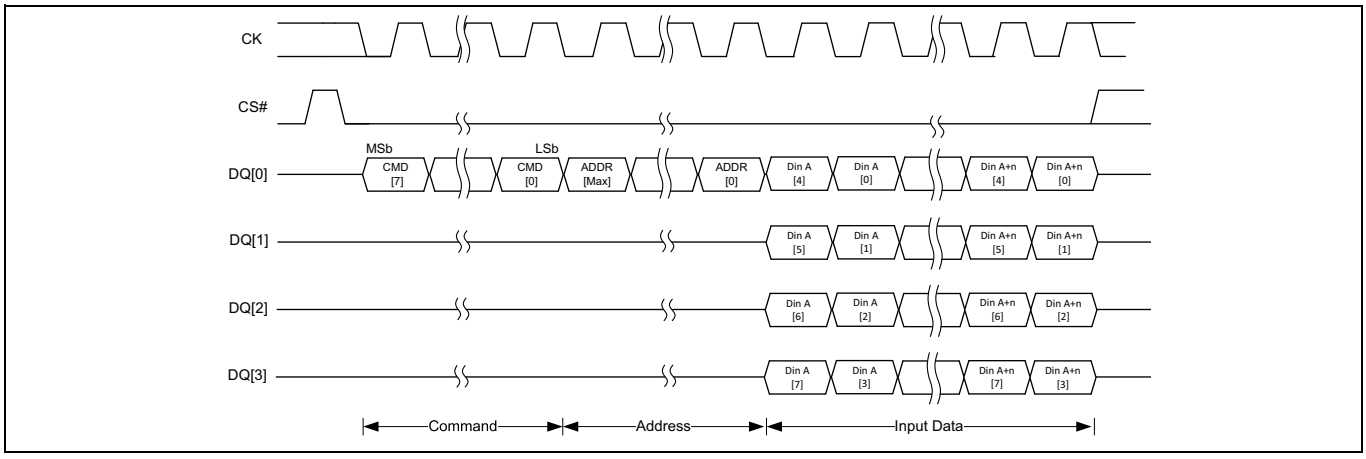


Figure 13 QIP SDR program transaction with command, address, and data input

3.3.4 Quad IO SPI (QIO, 1S-4S-4S)

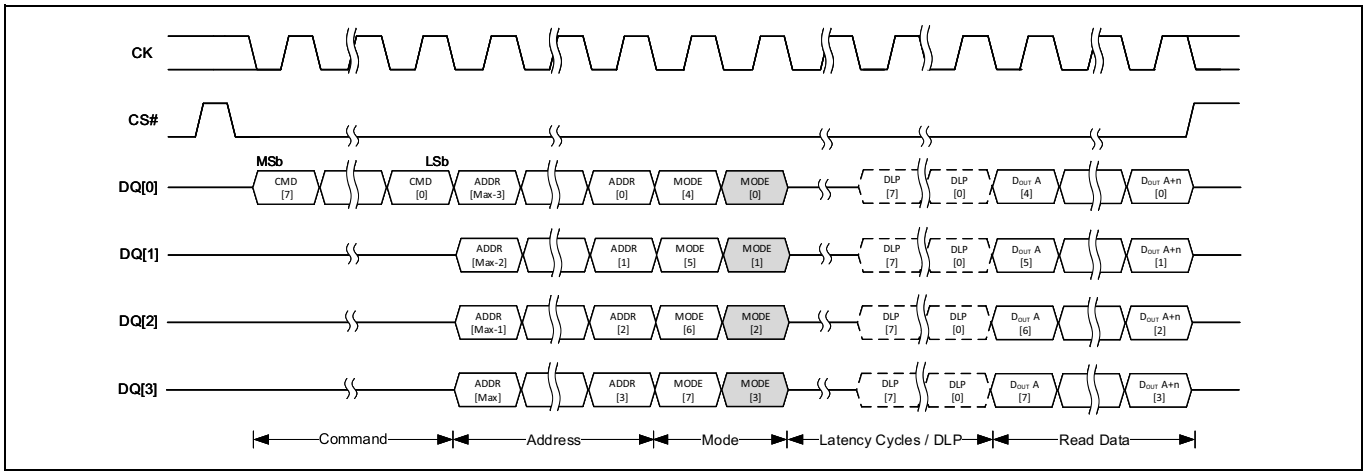


Figure 14 QIO SDR read transaction with command, address and mode input (Output latency)[5]

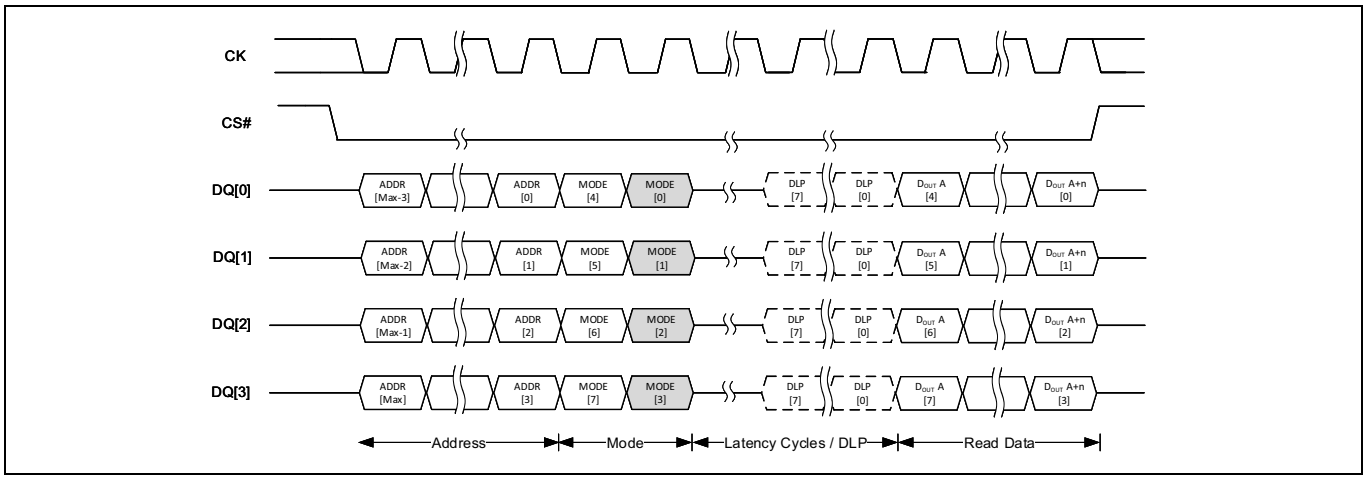


Figure 15 QIO SDR continuous read transaction with address and mode input (Output latency)[5]

Note
5. The gray bits data is don't care.

3.3.5 Register naming convention

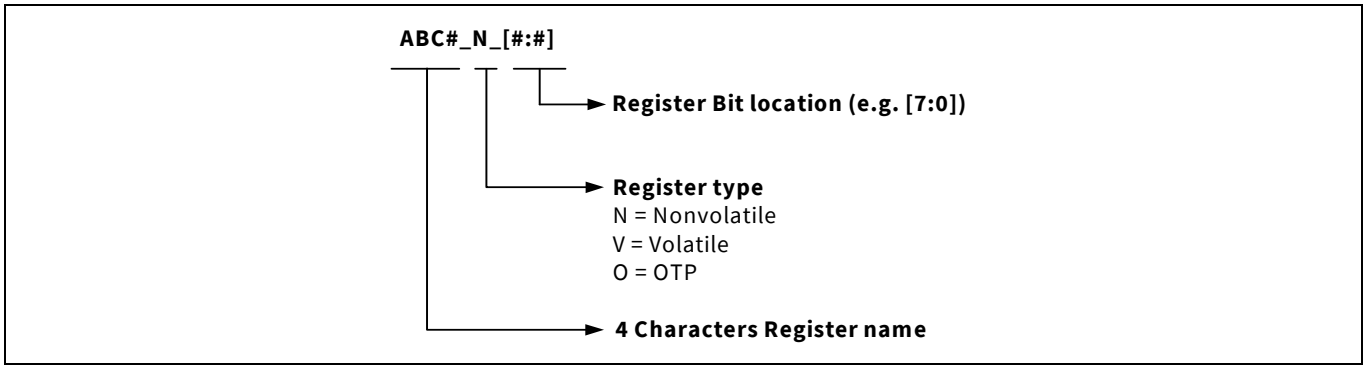


Figure 16 Register naming convention

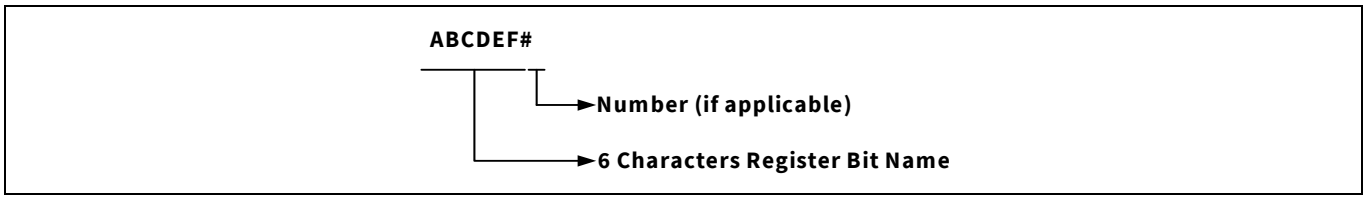


Figure 17 Register bit naming convention

3.3.6 Transaction naming convention

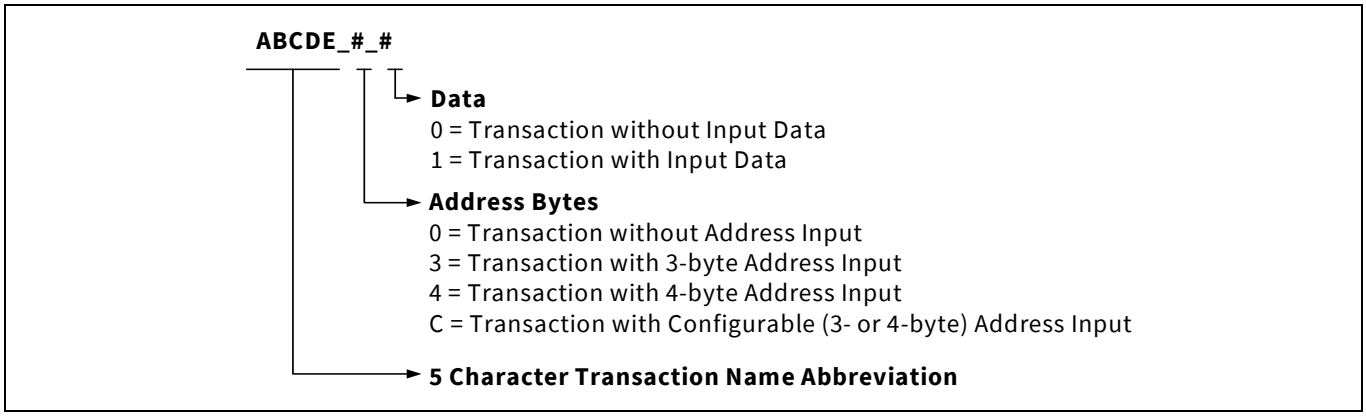


Figure 18 Transaction naming convention

4 Address space maps

The device supports 24-bit (3-byte) as well as 32-bit (4-byte) addresses. 4-byte addresses allow direct addressing of up to 4 GB (32 Gb) address space. The address byte option can be changed by writing the respective configuration registers OR there are separate transactions also available to enter (EN4BA_0_0) and exit (EX4BA_0_0) the 4-byte address mode.

Besides Flash memory array, The device includes separate address spaces for Manufacturer ID, Device ID, Unique ID, Serial Flash Discoverable Parameters (SFDP), Secure Silicon Region (SSR) and Registers.

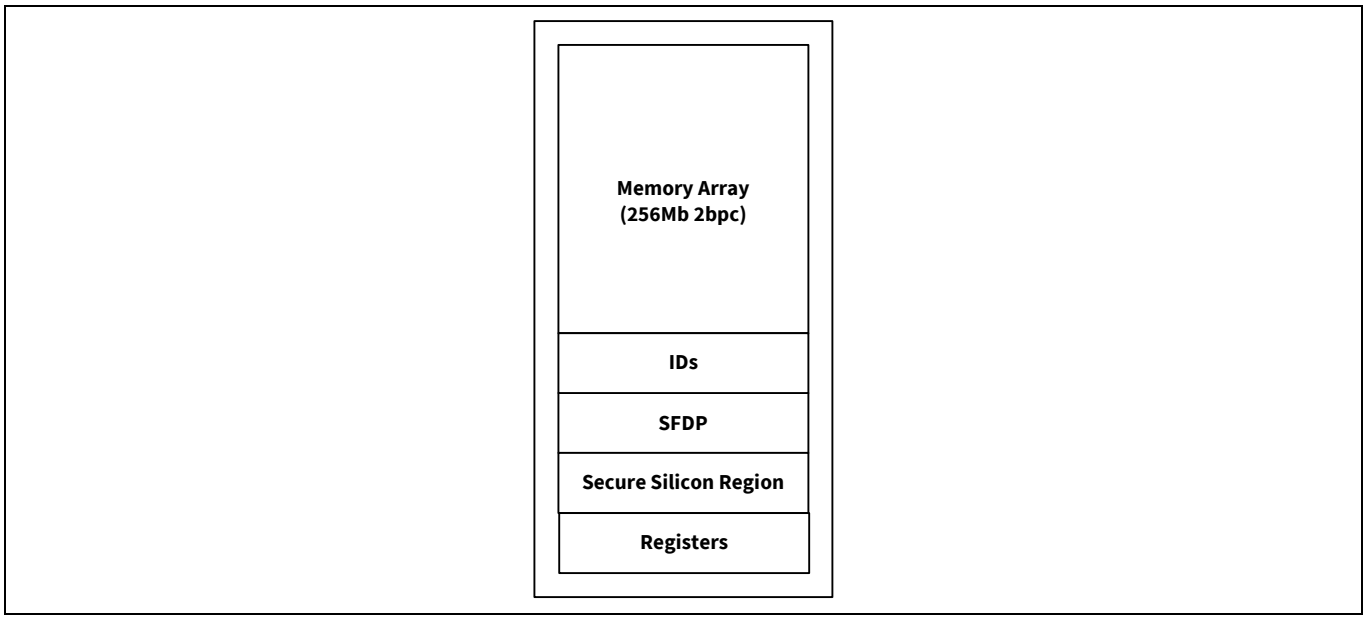


Figure 19 Quad device address space map overview

4.1 Flash memory array

The main flash array is divided into units called physical sectors. The device sector architecture has 16 configuration options, with selection of sectors in 128 KB 2bpc (bits per cell) or 64 KB 1bpc. The combination of the sector architecture selection bits in Architecture Configuration Register support the different sector architecture options of the device. See **"Architecture Configuration Register (ARCFN)"** on page 62 for more information. Configuration option 8–15 are reserved for future use.

4.1.1 Sector architecture configuration options

Table 2 Option 0 256 Mb (256 - 128 KB sectors) address map

Sector size (KB)	Sector count	Sector range	Byte address range (Sector starting address–Sector ending address)
128	256	SA00	00000000h–0001FFFFh
		:	:
		SA255	01FE0000h–01FFFFFFh

Table 3 Option 1: 240 Mb (223 - 128 KB, 32 - 64 KB, 1 - 128 KB sectors) address map

Sector size (KB)	Sector count	Sector range	Byte address range (Sector starting address–Sector ending address)
128	223	SA00	00000000h–0001FFFFh
		:	:
		SA222	01BC0000h–01BDFFFFh
64	32	SA223	01BE0000h–01BEFFFFh
		:	:
		SA254	01DD0000h–01DDFFFFh
128	1	SA255	01DE0000h–01DFFFFFh

Table 4 Option 2: 240 Mb (3 - 128 KB, 32 - 64 KB, 221 - 128 KB sectors) address map

Sector size (KB)	Sector count	Sector range	Byte address range (Sector starting address–Sector ending address)
128	3	SA00	00000000h–0001FFFFh
		SA01	00020000h–0003FFFFh
		SA02	00040000h–0005FFFFh
64	32	SA03	00060000h–0006FFFFh
		:	:
		SA34	00250000h–0025FFFFh
128	221	SA35	00260000h–0027FFFFh
		:	:
		SA255	01DE0000h–01DFFFFFh

Table 5 Option 3: 224 Mb (190 - 128 KB, 64 - 64 KB, 2 - 128 KB sectors) address map

Sector size (KB)	Sector count	Sector range	Byte address range (Sector starting address–Sector ending address)
128	190	SA00	00000000h–0001FFFFh
		:	:
		SA189	017A0000h–017BFFFFh
64	64	SA190	017C0000h–017CFFFFh
		:	:
		SA253	01BB0000h–01BBFFFFh
128	2	SA254	01BC0000h–01BDFFFFh
		SA255	01BE0000h–01BFFFFFh

Table 6 Option 4: 242 Mb (3 - 128 KB, 2 - 64 KB, 224 - 128 KB, 26 - 64 KB, 1 - 128 KB sectors) address map

Sector size (KB)	Sector count	Sector range	Byte address range (Sector starting address–Sector ending address)
128	3	SA00	00000000h–0001FFFFh
		SA01	00020000h–0003FFFFh
		SA02	00040000h–0005FFFFh
64	2	SA03	00060000h–0006FFFFh
		SA04	00070000h–0007FFFFh
128	224	SA05	00080000h–0009FFFFh
		:	:
		SA228	01C60000h–01C7FFFFh
64	26	SA229	01C80000h–01C8FFFFh
		:	:
		SA254	01E10000h–01E1FFFFh
128	1	SA255	01E20000h–01E3FFFFh

Table 7 Option 5: 242 Mb (220 - 128 KB, 2 - 64 KB, 7 - 128 KB, 26 - 64 KB, 1 - 128 KB sectors) address map

Sector size (KB)	Sector count	Sector range	Byte address range (Sector starting address–Sector ending address)
128	220	SA00	00000000h–0001FFFFh
		:	:
		SA219	01B60000h–01B7FFFFh
64	2	SA220	01B80000h–01B8FFFFh
		SA221	01B90000h–01B9FFFFh
128	7	SA222	01BA0000h–01BBFFFFh
		:	:
		SA228	01C60000h–01C7FFFFh
64	26	SA229	01C80000h–01C8FFFFh
		:	:
		SA254	01E10000h–01E1FFFFh
128	1	SA255	01E20000h–01E3FFFFh

Table 8 Option 6: 239 Mb (4 - 128 KB, 8 - 64 KB, 216 - 128 KB, 26 - 64 KB, 1 - 128 KB sectors) address map

Sector size (KB)	Sector count	Sector range	Byte address range (Sector starting address–Sector ending address)
128	4	SA00	00000000h–0001FFFFh
		:	:
		SA03	00060000h–0007FFFFh
64	8	SA04	00080000h–0008FFFFh
		:	:
		SA11	000F0000h–000FFFFFh
128	216	SA12	00100000h–0011FFFFh
		:	:
		SA227	01BE0000h–01BFFFFFh
64	26	SA228	01C00000h–01C0FFFFh
		:	:
		SA253	01D90000h–01D9FFFFh
128	2	SA254	01DA0000h–01DBFFFFh
		SA255	01DC0000h–01DDFFFFh

Table 9 Option 7: 238 Mb (4 - 128 KB, 36 - 64 KB, 221 - 116 KB sectors) address map

Sector size (KB)	Sector count	Sector range	Byte address range (Sector starting address–Sector ending address)
128	4	SA00	00000000h–0001FFFFh
		:	:
		SA03	00060000h–0007FFFFh
64	36	SA04	00080000h–0008FFFFh
		:	:
		SA39	002B0000h–002BFFFFh
128	216	SA40	002C0000h–002DFFFFh
		:	:
		SA255	01DA0000h–01DBFFFFh

4.2 ID address space

This particular region of the memory is assigned to manufacturer, device, and unique identification:

- The manufacturer identification is assigned by JEDEC.
- The device identification is assigned by Infineon.
- A 64-bit unique number is located in eight bytes of the Unique Device ID address space. This Unique ID can be used as a software readable serial number that is unique for each device.

There is no address space defined for these IDs as they can be read by providing the respective transactions only. The transactions do not need the address to read these IDs. The data in this address space is read-only data.

4.3 JEDEC JESD216 SFDP space

The SFDP standard provides a consistent method of describing the functional and feature capabilities of this serial flash device in a standard set of internal parameter tables. These parameter tables can be interrogated by host system software to enable adjustments needed to accommodate divergent features. The SFDP address space has a header starting at address zero that identifies the SFDP data structure and provides a pointer to each parameter. The SFDP address space is programmed by Infineon and read-only for the host system.

Table 10 SFDP overview address map

Byte address	Description
0000h	Location zero within JEDEC JESD216C SFDP space - start of SFDP header
,,,	Remainder of SFDP header followed by undefined space
0100h	Start of SFDP parameter tables The SFDP parameter table data starting at 0100h
...	Remainder of SFDP parameter tables followed by either more parameters or undefined space

4.4 SSR address space

Each S25FS256T memory device has a 1024-byte Secure Silicon Region which is OTP address space. This address space is separate from the main flash array. The SSR area is divided into 32 individually lockable, 32-byte aligned and length regions.

In the 32-byte region starting at address zero:

- The sixteen lowest bytes contain a 128-bit random number. The random number cannot be written to, erased or programmed and any attempts will return an PRGERR flag.
- The next four bytes are used to provide one bit per secure region (32 bits in total) to permanently protect once set to ‘0’ from writing, erasing or programming.
- All other bytes are reserved.

The remaining regions are erased when shipped from Infineon, and are available for programming of additional permanent data.

Table 11 SSR address map

Region	Byte address range	Contents	Initial delivery state
Region 0	000h	LSB of Infineon programmed random number	Infineon programmed random number
	...	...	
	00Fh	MSB of Infineon programmed random number	
	010h to 013h	Region locking bits Byte 10h [bit 0] locks region 0 from programming when = 0 ... Byte 13h [bit 7] locks region 31 from programming when = 0	All bytes = FFh
	014h to 01Fh	Reserved for future use (RFU)	All bytes = FFh
Region 1	020h to 03Fh	Available for user programming	All bytes = FFh
Region 2	040h to 05Fh	Available for user programming	All bytes = FFh
...	...	Available for user programming	All bytes = FFh
Region 31	3E0h to 3FFh	Available for user programming	All bytes = FFh

4.5 Registers

Registers are small groups of memory cells used to configure how the S25FS256T device operates, or to report the status of device operations. The registers are accessed by specific commands and addresses. **Table 12** shows the address map for every available register in this flash memory device.

Table 12 Register address map

Function	Register type	Register name	Volatile component address (hex)	Non-volatile component address (hex)
Device status	Status Register 1	STR1N[7:0], STR1V[7:0]	0x00800000	0x00000000
	Status Register 2	STR2V[7:0]	0x00800001	N/A
Device configuration	Configuration Register 1	CFR1N[7:0], CFR1V[7:0]	0x00800002	0x00000002
	Configuration Register 2	CFR2N[7:0], CFR2V[7:0]	0x00800003	0x00000003
	Configuration Register 3	CFR3N[7:0], CFR3V[7:0]	0x00800004	0x00000004
	Configuration Register 4	CFR4N[7:0], CFR4V[7:0]	0x00800005	0x00000005
	Architecture Configuration Register	ARCFN[7:0]	N/A	0x00000006
Error correction	ECC Status Register	ESCV[7:0]	0x00800089	N/A

5 Features

5.1 Read

The device supports different read transactions to access different memory maps, namely: Read Memory array, Read Device Identification, Read Register.

These read transactions can use any protocol mentioned in **"Transaction protocol"** on page 12.

The read transactions require latency cycles set by (CFR2V[2:0]) following the address to allow time to access the memory array (except RDAY1_4_0 and RDAY1_C_0 of 1S-1S-1S protocol).

If the inputted address is pass the array boundary, the data out is zeros.

5.1.1 Read Identification transactions

There are identification transactions, each support SPI protocols (see **Table 48**).

5.1.1.1 Read Device Identification transaction

The Read Device Identification (RDIDN_0_0) transaction provides read access to manufacturer identification and device identification. The transaction uses no latency cycles to enable maximum clock frequency of 104 MHz.

5.1.1.2 Read SFDP transaction

The Read Serial Flash Discoverable Parameters (RSFDP_3_0) transaction provides access to the JEDEC SFDP (see **Table 48**). The transaction uses a 3-byte address scheme. If a non-zero address is set, the selected location in the SFDP space is the starting point of the data read. This enables random access to any parameter in the SFDP space. Continuous (sequential) read is supported with the RSFDP_3_0 transaction. Eight latency cycles are required. The maximum clock frequency for the Read SFDP transaction is 50 MHz.

5.1.1.3 Read Unique Identification transaction

Read Unique Identification (RDUID_0_0) transaction is similar to Read Device Identification transaction, but accesses a different 64-bit number which is unique to each device. It is factory programmed. The transactions require 8 latency cycles.

5.1.1.4 Read Identification related register and transaction

Table 13 Read Identification related registers and transactions

Related registers	Related SPI transactions (See Table 48)
N/A	Read Identification (RDIDN_0_0)
	Read Serial Flash Discoverable (RSFDP_3_0)
	Read Unique Identification (RDUID_0_0)

5.1.2 Read memory array transactions

Memory array data can be read from the memory starting at any byte boundary. Data bytes are sequentially read from incrementally higher byte addresses until the host ends the data transfer by driving CS# input HIGH. If the byte address reaches the maximum address of the memory array, the read will continue at address zero of the array.

5.1.2.1 SPI read and read fast transactions

The SPI Read SDR and Read Fast SDR transactions (1S-1S-1S) are supported for Host systems that require backward compatibility to legacy SPI. Read Fast SDR transaction is available with 3- or 4-byte address options. The Read transaction is for maximum clock frequency of 50 MHz and requires no latency cycles. The Fast Read Transaction uses latency cycles set by (CFR2V[2:0]) to enable maximum clock frequency of 104 MHz (see **Table 48**).

5.1.2.2 Read SDR quad output transaction

The Read SDR quad output transaction uses the SDR quad output (1S-1S-4S) protocol. It supports 3- or 4-byte address options. This transaction uses latency cycles set by (CFR2V[2:0]) to enable maximum 104 MHz clock frequency (see **Table 49**).

5.1.2.3 Read SDR quad I/O transaction

The Read SDR quad I/O transaction uses the SDR Quad I/O (1S-4S-4S) protocol.The transaction also support the mode bits and continuous read transactions. They support 3- or 4-byte address options. This transaction latency cycles set by (CFR2V[2:0]) to enable maximum 104 MHz clock frequency (see **Table 50**).

The Quad I/O transaction has continuous read mode bits that follow the address so, a series of Read transactions can eliminate the eight-bit command after the first Read command sends a mode bit pattern of Axh that indicates the following transaction will also be a Read command. The first Read command in a series starts with the 8-bit command, followed by address, followed by mode bits, followed by an latency period. If the mode bit pattern is Axh the next transaction is assumed to be an additional Read transaction that does not provide command bits. That transaction starts with address, followed by mode bits, followed by latency. Then the memory contents, at the address given, are shifted out.

5.1.2.4 Read memory array related registers and transactions

Table 14 Read memory array related registers and transactions

Related registers	Related SPI transactions (See Table 48)	Related Quad output transactions (See Table 49)
Configuration Register 2 (CFR2N, CFR2V) (see **Table 42**)	Read SDR (RDAY1_4_0, RDAY1_C_0)	Read SDR Quad Output (RDAY4_4_0, RDAY4_C_0) Read SDR Quad I/O (RDAY5_4_0, RDAY5_C_0)
	Read Fast SDR (RDAY2_C_0)	

5.1.3 Read registers transactions

There are multiple registers for reporting embedded operation status or controlling device configuration options. Registers contain both volatile and non-volatile bits. There are two ways to read the Registers. The Read Any Register transaction provides a way to read all device registers: non-volatile and volatile by address selection. There are also dedicated Register Read transactions, which are defined per register and only read the contents of that register.

5.1.3.1 Read Any Register

The Read Any Register (RDARG_C_0) transaction is the best way to read all device registers, both non-volatile and volatile. The transaction includes the address of the register to be read. This is followed by latency cycles set by (CFR2V[2:0]) for reading non-volatile registers and no latency cycles for reading volatile registers. Then, the selected register contents are returned. If the read access is continued, the same addressed register contents are returned until the transaction is terminated; only one byte register location is read by each RDARG_C_0 transaction. For registers with more that one byte of data, the RDARG_C_0 transaction must again be used to read each byte of data.

The maximum clock frequency for the RDARG_C_0 transaction is 104 MHz.

The RDARG_C_0 transaction can be used during embedded operations to read Status Register 1 (STR1V). Reading undefined locations provides undefined data.

5.1.3.2 Read Status Registers transaction

The Read Status Register (RDSR1_0_0, RDSR2_0_0) transactions allow the Status Registers' volatile contents to be read. The transaction uses no latency cycles. The maximum clock frequency of 104 MHz.

The volatile version of Status Registers contents can be read at any time, even while a program, erase, or write operation is in progress.

It is possible to read Status Register 1 continuously by providing multiples of eight clock cycles. The status is updated for each eight cycle read.

5.1.3.3 Read Configuration Register transaction

The Read Configuration Register 1 (RDCR1_0_0) transaction allows the Configuration registers volatile contents be read. The transaction uses no latency cycles. The maximum clock frequency of 104 MHz.

The volatile version of Configuration Register 1 contents can be read at any time, even while a program, erase, or write operation is in progress.

It is possible to read Configuration Register 1 continuously by providing multiples of eight clock cycles. The status is updated for each eight cycle read.

5.1.3.4 Read ECC Data Unit Status

The Read ECC Data Unit Status (RDECC_4_0, RDECC_C_0) transaction is used to determine the ECC status of the addressed unit data. In this transaction, the LSb of the address must be aligned to an ECC data unit. This transaction latency cycles set by (CFR2V[2:0]) to enable maximum 104 MHz clock frequency (see **Table 48**). The byte contents of the ECC Status for the selected ECC unit is then output. Any following data will be indeterminate. To read the next ECC unit status, another RDECC_4_0 or RDECC_C_0 transaction should be sent out to the next address, incremented by 16 bytes.

5.1.3.5 Read register related registers and transactions

Table 15 Read register related registers and transactions

Related registers	Related SPI transactions (See Table 48)
Configuration Register 2 (CFR2N, CFR2V) (see Table 42)	Read Any Register (RDARG_C_0)
	Read Status Register 1 (RDSR1_0_0)
	Read Status Register 2 (RDSR2_0_0)
	Read Configuration Register 1 (RDCR1_0_0)
	Read ECC Status (RDECC_4_0, RDECC_C_0)

5.2 Write

There are write transactions for writing to the Registers. These write transactions use the SPI protocol as mentioned in the Transaction Protocols section.

5.2.1 Write Enable transaction

The Write Enable (WRENB_0_0) transaction sets the Write Program Enable Status (WRPGEN) bit of the Status Register 1 (STR1V[1]) to 1. The WRPGEN bit must be set to '1' by issuing the Write Enable (WRENB_0_0) transaction to enable write, program, and erase transactions (see Table 48).

5.2.2 Write Enable for Volatile Registers

The Volatile Status and Configuration Registers, can be written by sending the WRENV_0_0 transaction followed by any write register transactions. This gives more flexibility to change the system configuration and memory protection schemes quickly without waiting for the typical non-volatile bit write cycles or affecting the endurance of the status or configuration non-volatile register bits. The WRENV_0_0 transaction is used only to direct the following write register transaction to change the volatile status and configuration register bit values.

5.2.3 Write Disable transaction

The Write Disable (WRDIS_0_0) transaction clears the Write Program Enable Status (WRPGEN) bit of the Status Register 1 (STR1V[1]) to '0'.

The WRPGEN bit can be cleared to '0' by issuing the Write Disable (WRDIS_0_0) transaction to disable commands that requires WRPGEN be set to '1' for execution. The WRDIS_0_0 transaction can be used by the user to protect memory areas against inadvertent write, program, or erase operations that can corrupt the contents of the memory. The WRDIS_0_0 transaction is ignored during an embedded operation while RDYBSY bit = 1 (STR1V[0]) (see Table 48).

5.2.4 Clear Program and Erase Failure Flags transaction

The Clear Program and Erase Failure Flags (CLPEF_0_0) transaction resets bit STR1V[5] (Erase Error Flag) and bit STR1V[6] (Program Error Flag) to '0'. This transaction will be accepted even when the device remains busy with RDYBSY set to '1', as the device does remain busy when either error bit is set. The WRPGEN bit will be unchanged after this transaction is executed (see **"1-1-1 transaction table"** on page 64).

5.2.5 Clear ECC Status Register transaction

The Clear ECC Status Register (CLECC_0_0) transaction resets bit ECSV[4] (2-bit ECC Detection), bit ECSV[3] (1-bit ECC Correction). It is not necessary to set the WRPGEN bit before this transaction is executed. The Clear ECC Status Register transaction will be accepted even when the device remains busy with WRPGEN set to '1', as the device does remain busy when either error bit is set. The WRPGEN bit will be unchanged after this command is executed (see **"Transaction tables"** on page 64).

5.2.6 Write Registers transactions

The Write Registers (WRREG_0_1) transaction allows new values to be written to both the Status and Configuration Registers. Before the Write Registers transaction can be accepted by the device, a Write Enable or Write Enable for Volatile Registers transaction must be received. After the Write Enable command has been decoded successfully, the device will set the WRPGEN in the Status Register to enable any write operations.

The Write Registers transaction is entered by shifting the instruction and the data bytes on DQ0_SI. The Status and Configuration Registers are one data byte in length.

The WRR operation first erases the register then programs the new value as a single operation. The Write Registers transaction will set the PRGERR or ERSERR bits if there is a failure in the WRREG_0_1 operation.

5.2.7 Write Any Register transaction

The Write Any Register (WRARG_C_1) transaction provides a way to write any device register, non-volatile or volatile. The transaction includes the address of the register to be written, followed by one byte of data to write in the addressed register (see **Table 48**).

Before the WRARG_C_1 transaction can be accepted by the device, a Write Enable (WRENB_0_0) transaction must be issued and decoded, which sets the Write/Program Enable bit (WRPGEN) in the Status Register to enable any write operations. The RDYDSY bit in STR1V[0] can be checked to determine when the operation is completed. The PRGERR and ERSERR bits in STR1V[6:5] can be checked to determine if any error occurred during the operation.

Some registers have a mixture of bit types and individual rules controlling which bits can be modified. Some bits are read only, some are OTP, and some are designated Reserved (DNU).

Read only bits are never modified and the related bits in the WRARG_C_1 transaction data byte are ignored without setting a program or erase error indication (PRGERR or ERSERR in STR1V[6:5]). Hence, the value of these bits in the WRARG_C_1 data byte do not matter.

OTP bits can only be programmed to the level opposite of their default state. Writing of OTP bits back to their default state is ignored and no error is set.

Non-volatile bits which are changed by the WRARG_C_1 data, require non-volatile register write time (t_W) to be updated. The update process involves an erase and a program operation on the non-volatile register bits. If either the erase or program portion of the update fails, the related error bit and RDYBSY bit in STR1V will be set to '1'.

Status Register 1 can be repeatedly read (polled) to monitor the RDYBSY bit (STR1V[0]) and the error bits (STR1V[6,5]) to determine when the register write is completed or failed. If there is a write failure, the CLPEF_0_0 transaction is used to clear the error status and enable the device to return to standby state.

5.2.8 Write transactions related registers and transactions

Table 16 Write transactions related registers and transactions

Related registers	Related SPI transactions (See Table 48)
Status Register 1 (STR1N, STR1V) (See **Table 36**)	Write Enable (WRENB_0_0)
	Write Registers (WRREG_0_1)
	Write Enable Volatile (WRENV_0_0)
	Write Disable (WRDIS_0_0)
	Clear Program and Erase Failure Flags (CLPEF_0_0)
ECC Status Register (ECSV) (See **Table 47**)	Clear ECC Status Register (CLECC_0_0)
	Write Any Register (WRARG_C_1)

5.3 Program

There are program transactions for programming data to the Memory Array and Secure Silicon Region. The program transaction use SPI protocol:

Before any program transaction can be accepted by the device, a Write Enable (WRENB_0_0) transaction must be issued and decoded by the device. Program transactions can only be executed by the device if the Write/Program Enable (WRPGEN) in the Status Register is set to '1' to enable program operations. When a program transaction is completed, the WRPGEN bit is reset to a '0'.

While the program transaction is in progress, the Status Register 1 may be read to check the value of the Device Ready/Busy (RDYBSY) bit. The RDYBSY bit is a '1' during the self-timed program transaction, and is a '0' when it is completed.

The RD/BY# output is low during the erase transaction and goes high when completed (see **Figure 49**).

The PGMERR bit in STR1V[6] may be checked to determine if any error occurred during the program transaction.

A program transaction applied to a sector that has been Write Protected through any of the protection schemes, will not be executed and will set the PGMERR status fail bit. If the inputted address is pass the array boundary, the transaction is in error with RDYBSY status bit set to '1' and PRGERR status bit set to '1'.

The program transactions will be initiated when CS# is driven into the logic HIGH state.

5.3.1 Program granularity

The device supports Multi-pass programming by configuring CFR4N[3] = 0. It allows byte-programming, bit-walking, or multiple program operations to the same ECC data unit (without an erase) when programming a '0' over a '1'. Performing Multi-pass programming on a already programmed ECC data unit without an erase operation will disable the device's ECC functionality for that data unit and as a result, data integrity for this data unit will be affected. It is required to required to erase the sector and program only in ECC data unit (16-byte) granularity to keep ECC enabled. Note that when Multi-pass is disabled CFR4N[3] = 1, Programming on a previous programmed ECC data units will result in a program error.

5.3.2 Page programming

Page programming is done by loading a page buffer with data to be programmed and issuing a programming transaction to move data from the buffer to the memory array. This sets an upper limit on the amount of data that can be programmed with single programming transaction. Page programming allows up to a page size (either 256- or 512-bytes) to be programmed in one operation. The page size is determined by the Configuration Register 3 bit 4 (CFR3V[4]). The page is aligned on the page size address boundary. It is possible to program from one byte up to a page size in each page programming operation. For the very best page program throughput, programming should be done in full pages of 512 or 256 bytes (depends on CFR3V[4]) aligned on 512 or 256 byte boundaries with each page being programmed only once.

5.3.3 Program Page transaction

The Program Page transaction (PRPGE_4_1, PRPGE_C_1, PRPG2_4_1, PRPG2_C_1) programs data into the memory array. If data more than a page size (256B or 512B) is sent to the device, then the space between the starting address and the page aligned end boundary, the data loading sequence will wrap from the last byte in the page to the zero byte location of the same page and begin overwriting any data previously loaded in the page. If less than a page of data is sent to the device, then the sent data bytes will be programmed in sequence, starting at the provided address within the page, without having any effect on the other bytes of the same page. The programming process is managed by the device internal control logic. The PRGERR bit indicates if an error has occurred in the programming transaction that prevents successful completion of programming. This includes attempted programming of a protected area (see **Table 48**).

5.3.4 Program Secure Silicon Region transaction

The Program Secure Silicon transaction (PRSSR_C_1) programs data in the SSR, which is in a different address space from the main array data and is OTP. The SSR is 1024 bytes, so the address bits from A31 to A10 must be zero for this transaction (see **"Transaction tables"** on page 64). It is required to align start address to 32 bits while programming SSR space, which means the address bits A1 and A0 should be 0'b and host should deassert CS# to align with 32 bits.

The PRGERR bit in STR1V[6] may be checked to determine if any error occurred during the operation.

To program the OTP array in bit granularity, the rest of the bits within a data byte can be set to '1'.

Each SSR memory space can be programmed one or more times, provided that the region is not locked. Attempting to program zeros in a region that is locked will fail with the PRGERR bit in STR1V[6] set to '1'. Programming once, even in a protected area does not cause an error and does not set PRGERR bit. Subsequent programming can be performed only on the unprogrammed bits (that is, 1 data). When multi-pass programming is disabled (CFR4N[3] = 1) programming more than once within an ECC unit will cause program failure and when multi-pass programming is enabled (CFR4N[3] = 0) it will disable ECC on that data unit.

5.3.5 Program related registers and transactions

Table 17 Program related registers and transactions

Related registers	Related SPI transactions (See Table 48)
Status Register 1 (STR1N, STR1V) (See **Table 36**)	Write Enable (WRENB_0_0)
	Program Page (PRPGE_4_1, PRPGE_C_1, PRPG2_4_1, PRPG2_C_1)
	Clear Program and Erase Failure Flags (CLPEF_0_0)
	Program Secure Silicon (PRSSR_C_1)
ECC Status Register (ECSV) (See **Table 47**)	Clear Program and Erase Failure Flags (CLPEF_0_0)

5.4 Erase

There are erase transactions for erasing data bits to ‘1’ (all bytes are FFh) for the Memory Array.

Before any erase transaction can be accepted by the device, a Write Enable (WRENB_0_0) transaction must be issued and decoded by the device. Erase transactions can only be executed by the device if the Write/Program Enable bit (WRPGEN) in the Status Register is set to ‘1’ to enable erase operations. When an erase transaction is completed, the WRPGEN bit is reset to a ‘0’.

While the erase transaction is in progress, the Status Register 1 may be read to check the value of the Device Ready/Busy (RDYBSY) bit. The RDYBSY bit is a ‘1’ during the self-timed erase transaction, and is a ‘0’ when it is completed.

The RD/BY# output is low during the erase transaction and goes high when completed (see **Figure 50**).

The ERSERR bit in STR1V[5] can be checked to determine if any error occurred during the erase transaction.

An erase transaction applied to a sector that has been Write Protected through the Block Protection bits will not be executed and will set the ERSERR status fail bit. If the inputted address is pass the array boundary, the transaction is in error with RDYBSY status bit set to ‘1’ and ERSERR status bit set to ‘1’.

Erase transactions will be initiated when CS# is driven into the logic HIGH state.

5.4.1 Erase sector transaction

The Erase 128 KB (2bpc) or 64 KB (1bpc) Sector (ERSEC_4_0, ERSEC_C_0) transaction sets all bits in the addressed sector to ‘1’ (all bytes are FFh).

5.4.2 Erase chip transaction

The Erase Chip (ERCHP_0_0) transaction sets all bits to ‘1’ (all bytes are FFh) inside the entire flash memory array (see **Table 48**).

An Erase Chip transaction can be executed only when the Block Protection (BP2, BP1, BP0) bits are set to 0’s. If the BP bits are not zero, the transaction is not executed and ERSERR status fail bit is not set.

5.4.3 Erase status transaction

The Evaluate Erase Status (EVERS_C_0) transaction verifies that the last erase operation on the addressed sector was completed successfully. If the selected sector was successfully erased, then the erase status bit (STR2V[2]) is set to ‘1’. If the selected sector was not completely erased STR2V[2] is ‘0’. The Write/Program Enable transaction (to set the WRPGEN bit) is not required before this transaction. However, the RDYBSY bit is set by the device itself and cleared at the end of the operation, as visible in STR1V[0] when reading status.

The Evaluate Erase Status transaction can be used to detect when erase operations that have failed due to loss of power, during the erase operation. The transaction requires t_{EES} to complete and update the erase status in STR2V. The RDYBSY bit (STR1V[0]) can be read to determine when the Evaluate Erase Status transaction is completed. If a sector is found not erased with STR2V[2] = 0, the sector must be erased again to ensure reliable storage of data in the sector. If sector address is out of range output will be false results without any failure indication.

5.4.4 Erase related registers and transaction

Table 18 Erase related registers and transactions

Related registers	Related SPI transactions (See Table 48)
Status Register 1 (STR1N, STR1V) (See **Table 36**)	Write Enable (WRENB_0_0)
Status Register 2 (STR2V) (See **Table 39**)	Erase 64 KB or 128 KB Sector (ERSEC_4_0, ERSEC_C_0)
	Erase Chip (ERCHP_0_0)
	Evaluate Erase Status (EVERS_C_0)
ECC Status Register (ECSV) (See **Table 47**)	–

5.5 Suspend and resume embedded operation

Quad device can interrupt and suspend the running embedded operations such as Erase, Program. It can also resume the suspended operation once the host finishes the intermediate operation and sends the respective resume transaction to the device. Only single suspend and resume operation is allowed during an erase or a program embedded operation, multiple suspend and resume operations are not allowed per erase or program operation.

5.5.1 Erase, program suspend

The Suspend transaction allows the system to interrupt a program, erase operation and then read from any other non erase-suspended sector, non-program-suspended-page or the array. The Device Ready/Busy Status Flag (RDYBSY) in Status Register 1 (STR1V[0]) must be checked to know when the program, erase operation has stopped.

5.5.1.1 Program suspend

- Program Suspend is valid only during a programming operation.
- The Program Operation Suspend Status flag (PROGMS) in Status Register-2 (STR2V[0]) can be used to determine if a programming operation has been suspended or was completed at the time RDYBSY changes to ‘0’.
- A program operation can be suspended to allow a read operation.
- Reading at any address within a program-suspended page produces undetermined data.

5.5.1.2 Erase suspend

- Erase Suspend is valid only during a sector erase operation.
- The Erase operation Suspend status flag (ERASES) in Status Register-2 (STR2V[1]) can be used to determine if an erase operation has been suspended or was completed at the time RDYBSY changes to ‘0’.
- A Chip Erase operation cannot be suspended.
- An Erase operation can be suspended to allow a program operation or a read operation.
- A new erase operation is not allowed with an already suspended erase, program operation. An erase transaction is ignored in this situation.
- Reading at any address within an erase-suspended sector produces undetermined data.
- Program operation is allowed during erase suspend to any non suspended sector.

The Write Any Register transactions are not allowed during Erase, Program Suspend. It is therefore not possible to alter the Block Protection bits during Erase Suspend.

The time required for the suspend operation to complete is t_{PEDS}.

After an erase-suspended program operation is complete, the device returns to the erase-suspend mode. The system can determine the status of the program operation by reading the RDYBSY bit in the Status Register 1, just as in the standard program operation.

Table 19 lists the transactions allowed during the suspend operation.

Table 19 Transactions allowed during suspend

Transaction name	Allowed during erase suspend	Allowed during program suspend
Write Disable (WRDIS_0_0)	Yes	No
Read Status Register 1 (RDSR1_0_0)		Yes
Write Enable (WRENB_0_0)		No
Write Enable Volatile (WRENV_0_0)		
Read Status Register 2 (RDSR2_0_0)		Yes
Read Configuration Register 1 (RDCR1_0_0)		
Program Page (PRPGE_4_1, PRPGE_C_1, PRPG2_4_1, PRPG2_C_1)		No
Read ECC Status (RDECC_4_0, RDECC_C_0)		Yes
Clear ECC Status Register (CLECC_0_0)		
Resume Program / Erase (RSEPD_0_0)		
Resume Program / Erase (RSEPA_0_0)		
Read Unique ID (RDUID_0_0)		
Read SFDP (RSFDP_3_0)		
Read Any Register (RDARG_C_0)		
Software Reset Enable (SRSTE_0_0)		
Clear Program and Erase Failure Flags (CLPEF_0_0)		
Software Reset (SFRST_0_0)[6]		
Read Identification Register (RDIDIN_0_0) (manufacturer and device identification)		
Suspend Program / Erase(SPEPD_0_0)		No
Suspend Program / Erase (SPEPA_0_0)		
Read SDR (RDAY1_C_0, RDAY1_4_0)		Yes
Read Fast SDR (RDAY2_C_0)		
Read SDR Quad Output (RDAY4_C_0, RDAY4_4_0)		
Read SDR Quad I/O (RDAY5_C_0, RDAY5_4_0)		

Note
6. During suspended embedded operation the Software Reset (SFRST_0_0) transaction can be sent to the device after program or erase operation is suspended for t_{PEDS} time.

5.5.2 Erase, program resume

An Erase, Program Resume transaction must be written to resume a suspended operation. After program or read operations are completed during a Program, Erase suspend, the Resume transaction is sent to resume the suspended operation.

After an Erase, Program Resume transaction is issued, the RDYBSY bit in Status Register 1 will be set to '1' and the programming operation will resume if one is suspended. If no program operation is suspended, the suspended erase operation will resume. If there is no suspended program or erase operation, the resume transaction is ignored.

Program, Erase operations may be interrupted as often as necessary. For example, a program suspend transaction could immediately follow a program resume transaction, but for a program or erase operation to progress to completion there must be some period of time between resume and the next suspend transaction greater than or equal to t_{PEDRS}. **Figure 20** shows the flow of suspend and resume operation.

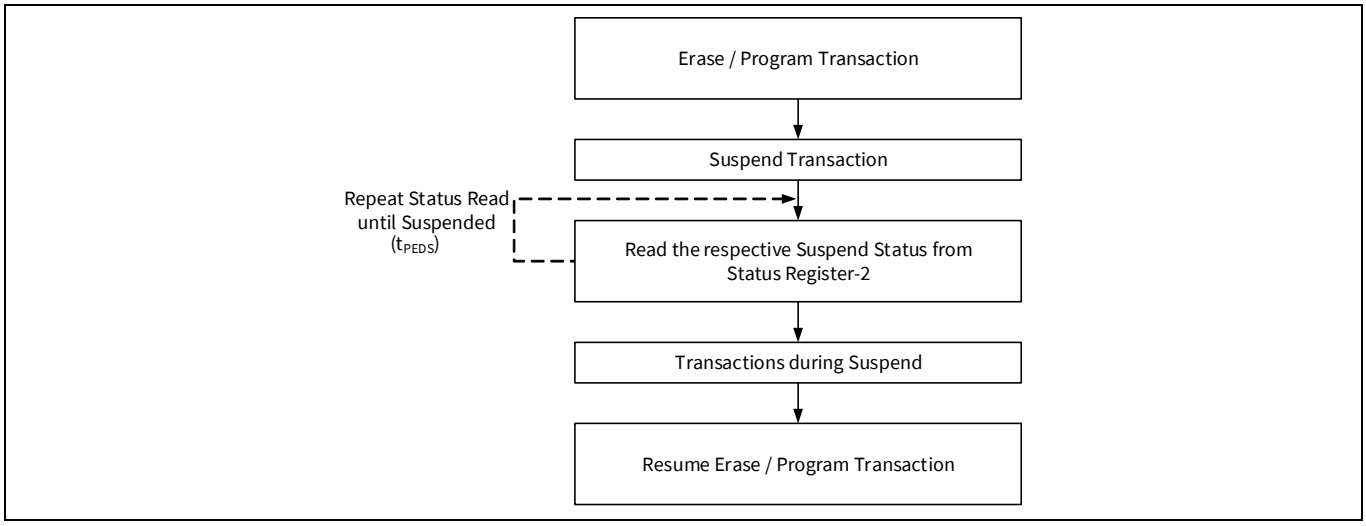


Figure 20 Suspend and resume sequence

5.5.3 Suspend and resume related registers and transactions

Table 20 Erase related registers and transactions

Related registers	Related SPI transactions (See Table 48)
Status Register 1 (STR1N, STR1V) (See Table 36)	Suspend Erase / Program (SPEPD_0_0)
Status Register 2 (STR2V) (See Table 39)	Resume Erase / Program (RSEPD_0_0)
	Suspend Erase / Program (SPEPA_0_0)
	Resume Erase / Program (RSEPA_0_0)
	Read Any Register (RDARG_C_0)
	Read Status Register-1 (RDSR1_0_0)
	Read Status Register-2 (RDSR2_0_0)

5.6 Error detection and correction

The device supports error detection and correction by generating an embedded Hamming ECC during memory array programming. This ECC code is then used for error detection and correction during read operations. The ECC is based on a 16-byte data unit. When the 16-byte data unit is loaded into the program buffer and is transferred to the 128-bits flash memory array line for programming (after an erase), an 8-bit ECC for each data unit is also programmed into a portion of the memory array that is not visible to the host system software. This ECC information is then checked during each Flash array read operation.

When multi-pass programming disabled (CFR4N[3] = 1, factory default configuration) the device has 1-bit error correction and 2-bit error detection configuration. In this configuration, any 1-bit error in a data units is corrected and any 2-bit error is detected and reported. There are 9 ECC code bits required to support this ECC configuration. Byte-programming, bit-walking, or multiple program operations to the same ECC data unit (without an erase) are not allowed and will result in a program error.

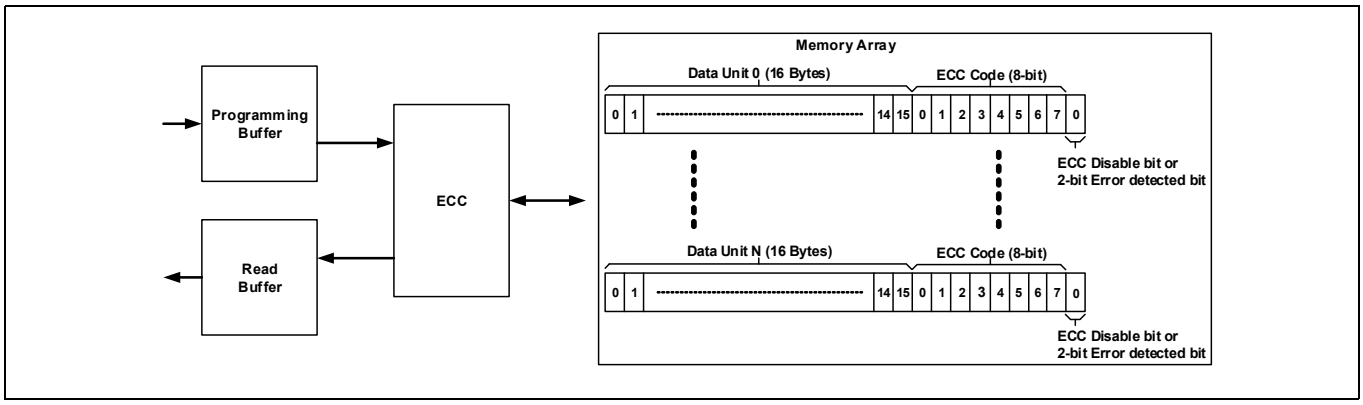


Figure 21 16-byte ECC data unit example

When multi-pass programming enabled (CFR4N[3] = 0) the device supports 1-bit error correction is the configuration. This configuration requires 8-bit ECC code bits and a ECC disable bit. When any amount of data is first programmed within a 16-byte data unit, the 8-bit ECC code value is set for the entire data unit. If additional data is subsequently programmed into the same data unit, ECC for that data unit is disabled and the ECC disable bit is set. A sector erase is needed to again enable ECC on that data unit. The disabling ECC on the data unit will affect its data integrity.

These are automatic operations transparent to the user. The transparency of the ECC feature enhances data reliability for typical programming operations which write data once to each data unit while also facilitating software compatibility with previous generations of products by still allowing for single-byte programming and bit-walking (in this case, ECC will be disabled).

Changing the ECC mode from multi-pass programming disable to enable, or from multi-pass programming enable to disable will invalidate all data in the memory array. When changing the ECC mode, the host must first erase all sectors in the device. If the ECC mode is changed without erasing programmed data, subsequent read operations will result in undefined behavior.

5.6.1 ECC error reporting

There are two methods for reporting to the host system when ECC errors are detected.

- ECC Data Unit Status provides the status of 1-bit and 2-bit errors in data units.
- ECC Status Register provides the status of 1-bit and 2-bit errors since the last ECC clear or reset.

5.6.1.1 ECC Data Unit Status (EDUS)

- The status of ECC in each data unit is provided by the 8-bit ECC Data Unit Status.
- The ECC status transaction outputs the ECC status of the addressed data unit. The contents of the ECC Data Unit status then indicate, for the selected data unit, whether there is a 1-bit error corrected, 2-bit error detected or ECC is disabled for that data unit.

Table 21 ECC Data Unit Status (EDUS)

Bits	Field name	Function	Read/Write N = Non-volatile V = Volatile	Factory default (Binary)	Description
EDUS[7:4]	RESRVD	Reserved for future use	V => R	0000	These bits are Reserved for future use.
EDUS[3]	ECC2BD	ECC Error 2-bit Error Detection Flag	V => R	0	This bit indicates whether a two bit error is detected in the data unit, when CFR4V[3] = 1. When CFR4V[3] = 0 then 2-bit error detection is disabled, ECC2BD bit will alway be '0'. Selection options: 1 = Two-bit error detected 0 = No error
EDUS[2]	RESRVD	Reserved for future use	V => R	0	This bit is Reserved for future use.
EDUS[1]	ECC1BC	ECC Error 1-bit Error Detection and Correction Flag	V => R	0	This bit indicates whether an error is corrected in the data unit. Selection options: 1 = Single-bit error corrected in the addressed data unit 0 = No single-bit error was corrected in the addressed data unit
EDUS[0]	ECCOFF	Data Unit ECC OFF/ON Flag	V => R	0	Selection options: 1 = ECC is OFF in the selected data unit 0 = ECC is ON in the selected data unit Dependency: CFR4x[3]

5.6.1.2 ECC Status Register (ECSV)

- An 8-bit ECC Status Register provides the status of 1-bit or 2-bit errors during normal reads since last ECC clear or reset. ECC Status Register does not have user programmable non-volatile bits, all defined bits are volatile read only bits. The default state of these bits are set by hardware.
- ECC Status Register can be accessed through the Read Any Register transaction. The correct sequence for Read Any Register based ECSV is read as follows:
  - Read data from memory array using any of the Read transaction
  - ECSV is updated by the device
  - Read Any Register transaction of ECSV provides the status of any ECC event since the last clear or reset.
- ECSV is cleared by POR,CS# Signaling Reset, Hardware/Software reset, or a Clear ECC Status Register transaction.

5.6.2 ECC related registers and transactions

Table 22 ECC related registers and transactions

Related registers	Related SPI transactions (see Table 48)
ECC Status Register (ECSV) (see Table 47)	Read Any Register (RDARG_C_0)
	Write Enable (WRENB_0_0)
	Write Any Register (WRARG_C_1)
	Read ECC Status (RDECC_4_0, RDECC_C_0)
	Clear ECC Status Register (CLECC_0_0)

5.7 Ready Busy (RD/BY#) output

RD/BY# is a dedicated, CMOS output pin indicates whether the device is performing an embedded operation or is in Standby mode ready to receive new transactions.

If the output is LOW (Busy), the device is actively writing registers, erasing and programming (this includes programming in the Erase Suspend mode).

If the output is HIGH (Ready), the device is ready to receive new transactions (including during the Erase Suspend mode), or is in the standby mode.

If there is a Program Error or Erase Error the RD/BY# output will remain LOW indicating the device is busy and is able to only receive limited transactions. The Status Register 1 can be read and the (PRGERR) and (ERSERR) status bits show the error. A Clear Program and Erase Failure Flags transaction must be executed to return the device to standby mode and RD/BY# to HIGH. The RD/BY# state during DPD is Tri-state.

5.8 Data protection schemes

Data protection is required to safeguard against unintended changes to stored data and device configuration. This includes inadvertent erasing or programming the memory array as well as writing to the configuration registers which can alter the functionality of the device.

5.8.1 Legacy block protection (LBP)

The legacy block protection (LBP) is a block-based data protection scheme. LBP supports compatibility with legacy serial NOR Flash devices. LBP provides protection for data in the sectors memory array and device configuration by protecting Status and Configuration registers.

5.8.1.1 Memory array protection

The protection for the memory array is with block size selection of protected sectors, which is achieved through a combination of bits present in the Status Register 1 (STR1N[4:2]/STR1V[4:2] - LBPROT[2:0]) and Configuration Register 1 (CFR1N[5]/CFR1V[5] - TBPROT). There are 256 sectors in the Memory Array, the top two sectors (254 and 255) are not protected by the LBP bits. **Table 23** provides the LBP memory array sector selection summary.

Table 23 Legacy block memory array protection selection

CFR1N[5]/ CFR1V[5] TBPROT	STR1N[4]/ STR1V[4] LBPROT[2]	STR1N[3]/ STR1V[3] LBPROT[1]	STR1N[2]/ STR1V[2] LBPROT[0]	Sector location	Number sectors protected
0	0	0	0	None	0
0	0	0	1	Upper [252 : 253]	2
0	0	1	0	Upper [248 : 253]	6
0	0	1	1	Upper [240 : 253]	14
0	1	0	0	Upper [224 : 253]	30
0	1	0	1	Upper [192 : 253]	62
0	1	1	0	Upper [128 : 253]	126
0	1	1	1	All sectors [0 : 253]	254
1	0	0	0	None	0
1	0	0	1	Lower [0 : 3]	4
1	0	1	0	Lower [0 : 7]	8
1	0	1	1	Lower [0 : 15]	16
1	1	0	0	Lower [0 : 31]	32
1	1	0	1	Lower [0 : 63]	64
1	1	1	0	Lower [0 : 127]	128
1	1	1	1	All sectors [0 : 253]	254
x	x	x	x	Sectors [254 : 255]	Not protected

5.8.2 Configuration protection

LBP has selection bits in Configuration Register 1 (CFR1N[4,0]/CFR1V[4,0] - PLPROT, TLPROT) which either permanently or temporarily protect Status and Configuration registers, thereby again protecting the device's configuration. The temporary protection remains in effect until the next power down.

Table 24 Option 2 - Legacy block configuration protection selection[7]

CFR1N[4]/ CFR1V[4] PLPROT	CFR1N[0]/ CFR1V[0] TLPROT	Register protection status
0	0	Status and Configuration registers are unprotected
1	X	Status and Configuration registers are permanently protected (TBPROT, LBPROT[2:0]) and Sector Architecture (SECOPT[3:0])
0	1	Status and Configuration registers are Protected till next power down (TBPROT, LBPROT[2:0])

5.8.3 Write Protect signal

The Write Protect (DQ2_WP#) input in combination with the Status Register Write Disable bit (STR1x[7]) provide hardware input signal controlled protection. When WP# is LOW and STR1x[7] is set to "1" Status Register 1 (STR1N and STR1V) and Configuration Register-1 (CFR1N and CFR1V) are protected from alteration. This prevents disabling or changing the protection defined by the Block Protect bits.

5.8.3.1 Legacy block protection flowchart

The LBP protection scheme flowchart is shown in **Figure 22**.

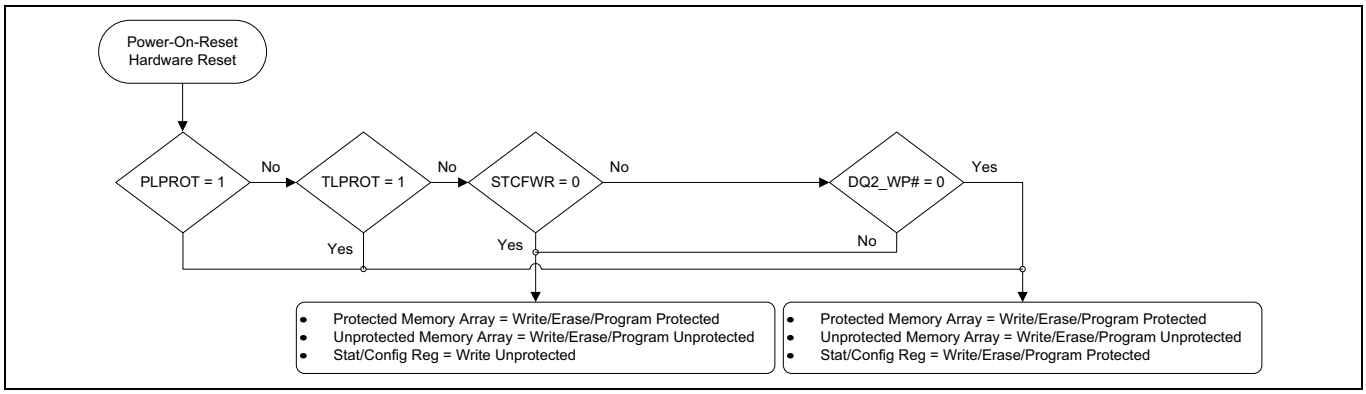


Figure 22 Legacy block protection flowchart

5.8.4 LBP related registers and transactions

Table 25 LBP related registers and transactions

Related registers	Related SPI transactions (See Table 48)
Status Register 1 (STR1N, STR1V) (see **Table 36**)	Read Any Register (RDARG_C_0)
Configuration Register 1 (CFR1N, CFR1V) (see **Table 40**)	Write Any Register (WRARG_C_1)
	Read Status Register 1 (RDSR1_0_0)
	Write Enable (WRENB_0_0)

Note
7. Protecting the configuration also protects the memory array blocks which have been selected for protection.

5.9 Secure silicon region (SSR)

Secure Silicon Region (SSR) is a 1024 byte memory region (separate from the main memory array). The 1024 bytes are divided into 32, individually lockable 32-byte regions. **Figure 23** provides an overview of SSR.

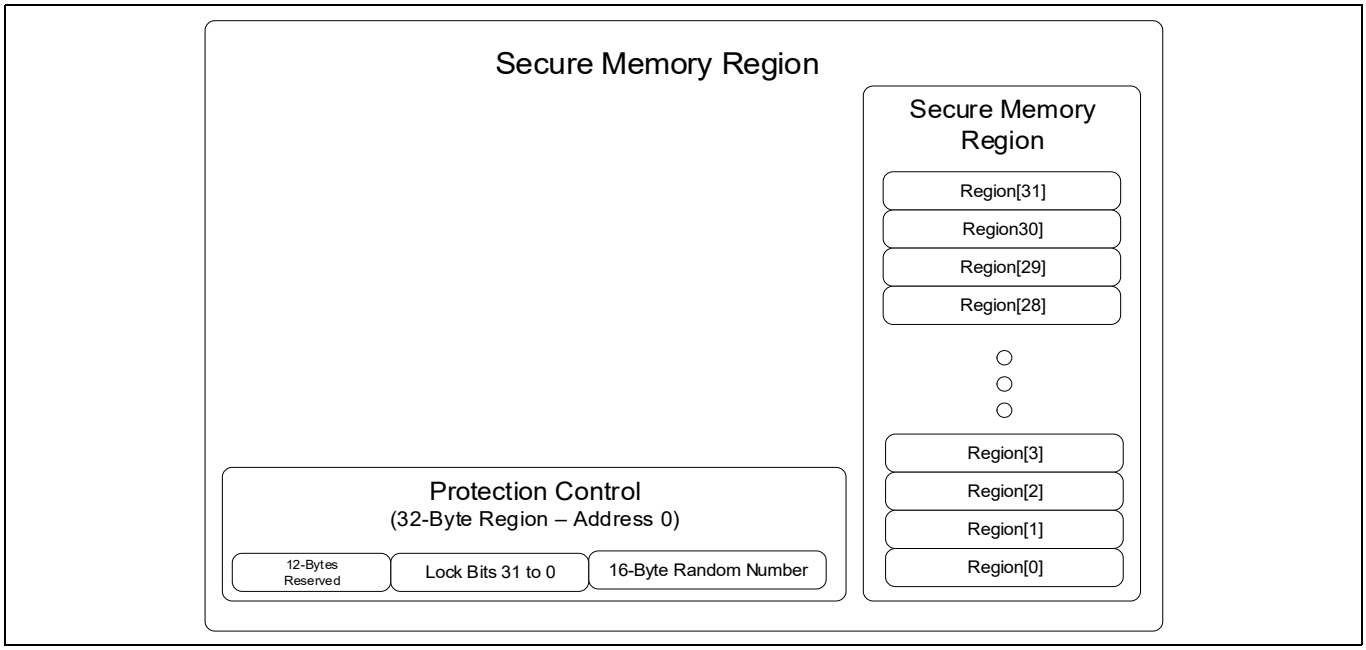


Figure 23 OTP protection (Non-volatile)

The first 32-byte region (starting at address 0) provides the protection mechanism for the other 32-byte regions. The sixteen lowest bytes of this region contain a 128-bit random number. The random number cannot be written to, erased or programmed. The next four bytes (32 bits in total) of this region provide protection from programming if set to '0' for the remaining 32-byte regions - one bit per 32-byte region. All other bytes are reserved.

Note Attempting to Erase or Program the 128-bit random number will result in ERSERR or PRGERR, respectively. A hardware Reset is required to bring the device back to Standby mode.

5.9.1 SSR related registers and transactions

Table 26 SSR related registers and transactions

Related registers	Related SPI transactions (see Table 48)
N/A	Program Secure Silicon Region (PRSSR_C_1)
	Read Secure Silicon Region (RDSSR_C_0)

5.10 SafeBoot

SEMPER™ Flash memory devices contain an embedded microcontroller which is used to initialize the device, manage embedded operations, and perform other advanced functionality. An initialization failure of this embedded microcontroller or corruption of the non-volatile configuration registers can render the flash device unusable. Baring a catastrophic event, such as permanent corruption of the embedded microcontroller firmware, it is possible to recover the device.

The SafeBoot feature allows Status Register polling to detect an embedded microcontroller initialization failure or configuration register corruption through error signatures.

5.10.1 Microcontroller initialization failure detection

If the microcontroller embedded in the flash device fails to initialize, a hardware or CS# signaling reset can recover the device, unless it is a catastrophic failure. This hardware or CS# signaling reset must be initiated by the Host controller. Upon detecting a failed microcontroller initialization, the Flash device automatically reverts to its Default Boot mode (1S-1S-1S) and provides a failure signature in its Status Register.

Table 27 shows the device's Status Register bits upon detecting an initialization failure.

Table 27 Status Register 1 power-on detection signature

Bit	Field name	Function	Detection signature
STR1V[7]	STCFWR	Status Register 1 and Configuration 1, 2, 3, 4 and Architecture Configuration Registers Protection Selection against write	0
STR1V[6]	PRGERR	Programming Error Status Flag	1
STR1V[5]	ERSERR	Erasing Error Status Flag	1
STR1V[4]	LBPROT[2:0]	Legacy Block Protection based memory Array size selection **Note** LBPRIT[2:0] can be anything from 000 to 111 based on Block Protection configuration.	0
STR1V[3]			0
STR1V[2]			0
STR1V[1]	WRPGEN	Write/Program Enable Status Flag	0
STR1V[0]	RDYBSY	Device Ready/Busy Status Flag	1

Table 28 Interface configuration upon detecting power-on failure[8]

Interface	Transactions supported	Register type	Address (# of bytes)	Frequency of operation	Register read (# of clock cycles)	Output impedance
SPI (1S-1S-1S)	Read Status Register 1 (RDSR1_0_0) Read Any Register (RDARG_C_0)	Status Register (Volatile Only)	4	Maximum (allowed for RDSR1_0_0, RDARG_C_0)	0	45 Ω

Note
8. For reading the Status Register, providing the Non-volatile Status Register address to RDARG_C_0 will produce indeterminate results.

5.10.2 Configuration corruption detection

If during device's configuration update, such as writing to a non-volatile register, a power loss occurs or a hardware or CS# signaling reset is initiated, the write register transaction will get interrupted. The device will return to Standby mode, but the non-volatile register data is most likely corrupted since the embedded write operation was prematurely terminated. During the next power-up, the configuration corruption is detected and the device reverts to its Default Boot mode (1S-1S-1S) and allows rewriting the configuration again. The device will maintain the configured protection scheme. **Table 29** shows the device's Status Register bits upon detecting a configuration corruption.

Table 29 Status Register 1 configuration corruption detection signature

Bit	Field name	Function	Detection signature
STR1V[7]	STCFWR	Status Register 1 and Configuration 1, 2, 3, 4 and Architecture Configuration Registers Protection Selection against write	0
STR1V[6]	PRGERR	Programming Error Status Flag	1
STR1V[5]	ERSERR	Erasing Error Status Flag	0
STR1V[4]	LBPROT[2:0]	Legacy Block Protection based memory array size selection **Note** LBPRIT[2:0] can be anything from 000 to 111 based on Block Protection configuration.	0
STR1V[3]			0
STR1V[2]			0
STR1V[1]	WRPGEN	Write/Program Enable Status Flag	0
STR1V[0]	RDYBSY	Device Ready/Busy Status Flag	1

Table 30 Interface configuration upon detecting configuration corruption

Interface	Transactions supported	Address (# of bytes)	Frequency of operation	Register read latency (# of clock cycles)	Output impedance
SPI (1S-1S-1S)	All SPI (1S-1S-1S) transactions	4	Maximum	0	45 Ω

5.10.3 Related registers and transactions

Table 31 SafeBoot related registers and transactions

Related registers	Related SPI transactions (see Table 48)
Status Register 1 Volatile (STR1V) (see **Table 36**)	Read Any Register (RDARG_C_0)
	Read Status Register-1 (RDSR1_0_0)

5.10.4 SafeBoot host polling behavior

The host will need to go through a Status Register polling sequence to determine if a Initialization failure or Configuration corruption has occurred. The flowchart for the sequence is shown in **Figure 24**.

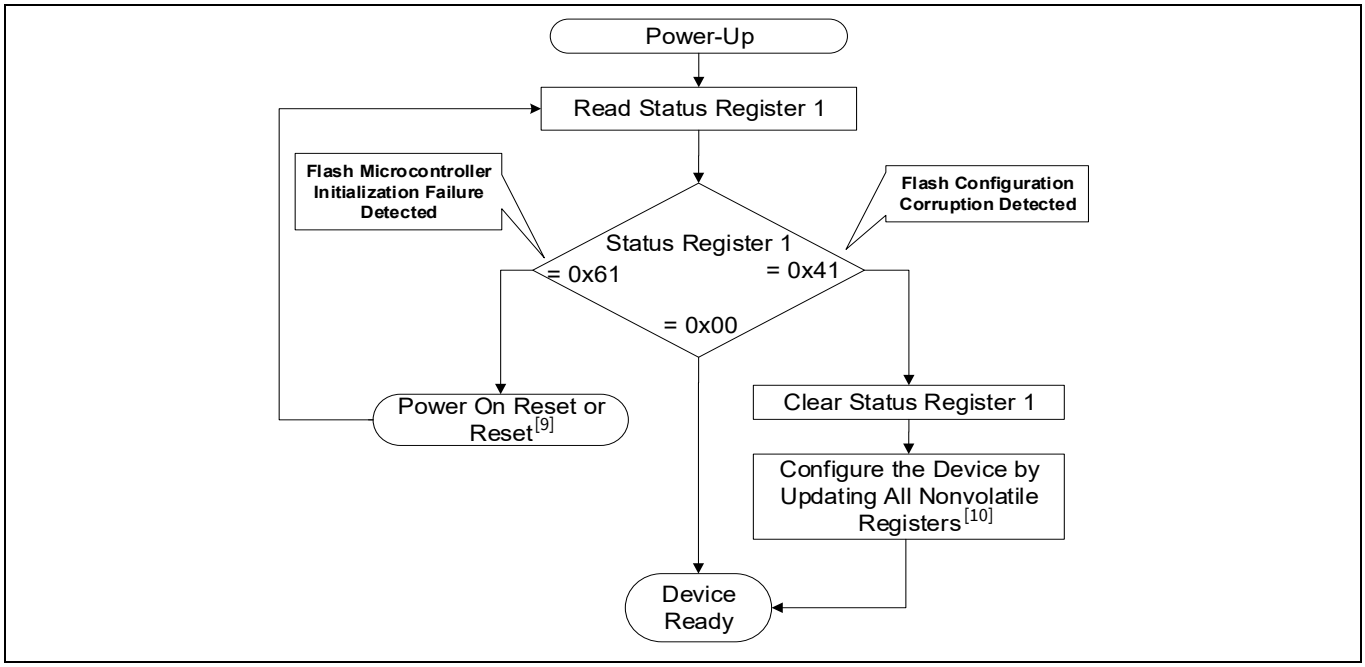


Figure 24 Host polling sequence for initialization failure and configuration corruption detection[11]

Notes
9. If you have Vcc within specifications and a hardware or CS# signaling reset does not resolve the issue, replace the flash device.
10. Non-volatile registers can be configured using the Write Any Register transaction, As soon as first Write Any Register transaction updates the non-volatile status register or configuration register, all remaining non-volatile status and configuration registers go back to the predefined state (STR1N = 0x00, CFR1N = 0x00, CFR2N = 0x00, CFR3N = 0x00, CFR4N = 0x00). It is recommended to initiate SafeBoot recovery operation by configuring the Address byte length, latency and memory array sector configuration followed by rest of the configurations.
11. When a Initialization or Configuration corruption failure occurs the RD/BY# will timeout (RD/BY# will remain LOW).

5.11 Reset

Quad devices support four types of reset mechanisms.

- Hardware Reset (RESET#)
- POR
- CS# Signaling Reset
- Software Reset

5.11.1 Hardware reset (using RESET# input pin)

The RESET# input initiates the reset operation with a transition from logic HIGH to logic LOW for > t_{RP}, and causes the device to perform the full reset process that is performed during POR. The hardware reset process requires a period of t_{RH} to complete. See **Table 57** for timing specifications.

The hardware reset process requires a period of t_{RH} to complete. If the POR process did not complete correctly for any reason during power-up (t_{PU}), RESET# going LOW will initiate the full POR process instead of the hardware reset process and will require t_{PU} to complete the POR process. During reset the RD/BY# is driven LOW and returns to HIGH when Reset is completed.

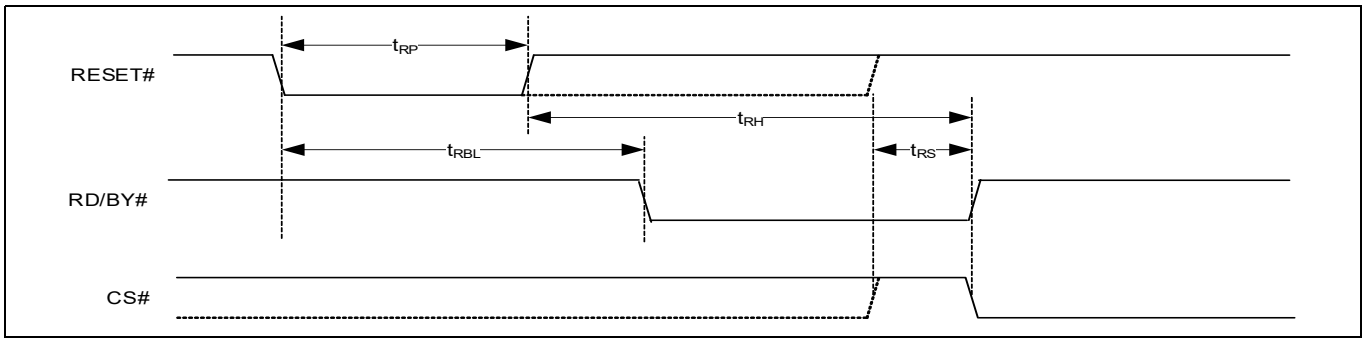


Figure 25 Hardware reset using RESET# input (Reset pulse = t_{RP}(Min))

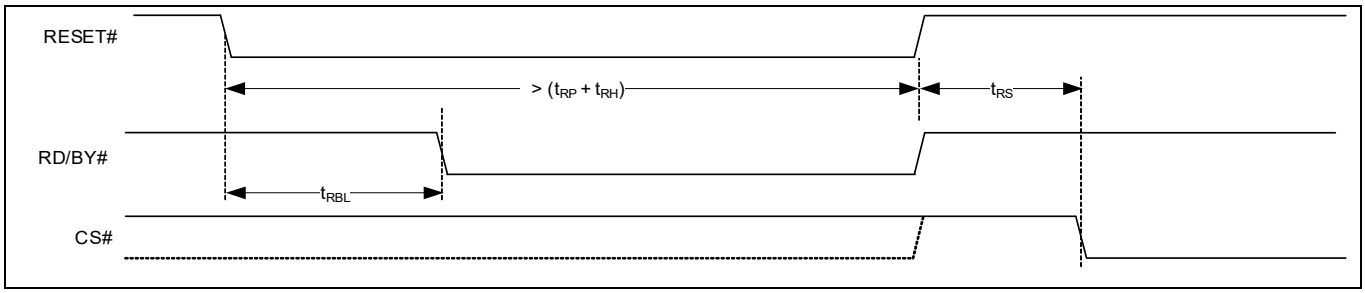


Figure 26 Hardware reset using RESET# input (Reset pulse > (t_{RP} + t_{RH}))

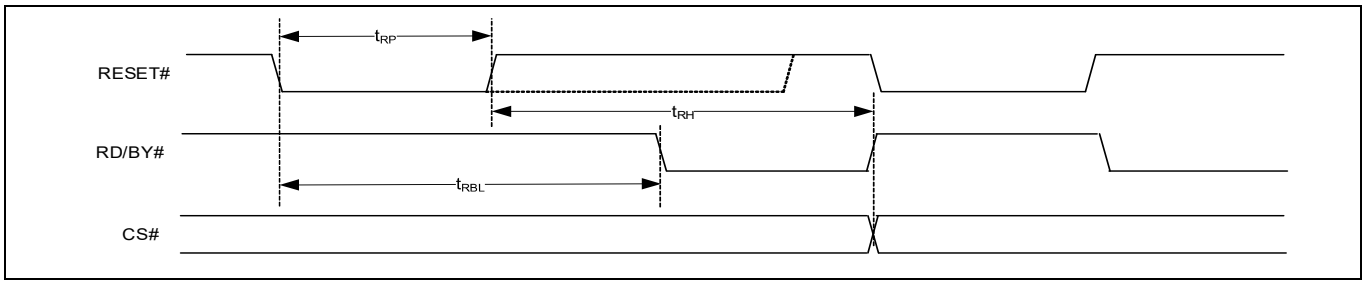


Figure 27 Hardware reset using RESET# input (Back to back hardware reset)

5.11.2 Power-on reset (POR)

The device executes a POR process until a time delay of t_{PU} has elapsed after the moment that V_{CC} rises above the minimum V_{CC} threshold (see **Figure 33**). The device must not be selected during power-up (t_{PU}). Therefore, CS# must rise with V_{CC}. No transactions may be sent to the device until the end of t_{PU}. See **Table 57** for timing specifications.

RESET# is ignored during POR. If RESET# is LOW during POR and remains LOW through and beyond the end of t_{PU}, CS# must remain HIGH until t_{RS} after RESET# returns HIGH. During reset the RD/BY# is driven LOW and returns to HIGH when Reset is completed.

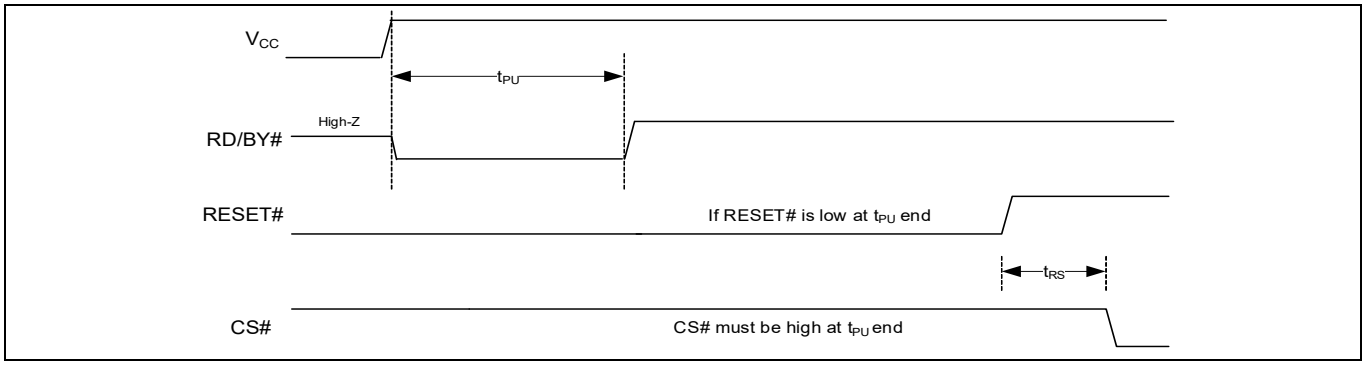


Figure 28 Reset LOW at the end of POR

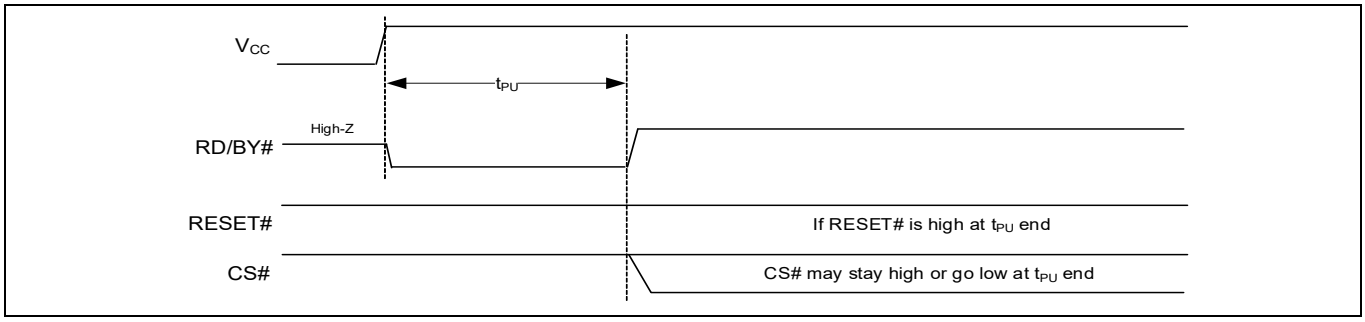


Figure 29 Reset HIGH at the end of POR

5.11.3 CS# signaling reset

The CS# Signaling Reset requires CS# and DQ0 signals. This reset method defines a signaling protocol, using existing signals, to initiate an SPI Flash hardware reset, independent of the device operating mode or number of package pins.

The Signaling Protocol is shown in **Figure 30**. See **Table 57** for timing specifications. The CS# signaling reset steps are as follows:

- CS# is driven active LOW.
- CK remains stable in either HIGH or LOW state.
- CS# and DQ0 are both driven LOW.
- CS# is driven HIGH (inactive).
- Repeat the above four steps, each time alternating the state of DQ0 for a total of four times.
- Reset occurs after the fourth CS# cycle completes and it goes HIGH (inactive).

After the fourth CS# pulse, the slave triggers its internal reset, the device terminates any operation in progress, makes all outputs high impedance, and ignores all read/write transactions for the duration of t_{RESET}. Then the device will be in standby state. During reset the RD/BY# is driven LOW and returns to HIGH when Reset is completed.

This reset sequence is not intended to be used at normal power on, but to be used only when the device is not responding to the system. This reset sequence will be operational from any state that the device may be in. Hence, CS# signaling reset is useful for packages that don't support a RESET# pin to provide behavior identical to Hardware Reset.

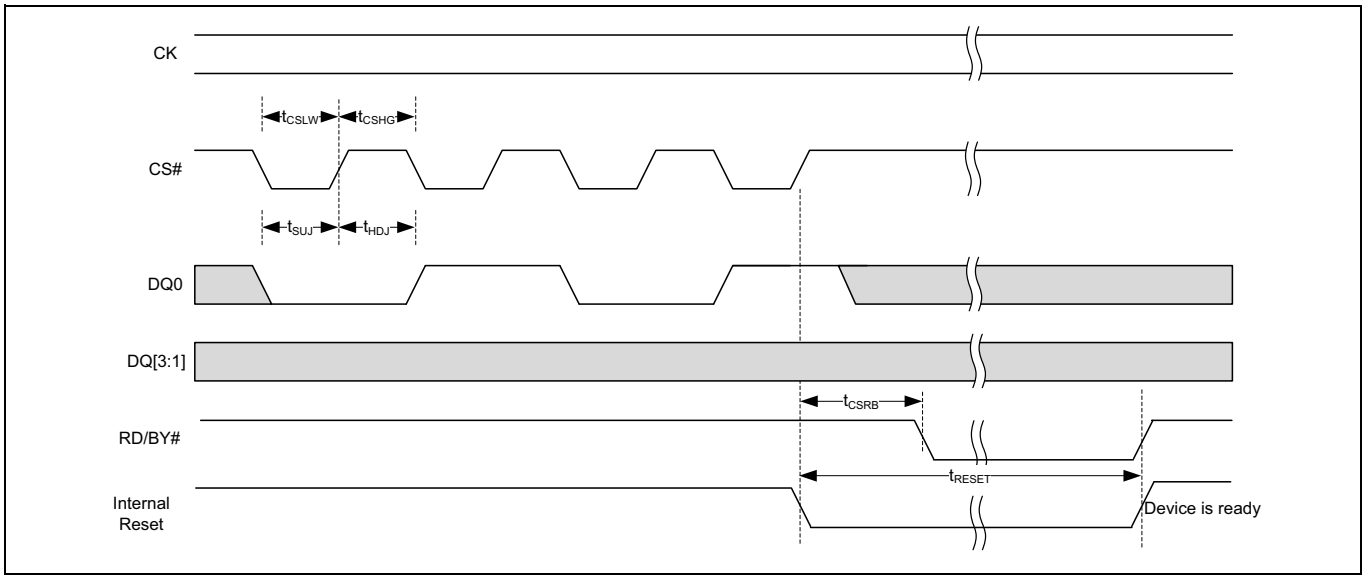


Figure 30 CS# signaling reset protocol

5.11.4 Software reset

Software controlled Reset transaction restores the device to its initial power up state, by reloading volatile registers from non-volatile default values except the protection registers. It also terminates the embedded operations. A reset transaction (SFRST_0_0) is executed when CS# is brought HIGH at the end of the transaction and requires t_{SR} time to execute. See **Table 57** for timing specifications. For the RD/BY# operation during Software Reset, see **Figure 31**.

The Software Reset Enable (SRSTE_0_0) transaction is required immediately before a Reset transaction (SFRST_0_0) such that a software reset is a sequence of the two transactions. Any transaction other than SFRST_0_0 following the SRSTE_0_0 transaction will clear the reset enable condition and prevent a later SFRST_0_0 transaction from being recognized.

The Software Reset (SFRST_0_0) transaction immediately following a SRSTE_0_0 transaction, initiates the software reset process. During software reset, only RDSR1_0_0 and RDARG_C_0 of Status Register 1 are supported operations as long as the volatile and non-volatile configuration states of the device are the same. If the configuration state is changing during software reset, reading Status Register 1 should only be done after the software reset time has elapsed.

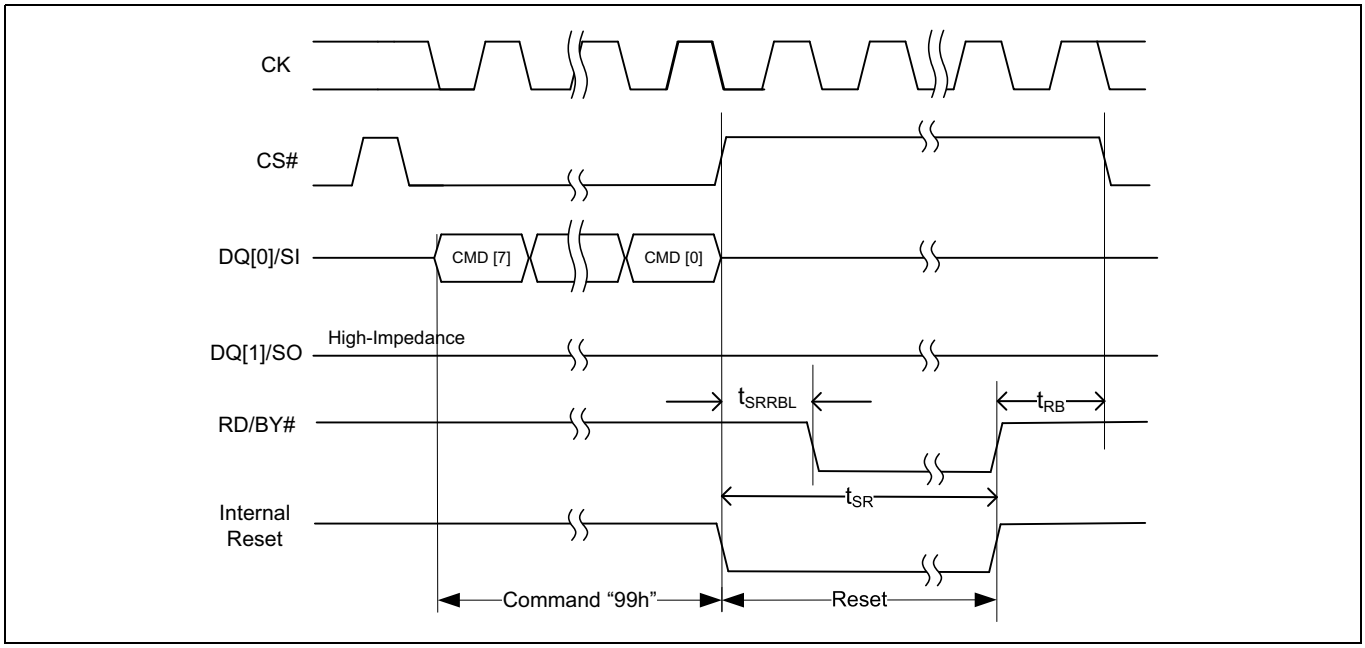


Figure 31 Software reset

5.11.4.1 Software reset related registers and transactions

Table 32 Software reset related registers and transactions

Related registers	Related SPI transactions (See Table 48)
N/A	Software Reset Enable (SRSTE_0_0)
	Software Reset (SFRST_0_0)

5.11.5 Reset behavior

Table 33 Reset behavior

Transaction / register name	POR	Hardware reset and CS# signaling reset	Software reset
Summary	• Device reset • Status bits reset • All volatile registers reset • Configuration reload to default • Volatile protection reset to default • Non-volatile protection unchanged • Reset all embedded operations	• Device reset • Status bits reset • All volatile registers reset • Configuration reload to default • Volatile protection reset to default • Non-volatile protection unchanged • Reset all embedded operations	• Device reset • Status bits reset • Configuration reload to default • Volatile protection reset to default • Non-volatile protection unchanged • Reset all embedded operations
Interface requirements	• All inputs - Ignored • All outputs - Tristated	• All inputs - Ignored • All outputs - Tristated	Transactions (SRSTE_0_0, SFRST_0_0)
Status Registers	Load from non-volatile registers	Load from non-volatile registers	Load from non-volatile registers
Configuration Registers	Load from non-volatile registers	Load from non-volatile registers	Load from non-volatile registers
ECC Status Register	Load 0x00	Load 0x00	Load 0x00
I/O mode	Load from non-volatile registers	Load from non-volatile registers	No change
Memory/register erase in progress	Not applicable	Abort erase	Abort erase
Memory/register program in progress	Not applicable	Abort program	Abort program
Memory/register read in progress	Not applicable	Abort read	Not applicable

5.12 Power modes

5.12.1 Active power and standby power modes

The device is enabled and in the Active Power mode when Chip Select (CS#) is LOW. When CS# is HIGH, the device is disabled, but may still be in an Active Power mode until all program, erase, and write operations have completed. The device then goes into the Standby Power mode, and power consumption drops to I_{SB}. See **Table 55** for parameter specifications.

5.12.2 Deep power down (DPD) mode

Although the standby current during normal operation is relatively low, standby current can be further reduced with the DPD mode. The lower power consumption makes the DPD mode especially useful for battery powered applications.

5.12.2.1 Enter DPD

The device can enter DPD mode by the Enter DPD Mode Transaction [ENDPD_0_0].

Enter DPD Mode using the Enter Deep Power Down Mode Transaction.

The DPD mode is enabled by sending the Enter Deep Power Down Mode Transaction (ENDPD_0_0) then waiting for a delay of t_{ENTDPD}. The CS# pin must be driven HIGH after the command byte has been latched. If this is not done, then the DPD transaction will not be executed. After CS# is driven HIGH, the power-down state will be entered within the time duration of t_{ENTDPD} (see **Table 57** for timing specifications) and power consumption drops to I_{DPD}. See **Table 55** for parameter specifications.

DPD can only be entered from an idle state. The DPD transaction is accepted only while the device is not performing an embedded algorithm as indicated by the Status Register 1 volatile, Device Ready/Busy Status Flag (RDYBSY) bit being cleared to zero (STR1V[0] = RDYBSY = 0). It is not allowed to send any transaction to device during t_{ENTDPD} time. The RD/BY# state during DPD is Tri-state.

5.12.2.2 Exit DPD

Device leaves DPD mode in one of the following ways:

Exit DPD Mode upon POR reset

When the device is in DPD a POR reset will return the device to Standby mode.

Exit DPD Mode upon CS# Pulse

Device exits DPD upon receipt of CS# pulse of width t_{CSDPD}. The CS# should be driven HIGH after the pulse. HIGH to LOW transition on CS# is required to start a transaction cycle after the DPD exit. It takes t_{EXTDPD} to come out of DPD mode. The device will not respond until after t_{EXTDPD}. During Exit of DPD RD/BY# will go LOW and then will go HIGH when Exit from DPD mode is completed.

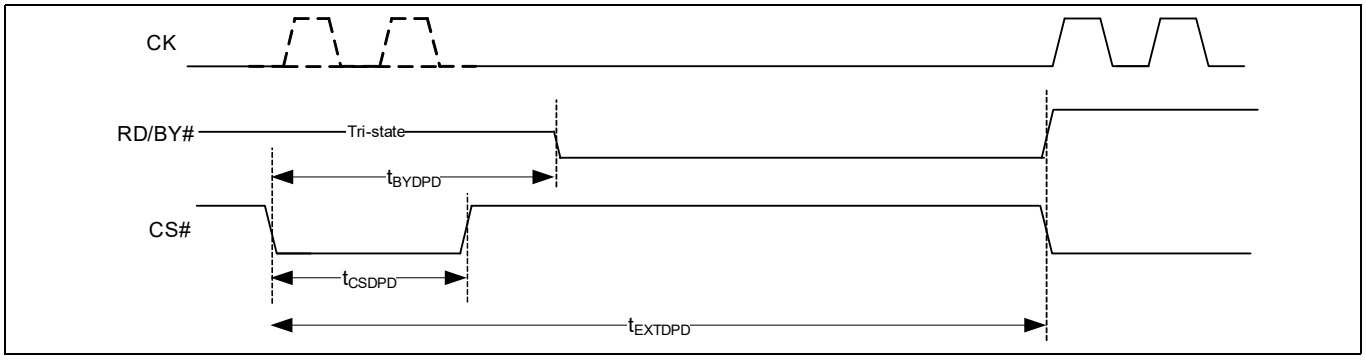


Figure 32 Exit DPD mode

The device maintains its configuration during DPD, meaning the device exits DPD in the same state as it entered. The ECC Status and Ready Busy Status Registers will be cleared.

5.12.2.3 DPD related registers and transactions

Table 34 DPD related registers and transactions

Related registers	Related SPI transactions (see Table 48)
N/A	Enter Deep Power Down Mode (ENDPD_0_0)

5.13 Power up and power down

The device must not be selected at power up or power down until V_{CC} reaches the correct value as follows:

- V_{CC} (min) at power up, and then for a further delay of t_{PU}
- V_{SS} at power down

5.13.1 Power up

The device ignores all transactions until a time delay of t_{PU} has elapsed after the moment that V_{CC} rises above the minimum V_{CC} threshold (see **Figure 33**). However, correct operation of the device is not guaranteed if V_{CC} returns below V_{CC} (min) during t_{PU}. No transaction should be sent to the device until the end of t_{PU}.

The device draws I_{POR} current during t_{PU}. After power up (t_{PU}), the WRPGEN bit is reset and there is the option to be in the Standby mode.

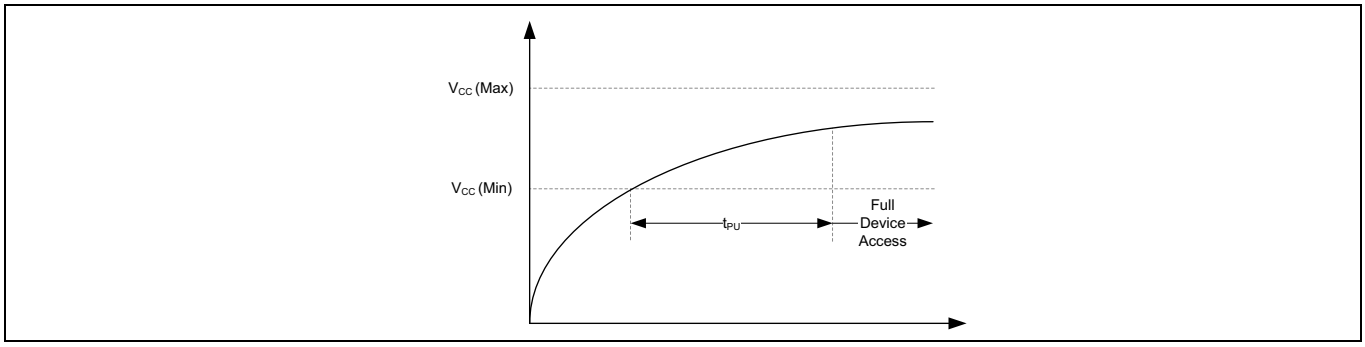


Figure 33 Power up

5.13.2 Power down

During power down or voltage drops below V_{CC}(cut-off), the voltage must drop below V_{CC}(LOW) for a period of t_{PD} for the part to initialize correctly on power up (see **Figure 34**). If during a voltage drop the V_{CC} stays above V_{CC}(cut-off), the part will stay initialized and will work correctly when V_{CC} is again above V_{CC}(min). In the event POR did not complete correctly after power up, the assertion of the RESET# signal or CS# Toggling reset will restart the POR process.

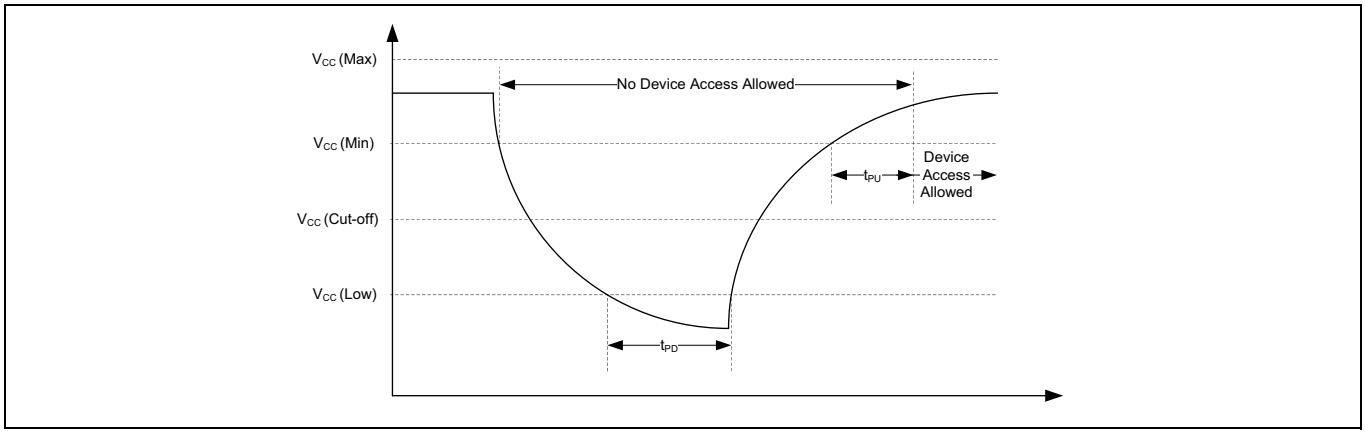


Figure 34 Power down and voltage drop

6 Registers

Registers are small groups of storage cells used to configure as well as report the status of the device operations. The device of devices use separate non-volatile and volatile storage groups to implement the different register bit types for legacy compatibility as well as new functionality. Each register is organized as a group of volatile bits with associated non-volatile bits (if permanence is required). During power-up, hardware or CS signaling reset or software reset, the data in the non-volatile bits of the register is transferred to the volatile bits to provide the default state of the volatile bits. When writing new data to non-volatile bits of the register, the volatile bits are also updated with the new data. However, when writing new data to the volatile register bits the non-volatile bits retain the old data. The register structure is shown in **Figure 35**.

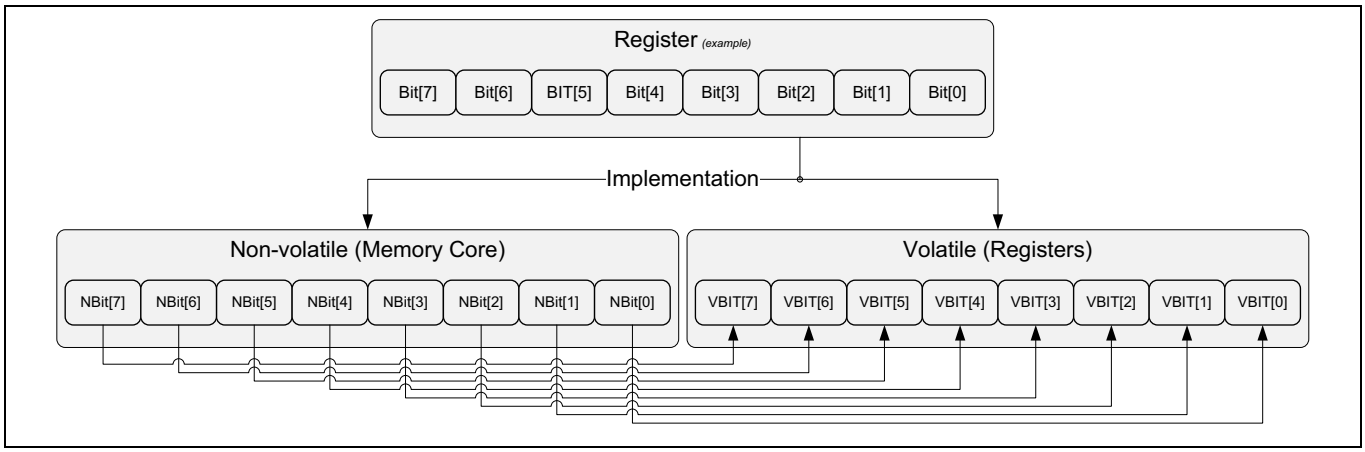


Figure 35 Register structure

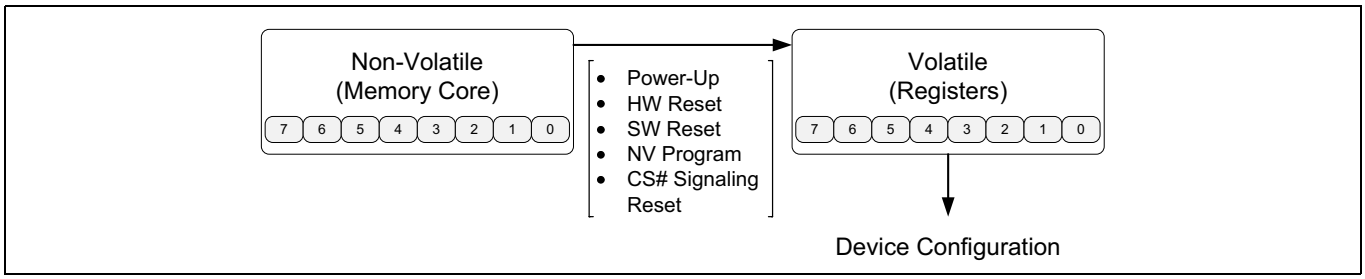


Figure 36 Data movement within register components

6.1 Register naming convention

Table 35 Register bit description convention

Bit number	Name	Function	Read/write	Factory default (Binary)	Description
REGNAME#T[x] T = N, V, O Descending Order	–	–	Possible Options: N/A - Not Applicable R - Readable Only R/W - Readable and Writable R/1 - Readable and One Time Programmable	Possible Options: 0 1	Format: Description of the Configuration bit 0 = Option '0' selection of the Bit 1 = Option '1' selection of the Bit Dependency: This Bit may be part of a function which requires multiple bits for implementation.

6.2 Status Register 1 (STR1x)

Status Register 1 contains both status and control bits. The functionality of supported Status Register 1 type is described in **Table 36**.

Table 36 Status Register 1[12]

Bit number	Name	Function	Read/write N = Non-volatile V = Volatile	Factory default (Binary)	Description
STR1N[7] STR1V[7]	STCFWR	Status Register 1 and Configuration Protection Selection against write (erase/program)	N->R/W V->R/W	0	Description: The STCFWR bit selects enabling and disabling writes (erase/program) to Status Register 1 and configuration registers 1, 2, 3, 4 based on WP# (Write Protect Pin) in Single SPI mode. When STCFWR bit is enabled with WP# LOW, any transaction that can change status or configuration registers is ignored, effectively locking the state of the device. If WP#/DQ[2] is HIGH (irrespective of STCFWR), Status and Configuration Registers can be changed. Selection Options: 1 = WP# based protection is enabled 0 = WP# based protection is disabled Dependency: N/A
STR1V[6]	PRGERR	Programming Error Status Flag	V -> R	0	Description: The PRGERR bit indicates program operation success or failure. When the PRGERR bit is set to a '1', it indicates that there was an error in the last programming operation. PRGERR bit is also set when a program operation is attempted within a protected memory region. When PRGERR is set, it can only be cleared with the Clear Program and Erase Failure Flags transaction or a hardware/software reset (see **Table 37**). **Note** The device will only go to standby mode once the PRGERR flag is cleared. Selection Options: 0 = Last programming operation was successful 1 = Last programming operation was unsuccessful Dependency: N/A

Note
12.STR1x value during POR, Hardware Reset, CS# Signaling Reset, Software Reset and DPD Exit is not valid.

Table 36 Status Register 1[12] (Continued)

Bit number	Name	Function	Read/write N = Non-volatile V = Volatile	Factory default (Binary)	Description
STR1V[5]	ERSERR	Erasing Error Status Flag	V -> R	0	Description: The ERSERR bit indicates erase operation success or failure. When the ERSERR bit is set to a '1', it indicates that there was an error in the last erasing operation. ERSERR bit is also set when a erase operation is attempted within a protected memory sector. When ERSERR is set, it can only be cleared with the Clear Program and Erase Failure Flags transaction or a hardware/software reset (see **Table 38**). **Note** The device will only go to standby mode once the ERSERR flag is cleared. Selection Options: 0 = Last erase operation was successful 1 = Last erase operation was unsuccessful Dependency: N/A
STR1N[4:2] STR1V[4:2]	LBPROT[2:0]	Legacy Block Protection based Memory Array size selection	If PLPROT = 0 N -> R/W V -> R/W If PLPROT = 1 N -> R V -> R	000	Description: The LBPROT[2:0] bits define the memory array size to be protected against program and erase transactions. Based on the LBPROT[2:0] configuration, either top 4, 8, 16, etc.sectors or bottom 4, 8, 16, etc.sectors, or up to the entire array is protected. **Note** If PLPROT bit - Permanent Locking selection of Legacy Block Protection the LBPROT[2:0] bits cannot be erased or programmed. Selection Options: 000 = Protection is disabled 001 = 4 sectors of the (top/bottom) array protection is enabled 010 = 8 sectors of the (top/bottom) array protection is enabled ….. 111 = All sectors are protected, except last 2 sectors [254, 255] Dependency: TBPROT (CFR1x[5])

Note
12.STR1x value during POR, Hardware Reset, CS# Signaling Reset, Software Reset and DPD Exit is not valid.

Table 36 Status Register 1[12] (Continued)

Bit number	Name	Function	Read/write N = Non-volatile V = Volatile	Factory default (Binary)	Description
STR1V[1]	WRPGEN	Write/Program Enable Status Flag	V -> R	0	Description: The WRPGEN bit must be set to '1' to enable all program, erase or register write operations - it provides protection against inadvertent changes to memory or register values. The Write Enable and Write Enable Volatile transactions set the WRPGEN bit to '1' to allow program, erase or write transactions to execute. The Write Disable (WRDIS_0_0) transaction resets WRPGEN to a '0' to prevent all program, erase, and write transactions from execution. The WRPGEN bit is cleared to '0' at the end of any successful program, erase or register write operation. After a power down / power up sequence or a hardware/software reset, the Deep Power Down WRPGEN bit is cleared to '0'. Selection Options: 0 = Program, erase or register write is disabled 1 = Program, erase or register write is enabled Dependency: N/A
STR1V[0]	RDYBSY	Device Ready/Busy Status Flag	V -> R	0	Description: The RDYBSY bit indicates whether the device is performing an embedded operation or is in standby mode ready to receive new transactions. **Note** The PRGERR and ERSERR status bits are updated while RDYBSY is set. If PRGERR or ERSERR are set, the RDYBSY bit will remain set indicating the device is busy and unable to receive new transactions. A Clear Program and Erase Failure Flags transaction must be executed to return the device to standby mode. Selection Options: 0 = Device is in standby mode ready to receive new operation transactions 1 = Device is busy and unable to receive new operation transactions Dependency: N/A

Note
12.STR1x value during POR, Hardware Reset, CS# Signaling Reset, Software Reset and DPD Exit is not valid.

Table 37 PRGERR summary

Error flag	Symbol	Conditions
Program Error	PRGERR	Bits cannot be programmed '1' to '0'
		Trying to program in a protected region in ECC data unit

Table 38 ERSERR summary

Error flag	Symbol	Conditions
Erase Error	ERSERR	Sector Device Erase - All bits cannot be erased to '1's
		Trying to erase a protected regions
		Register Erase - All bits cannot be erased to '1's during Erase portion of Register Write

6.3 Status Register 2 (STR2x)

Status Register 2 provides device status on operations. The functionality of supported Status Register 2 type is described in **Table 39**.

Table 39 Status Register 2[13]

Bit number	Name	Function	Read/write N = Non-volatile V = Volatile	Factory default (Binary)	Description
STR2V[7:3]	RESRVD	Reserved for future use	V -> R	0	This bit is Reserved for future use. This bit must always be written/loaded to its default state.
STR2V[2]	SESTAT	Sector Erase Success/Failure Status Flag	V -> R	0	Description: The SESTAT bit indicates whether the erase operation on the sector completed successfully. Evaluate Erase Status transaction must be executed prior to reading SESTAT bit which specifies the sector address. Selection Options: 1 = Addressed sector was erased successfully 0 = Addressed sector was not erased successfully Dependency: N/A
STR2V[1]	ERASES	Erase operation Suspend Status Flag	V -> R	0	Description: The ERASES bit is used to indicate if the Erase operation is suspended. Selection Options: 0 = Erase operation is not in suspend mode 1 = Erase operation is in suspend mode Dependency: N/A
STR2V[0]	PROGMS	Program operation Suspend Status Flag	V -> R	0	Description: The PROGMS bit is used to indicate if the Program operation is suspended. Selection Options: 0 = Program operation is not in suspend mode 1 = Program operation is in suspend mode Dependency: N/A

Note
13. STR2x value during POR, Hardware Reset, CS# Signaling Reset, Software Reset and DPD Exit is not valid. STR2x bits are valid only when STR1V[0] / RDYBSY = 0.

6.4 Configuration Register 1 (CFR1x)

Configuration Register 1 controls interface and data protection functions.

Table 40 Configuration Register 1

Bit number	Name	Function	Read/write N = Non-volatile V = Volatile	Factory default (Binary)	Description
CFR1N[7:6] CFR1V[7:6]	RESRVD	Reserved for future use	V -> R	0	This bit is Reserved for future use. This bit must always be written/loaded to its default state.
CFR1N[5] CFR1V[5]	TBPROT	Top or Bottom Protection selection for Legacy Protection Mode	If PLPROT = 0 N -> R/W V -> R If PLPROT = 1 N -> R V -> R	0	Description: The TBPROT bit selects the reference point of the Legacy Block Protection bits (LBPROT[2:0]) in the Status Register on whether the protection starts from the top or starts from the bottom of the address range. (see **Table 41**). Selection Options: 0 = Legacy Protection is applicable in the top half of the address range 1 = Legacy Protection is applicable in the bottom half of the address range Dependency: LBPROT[2:0] (STR1x[3:1])
CFR1N[4] CFR1V[4]	PLPROT	Permanent Locking selection of Legacy Block Protection and Sector Architecture option	N -> R/1 V -> R	0	Description: The PLPROT bit permanently protects the Legacy Block Protection. It thereby permanently protects the memory array protection scheme and sector architecture (see **Table 41**). **Note** PLPROT protects LBPROT[2:0], TBPROT[5], and SECOPT[3:0] bits from program and erase. It is recommended to configure these bits before configuring the PLPROT bit. Selection Options: 0 = Legacy Block Protection and Sector Architecture option are not protected 1 = Legacy Block Protection and Sector Architecture option are protected Dependency: N/A
CFR1N[3:2] CFR1V[3:2]	RESRVD	Reserved for future use	V -> R	00	This bit is Reserved for future use. This bit must always be written/loaded to its default state.

Table 40 Configuration Register 1 (Continued)

Bit number	Name	Function	Read/write N = Non-volatile V = Volatile	Factory default (Binary)	Description
CFR1N[1] CFR1V[1]	QUADIT	Quad SPI Interface Selection - I/O width set to 4 bits (1-1-4, 1-4-4)	N -> R/W V -> R/W	1	Description: The QUADIT bit selects the I/O width of the device. When configured to 4-bits (QUAD), WP# becomes DQ2 and The QUADIT transactions require Opcode sent on a single I/O, Address either on a single or all four I/Os and Data always sent on all four I/Os. Selection Options: 0 = Data Width set to 1 (1x - Single) 1 = Data Width set to 4 wide (4x - Quad) Dependency: N/A
CFR1N[0] CFR1V[0]	TLPROT	Temporary Locking selection of Legacy Block Protection	N -> R V -> R/W	0	Description: The TLPROT bit temporarily protects the Legacy Block Protection. Upon power-up or a hardware or CS# signaling reset, TLPROT is set to its default state. When selected, it protects the memory array protection scheme from any changes. **Note** TLPROT protects LBPROT[2:0], TBPROT[5], bits from program and erase. Selection Options: 0 = Legacy Block Protection are not protected 1 = Legacy Block Protection are temporarily protected Dependency: N/A

Table 41 PLPROT and TLPROT protection

PLPROT	TLPROT	Array and sector architecture protection
0	0	Unprotected (Unlocked)
1	x	LBPROT[2:0], TBPROT[5], and SECOPT[3:0] Permanently Protected (Locked)
0	1	LBPROT[2:0], and TBPROT[5] Protected (Locked) till next Power-down

6.5 Configuration Register 2 (CFR2x)

Configuration Register 2 controls address byte length selection.

Table 42 Configuration Register 2

Bit number	Name	Function	Read/write N = Non-volatile V = Volatile	Factory default (Binary)	Description
CFR2N[7] CFR2V[7]	ADRBYT	Address Byte Length selection between 3 or 4 bytes for Instructions	N -> R/W V -> R/W	1	Description: The ADRBYT bit controls the expected address length for all instructions that require address and is selectable between 3 Bytes or 4 Bytes. Selection Options: 0 = Instructions will use 3 Bytes for address 1 = Instructions will use 4 Bytes for address Dependency: N/A
CFR2N[6:3] CFR2V[6:3]	RESRVD	Reserved for future use	N -> R/W V -> R/W	0	These bits are Reserved for future use. This bit must always be written/loaded to its default state.
CFR2N[2:0] CFR2V[2:0]	MEMLAT[2:0]	Memory Array Read Latency selection - Dummy cycles required for initial data access	N -> R/W V -> R/W	000	Description: The MEMLAT[2:0] bits control the read latency (dummy cycles) delay in all variable latency memory array and non-volatile register read transactions. MEMLAT selection allows the user to adjust the read latency during normal operation based on different operating frequencies (see **Table 43**). Selection Options: 000 = 8 Latency Cycle Selection based on transaction opcodes ….. 111 = 15 Latency Cycles Selection based on transaction opcodes Dependency: N/A

Table 43 Latency code (cycles) versus frequency[14, 15, 16, 17]

Latency code	Latency cycles	Read transaction maximum frequency (MHz)	
		RDAY2_C_0 (1-1-1), RDSSR_C_0 (1-1-1), RDECC_C_0 (1-1-1), RDECC_4_0 (1-1-1), RDARG_C_0 (1-1-1)[18], RDAY4_C_0 (1-1-4), RDAY4_4_0 (1-1-4)	RDAY5_C_0 (1-4-4), RDAY5_4_0 (1-4-4)
		Mode cycle = 0	Mode cycle = 2
0 (Default)	8	80	60
1	9	80	70
2	10	80	80
3	11	80	80
4	12	104	80
5	13	104	80
6	14	104	104
7	15	104	104

Notes
14. When using the ECC error reporting mechanisms, the read output data must be at least 2 bytes for correct ECC reporting.
15. CK frequency > 104 MHz SDR, is not supported by this family of devices.
16. The Quad I/O, protocols include Continuous Read Mode bits following the address. The clock cycles for these bits are not counted as part of the latency cycles shown in the table. For example, the Quad I/O transaction has two Continuous Read mode cycles following the address. Therefore, the Quad I/O transaction without additional read latency is supported only up to the frequency shown in the table for a read latency of 0 cycles. By increasing the variable read latency, the frequency of the Quad I/O transaction can be increased to allow operation up to the maximum supported 104 MHz frequency.
17. Read SFDP transaction always have a dummy cycle of 8 and the maximum frequencies for different interfaces related to eight dummy cycles. Read Unique ID has 8 cycles of latency.
18. Read Any Register transaction uses these latency cycles for reading non-volatile registers.

6.6 Configuration Register 3 (CFR3x)

Configuration Register 3 controls Buffer size.

Table 44 Configuration Register 3

Bit number	Name	Function	Read/write N = Non-volatile V = Volatile	Factory default (Binary)	Description
CFR3N[7:6] CFR3V[7:6]	RESRVD	Reserved for future use	N -> R/W V -> R/W	00	This bit is Reserved for future use. This bit must always be written/loaded to its default state.
CFR3N[5] CFR3V[5]	BLKCHK	Blank Check selection during Erase operation for better endurance	N -> R/W V -> R/W	1	Description: When this feature is enabled, an erase transaction first evaluates the erase status of the sector. If the sector is found to erased, the erase operation is aborted. In other words, the erase operation is only executed if programmed bits are found in the sector. Disabling BLKCHK executes an erase operation unconditionally. Selection Options: 0 = Blank Check is disabled before executing an erase operation 1 = Blank Check evaluation is enabled before executing an erase operation Dependency: N/A
CFR3N[4] CFR3V[4]	PGMBUF	Program Buffer Size selection	N -> R/W V -> R/W	0	Description: The PGMBUF bit selects the Programming Buffer size which is used for page programming. Program buffer size affects the device programming time. **Note** If programming data exceeds the program buffer size, data gets wrapped. Selection Options: 0 = 256 Byte Write Buffer Size 1 = 512 Byte Write Buffer Size Dependency: N/A
CFR3N[3:0] CFR3V[3:0]	RESRVD	Reserved for future use	N -> R/W V -> R/W	0000	This bit is Reserved for future use. This bit must always be written/loaded to its default state.

6.7 Configuration Register 4 (CFR4x)

Configuration Register 4 controls output driver impedance.

Table 45 Configuration Register 4

Bit number	Name	Function	Read/write N = Non-volatile V = Volatile	Factory default (Binary)	Description
CFR4N[7:5] CFR4V[7:5]	IOIMPD[2:0]	I/O Driver Output Impedance selection	N -> R/W V -> R/W	000	Description: The IOIMPD[2:0] bits select the IO driver output impedance (drive strength). The output impedance configuration bits adjust the drive strength during normal device operation to meet system signal integrity requirements. Selection Options: 000 = 45 Ω (Factory Default) 001 = 120 Ω 010 = 90 Ω 011 = 60 Ω 100 = 45 Ω 101 = 30 Ω 110 = 20 Ω 111 = 15 Ω
CFR4N[4] CFR4V[4]	RESRVD	Reserved for future use	N -> R/W V -> R/W	0	This bit is Reserved for future use. This bit must always be written/loaded to its default state.
CFR4N[3] CFR4V[3]	ECC12S	Multi-pass programming	N -> R/W V -> R/W	1	Description: The ECC12S bit selects between multi-pass programming enabled, 1-bit ECC error detection/correction or multi-pass programming disabled with both 1-bit ECC error detection and correction / 2-bit ECC error detection. The host needs to erase and reprogram the data in the Semper Flash memory upon ECC configuration change. Selection Options: 0 = Multi-pass programming enabled with 1-bit ECC Error Detection/Correction. Multi-pass programming in the ECC data unit will disable ECC in that unit. 1 = Multi-pass programming disabled with1-bit ECC Error Detection/Correction and 2-bit ECC error detection. Multi-pass programming in the ECC data unit will cause a program error. Dependency: N/A
CFR4N[2:0] CFR4V[2:0]	RESRVD	Reserved for future use	N -> R/W V -> R/W	000	This bit is Reserved for future use. This bit must always be written/loaded to its default state.

6.8 Architecture Configuration Register (ARCFN)

Architecture Configuration Register sector architecture options. After writing the ARCFN[3:0] bits there need to be CS# Signaling Reset, Hardware Reset or Power on Reset to activate memory architecture on the device.

Architecture configuration needs to be set at initial configuration of the device before any programming of memory array.

If the architecture configuration needs to be changed from Factory default, this can be done only once by writing the SECOPT bits to select the desired configuration. After this change, the SECOPT bits are locked and no further changes to architecture are allowed.

If the default configuration option SECOPT bits are written to the same value, the default configuration option is locked and cannot be changed.

Table 46 Architecture Configuration Register

Bit number	Name	Function	Read/write N = Non-volatile V = Volatile	Factory default (Binary)	Description
ARCFN[7:4]	RESRVD	Reserved for future use	N -> R/W	0	These bits are Reserved for future use. This bit must always be written/loaded to its default state.
ARCFN[3:0]	SECOPT	Memory Sector Options	N -> R/1	0101 (Model 10) 0000 (Model 11)	Description: The SECOPT[3:0] bits selects the option of memory array architecture for sector 2bpc and 1bpc (see **"Flash memory array"** on page 19). Selection Options: 0000 = Option 0 1000 = Option 8 0001 = Option 1 1001 = Option 9 0010 = Option 2 1010 = Option 10 0011 = Option 3 1011 = Option 11 0100 = Option 4 1100 = Option 12 0101 = Option 5 1101 = Option 13 0110 = Option 6 1110 = Option 14 0111 = Option 7 1111 = Option 15 **Notes** • If PLPROT bit - Permanent Locking selection of Architecture the ARCFN[3:0] bits cannot be erased or programmed. • Options 8 -15 are Reserved for Future Use. • Factory Default setting are by OPN model number. Dependency: PLPROT (CFR1x[4])

To changed configuration to another option, three actions are needed to complete the procedure:

- An erase operation of the previously defined 1bpc sectors will need to be performed. This can be done in two ways:
  - Chip Erase
  - Sector Erase of previously define 1bpc sectors
- The Blank Check bit (GLKCHK) needs to be disabled (CFR3x[5] = 0) before executing the chip or sector erase operation to make sure 1bpc sectors are erased. This is needed even if they are already blank.
- Check the ERSERR bit in status register is '1' to verify erase operation completed with no error.

6.9 ECC Status Register (ECSV)

The ECC Status Register (ECSV) contains the ECC status of any error correction action performed on the unit data whose byte was addressed during last read.

Unit data is defined as the number of bytes over which the ECC is calculated. The devices have a 16 bytes (128 bits) unit data.

Table 47 ECC Status Register

Bit number	Name	Function	Read/write N = Non-volatile V = Volatile	Factory default (Binary)	Description
ECSV[7:5]	RESRVD	Reserved for future use	V -> R	000	This bit is Reserved for future use. This bit must always be written/loaded to its default state.
ECSV[4]	ECC2BT	ECC Error 2-bit Error Detection Flag	V -> R	0	Description: The ECC2BT bit indicates that a 2-bit ECC Error was detected in the data unit (16 bytes). A Clear ECC Status Register transaction (CLECC_0_0) will reset ECC2BT. **Note** ECC2BT is updated every time any memory address is read and is sticky, i.e. once it is set, it remains set. The ECC2BT status is maintained until a Clear ECC Status Register transaction (CLECC_0_0) is executed. **Note** ECC1BT is not valid if ECC2BT status flag is set. Selection Options: 0 = No 2-Bit ECC Error was detected in the data unit (16 bytes) 1 = 2-bit ECC Error was detected in the data unit (16 bytes) Dependency: N/A
ECSV[3]	ECC1BT	ECC Error 1-bit Error Detection and Correction Flag	V -> R	0	Description: The ECC1BT bit indicates that a 1-bit ECC Error was detected and corrected in the data unit (16 bytes). A Clear ECC Status Register transaction (CLECC_0_0) will reset ECC1BT. **Note** ECC1BT is updated every time any memory address is read and is sticky, i.e. once it is set, it remains set. The ECC1BT status is maintained until a Clear ECC Status Register transaction (CLECC_0_0) is executed. Selection Options: 0 = No 1-Bit ECC Error was detected in the data unit (16 bytes) 1 = 1-bit ECC Error was detected in the data unit (16 bytes) Dependency: N/A
ECSV[2:0]	RESRVD	Reserved for future use	V -> R	000	This bit is Reserved for future use. This bit must always be written/loaded to its default state.

7 Transaction tables

7.1 1-1-1 transaction table

Table 48 1-1-1 transaction table

Function	Transaction name	Description	Prerequisite transaction	Byte 1 (Hex)	Byte 2 (Hex)	Byte 3 (Hex)	Byte 4 (Hex)	Byte 5 (Hex)	Byte 6 (Hex)	Byte 7 (Hex)	Byte 8 (Hex)	Transaction format	Max freq. (MHz)	Address length
Read Device ID	RDIDN_0_0	**Read manufacturer and device identification** transaction provides read access to manufacturer and device identification.	–	9F (CMD)	–	–	–	–	–	–	–	Figure 9	104	N/A
	RSFDP_3_0	**Read JEDEC Serial Flash Discoverable Parameters** transaction sequentially accesses the Serial Flash Discovery Parameters (SFDP).	–	5A (CMD)	ADDR [23:16]	ADDR [15:8]	ADDR [7:0]	–	–	–	–	Figure 10	50	3
	RDUID_0_0	**Read Unique ID** accesses a factory programmed 64-bit number which is unique to each device.	–	4C (CMD)	–	–	–	–	–	–	–	Figure 9	104	N/A
Register Access	RDSR1_0_0	**Read Status Register 1** transaction allows the Status Register 1 contents to be read from DQ1/SO.	–	05 (CMD)	–	–	–	–	–	–	–			
	RDSR2_0_0	**Read Status Register-2** transaction allows the Status Register-2 contents to be read from DQ1/SO.	–	07 (CMD)	–	–	–	–	–	–	–			
	RDCR1_0_0	**Read Configuration Register-1** transaction allows the Configuration Register-1 contents to be read from DQ1/SO.	–	35 (CMD)	–	–	–	–	–	–	–			
	RDARG_C_0	**Read Any Register** transaction provides a way to read all addressed non-volatile and volatile device registers.	–	65 (CMD)	ADDR [23:16]	ADDR [15:8]	ADDR [7:0]	–	–	–	–	Figure 10		3
			–		ADDR [31:24]	ADDR [23:16]	ADDR [15:8]	ADDR [7:0]	–	–	–			4
	WRENB_0_0	**Write Enable** sets the Write Enable Latch bit of the Status Register 1 to '1' to enable write, program, and erase transactions.	–	06 (CMD)	–	–	–	–	–	–	–	Figure 5		N/A
	WRENV_0_0	**Write Enable Volatile** enable write of volatile Registers.	–	50 (CMD)	–	–	–	–	–	–	–			
	WRDIS_0_0	**Write Disable** sets the Write Enable Latch bit of the Status Register 1 to '0' to disable write, program, and erase transactions executaion.	–	04 (CMD)	–	–	–	–	–	–	–			
Register Access	WRREG_0_1	**Write Register** transaction provides a way to write Status Register 1 and Configuration Registers 1–4 & ANCFN	WRENB_0_0	01 (CMD)	Input STR1 data [7:0]	Input CFR1 data [7:0]	Input CFR2 data [7:0]	Input CFR3 data [7:0]	Input CFR4 data [7:0]	Input ARCF data [7:0]	–	Figure 8	104	
	WRARG_C_1	**Write Any Register** transaction provides a way to write all addressed non-volatile and volatile device registers.	WRENB_0_0	71 (CMD)	ADDR [23:16]	ADDR [15:8]	ADDR [7:0]	Input Data [7:0]	–	–	–	Figure 7		3
					ADDR [31:24]	ADDR [23:16]	ADDR [15:8]	ADDR [7:0]	Input Data [7:0]	–	–			4
	CLPEF_0_0	**Clear Program and Erase Failure Flags** transaction resets STR1V[5] (Erase failure flag) and STR1V[6] (Program failure flag)	WRENB_0_0	82 (CMD)	–	–	–	–	–	–	–	Figure 5		N/A
	EN4BA_0_0	**Enter 4 Byte Address Mode** transaction sets the Address Legth bit CFR2V[7] to 1	–	B7 (CMD)	–	–	–	–	–	–	–			
	EX4BA_0_0	**Exit 4 Byte Address Mode** transaction sets the Address Length bit CFR2V[7] to 0	–	B8 (CMD)	–	–	–	–	–	–	–			

Table 48 1-1-1 transaction table *(Continued)*

Function	Transaction name	Description	Prerequisite transaction	Byte 1 (Hex)	Byte 2 (Hex)	Byte 3 (Hex)	Byte 4 (Hex)	Byte 5 (Hex)	Byte 6 (Hex)	Byte 7 (Hex)	Byte 8 (Hex)	Transaction format	Max freq. (MHz)	Address length
ECC	RDECC_C_0	**Read ECC Status** is used to determine the ECC status of the addressed data unit.	–	19 (CMD)	ADDR [23:16]	ADDR [15:8]	ADDR [7:0]	–	–	–	–	Figure 11	104	3
			–		ADDR [31:24]	ADDR [23:16]	ADDR [15:8]	ADDR [7:0]	–	–	–			4
	RDECC_4_0		–	18 (CMD)	ADDR [31:24]	ADDR [23:16]	ADDR [15:8]	ADDR [7:0]	–	–	–			4
	CLECC_0_0	**Clear ECC Status Register** transaction resets ECC ECC Status Register bit[3] (1-bit ECC Correction), ECC Status Register bit[4] (2-bit ECC Detection)	WRENB_0_0	1B (CMD)	–	–	–	–	–	–	–	Figure 5		N/A
Read Flash Array	RDAY1_C_0	**Read SDR** transaction reads out the memory contents starting at the given address.	–	03 (CMD)	ADDR [23:16]	ADDR [15:8]	ADDR [7:0]	–	–	–	–	Figure 11	50	3
			–		ADDR [31:24]	ADDR [23:16]	ADDR [15:8]	ADDR [7:0]	–	–	–			4
	RDAY1_4_0		–	13 (CMD)	ADDR [31:24]	ADDR [23:16]	ADDR [15:8]	ADDR [7:0]	–	–	–			4
	RDAY2_C_0	**Read Fast SDR** transaction reads out the memory contents starting at the given address.	–	0B (CMD)	ADDR [23:16]	ADDR [15:8]	ADDR [7:0]	–	–	–	–	Figure 10	104	3
			–		ADDR [31:24]	ADDR [23:16]	ADDR [15:8]	ADDR [7:0]	–	–	–			4
Program Flash Array	PRPGE_C_1	**Program Page** programs 256B or 512B data to the memory array in one transaction.	WRENB_0_0	02 (CMD)	ADDR [23:16]	ADDR [15:8]	ADDR [7:0]	Input Data 1 [7:0]	Input Data 2 [7:0]	(Continue)	–	Figure 7	104	3
					ADDR [31:24]	ADDR [23:16]	ADDR [15:8]	ADDR [7:0]	Input Data 1 [7:0]	Input Data 2 [7:0]	(Continue)			4
	PRPGE_4_1		WRENB_0_0	12 (CMD)	ADDR [31:24]	ADDR [23:16]	ADDR [15:8]	ADDR [7:0]	Input Data 1 [7:0]	Input Data 2 [7:0]	(Continue)			4
Erase Flash Array	ERSEC_C_0	**Erase 128-KB or 64-KB Sector** transaction sets all the bits of a sector to 1 (all bytes are FFh).	WRENB_0_0	D8 (CMD)	ADDR [23:16]	ADDR [15:8]	ADDR [7:0]	–	–	–	–	Figure 6	104	3
					ADDR [31:24]	ADDR [23:16]	ADDR [15:8]	ADDR [7:0]	–	–	–			4
	ERSEC_4_0		WRENB_0_0	DC (CMD)	ADDR [31:24]	ADDR [23:16]	ADDR [15:8]	ADDR [7:0]	–	–	–			4
	ERCHP_0_0	**Erase Chip** transaction sets all bits to 1 (all bytes are FFh) inside the entire flash memory array.	WRENB_0_0	60 or C7 (CMD)	–	–	–	–	–	–	–	Figure 5		N/A
	EVERS_C_0	**Evaluate Erase Status** transaction verifies that the last erase operation on the addressed sector was completed successfully.	–	D0 (CMD)	ADDR [23:16]	ADDR [15:8]	ADDR [7:0]	–	–	–	–	Figure 6		3
			–		ADDR [31:24]	ADDR [23:16]	ADDR [15:8]	ADDR [7:0]	–	–	–			4
Suspend / Resume	SPEPD_0_0	**Suspend Erase / Program Check** transaction allows the system to interrupt a programming, erase or data integrity check operation	–	75 (CMD	–	–	–	–	–	–	–	Figure 5	104	N/A
	RSEPD_0_0	**Resume Erase / Program** transaction allows the system to resume a programming, erase or data integrity check operation	–	7A (CMD)	–	–	–	–	–	–	–			

Table 48 1-1-1 transaction table *(Continued)*

Function	Transaction name	Description	Prerequisite transaction	Byte 1 (Hex)	Byte 2 (Hex)	Byte 3 (Hex)	Byte 4 (Hex)	Byte 5 (Hex)	Byte 6 (Hex)	Byte 7 (Hex)	Byte 8 (Hex)	Transaction format	Max freq. (MHz)	Address length
Secure Silicon Region Array	PRSSR_C_1	**Program Secure Silicon Region** transaction programs data in 1024 bytes of Secure Silicon Region	WRENB_0_0	42 (CMD)	ADDR [23:16]	ADDR [15:8]	ADDR [7:0]	Input Data 1 [7:0]	Input Data 2 [7:0]	(Continue)	-	Figure 7	104	3
					ADDR [31:24]	ADDR [23:16]	ADDR [15:8]	ADDR [7:0]	Input Data 1 [7:0]	Input Data 2 [7:0]	(Continue)			4
	RDSSR_C_0	**Read Secure Silicon Region** transaction reads data from the SSR.	–	4B (CMD)	ADDR [23:16]	ADDR [15:8]	ADDR [7:0]	–	–	–	–	Figure 10		3
			–		ADDR [31:24]	ADDR [23:16]	ADDR [15:8]	ADDR [7:0]	–	–	–			4
Reset	SRSTE_0_0	**Software Reset Enable** command is required immediately before a SFRST_0_0 transaction	–	66 (CMD)	–	–	–	–	–	–	–	Figure 5	104	N/A
	SFRST_0_0	**Software Reset** transaction restores the device to its initial power up state, by reloading volatile registers from non-volatile default values	SRSTE_0_0	99 (CMD)	–	–	–	–	–	–	–			
Deep Power Down	ENDPD_0_0	**Enter Deep Power Down Mode** transaction shifts device in the lowest power consumption mode	–	B9 (CMD)	–	–	–	–	–	–	–			

7.2 1-1-4 transaction table

Table 49 1-1-4 transaction table

Function	Transaction name	Description	Prerequisite transaction	Byte 1 (Hex)	Byte 2 (Hex)	Byte 3 (Hex)	Byte 4 (Hex)	Byte 5 (Hex)	Byte 6 (Hex)	Byte 7 (Hex)	Byte 8 (Hex)	Transaction format	Max freq. (MHz)	Address length
Read Flash Array	RDAY4_C_0	**Read SDR Quad Output** transaction reads out the memory contents starting at the given address.	–	6B (CMD)	ADDR [23:16]	ADDR [15:8]	ADDR [7:0]	–	–	–	–	Figure 12	104	3
			–		ADDR [31:24]	ADDR [23:16]	ADDR [15:8]	ADDR [7:0]	–	–	–			4
	RDAY4_4_0		–	6C (CMD)	ADDR [31:24]	ADDR [23:16]	ADDR [15:8]	ADDR [7:0]	–	–	–			
Program Flash Array	PRPG2_C_1	**Program Page Quad Input** programs 256B or 512B data to the memory array in one transaction.	WRENB_0_0	32 (CMD)	ADDR [23:16]	ADDR [15:8]	ADDR [7:0]	Input Data 1 [7:0]	Input Data 2 [7:0]	(Continue)	-	Figure 13	104	3
					ADDR [31:24]	ADDR [23:16]	ADDR [15:8]	ADDR [7:0]	Input Data 1 [7:0]	Input Data 2 [7:0]	(Continue)			4
	PRPG2_4_1		WRENB_0_0	34 (CMD)	ADDR [23:16]	ADDR [15:8]	ADDR [7:0]	ADDR [7:0]	Input Data 1 [7:0]	Input Data 2 [7:0]	(Continue)			

7.3 1-4-4 transaction table

Table 50 1-4-4 transaction table

Function	Transaction name	Description	Prerequisite transaction	Byte 1 (Hex)	Byte 2 (Hex)	Byte 3 (Hex)	Byte 4 (Hex)	Byte 5 (Hex)	Byte 6 (Hex)	Byte 7 (Hex)	Byte 8 (Hex)	Byte 9 (Hex)	Transaction format	Max freq. (MHz)	Address length
Read Flash Array	RDAY5_C_0	**Read SDR Quad I/O** transaction reads out the memory contents starting at the given address.	–	EB (CMD)	ADDR [23:16]	ADDR [15:8]	ADDR [7:0]	Mode [7:0]	–	–	–	–	Figure 14	104	3
			–		ADDR [31:24]	ADDR [23:16]	ADDR [15:8]	ADDR [7:0]	Mode [7:0]	–	–	–			4
	RDAY5_4_0		–	EC (CMD)	ADDR [31:24]	ADDR [23:16]	ADDR [15:8]	ADDR [7:0]	Mode [7:0]	–	–	–			
	RDAY6_C_0	Continuous Read SDR Quad I/O transaction reads out the memory contents starting at the given address.	RDAY5_C_0	ADDR [23:16]	ADDR [15:8]	ADDR [7:0]	Mode [7:0]	–	–	–	–	–	Figure 15		3
				ADDR [31:24]	ADDR [23:16]	ADDR [15:8]	ADDR [7:0]	Mode [7:0]	–	–	–	–			4
	RDAY6_4_0		RDAY5_4_0	ADDR [31:24]	ADDR [23:16]	ADDR [15:8]	ADDR [7:0]	Mode [7:0]	–	–	–	–			

8 Electrical characteristics

8.1 Absolute maximum ratings[19, 20, 21]

Storage temperature plastic packages	–65°C to +150°C
Ambient temperature with power applied	–65°C to + 85°C
V_{CC}	–0.5 V to +2.5 V
Input voltage with respect to Ground (V_{SS})	–0.5 V to V_{CC} + 0.5 V
Output short circuit current	100 mA

8.2 Operating range

Operating ranges define those limits between which the functionality of the device is guaranteed.

8.2.1 Power supply voltages

V_{CC}	1.7 V to 2.0 V

8.2.2 Temperature ranges

Table 51 Temperature range

Parameter	Symbol	Devices	Spec		Unit
			Min	Max	
Ambient temperature	T_A	Industrial	–40	+85	°C
		Commercial	0	+70	

8.3 Thermal resistance

Table 52 Thermal resistance

Parameter	Description	Test Condition		24-ball BGA	WLCSP	Unit
Theta JA	Thermal resistance (Junction to ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance in accordance with EIA/JESD51	With still air (0 m/s)	37.1	23	°C/W
Theta JB	Thermal resistance (Junction to board)			19	5	
Theta JC	Thermal resistance (Junction to case)			11	0.3	

8.4 Capacitance characteristics

Table 53 Capacitance

Package	Input capacitance		Output capacitance	
	Typ	Min	Typ	Max
24-ball BGA	3.0 pF	6.5 pF	7.0 pF	7.5 pF

Notes
19. See **"Input signal overshoot"** on page 69 for allowed maximums during signal transition.
20. No more than one output may be shorted to ground at a time. Duration of the short circuit should not be greater than one second.
21. Stresses above those listed under **Absolute maximum ratings[19, 20, 21]** may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this datasheet is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.

8.5 Latchup characteristics

Table 54 Latchup specification[22]

Description	Min	Max	Unit
V_{CC} Current	–100	+100	mA

8.6 DC characteristics

8.6.1 Input signal overshoot

During DC conditions, input or I/O signals should remain equal to or between V_{SS} and V_{CC}. During voltage transitions, inputs or I/Os may overshoot V_{SS} to –1.0 V or overshoot to V_{CC} + 1.0 V, for periods up to 20 ns.

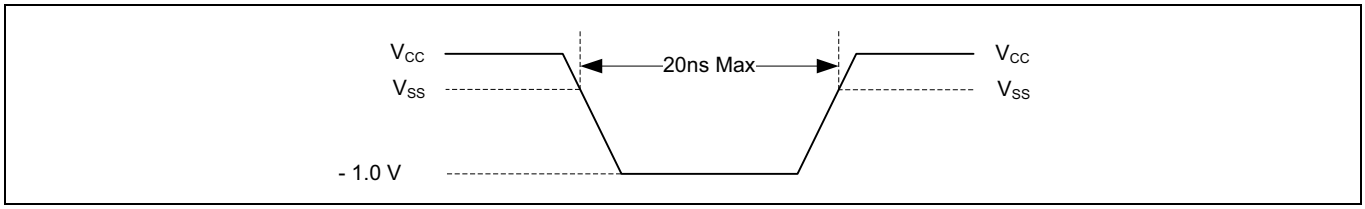


Figure 37 Maximum negative overshoot waveform

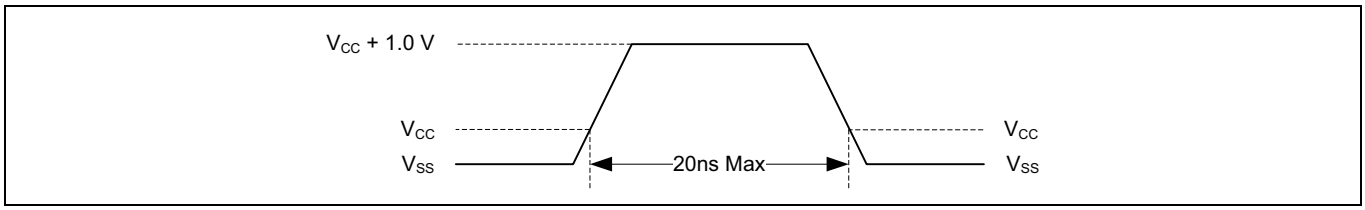


Figure 38 Maximum positive overshoot waveform

Note
22.Excludes power supply V_{CC}. Test conditions: V_{CC} = 1.8 V one connection at a time tested, connections not being tested are at V_{SS}.

8.6.2 DC characteristics (all temperature ranges)

Table 55 DC characteristics[23, 24]

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit	Reference figure
V_{IL}	Input Low voltage	–	$V_{CC} \times -0.15$	–	$V_{CC} \times 0.35$	V	–
V_{IH}	Input High voltage	–	$V_{CC} \times 0.65$	–	$V_{CC} \times 1.15$		
V_{OL}	Output Low voltage	At 0.1 mA	–	–	0.2		
V_{OH}	Output High voltage	At –0.1 mA	V_{CC} – 0.20	–	–		
I_{LI}	Input leakage current	$V_{CC} = V_{CC}$ Max; $V_{IN} = V_{IH}$ or V_{SS}; CS# = V_{IH}	–	–	±2	µA	
I_{LO}	Output leakage current	$V_{CC} = V_{CC}$ Max; $V_{IN} = V_{IH}$ or V_{SS}; CS# = V_{IH}	–	–	±2		
I_{CC1}	Active power supply current (READ)[24]	50 MHz	–	10	15	mA	
		80 MHz	–	17	20		
		104 MHz	–	19	25		
I_{CC2}	Active power supply current (Page Program)	$V_{CC} = V_{CC}$ Max; CS# = V_{IH}	–	29	38		
I_{CC3}	Active power supply current (Write Register and Write Any Register)	$V_{CC} = V_{CC}$ Max; CS# = V_{IH}	–	29	42		
I_{CC4}	Active power supply current (Sector Erase)	$V_{CC} = V_{CC}$ Max; CS# = V_{IH}	–	27	38		
I_{CC5}	Active power supply current (Chip Erase)	$V_{CC} = V_{CC}$ Max; CS# = V_{IH}	–	40	55		
I_{SB}	Standby current @ 85°C	RESET#, CS# = V_{CC}; All I/Os = V_{CC} or V_{SS}	–	5	100	µA	
I_{SB}	Standby current @ 70°C	RESET#, CS# = V_{CC}; All I/Os = V_{CC} or V_{SS}	–	5	55		
I_{DPD}	DPD current @ 85°C	RESET#, CS# = V_{CC}; All I/Os = V_{CC} or V_{SS}	–	1	10		
I_{DPD}	DPD current @ 70°C	RESET#, CS# = V_{CC}; All I/Os = V_{CC} or V_{SS}	–	1	7.5		
I_{POR}	POR current (Average)	CS# = V_{CC}; All I/Os = V_{CC} or V_{SS}	–	–	25	mA	
Power up / Power down voltage							
V_{CC}(min)	V_{CC} (Minimum operation voltage)	–	1.7	–	–	V	Figure 33 / Figure 34
V_{CC}(cut-off)	V_{CC} (Cut off where re-initialization is needed)	–	1.55	–	–	V	Figure 34
V_{CC}(Low)	V_{CC} (Low voltage for initialization to occur)	–	0.7	–	–	V	

Notes
23.Typical values are at T_{AI} = 25°C and V_{CC} = 1.8 V.
24.Outputs unconnected during read data return. Output switching current is not included.

8.7 AC test conditions

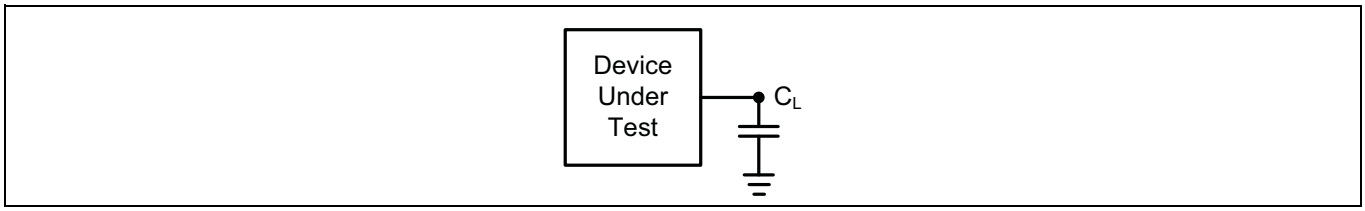


Figure 39 Test setup

Table 56 AC measurement conditions[26]

Parameter	Min	Max	Unit	Reference figure
Load capacitance (C_L)	–	30	pF	Figure 39
Input pulse voltage	0	V_{CC}	V	–
Input Rise (t_{CRT}) and Fall (t_{CFT}) slew rates at 80 MHz[25]	0.38	–	V/ns	Figure 43
Input Rise (t_{CRT}) and Fall (t_{CFT}) slew rates at 104 MHz[25]	0.75	–	V/ns	
$V_{IL(ac)}$	$-0.30 \times V_{CC}$	$0.30 \times V_{CC}$	V	–
$V_{IH(ac)}$	$0.70 \times V_{CC}$	$1.30 \times V_{CC}$		
$V_{OH(ac)}$	$0.75 \times V_{CC}$	–		
$V_{OL(ac)}$	–	$0.25 \times V_{CC}$		
Input timing ref voltage	$0.5 \times V_{CC}$			
Output timing ref voltage				

Notes
25.Input slew rate measured from input pulse min to max at V_{CC} max.
26.AC characteristics tables assume clock and data signals have the same slew rate (slope).

9 Timing characteristics

Table 57 Timing characteristics[27]

Symbol	Parameter	Min	Typ	Max	Unit	Reference figure
SDR timing characteristics						
f_{CK}	Clock frequency	DC	–	104	MHz	–
p_{CK}	CK clock period	$1/f_{CK}$	–	∞	ns	Figure 43
t_{CH}	Clock High time	45% p_{CK}	–	55% p_{CK}		
t_{CL}	Clock Low time		–			
t_{CS}	CS# High time (Read transactions)	10	–	–		Figure 44
	CS# High time (Program / Erase transactions)	50	–	–		
t_{CSS}	CS# Active setup time relative to CK ($f_{CK} \leq 50$ MHz / $f_{CK} > 50$ MHz)	5 / 4	–	–		
t_{CSH0}	CS# Active hold time (relative to CK in Mode 0)	4	–	–		
t_{CSH3}	CS# Active hold time (relative to CK in Mode 3)	6	–	–		
t_{SU}	Data setup time (all V_{CC}) ($f_{CK} \leq 50$ MHz / $f_{CK} > 50$ MHz)	5 / 2	–	–		
t_{HD}	Data Hold time (all V_{CC}) ($f_{CK} \leq 50$ MHz / $f_{CK} > 50$ MHz)	5 / 2	–	–		
t_V	Clock Low to Output Valid (15 pF Loading)[28]	–	–	6		Figure 45
	Clock Low to Output Valid (30 pF Loading)[28]	–	–	8		
t_{HO}	Output Hold time[29]	1.5	–	–		
t_{DIS}	CS# Inactive to Output Disable time	–	–	8		
t_{WPS}	WP# Setup time (Applicable as a constraint for write register transactions when STCFWR is set to '1')	20	–	–		Figure 46
t_{WPH}	WP# Hold time (Applicable as a constraint for write register transactions when STCFWR is set to '1')	20	–	–		
Power up / power down timing						
t_{PU}	V_{CC}(min) to Read operation	–	–	450	µs	Figure 33
t_{PD}	V_{CC}(Low) time	25	–	–		Figure 34
t_{VR}[30]	V_{CC} Power Up ramp rate	1	–	–	µs/V	–
t_{VF}	V_{CC} Power Down ramp rate	30	–	–		

Notes
27. Output HI-Z is defined as the point where data is no longer driven.
28. Applicable across all operating temperature options.
29. Typical program and erase times assume the following conditions: 25°C, V_{CC} = 1.8 V; checkerboard data pattern.
30. Values are guaranteed by characterization and not 100% tested in production.
31. Guaranteed by design.
32. The Joint Electron Device Engineering Council (JEDEC) standard JESD22-A117 defines the procedural requirements for performing valid endurance and retention tests based on a qualification specification. This methodology is intended to determine the ability of a flash device to sustain repeated data changes without failure (program/erase endurance) and to retain data for the expected life (data retention). Endurance and retention qualification specifications are specified in JESD47 or may be developed using knowledge-based methods as in JESD94.
33. Minimum Output load of 15 pF.

Table 57 Timing characteristics[27] (Continued)

Symbol	Parameter	Min	Typ	Max	Unit	Reference figure
Deep power down mode timing						
t_{ENTDPD}[32]	Time to Enter DPD mode	–	–	3	µs	–
t_{EXTDPD}	Time to Exit DPD mode	–	–	430		Figure 32
t_{CSDPD}	Chip Select pulse width to Exit DPD	0.02	–	3		
t_{BYDPD}	Chip Select pulse to RD/BY# to LOW	–	–	30		
Reset timing						
t_{RS}	Reset setup - RESET# HIGH before CS# LOW	50	–	–	ns	Figure 25 Figure 26 Figure 27
t_{RH}	Reset Pulse Hold - RESET# LOW to CS# LOW	450	–	–	µs	
t_{RP}	RESET# pulse width	200	–	–	ns	
t_{SR}	Internal Device Reset from Software Reset command	–	–	60	µs	Figure 31
t_{SRRBL}	RD/BY# Low from Software Reset command	–	–	80	ns	
t_{RBL}	RD/BY# Low from RESET# Low	–	–	25	µs	Figure 25 Figure 26 Figure 27
CS# signaling reset timing						
t_{CSLW}	Chip Select LOW	500	–	–	ns	Figure 30
t_{CSHG}	Chip Select HIGH	500	–	–		
t_{RESET}	Internal device reset	–	–	450	µs	
t_{SUJ}	Data in Setup time (w.r.t CS#)	50	–	–	ns	
t_{HDJ}	Data in Hold time (w.r.t CS#)	50	–	–		
t_{CSRBL}	RD/BY# LOW from CS# Signaling reset	–	–	25	µs	
Embedded algorithm (erase, program performance[29, 32]**)**						
t_W	Non-volatile Register Write time	–	700	2600	ms	–
t_{PP}	256B page programming	–	590	2300	µs	
t_{PP}	512B page programming	–	840	2300		
t_{SE}	Sector Erase time (128 KB 2bpc)	–	660	1600	ms	–
	Sector Erase time (64 KB 1bpc)	–	700	2600		
t_{BE}	Chip Erase time	–	128	665	sec	–
t_{EES}	Evaluate Erase Status time	–	45	51	µs	–
t_{BUSY}	Embedded Algorithm valid to RD/BY# Delay	–	–	80	ns	Figure 49 Figure 50 Figure 31
t_{RB}	RD/BY# Recovery time	–	0	–		
Program, erase suspend/resume timing						
t_{PEDS}	Program / Erase Suspend	–	–	75	µs	–

Notes
27.Output HI-Z is defined as the point where data is no longer driven.
28.Applicable across all operating temperature options.
29.Typical program and erase times assume the following conditions: 25°C, V_{CC} = 1.8 V; checkerboard data pattern.
30.Values are guaranteed by characterization and not 100% tested in production.
31.Guaranteed by design.
32.The Joint Electron Device Engineering Council (JEDEC) standard JESD22-A117 defines the procedural requirements for performing valid endurance and retention tests based on a qualification specification. This methodology is intended to determine the ability of a flash device to sustain repeated data changes without failure (program/erase endurance) and to retain data for the expected life (data retention). Endurance and retention qualification specifications are specified in JESD47 or may be developed using knowledge-based methods as in JESD94.
33.Minimum Output load of 15 pF.

9.1 Timing waveforms

9.1.1 Key to timing waveform

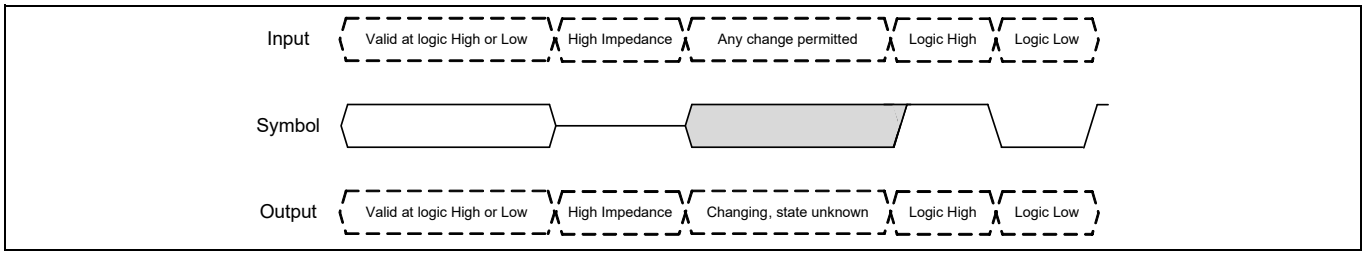


Figure 40 Waveform element meaning

9.1.2 Timing reference levels

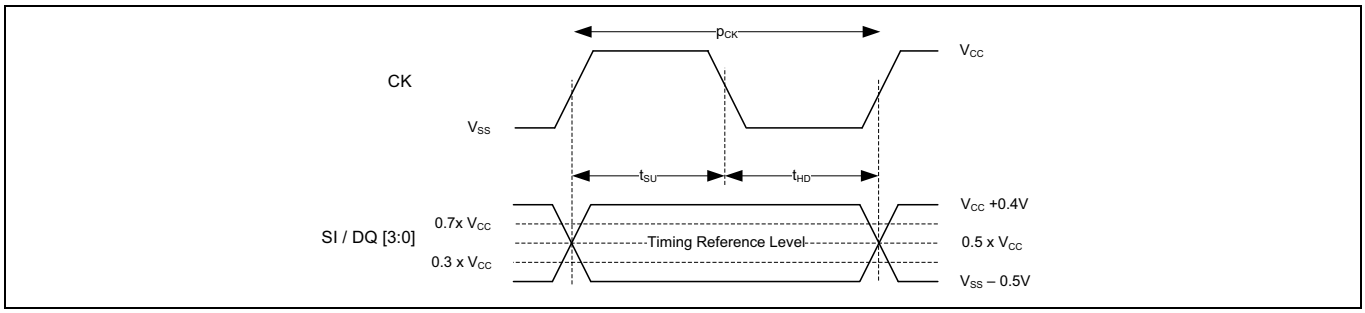


Figure 41 SDR input timing reference level

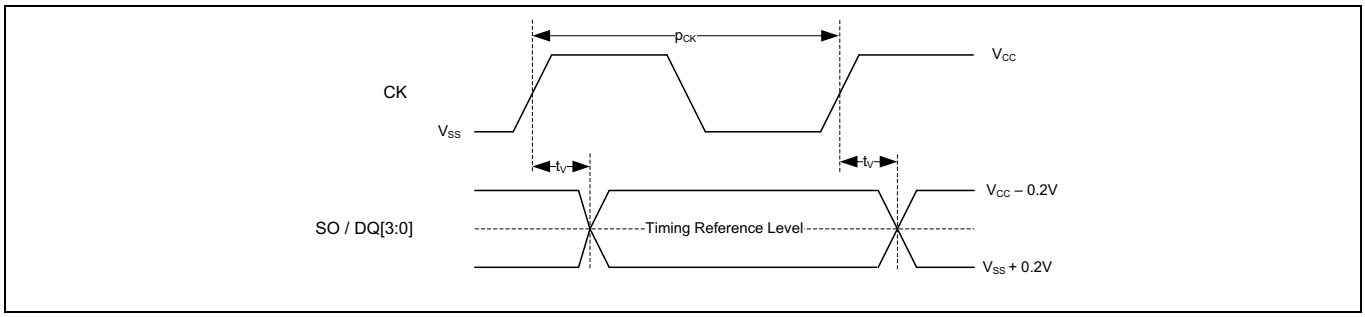


Figure 42 SDR output timing reference level

9.1.3 Clock timing

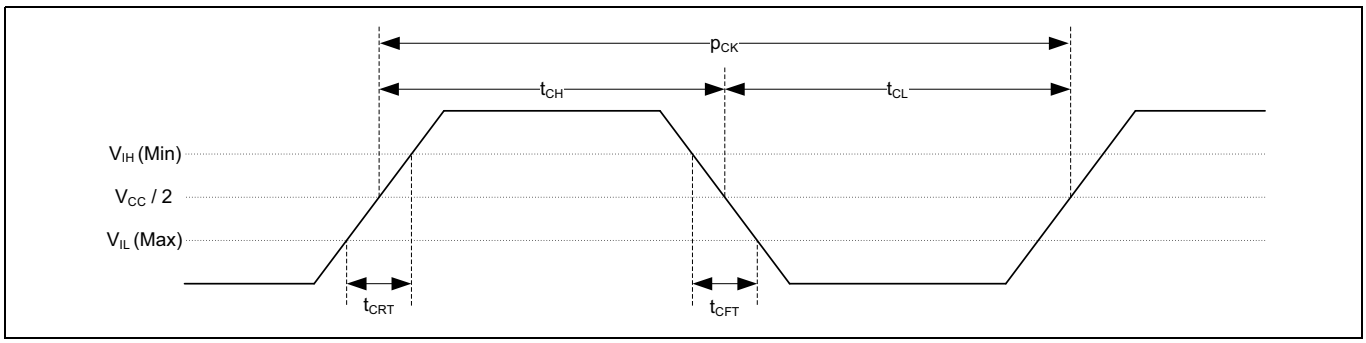


Figure 43 Clock timing

9.1.4 Input / output timing

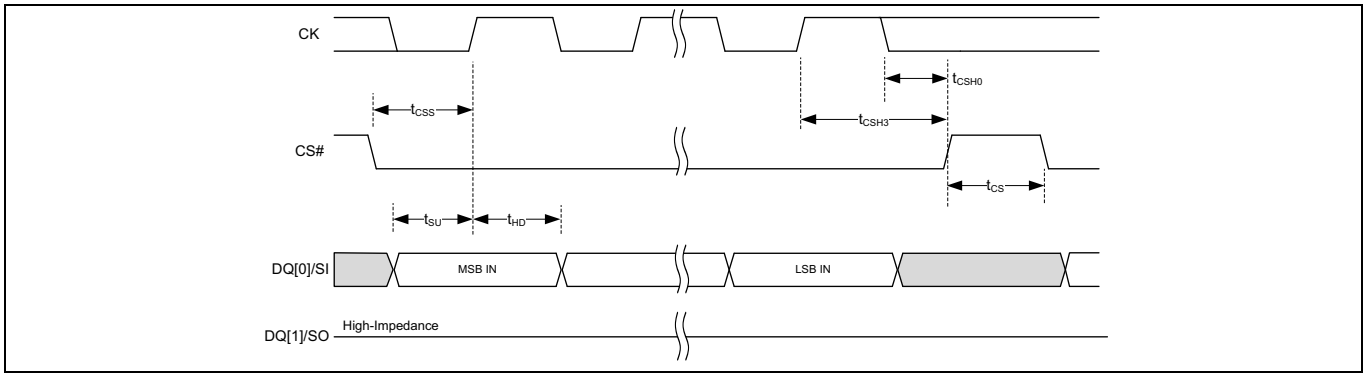


Figure 44 SPI input timing

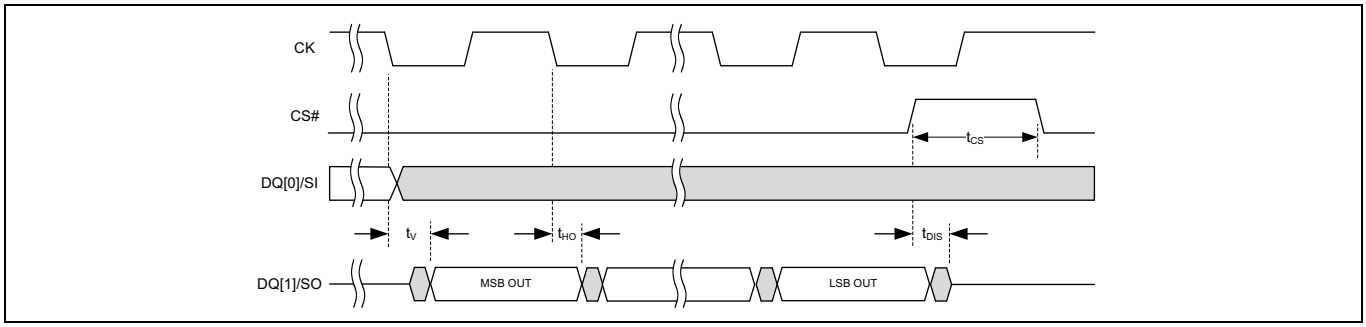


Figure 45 SPI output timing

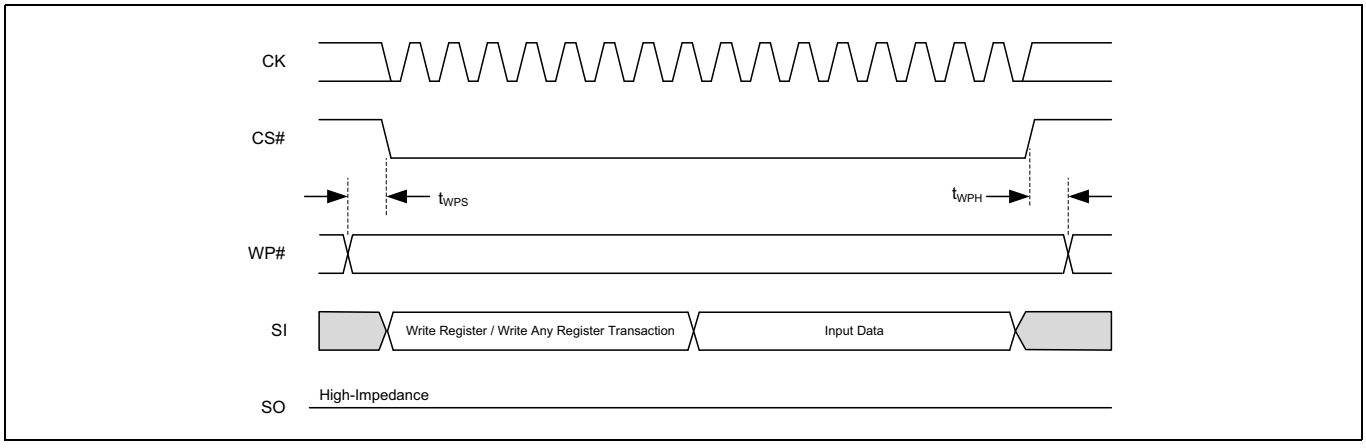


Figure 46 WP# input timing

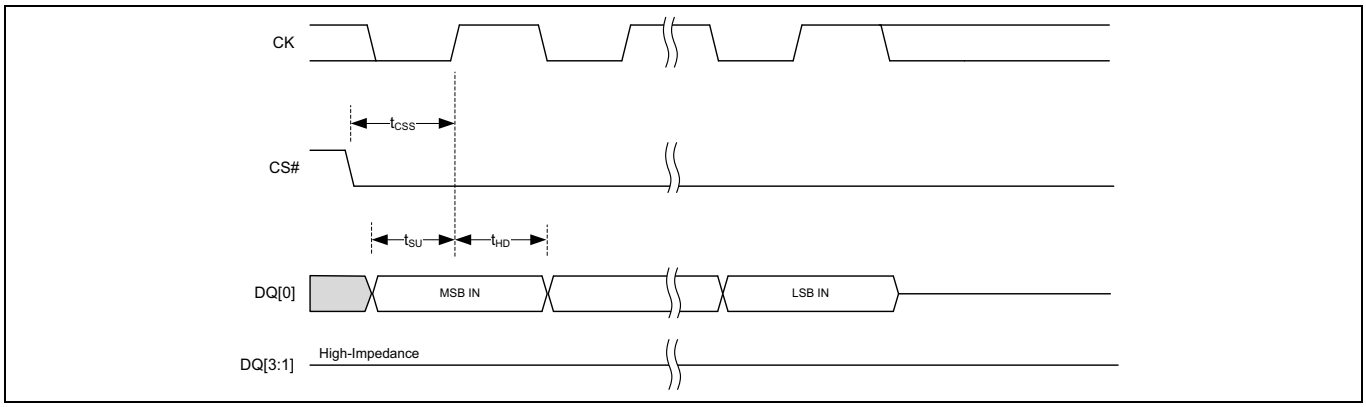


Figure 47 Quad input timing

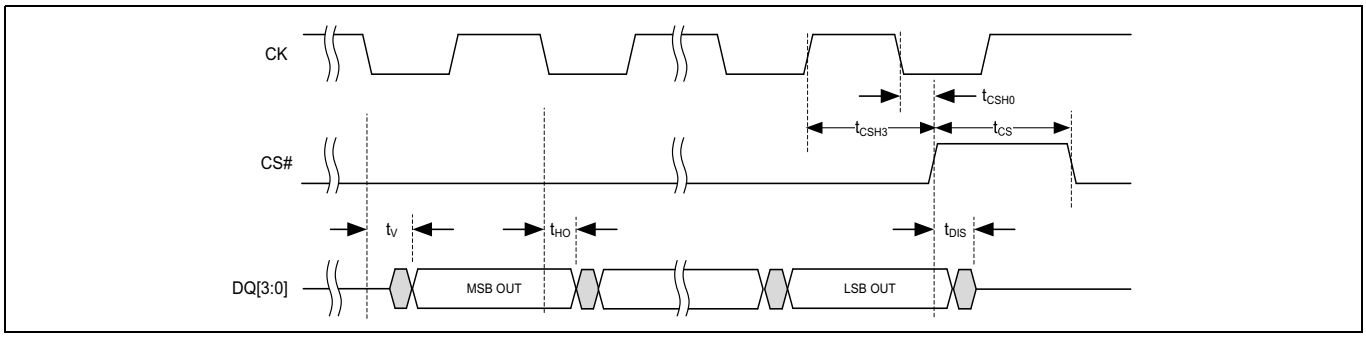


Figure 48 Quad output timing

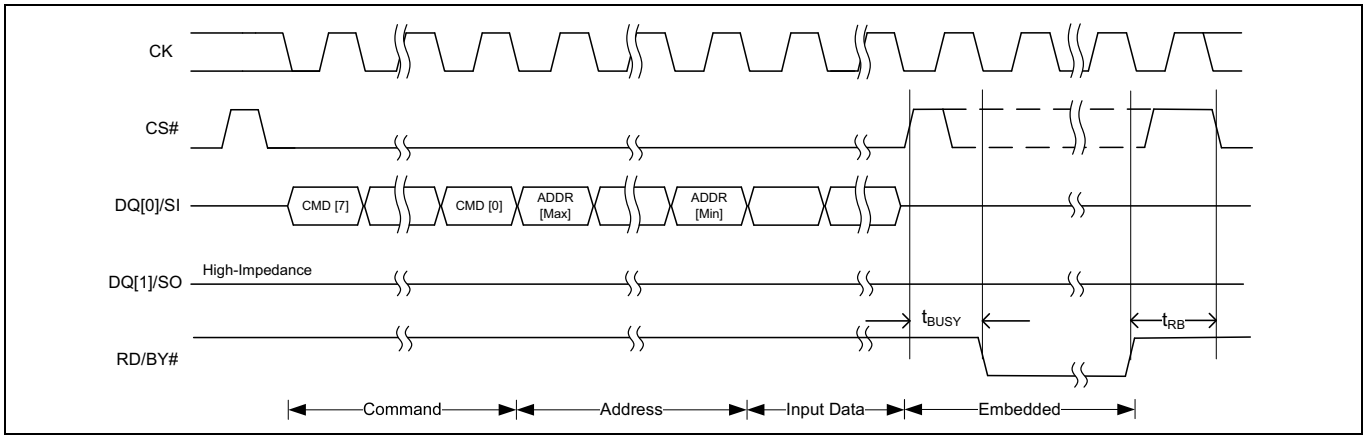


Figure 49 RD/BY# program timing

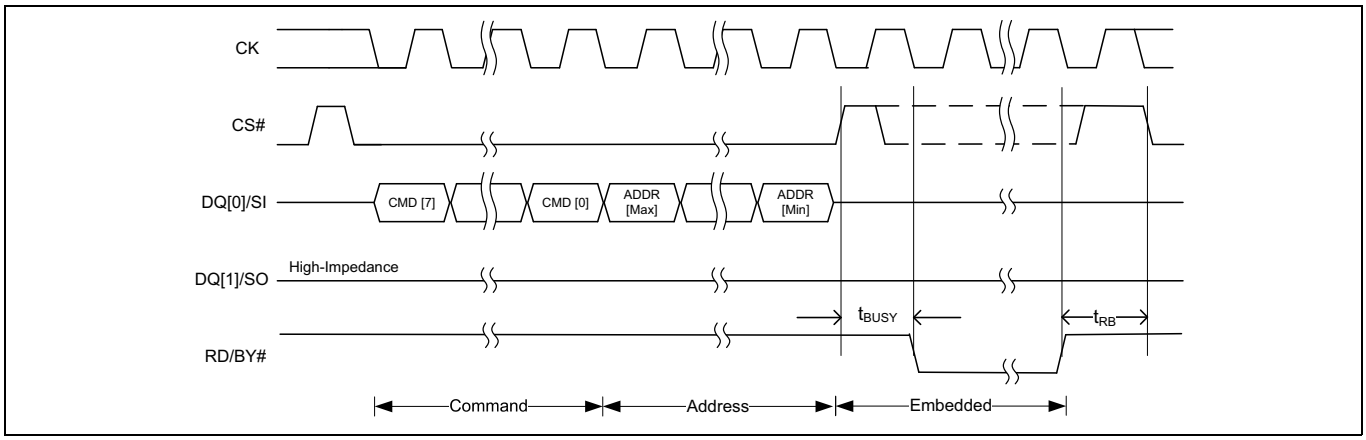


Figure 50 RD/BY# erase timing

10 Device identification

10.1 JEDEC SFDP Rev D

10.1.1 JEDEC SFDP Rev D header table

Table 58 JEDEC SFDP Rev D header table

SFDP byte address	SFDP DWORD name	Data	Description
00h	SFDP Header	53h	This is the entry point for Read SFDP (5Ah) command i.e., location zero within SFDP space ASCII “S”
01h		46h	ASCII “F”
02h		44h	ASCII “D”
03h		50h	ASCII “P”
04h		08h	SFDP Minor Revision (08h = JEDEC JESD216 Revision D)
05h		01h	SFDP Major Revision (01h = JEDEC JESD216 Revision D) This is the original major revision. This major revision is compatible with all SFDP reading and parsing software.
06h		01h	Number of Parameter Headers (zero based, 01h = 2 parameters)
07h		FFh	SFDP Access Protocol (Backward Compatible)
08h	1st Parameter Header	00h	Parameter ID LSB (00h = JEDEC SFDP Basic SPI Flash Parameter)
09h		00h	Parameter Minor Revision (00h = JEDEC JESD216 Revision D)
0Ah		01h	Parameter Major Revision (01h = The original major revision - all SFDP software is compatible with this major revision.)
0Bh		14h	Parameter Table Length (14h = 20 DWORDs are in the Parameter table)
0Ch		00h	Parameter Table Pointer Byte 0 (DWORD = 4-byte aligned) JEDEC Basic SPI Flash parameter byte offset = 0100h
0Dh		01h	Parameter Table Pointer Byte 1
0Eh		00h	Parameter Table Pointer Byte 2
0Fh		FFh	Parameter ID MSB (FFh = JEDEC defined legacy Parameter ID)
10h	2nd Parameter Header	84h	Parameter ID LSB (84h = 4-Byte Address Instruction Table)
11h		00h	Parameter Table Minor Revision (00h = JEDEC JESD216 Revision D)
12h		01h	Parameter Table Major Revision (01h = JEDEC JESD216 Revision D)
13h		02h	Parameter Table Length (2h = 2 DWORDs are in the Parameter table)
14h		50h	Parameter Table Pointer Byte 0 (DWORD = 4-byte aligned) 4-Byte Address Instruction Table byte offset = 0150h address
15h		01h	Parameter Table Pointer Byte 1
16h		00h	Parameter Table Pointer Byte 2
17h		FFh	Parameter ID MSB (FFh = JEDEC defined Parameter)

10.1.2 JEDEC SFDP Rev D parameter table

Table 59 JEDEC SFDP Rev D parameter table

SFDP byte address	SFDP DWORD name	Data	Description
100h	JEDEC Basic Flash Parameter DWORD-1	E7h	Bits 7:5 = unused = 111b Bit 4 = 50h is Volatile Status Register write instruction and Status Register is default = 0b Bit 3 = Block Protect Bits are non-volatile / volatile non-volatile = 0b Bit 2 = Program Buffer > 64Bytes = 1b Bits 1:0 = Uniform 4 KB erase is unavailable = 11b
101h		FFh	Bits 15:8 = Uniform 4 KB erase opcode = not supported FFh
102h		E2h	Bit 23 = Unused = 1b Bit 22 = Supports Quad Out (1-1-4) Read = Yes = 1b Bit 21 = Supports Quad I/O (1-4-4) Read = Yes =1b Bit 20 = Supports Dual I/O (1-2-2) Read = No = 0b Bit 19 = Supports DDR = No = 0b Bit 18:17 = Number of Address Bytes = 3- or 4-Bytes = 01b Bit 16 = Supports Dual Out (1-1-2) Read = No = 0b
103h		FFh	Bits 31:24 = Unused = FFh
104h	JEDEC Basic Flash Parameter DWORD-2	FFh	Density in bits, zero based, 256 Mb = 0FFFFFFFh
105h		FFh	
106h		FFh	
107h		0Fh	
108h	JEDEC Basic Flash Parameter DWORD-3	48h	Bits 7:5 = number of Quad I/O (1-4-4) Mode cycles = 010b Bits 4:0 = number of Quad I/O Dummy cycles = 01000b (Initial Delivery State)
109h		EBh	Quad I/O instruction code
10Ah		08h	Bits 23:21 = number of Quad Out (1-1-4) Mode cycles = 000b Bits 20:16 = number of Quad Out Dummy cycles = 01000b
10Bh		6Bh	1-1-4 Quad Out instruction code = 6Bh
10Ch	JEDEC Basic Flash Parameter DWORD-4	FFh	Bits 7:5 = number of Dual Out (1-1-2) Mode cycles = Not supported Bits 4:0 = number of Dual Out Dummy cycles = Not supported
10Dh		FFh	Dual Out instruction code not supported
10Eh		FFh	Bits 23:21 = number of Dual I/O (1-2-2) Mode cycles not supported Bits 20:16 = number of Dual I/O Dummy cycles not supported
10Fh		FFh	Dual I/O instruction code not supported
110h	JEDEC Basic Flash Parameter DWORD-5	EEh	Bits 7:5 RFU = 111b Bit 4 = QPI supported = No = 0b Bits 3:1 RFU = 111b Bit 0 = 2-2-2 not supported = 0b
111h		FFh	Bits 15:8 = RFU = FFh
112h		FFh	Bits 23:16 = RFU = FFh
113h		FFh	Bits 31:24 = RFU = FFh
114h	JEDEC Basic Flash Parameter DWORD-6	FFh	Bits 7:0 = RFU = FFh
115h		FFh	Bits 15:8 = RFU = FFh
116h		00h	Bits 23:21 = number of 2-2-2 Mode cycles = 000b not supported Bits 20:16 = number of 2-2-2 Dummy cycles = 00000b not supported
117h		FFh	2-2-2 instruction code not supported
118h	JEDEC Basic Flash Parameter DWORD-7	FFh	Bits 7:0 = RFU = FFh
119h		FFh	Bits 15:8 = RFU = FFh
11Ah		00h	Bits 23:21 = Number of QPI Mode cycles = 000b not supported Bits 20:16 = Number of QPI Dummy cycles = 00000b not supported
11Bh		FFh	QPI mode Quad I/O (4-4-4) instruction code not supported

Table 59 JEDEC SFDP Rev D parameter table (Continued)

SFDP byte address	SFDP DWORD name	Data	Description
11Ch	JEDEC Basic Flash Parameter DWORD-8	11h	Erase type 1 size 2^N Bytes = 2^17 Bytes = 128 KB (Initial Delivery State)
11Dh		D8h	Erase type 1 instruction
11Eh		10h	Erase type 2 size2^N Bytes = 2^16 Bytes = 64 KB
11Fh		D8h	Erase type 2 instruction
120h	JEDEC Basic Flash Parameter DWORD-9	00h	Erase type 3 size 2^N Bytes = Not Supported
121h		FFh	Erase type 3 instruction = Not Supported = FFh
122h		00h	Erase type 4 size 2^N Bytes = Not Supported
123h		FFh	Erase type 4 instruction = Not Supported = FFh
124h	JEDEC Basic Flash Parameter DWORD-10	51	Bits 31:30 = Erase type 4 Erase, Typical time units (00b: 1 ms, 01b: 16 ms, 10b: 128 ms, 11b: 1 s) = 1S = 11b (RFU) Bits 29:25 = Erase type 4 Erase, Typical time count = 11111b (RFU) Bits 24:23 = Erase type 3 Erase, Typical time units (00b: 1 ms, 01b: 16 ms, 10b: 128 ms, 11b: 1 s) = 1S = 11b (RFU) Bits 22:18 = Erase type 3 Erase, Typical time count = 11111b (RFU) Bits 17:16 = Erase type 2 Erase, Typical time units (00b: 1 ms, 01b: 16 ms, 10b: 128 ms, 11b: 1 s) = 128 ms = 10b Bits 15:11 = Erase type 2 Erase, Typical time count = 00101b (typ erase time = count +1 * units = 6 * 128 ms = 768 ms Bits 10:9 = Erase type 1 Erase, Typical time units (00b: 1 ms, 01b: 16 ms, 10b: 128 ms, 11b: 1 s) = 128 ms = 10b Bits 8:4 = Erase type 1 Erase, Typical time count = 00101b (typ erase time = count +1 * units = 6 * 128 ms = 768 ms) Bits 3:0 = Count = (Max Erase time / (2 * Typical Erase time))- 1 = 0001b
125h		2Ch	
126h		FEh	
127h		FFh	
128h	JEDEC Basic Flash Parameter DWORD-11	81h	Bits 31 = Reserved = 1b Bits 30:29 = Chip Erase Typical time units (00b: 16 ms, 01b: 256 ms, 10b: 4 s, 11b: 64 s) = 11b Bits 28:24 = Chip Erase Typical time count = 00001b Bits 23:19 = Byte Program Typical Time, additional byte = 11111b do not specify. Bits 18:14 = Byte Program Typical Time, first byte = 11111b do not specify Bits 13 = Page Program Typical Time unit (0: 8 µs, 1: 64 µs) = 64 µs = 1b Bits 12:8 = Page Program Typical Time Count = 01001 (typ Program time = count +1 * units = 10 * 64 µs = 640 µs) Bits 7:4 = Page Size (256B) = 2^N bytes = 1000 Bits 3:0 = Count = [Max page program time / (2 * Typical page program time)] - 1 = 0001b
129h		E9h	
12Ah		FFh	
12Bh		E1h	
12Ch	JEDEC Basic Flash Parameter DWORD-12	ECh	Bit 31 = Suspend and Resume supported = 0b Bits 30:29 = Suspend in-progress erase max latency units (00b: 128ns, 01b: 1µs, 10b: 8µs, 11b: 64µs) = 8 µs = 11b Bits 28:24 = Suspend in-progress erase max latency count = 01001, max erase suspend latency = count +1 * units = 10 * 8 µs = 80 µs Bits 23:20 = Erase resume to suspend interval count = 0001b, interval = count +1 * 64 µs = 2 * 64 µs = 128 µs Bits 19:18 = Suspend in-progress program max latency units (00b: 128ns, 01b: 1us, 10b: 8us, 11b: 64µs) = 8 µs = 10b Bits 17:13 = Suspend in-progress program max latency count = 01001, max erase suspend latency = count +1 * units = 10 * 8 µs = 80 µs Bits 12:9 = Program resume to suspend interval count = 0001b, interval = count +1 * 64 µs = 2 * 64 µs = 128 µs Bit 8 = Reserved = 1b Bits 7:4 = Prohibited operations during erase suspend = xxx0b: May not initiate a new erase anywhere (erase nesting not permitted) + xx1xb: May not initiate a page program in the erase suspended sector size + x1xxb: May not initiate a read in the erase suspended sector size + 1xxxb: The erase and program restrictions in bits 5:4 are sufficient = 1110b Bits 3:0 = Prohibited Operations During Program Suspend = xxx0b: May not initiate a new erase anywhere (erase nesting not permitted) + xx0xb: May not initiate a new page program anywhere (program nesting not permitted) + x1xxb: May not initiate a read in the program suspended page size + 1xxxb: The erase and program restrictions in bits 1:0 are sufficient = 1100b
12Dh		23h	
12Eh		19h	
12Fh		49h	

Table 59 JEDEC SFDP Rev D parameter table (Continued)

SFDP byte address	SFDP DWORD name	Data	Description
130h	JEDEC Basic Flash Parameter DWORD-13	7Ah	Bits 31:24 = Suspend Instruction = 75h Bits 23:16 = Resume Instruction = 7Ah Bits 15:8 = Program Suspend Instruction = 75h Bits 7:0 = Program Resume Instruction = 7Ah
131h		75h	
132h		7Ah	
133h		75h	
134h	JEDEC Basic Flash Parameter DWORD-14	F7h	Bits 7:4 = RFU = Fh Bit 3:2 = Status Register Polling Device Busy = 01b: Legacy status polling supported = Use legacy polling by reading the Status Register with 05h instruction and checking WIP bit[0] (0 = ready; 1 = busy). Bits 1:0 = RFU = 11b
135h		66h	Bit 31 = DPD Supported = supported = 0 Bits 30:23 = Enter DPD Instruction = B9h Bits 22:15 = Exit DPD Instruction not supported = 00h Bits 14:13 = Exit DPD to next operation delay units = (00b: 128ns, 01b: 1µs, 10b: 8µs, 11b: 64µs) = 64 µs = 11b Bits 12:8 = Exit DPD to next operation delay count = 00110, Exit DPD to next operation delay = (count+1) * units = (6 + 1) * 64 µs = 448 µs
136h		80h	
137h		5Ch	
138h	JEDEC Basic Flash Parameter DWORD-15	00h	Bits 31:24 = RFU = FFh Bit 23 = HOLD or RESET Disable = Supported = 0 Bits 22:20 = Quad Enable Requirements = 101b Bits 19:16 = 0-4-4 Mode Entry Method = xxx1b: Mode Bits[7:0] = A5h Note: QE must be set prior to using this mode + x1xxb: Mode Bit[7:0] = Axh + 1xxxb: RFU = 1101b Bits 15:10 = 0-4-4 Mode Exit Method = xx_xxx1b: Mode Bits[7:0] = 00h will terminate this mode at the end of the current read operation + xx_x1xxb: RFU + xx_1xxxb: Input Fh (mode bit reset) on DQ0-DQ3 for 8 clocks. This will terminate the mode prior to the next read operation. + x1_xxxxb: Mode Bit[7:0] = Axh + 1x_x1xxb: RFU = 11_0101b Bit 9 = 0-4-4 mode supported = 1b Bits 8:4 = 4-4-4 mode enable sequences = x_xx1xb: Issue instruction 38h. + x_1xxxb: Device uses a read-modify-write sequence of operations: read configuration using instruction 65h followed by address 800003h, set bit 6, write configuration using instruction 71h followed by address 800003h. This configuration is volatile. = 00000 Bits 3:0 = 4-4-4 mode disable sequences = xxx1b: Issue FFh instruction + xx0xb: Issue F5h instruction + x1xxb: Device uses a read-modify-write sequence of operations: read configuration using instruction 65h followed by address 800003h, clear bit 6, write configuration using instruction 71h followed by address 800003h. This configuration is volatile. + 1xxxb: Issue the Soft Reset 66/99 sequence = 0000
139h		D6h	
13Ah		5Dh	
13Bh		FFh	

Table 59 JEDEC SFDP Rev D parameter table (Continued)

SFDP byte address	SFDP DWORD name	Data	Description
13Ch	JEDEC Basic Flash Parameter DWORD-16	F9h	Bits 31:24 = Enter 4-Byte Addressing = xxxx_xxx1b: issue instruction B7h (preceding write enable not required) + xx1x_xxxxb: Supports dedicated 4-Byte address instruction set. Refer to the vendor datasheet for the instruction set definition. + 1xxx_xxxxb: Reserved = 10100001b Bits 23:14 = Exit 4-Byte Addressing =+ x1_xxxx_xxxxb: Reserved + 1x_xxxx_xxxxb: Reserved = 11_0000_0000b Bits 13:8 = Soft Reset and Rescue Sequence Support = x1_xxxxb: Issue reset enable instruction 66h, then issue reset instruction 99h. The reset enable, reset sequence may be issued on 1, 2, or 4 wires depending on the device operating mode. + 1x_xxxxb: Exit 0-4-4 mode is required prior to other reset sequences above if the device may be operating in this mode. = 111000b Bit 7 = RFU = 1 Bits 6:0 = Volatile or Non-volatile Register and Write Enable Instruction for Status Register 1 = xxx_xxx1b: Non-volatile Status Register 1, powers-up to last written value, use instruction 06h to enable write. + xxx_1xxxb: Non-volatile/Volatile Status Register 1 powers-up to last written value in the non-volatile status register, use instruction 06h to enable write to non-volatile status register. Volatile status register may be activated after power-up to override the non-volatile status register, use instruction 50h to enable write and activate the volatile status register. + xx1_xxxxb: Status Register 1 contains a mix of volatile and non-volatile bits. The 06h instruction is used to enable writing of the register. + x1x_xxxxb: Reserved + 1xx_xxxxb: Reserved = 1111001b
13Dh		38h	
13Eh		C0h	
13Fh		A1h	
140h	JEDEC Basic Flash Parameter DWORD-17	00h	Not Supported
141h			
142h			
143h			
144h	JEDEC Basic Flash Parameter DWORD-18	00h	Bits 31: 24 = 00h
145h		00h	Bit 23 = 1b = JEDEC SPI Protocol Reset implemented as described in JESD252
146h		80h	Bits 22:18 = 00000b
147h		00h	Bits 17:0 = 000h
148h	JEDEC Basic Flash Parameter DWORD-19	00h	Not supported
149h			
14Ah			
14Bh			
14Ch	JEDEC Basic Flash Parameter DWORD-20	FFh	Bits 31:16 = Not Supported = 1111_1111_1111_1111b Bit 15:12 = 1111b = 4S-4D-4D Data Strobe is not supported Bit 11:8 = 1111b = 100 MHz 4S-4D-4D is not supported Bit 7:4 = 1111b = 4S-4S-4S Data Strobe is not supported Bit 0:3 = 1111b = 4S-4S-4S is not supported
14Dh		FFh	
14Eh		FFh	
14Fh		FFh	

Table 59 JEDEC SFDP Rev D parameter table (Continued)

SFDP byte address	SFDP DWORD name	Data	Description
150h	JEDEC 4-Byte Address Instructions Parameter DWORD-1	71h	Supported = 1, Not Supported = 0 Bits 31:25 = Reserved = 1111_111b Bit 24 = Support for (1-8-8) Page Program Command, Instruction = 8Eh = 0b Bit 23 = Support for (1-1-8) Page Program Command, Instruction = 84h = 0b Bit 22 = Support for (1-8-8) DTR READ Command, Instruction = FDh = 0b Bit 21 = Support for (1-8-8) FAST_READ Command, Instruction = CCh = 0b Bit 20 = Support for (1-1-8) FAST_READ Command, Instruction = 7Ch = 0b Bit 19 = Support for non-volatile individual sector lock write command, Instruction = E3h = 0b Bit 18 = Support for non-volatile individual sector lock read command, Instruction = E2h = 0b Bit 17 = Support for volatile individual sector lock Write command, Instruction = E1h = 0b Bit 16 = Support for volatile individual sector lock Read command, Instruction = E0h = 0b Bit 15 = Support for (1-4-4) DTR_Read Command, Instruction = EEh = 0b Bit 14 = Support for (1-2-2) DTR_Read Command, Instruction = BEh = 0b Bit 13 = Support for (1-1-1) DTR_Read Command, Instruction = 0Eh = 0b Bit 12 = Support for Erase Command – Type 4 = 0b Bit 11 = Support for Erase Command – Type 3 = 0b Bit 10 = Support for Erase Command – Type 2 = 1b Bit 9 = Support for Erase Command – Type 1 = 1b Bit 8 = Support for (1-4-4) Page Program Command, Instruction = 3Eh = 0b Bit 7 = Support for (1-1-4) Page Program Command, Instruction = 34h = 0b Bit 6 = Support for (1-1-1) Page Program Command, Instruction = 12h = 1b Bit 5 = Support for (1-4-4) FAST_READ Command, Instruction = ECh = 1b Bit 4 = Support for (1-1-4) FAST_READ Command, Instruction = 6Ch = 1b Bit 3 = Support for (1-2-2) FAST_READ Command, Instruction = BCh = 0b Bit 2 = Support for (1-1-2) FAST_READ Command, Instruction = 3Ch = 0b Bit 1 = Support for (1-1-1) FAST_READ Command, Instruction = 0Ch = 0b Bit 0 = Support for (1-1-1) READ Command, Instruction = 13h = 1b
151h		06h	
152h		00h	
153h		FEh	
154h	JEDEC 4-Byte Address Instructions Parameter DWORD-2	DCh	Bits 31:24 = Instruction for Erase Type 4 RFU Bits 23:16 = Instruction for Erase Type 3: RFU Bits 15:8 = DCh = Instruction for Erase Type 2 Bits 7:0 = DCh = Instruction for Erase Type 1
155h		DCh	
156h		FFh	
157h		FFh	

10.2 Manufacturer and Device ID

Table 60 Manufacturer and Device ID

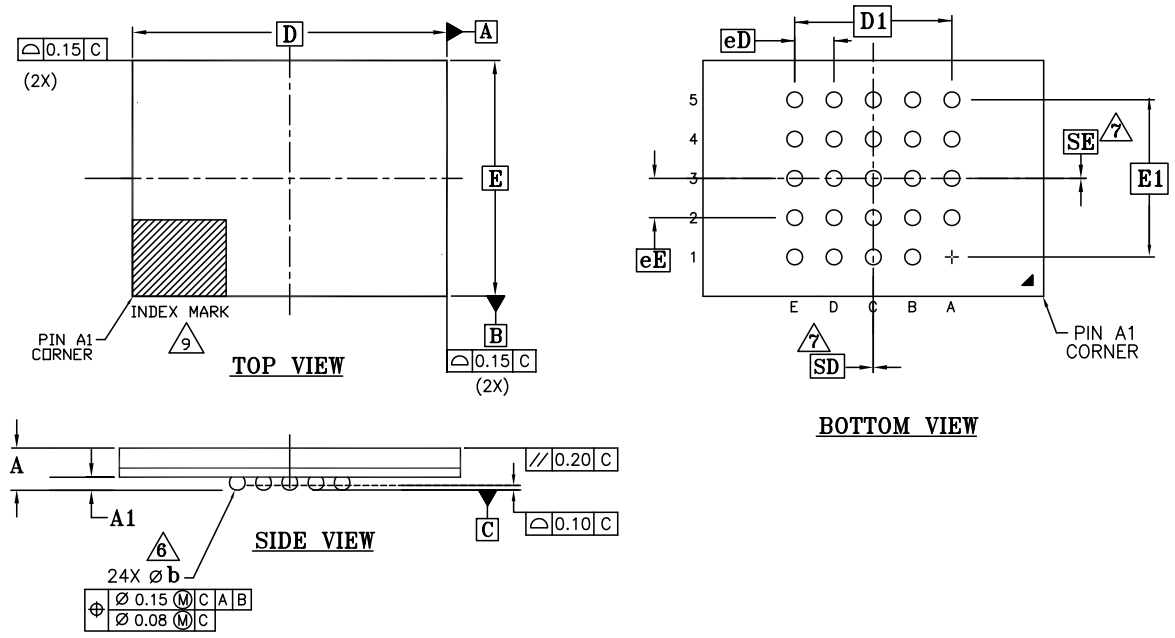
Byte address	Data	Description
00h	34h	Manufacturer ID for CYPRESS (Infineon)
01h	2Bh	Device ID MSB - Memory Interface Type
02h	19h (256 Mb)	Device ID LSB - Density
03h	0Fh	ID Length - number bytes following. Adding this value to the current location of 03h gives the address of the last valid location in the ID legacy address map.
04h	08h (Default Configuration)	Physical Sector Architecture 08h = Uniform 128 KB Sectors
05h	90h (The device)	Family ID
06h–0Fh	FFh	Reserved

10.3 Unique Device ID

Table 61 Unique Device ID

Byte address	Data	Description
00h to 07h	8-Byte Unique Device ID	64-bit unique ID number

10.4 Package diagrams



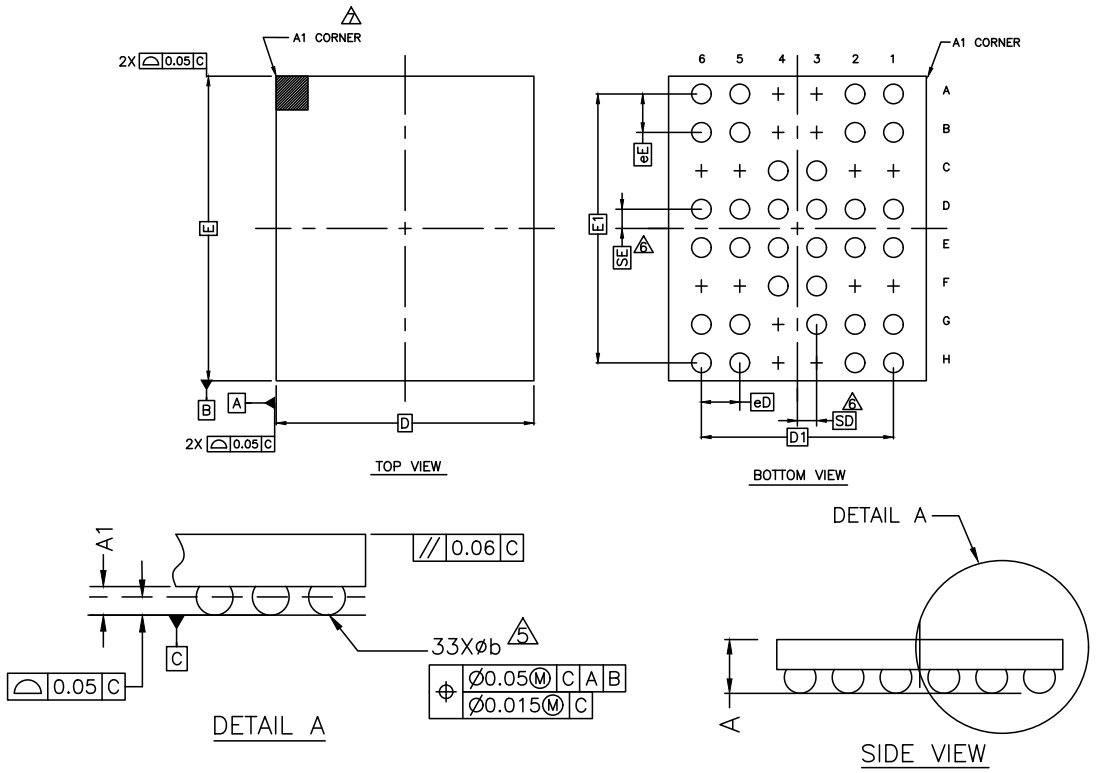
SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	-	-	1.00
A1	0.20	-	-
D		8.00 BSC	
E		6.00 BSC	
D1		4.00 BSC	
E1		4.00 BSC	
MD		5	
ME		5	
N		24	
⌀ b	0.35	0.40	0.45
eE		1.00 BSC	
eD		1.00 BSC	
SD		0.00 BSC	
SE		0.00 BSC	

NOTES:

1. DIMENSIONING AND TOLERANCING METHODS PER ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. BALL POSITION DESIGNATION PER JEP95, SECTION 3, SPP-020.
4. "e" REPRESENTS THE SOLDER BALL GRID PITCH.
5. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.
   SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.
   N IS THE NUMBER OF POPULATED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.
6. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
7. "SD" AND "SE" ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.
   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW "SD" OR "SE" = 0.
   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" = eD/2 AND "SE" = eE/2.
8. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.
9. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK, METALLIZED MARK INDENTATION OR OTHER MEANS.
10. JEDEC SPECIFICATION NO. REF: N/A

002-15550 *A

Figure 51 24-ball BGA (8.0 × 6.0 × 1.0 mm) package outline, 002-15550



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	-	-	0.25
A1	0.058	-	-
D	3.356 BSC		
E	3.965 BSC		
D1	2.50 BSC		
E1	3.50 BSC		
MD	6		
ME	8		
N	33		
Øb	0.225	0.250	0.275
eD	0.50 BSC		
eE	0.50 BSC		
SD/SE	0.25 BSC		

NOTES:

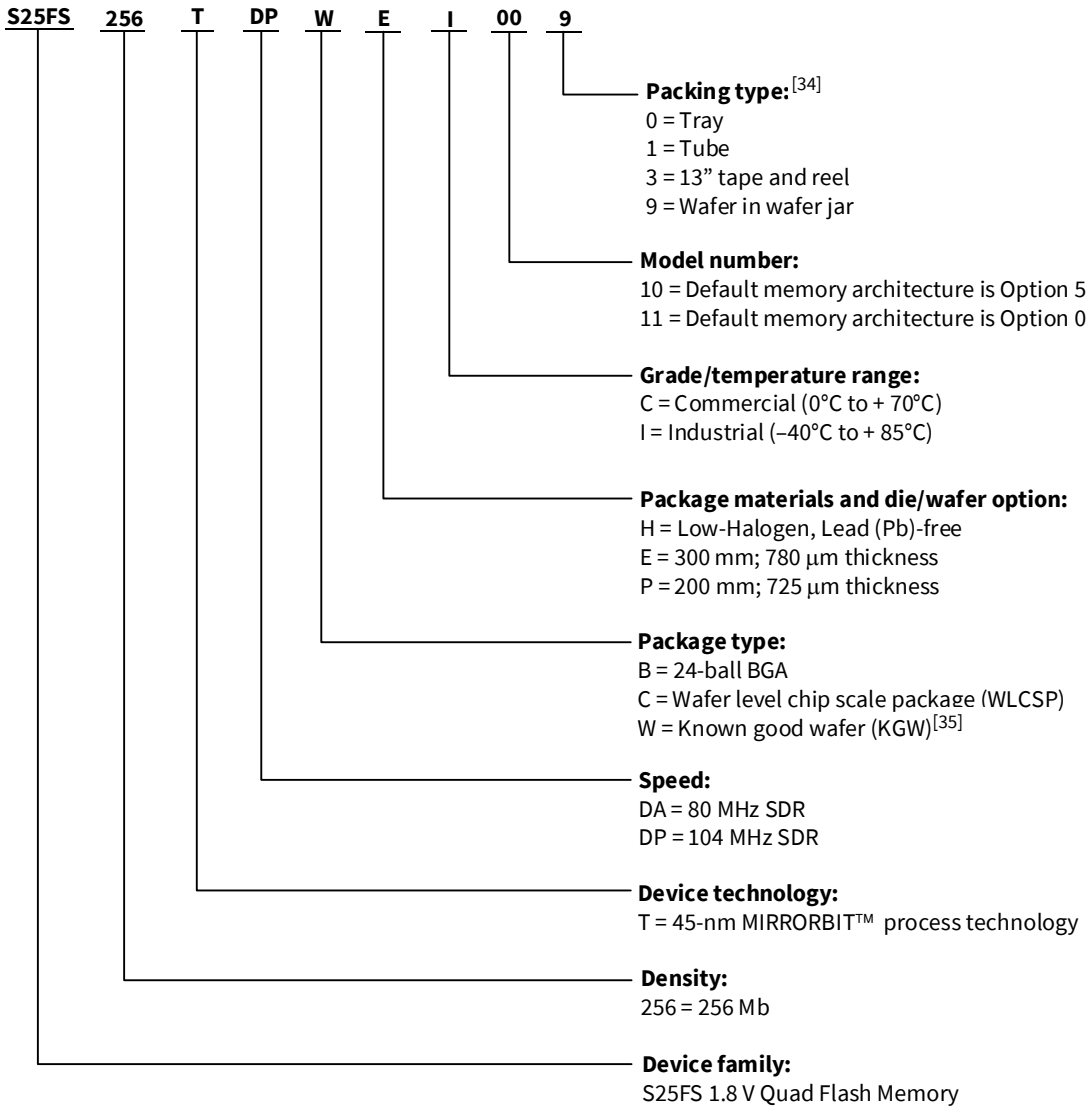
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. SOLDER BALL POSITION DESIGNATION PER JEP95, SECTION 3, SPP-020.
3. "e" REPRESENTS THE SOLDER BALL GRID PITCH.
4. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.
   SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.
   N IS THE NUMBER OF POPULATED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.
5. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
6. "SD" AND "SE" ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.
   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" OR "SE" = 0.
   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" = eD/2 AND "SE" = eE/2.
7. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK, METALIZED MARK, INDENTATION OR OTHER MEANS.
8. JEDEC SPECIFICATION NO. REF. : N/A.

002-29952 *C

Figure 52 33-ball WLCSP (3.356 × 3.965 × 0.25 mm) package outline, 002-29952

11 Ordering information

The ordering part number is formed by a valid combination of the following:



Notes
34.See the **Packing and Packaging Handbook** for further information.
35.Contact Infineon Sales for SEMPER™ Nano KGW datasheet.

11.1 Valid combinations — standard grade

Valid combinations list configurations planned to be supported in volume for this device. Contact your local sales office to confirm availability of specific valid combinations and to check on newly released combinations.

Table 62 Valid combinations — Production

Base ordering part number	Speed option	Package and die/wafer	Temperature range	Model number	Packing type	Ordering part number (x = packing type)	Package marking
S256FS256T	DA	WE	C	10	9	S25FS256TDAWEC10x	–
				11		S25FS256TDAWEC11x	
		CH	I	11	3	S25FS256TDACHI11x	S256AI1
			C	11		S25FS256TDACHC11x	S256AC1

Table 63 Valid combinations — Contact sales

Base ordering part number	Speed option	Package and die/wafer	Temperature range	Model number	Packing type	Ordering part number (x = packing type)	Package marking
S25FS256T	DP	BH	I	11	0, 3	S25FS256TDPBHI11x	25FS256TPI11
	DA	WP	C	10	9	S25FS256TDAWPC10x	–
				11		S25FS256TDAWPC11x	

12 Acronyms

Table 64 Acronyms used in this document

Acronym	Description
DPD	deep power down
EA	embedded algorithms
ECC	error correction code
HIC	host interface controller
KGW	known good wafer
LBP	legacy block protection
LSb	least significant bit
MSb	most significant bit
OTP	one time programmable
POR	power-on reset
QIO	quad I/O
SDR	single data rate
SFDP	serial flash discoverable parameters
2bpc	Two bits per cell
1bpc	One bit per cell

13 Document conventions

13.1 Units of measure

Table 65 Units of measure

Symbol	Unit of measure
°C	degrees Celsius
Hz	hertz
KB	Kilobytes
kHz	kilohertz
kΩ	kilo ohm
MBps	mega byte per second
MHz	megahertz
MΩ	mega-ohm
Msps	megasamples per second
µA	microampere
µF	microfarad
µs	microsecond
µV	microvolt
µW	microwatt
mA	milliampere
mm	millimeters
ms	millisecond
mV	millivolt
nA	nanoampere
ns	nanosecond
Ω	ohm
pF	picofarad
ppm	parts per million
ps	picosecond
s	second
sps	samples per second
V	volt
W	watt

Revision history

Document revision	Date	Description of changes
*J	2022-04-01	Post to external web.
*K	2022-09-21	Updated **Device overview**: Updated description. Updated **Performance summary**: Updated table “Maximum read rates”. Updated **Data integrity**: Updated table “Program / erase (PE) endurance - Commercial (0°C to +70°C) Multi-pass Programming disabled” (caption only). Updated table “Program / erase (PE) endurance - Industrial (–40°C to +85°C) Multi-pass Programming disabled” (caption only). Added table “Program / erase (PE) endurance - Commercial (0°C to +70°C) Multi-pass Programming enabled”. Added table “Program / erase (PE) endurance - Industrial (–40°C to +85°C) Multi-pass Programming enabled”. Updated **Features**: Updated **Read**: Updated **Read registers transactions**: Updated **Read ECC Data Unit Status**: Updated description. Updated **Program**: Updated **Program granularity**: Updated description. Updated **Page programming**: Updated description. Updated **Program Secure Silicon Region transaction**: Updated description. Updated **Error detection and correction**: Updated description. Updated **ECC error reporting**: Updated **ECC Data Unit Status (EDUS)**: Updated description. Updated **Table 21**. Updated **Registers**: Updated **Configuration Register 3 (CFR3x)**: Updated **Table 44**. Updated **Configuration Register 4 (CFR4x)**: Updated **Table 45**. Updated **Electrical characteristics**: Updated **Thermal resistance**: Updated **Table 52**. Updated to new template.
*L	2022-12-21	Updated **Table 62** and **Table 63** in **Valid combinations — standard grade**.

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