DUAL HIGH-SPEED AUDIO OPERATIONAL AMPLIFIER

Check for Samples: LM833

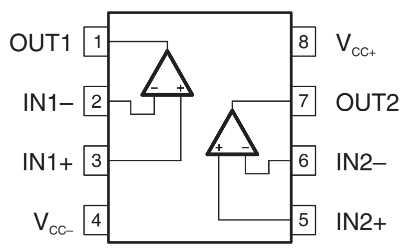
FEATURES

- **Dual-Supply Operation: ±5 V to ±18 V**
- **Low Noise Voltage: 4.5 nV/√Hz**
- **Low Input Offset Voltage: 0.15 mV**
- **Low Total Harmonic Distortion: 0.002%**
- **High Slew Rate: 7 V/µs**
- **High-Gain Bandwidth Product: 16 MHz**
- **High Open-Loop AC Gain: 800 at 20 kHz**
- **Large Output-Voltage Swing: 14.1 V to –14.6 V**
- **Excellent Gain and Phase Margins**
- **Available in 8-Pin MSOP Package (3mm x 4.9mm x 0.65mm)**

APPLICATIONS

- **HiFi Audio System Equipment**
- **Preamplification and Filtering**
- **Set Top Box**
- **Microphone PreAmplifier Circuit**
- **General-Purpose Amplifier Applications**

D (SOIC), DGK (MSOP), OR P (PDIP) PACKAGE (TOP VIEW)



DESCRIPTION

The LM833 is a dual operational amplifier with high-performance specifications for use in quality audio and data-signal applications. This device operates over a wide range of single- and dual-supply voltage with low noise, high-gain bandwidth, and high slew rate. Additional features include low total harmonic distortion, excellent phase and gain margins, large output voltage swing with no deadband crossover distortions, and symmetrical sink/source performance.

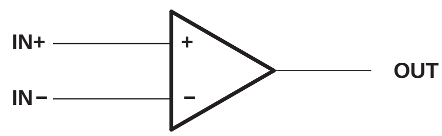
The dual amplifiers are utilized widely in circuit of audio optimized for all preamp and high level stages in PCM and HiFi systems. LM833 is pin-for-pin compatible with industry-standard dual operation amplifiers' pin assignments. With addition of a preamplifier, the gain of the power stage can be greatly reduced to improve performance.

ORDERING INFORMATION(1)

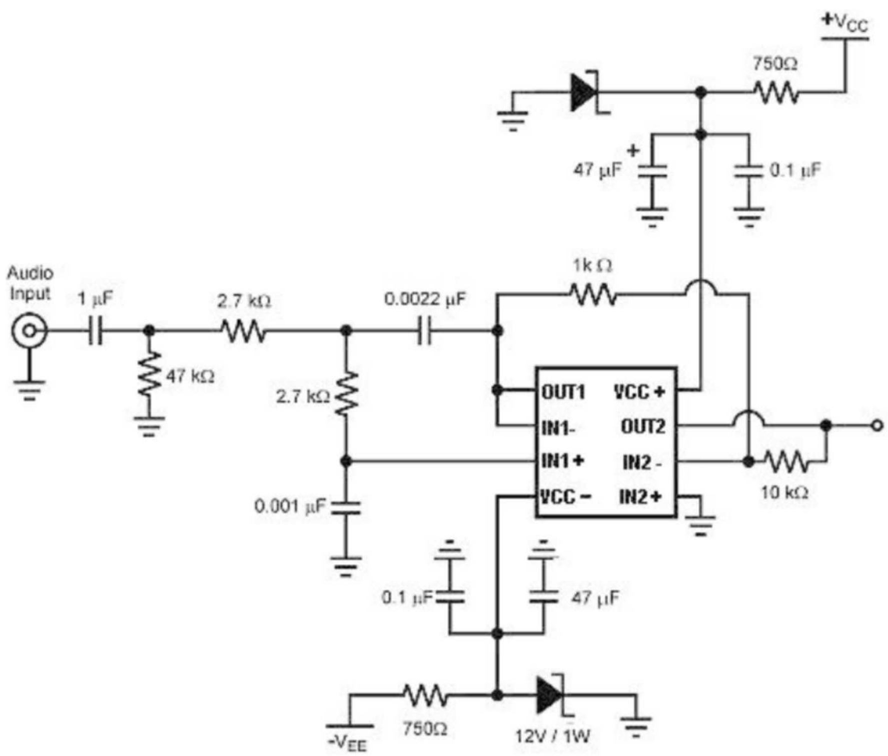
T_A	PACKAGE(2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING(3)
–40°C to 85°C	PDIP – P	Tube of 50	LM833P	LM833P
	SOIC – D	Tube of 75	LM833D	LM833
		Reel of 2500	LM833DR	
	VSSOP/MSOP – DGK	Reel of 2500	LM833DGKR	RS_
		Reel of 250	LM833DGKT	

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.
(3) DGK: The actual top-side marking has one additional character that designates the wafer fab/assembly site.

Symbol (Each Amplifier)



Typical Design Example Audio Pre-Amplifier



ABSOLUTE MAXIMUM RATINGS[1]

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC+}	Supply voltage[2]			18	V
V_{CC-}	Supply voltage[2]			–18	V
$V_{CC+} – V_{CC-}$	Supply voltage			36	V
	Input voltage, either input[2] [3]			V_{CC+} or V_{CC-}	V
	Input current[4]			±10	mA
	Duration of output short circuit[5]			Unlimited	
θ_{JA}	Package thermal impedance, junction to free air[6] [7]	D package		97	°C/W
		DGK package		172	
		P package		85	
T_J	Operating virtual junction temperature			150	°C
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential voltages, are with respect to the midpoint between V_{CC+} and V_{CC-}.
(3) The magnitude of the input voltage must never exceed the magnitude of the supply voltage.
(4) Excessive input current will flow if a differential input voltage in excess of approximately 0.6 V is applied between the inputs, unless some limiting resistance is used.
(5) The output may be shorted to ground or either power supply. Temperature and/or supply voltages must be limited to ensure the maximum dissipation rating is not exceeded.
(6) Maximum power dissipation is a function of T_J(max), θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) – T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
(7) The package thermal impedance is calculated in accordance with JESD 51-7.

ELECTROSTATIC DISCHARGE RATINGS

		MIN	MAX	UNIT
ESD	Human-Body Model (HBM)		2.5	kV
	Charged-Device Model (CDM)		1.5	

RECOMMENDED OPERATING CONDITIONS

		MIN	MAX	UNIT
V_{CC-}	Supply voltage	–5	–18	V
V_{CC+}		5	18	
T_A	Operating free-air temperature range	–40	85	°C

ELECTRICAL CHARACTERISTICS

V_{CC-} = –15 V, V_{CC+} = 15 V, T_A = 25°C (unless otherwise noted)

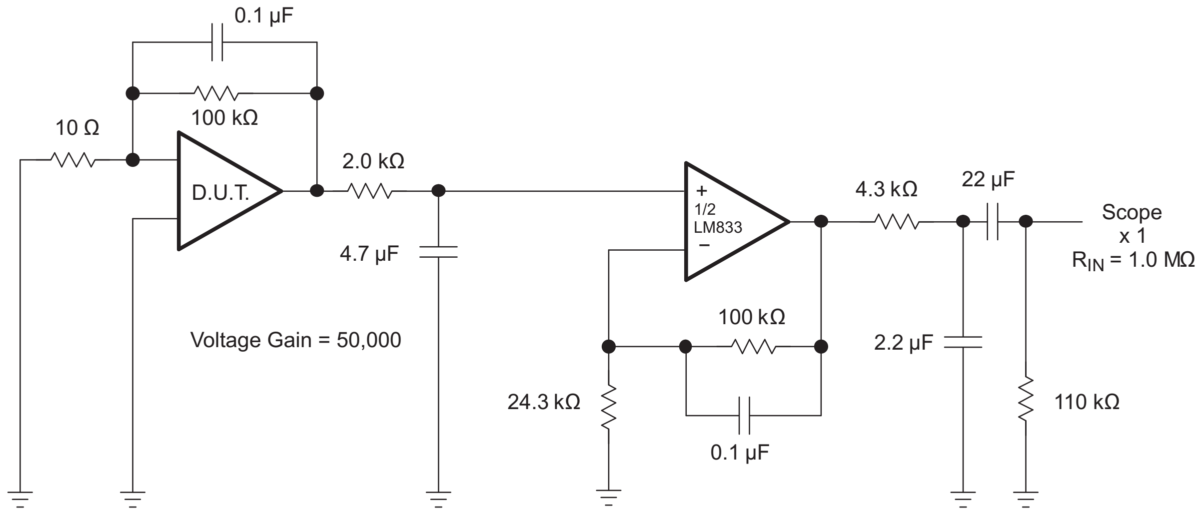
PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	V_O = 0, R_S = 10 Ω, V_{CM} = 0		T_A = 25°C		0.15	2	mV
				T_A = –40°C to 85°C			3	
αV_{IO}	Input offset voltage temperature coefficient	V_O = 0, R_S = 10 Ω, V_{CM} = 0		T_A = –40°C to 85°C		2		μV/°C
I_{IB}	Input bias current	V_O = 0, V_{CM} = 0		T_A = 25°C		300	750	nA
				T_A = –40°C to 85°C			800	
I_{IO}	Input offset current	V_O = 0, V_{CM} = 0		T_A = 25°C		25	150	nA
				T_A = –40°C to 85°C			175	
V_{ICR}	Common-mode input voltage range	ΔV_{IO} = 5 mV, V_O = 0			±13	±14		V
A_{VD}	Large-signal differential voltage amplification	R_L ≥ 2 kΩ, V_O = ±10 V		T_A = 25°C	90	110		dB
				T_A = –40°C to 85°C	85			
V_{OM}	Maximum output voltage swing	V_{ID} = ±1 V	R_L = 600 Ω	V_{OM+}		10.7		V
				V_{OM-}		–11.9		
			R_L = 2k Ω	V_{OM+}	13.2	13.8		
				V_{OM-}	–13.2	–13.7		
			R_L = 10k Ω	V_{OM+}	13.5	14.1		
				V_{OM-}	–14	–14.6		
CMMR	Common-mode rejection ratio	V_{IN} = ±13 V			80	100		dB
k_{SVR} (1)	Supply-voltage rejection ratio	V_{CC+} = 5 V to 15 V, V_{CC-} = –5 V to –15 V			80	105		dB
I_{OS}	Output short-circuit current	$\|V_{ID}\|$ = 1 V, Output to GND		Source current	15	29		mA
				Sink current	–20	–37		
I_{CC}	Supply current (per channel)	V_O = 0		T_A = 25°C		2.05	2.5	mA
				T_A = –40°C to 85°C			2.75	

(1) Measured with $V_{CC\pm}$ differentially varied at the same time

OPERATING CHARACTERISTICS

V_{CC-} = –15 V, V_{CC+} = 15 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	A_{VD} = 1, V_{IN} = –10 V to 10 V, R_L = 2 kΩ, C_L = 100 pF		5	7		V/μs
GBW	Gain bandwidth product	f = 100 kHz		10	16		MHz
B_1	Unity gain frequency	Open loop			9		MHz
G_m	Gain margin	R_L = 2 kΩ	C_L = 0 pF		–11		dB
			C_L = 100 pF		–6		
Φ_m	Phase margin	R_L = 2 kΩ	C_L = 0 pF		55		deg
			C_L = 100 pF		40		
	Amp-to-amp isolation	f = 20 Hz to 20 kHz			–120		dB
	Power bandwidth	V_O = 27 $V_{(PP)}$, R_L = 2 kΩ, THD ≤ 1%			120		kHz
THD	Total harmonic distortion	V_O = 3 V_{rms}, A_{VD} = 1, R_L = 2 kΩ, f = 20 Hz to 20 kHz			0.002		%
z_o	Open-loop output impedance	V_O = 0, f = 9 MHz			37		Ω
r_{id}	Differential input resistance	V_{CM} = 0			175		kΩ
C_{id}	Differential input capacitance	V_{CM} = 0			12		pF
V_n	Equivalent input noise voltage	f = 1 kHz, R_S = 100 Ω			4.5		nV/√Hz
I_n	Equivalent input noise current	f = 1 kHz			0.5		pA/√Hz

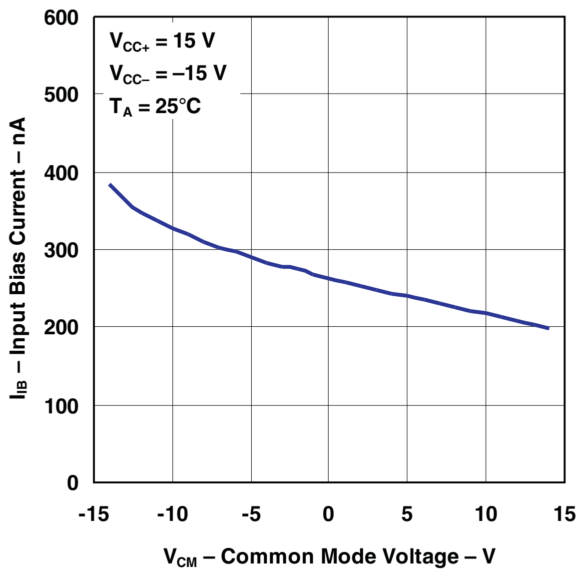


NOTE: All capacitors are non-polarized.

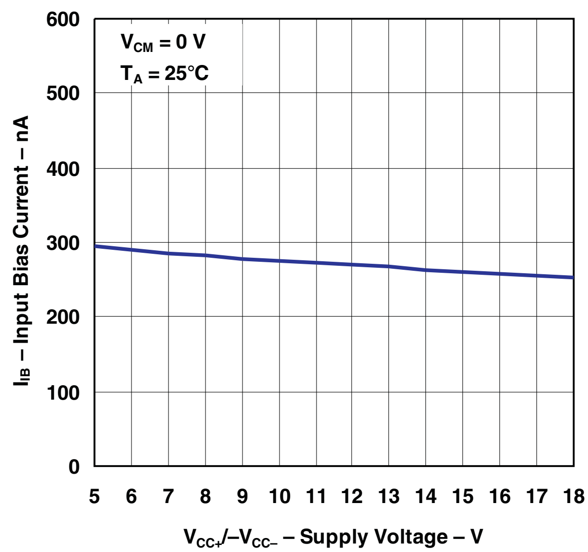
Figure 1. Voltage Noise Test Circuit (0.1 Hz to 10 Hz)

TYPICAL CHARACTERISTICS

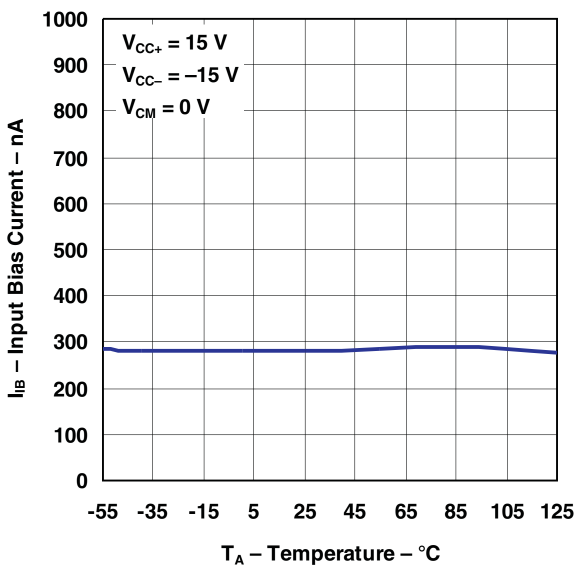
INPUT BIAS CURRENT vs COMMON-MODE VOLTAGE



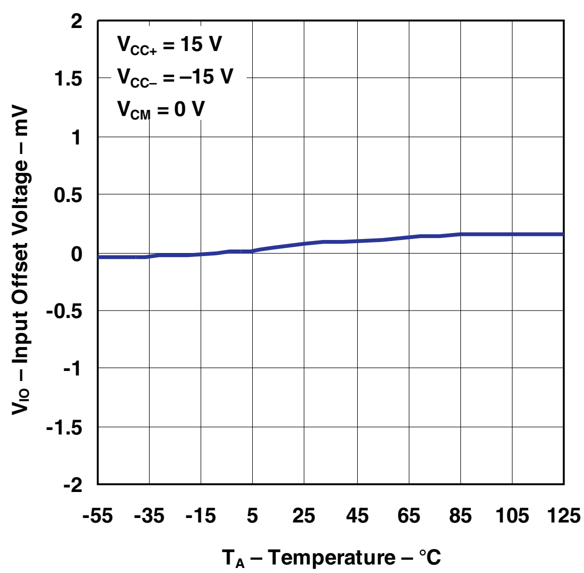
INPUT BIAS CURRENT vs SUPPLY VOLTAGE



INPUT BIAS CURRENT vs TEMPERATURE

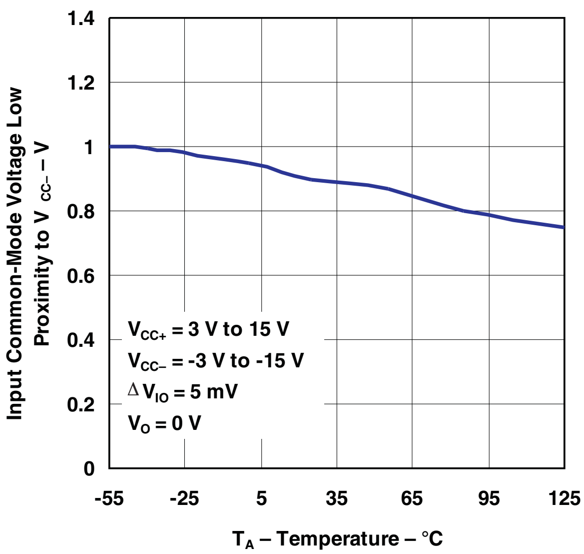


INPUT OFFSET VOLTAGE vs TEMPERATURE

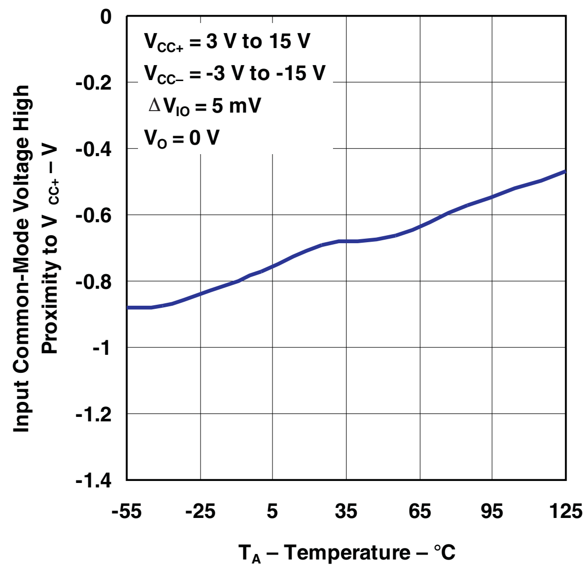


TYPICAL CHARACTERISTICS (continued)

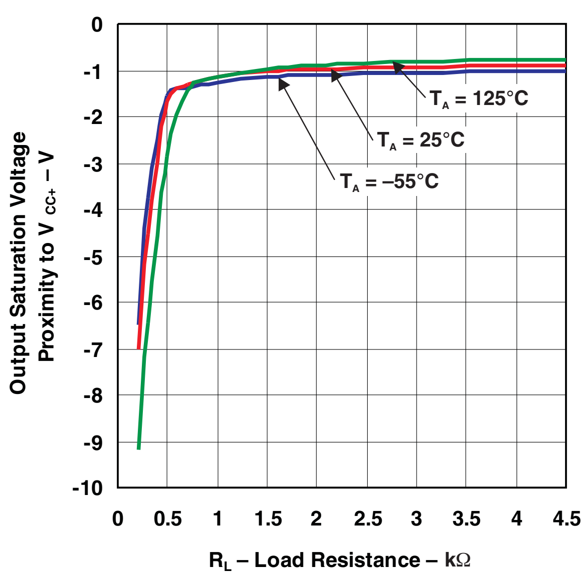
INPUT COMMON-MODE VOLTAGE LOW PROXIMITY TO V_{CC-} vs TEMPERATURE



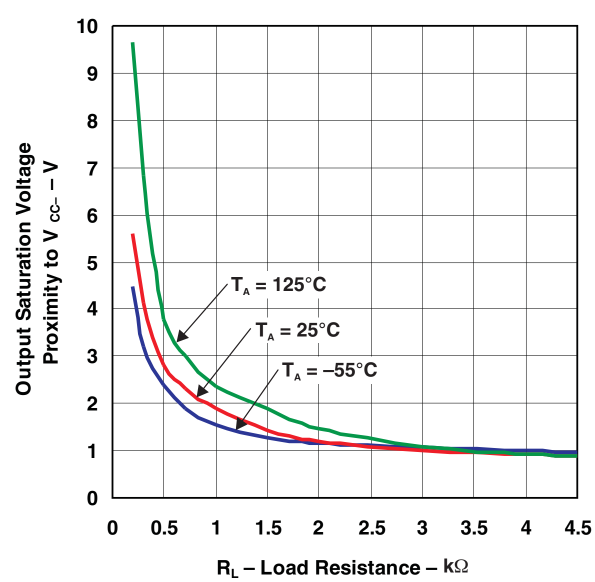
INPUT COMMON-MODE VOLTAGE HIGH PROXIMITY TO V_{CC+} vs TEMPERATURE



OUTPUT SATURATION VOLTAGE PROXIMITY TO V_{CC+} vs LOAD RESISTANCE

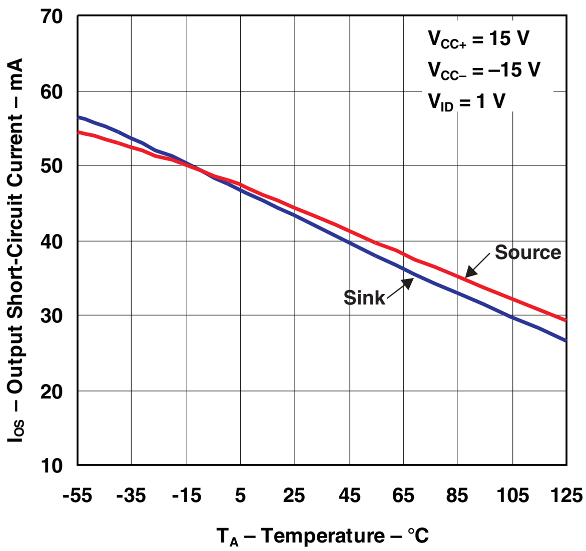


OUTPUT SATURATION VOLTAGE PROXIMITY TO V_{CC-} vs LOAD RESISTANCE

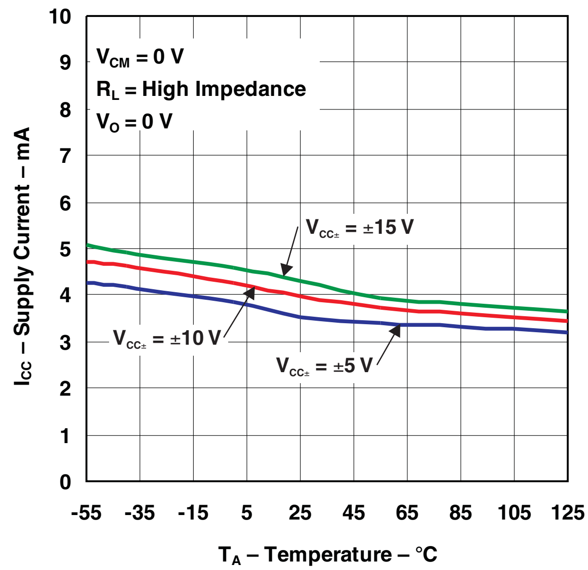


TYPICAL CHARACTERISTICS (continued)

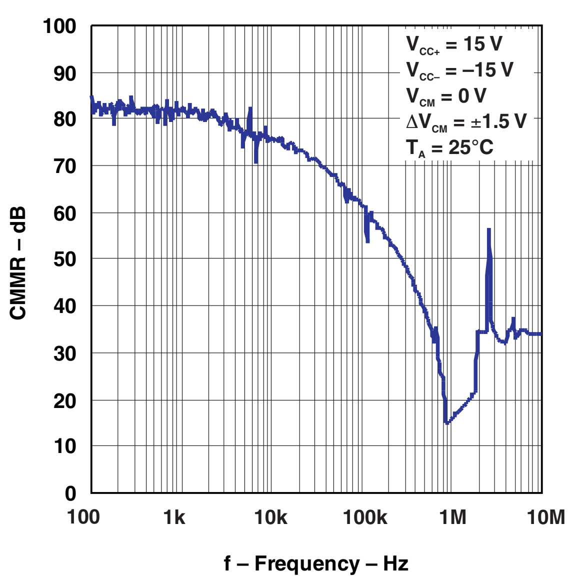
OUTPUT SHORT-CIRCUIT CURRENT vs TEMPERATURE



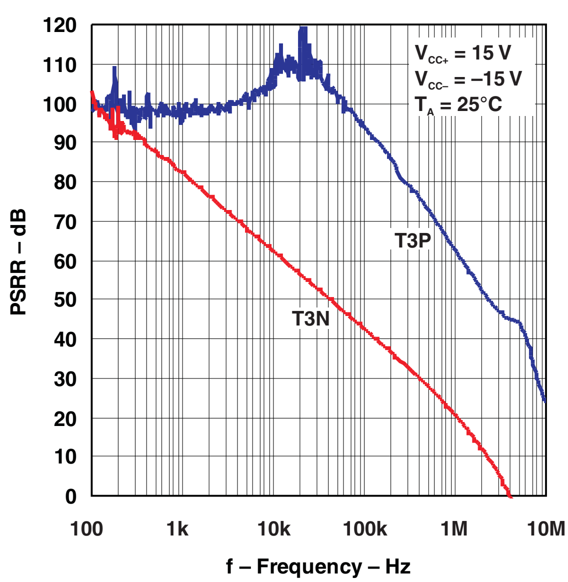
SUPPLY CURRENT vs TEMPERATURE



CMRR vs FREQUENCY

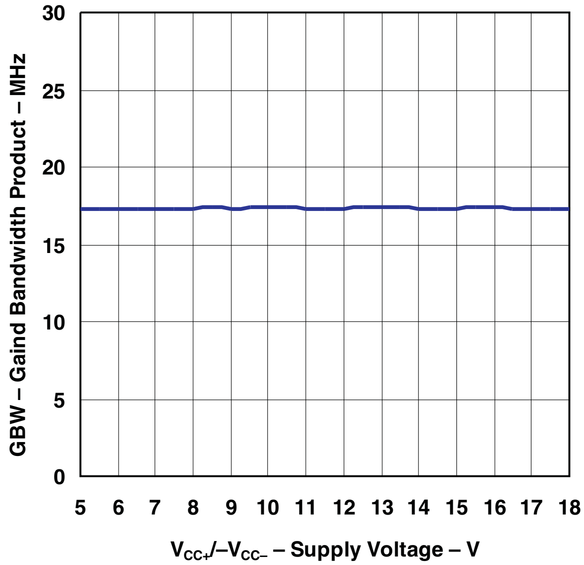


PSSR vs FREQUENCY

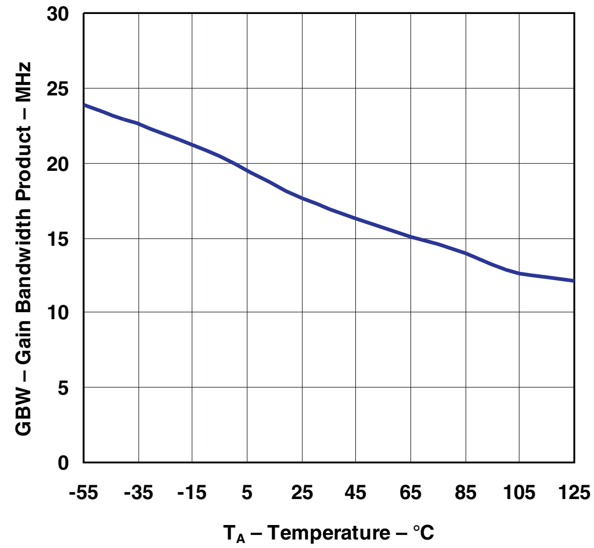


TYPICAL CHARACTERISTICS (continued)

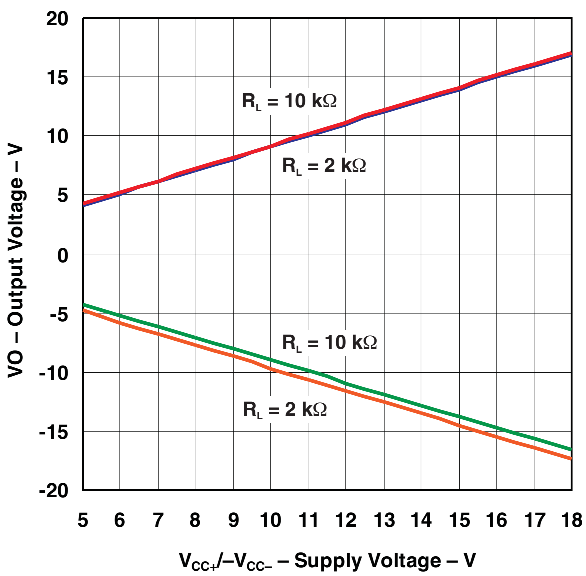
GAIN BANDWIDTH PRODUCT vs SUPPLY VOLTAGE



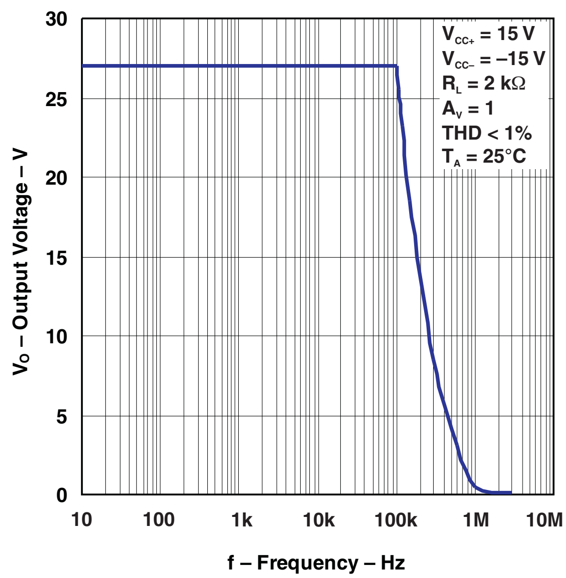
GAIN BANDWIDTH PRODUCT vs TEMPERATURE



OUTPUT VOLTAGE vs SUPPLY VOLTAGE

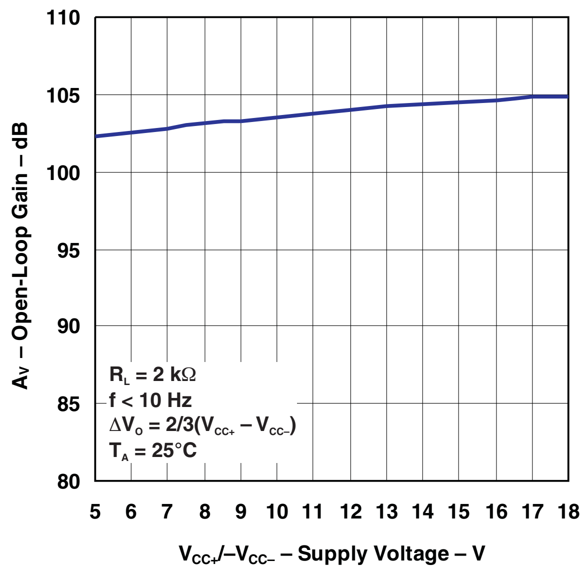


OUTPUT VOLTAGE vs FREQUENCY

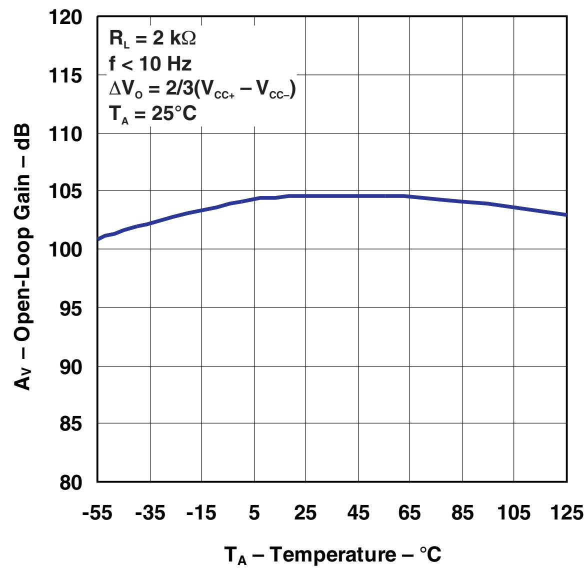


TYPICAL CHARACTERISTICS (continued)

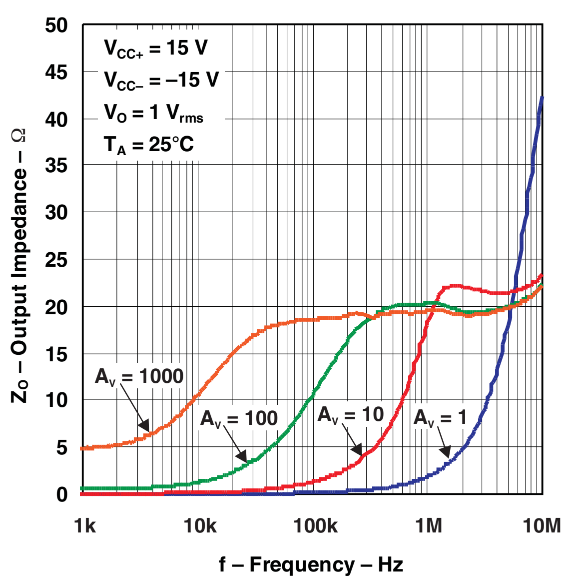
OPEN-LOOP GAIN vs SUPPLY VOLTAGE



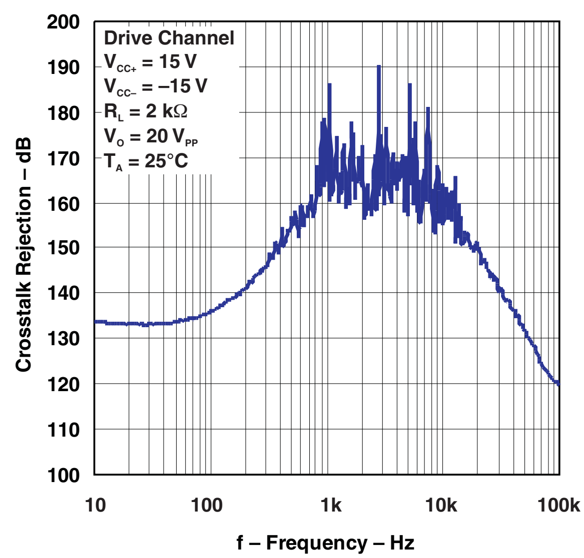
OPEN-LOOP GAIN vs TEMPERATURE



OUTPUT IMPEDANCE vs FREQUENCY

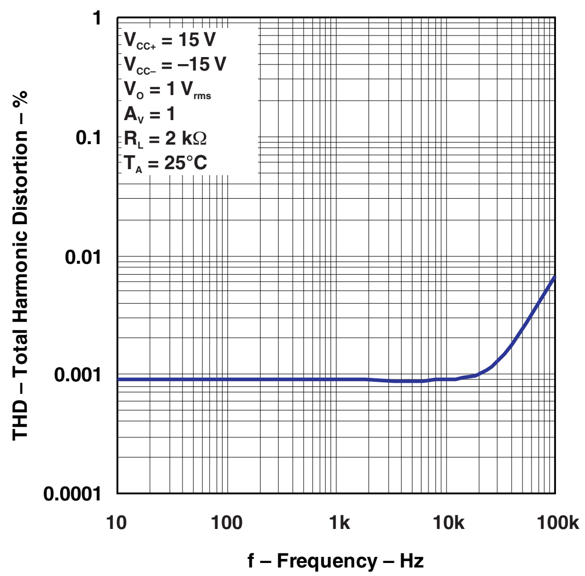


CROSSTALK REJECTION vs FREQUENCY

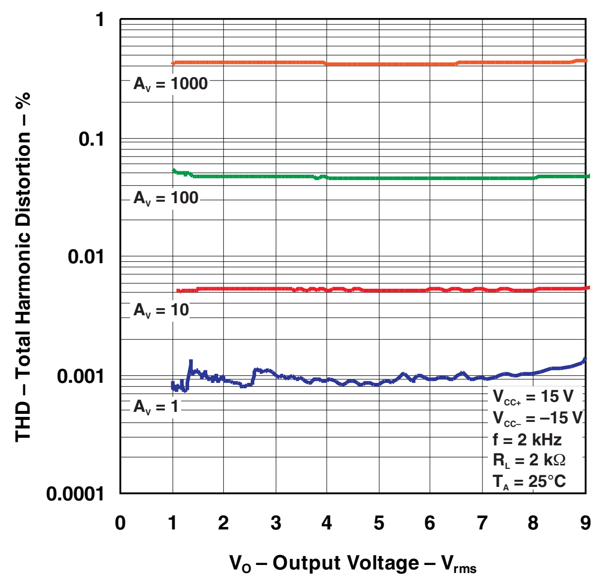


TYPICAL CHARACTERISTICS (continued)

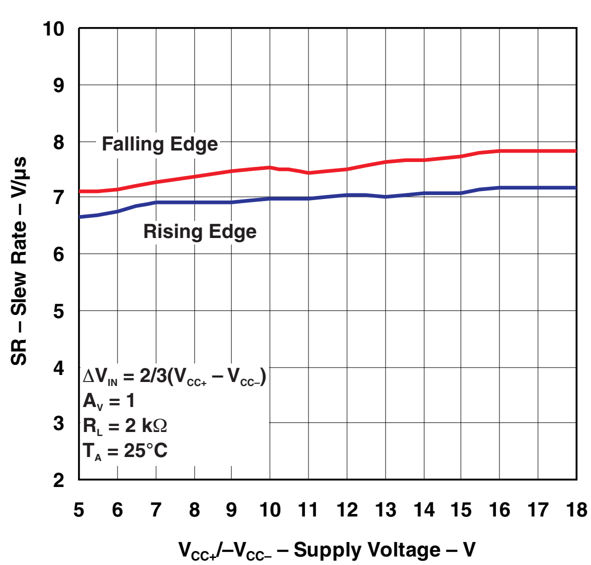
TOTAL HARMONIC DISTORTION vs FREQUENCY



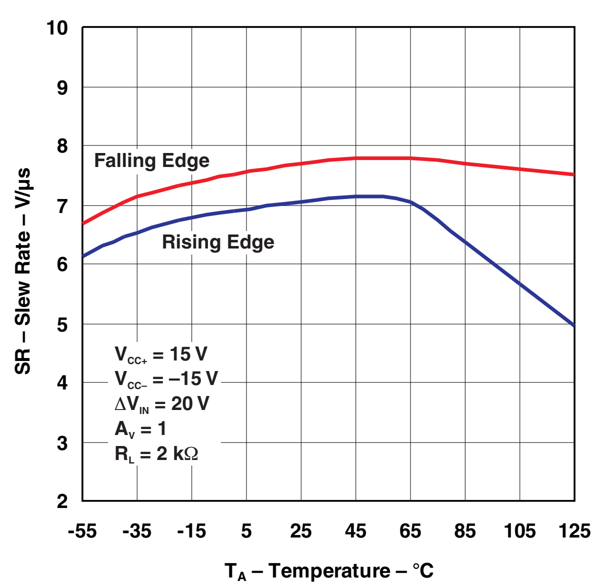
TOTAL HARMONIC DISTORTION vs OUTPUT VOLTAGE



SLEW RATE vs SUPPLY VOLTAGE

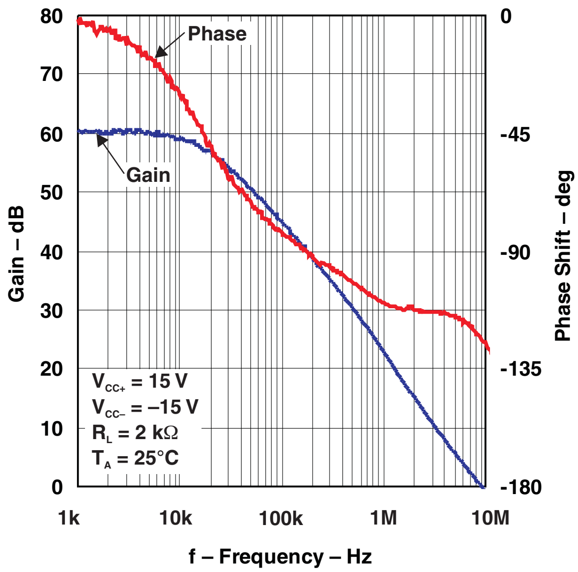


SLEW RATE vs TEMPERATURE

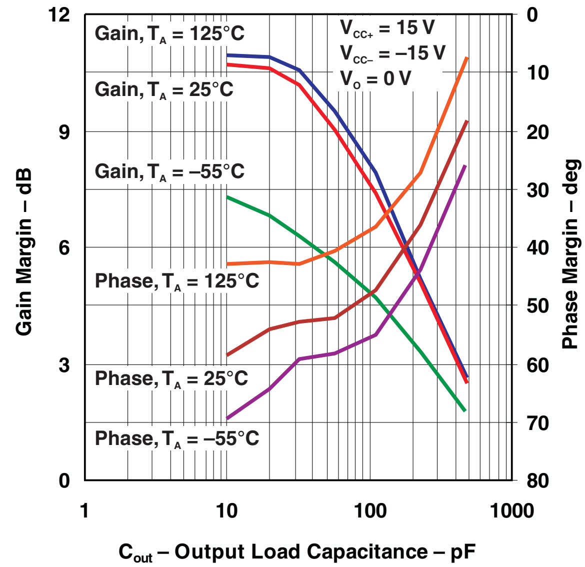


TYPICAL CHARACTERISTICS (continued)

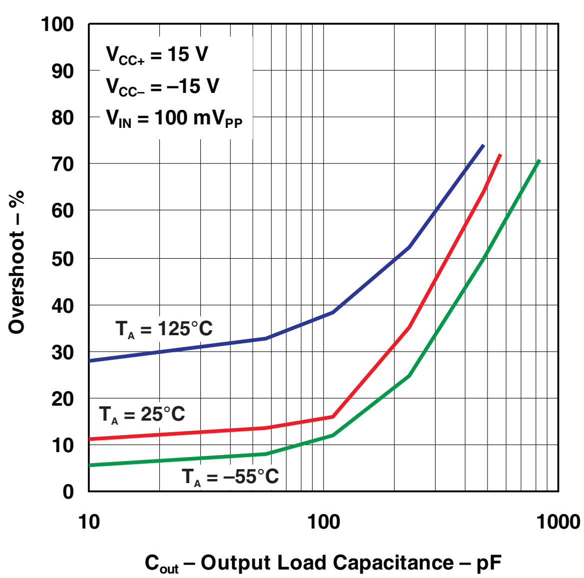
GAIN AND PHASE vs FREQUENCY



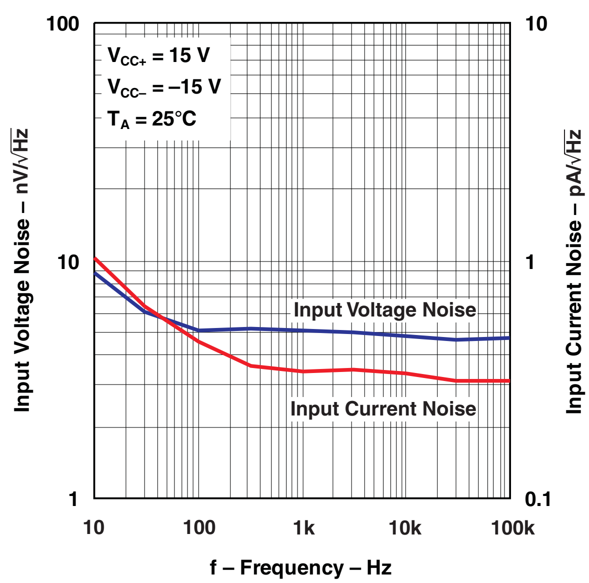
GAIN AND PHASE MARGIN vs OUTPUT LOAD CAPACITANCE



OVERSHOOT vs OUTPUT LOAD CAPACITANCE

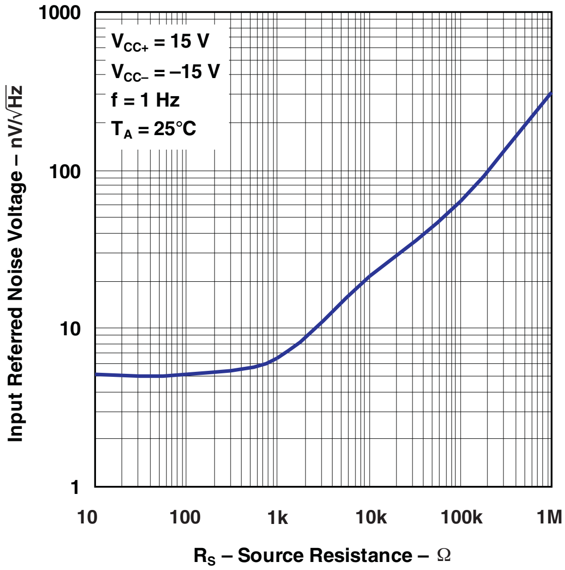


INPUT VOLTAGE AND CURRENT NOISE vs FREQUENCY

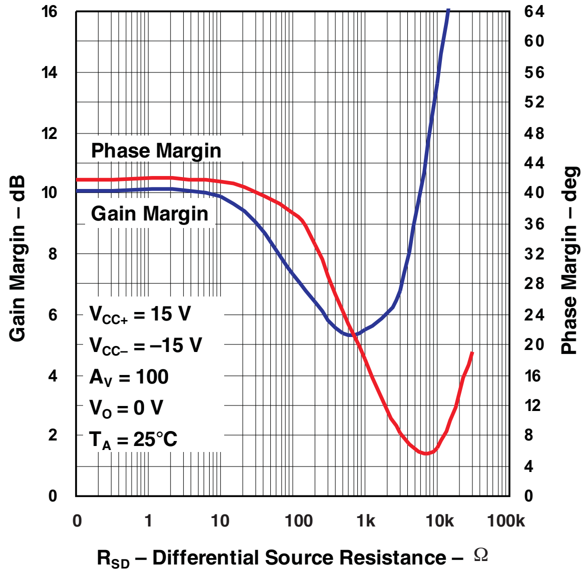


TYPICAL CHARACTERISTICS (continued)

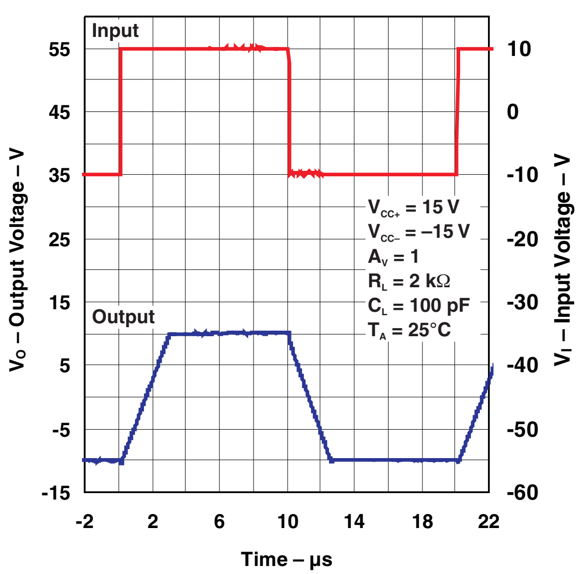
INPUT REFERRED NOISE VOLTAGE vs SOURCE RESISTANCE



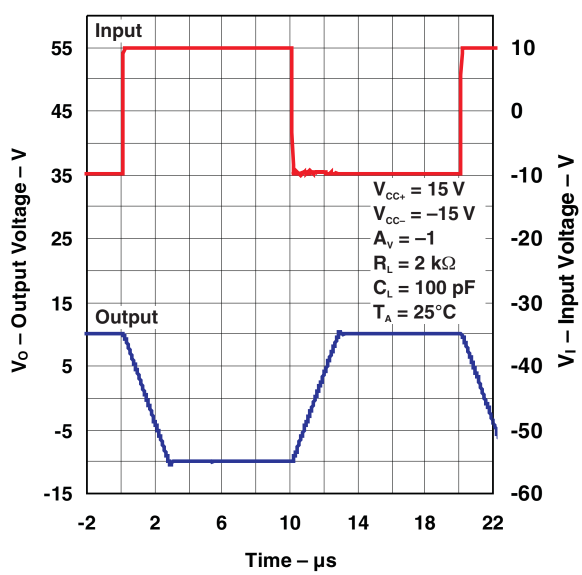
GAIN AND PHASE MARGIN vs DIFFERENTIAL SOURCE RESISTANCE



LARGE SIGNAL TRANSIENT RESPONSE (A_V = 1)

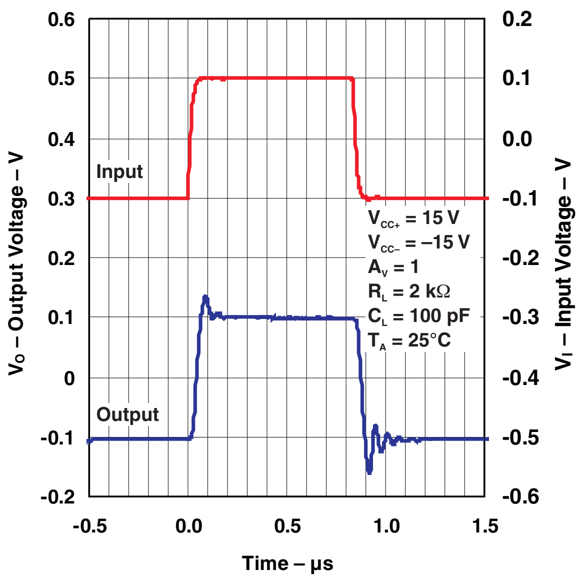


LARGE SIGNAL TRANSIENT RESPONSE (A_V = –1)

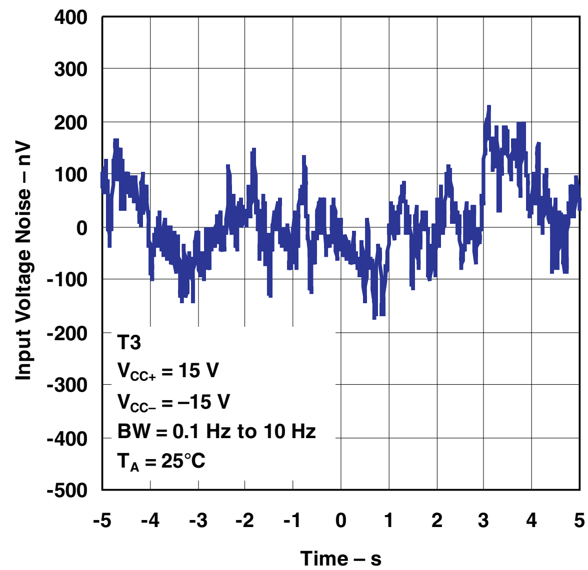


TYPICAL CHARACTERISTICS (continued)

SMALL SIGNAL TRANSIENT RESPONSE



LOW_FREQUENCY NOISE

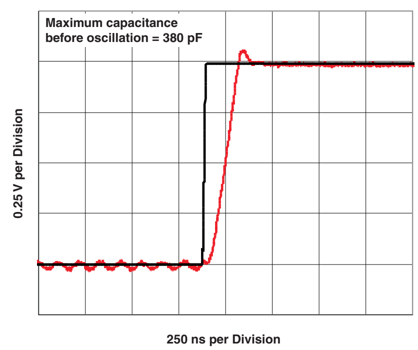


APPLICATION INFORMATION

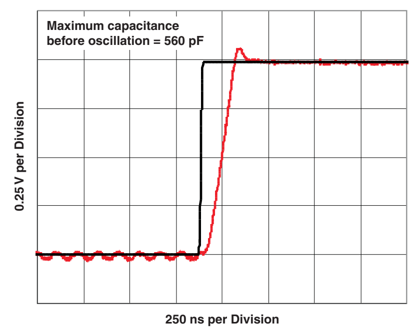
Output Characteristics

All operating characteristics are specified with 100-pF load capacitance. The LM833 can drive higher capacitance loads. However, as the load capacitance increases, the resulting response pole occurs at lower frequencies, causing ringing, peaking, or oscillation. The value of the load capacitance at which oscillation occurs varies from lot to lot. If an application appears to be sensitive to oscillation due to load capacitance, adding a small resistance in series with the load should alleviate the problem (see Figure 2).

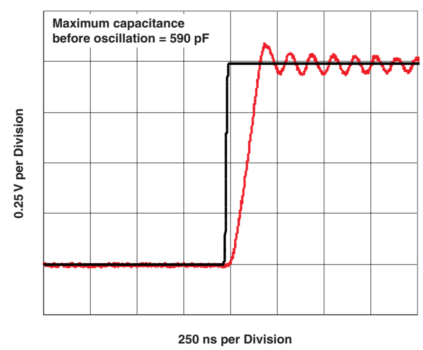
PULSE RESPONSE
(R_L = 600 Ω, C_L = 380 pF)



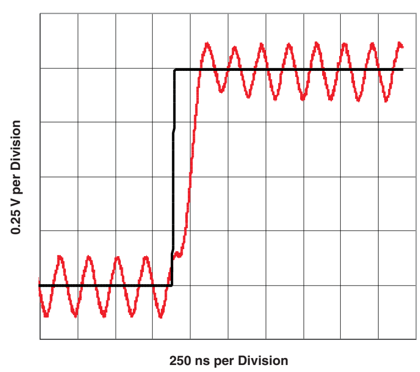
PULSE RESPONSE
(R_L = 2 kΩ, C_L = 560 pF)



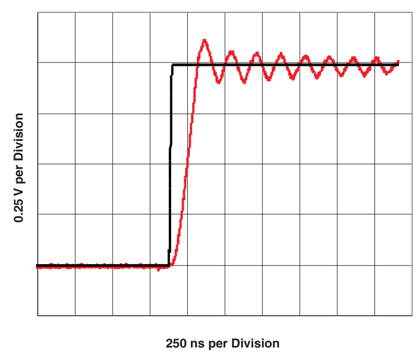
PULSE RESPONSE
(R_L = 10 kΩ, C_L = 590 pF)



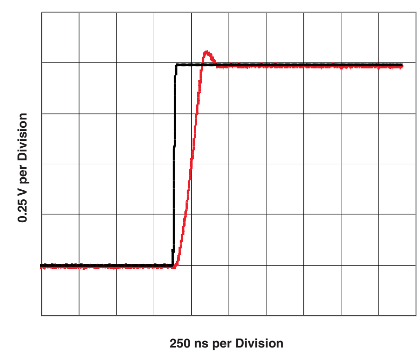
PULSE RESPONSE
(R_O = 0 Ω, C_O = 1000 pF, R_L = 2 kΩ)



PULSE RESPONSE
(R_O = 4 Ω, C_O = 1000 pF, R_L = 2 kΩ)



PULSE RESPONSE
(R_O = 35 Ω, C_O = 1000 pF, R_L = 2 kΩ)



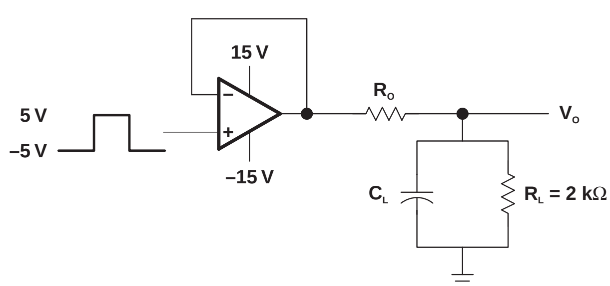


Figure 2. Output Characteristics

REVISION HISTORY

Changes from Original (July 2010) to Revision A	Page
• Changed Datasheet status from Product Preview to Production Data.	1

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/ Ball Finish	MSL Peak Temp [3]	Samples (Requires Login)
LM833D	ACTIVE	SOIC	D	8	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Purchase Samples
LM833DGKR	ACTIVE	MSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Request Free Samples
LM833DGKT	ACTIVE	MSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Purchase Samples
LM833DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Request Free Samples
LM833P	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	Request Free Samples

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

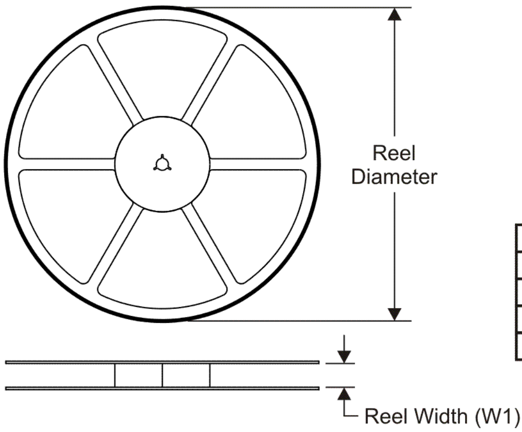
[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

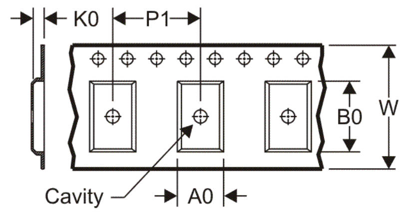
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

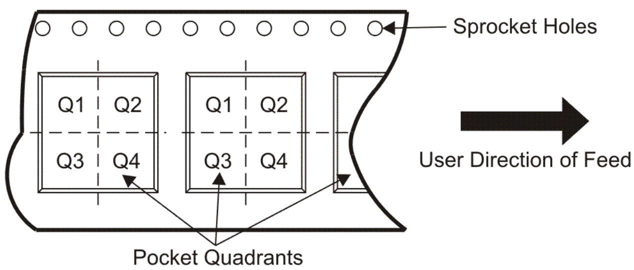


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

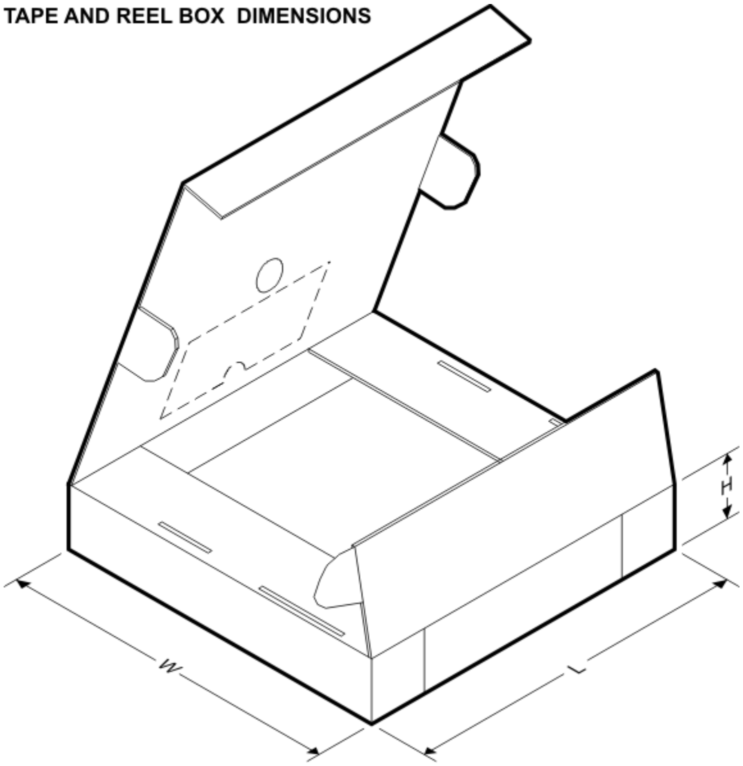
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM833DGKR	MSOP	DGK	8	2500	330.0	12.4	5.3	3.3	1.3	8.0	12.0	Q1
LM833DGKT	MSOP	DGK	8	250	180.0	12.4	5.3	3.3	1.3	8.0	12.0	Q1
LM833DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
LM833DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

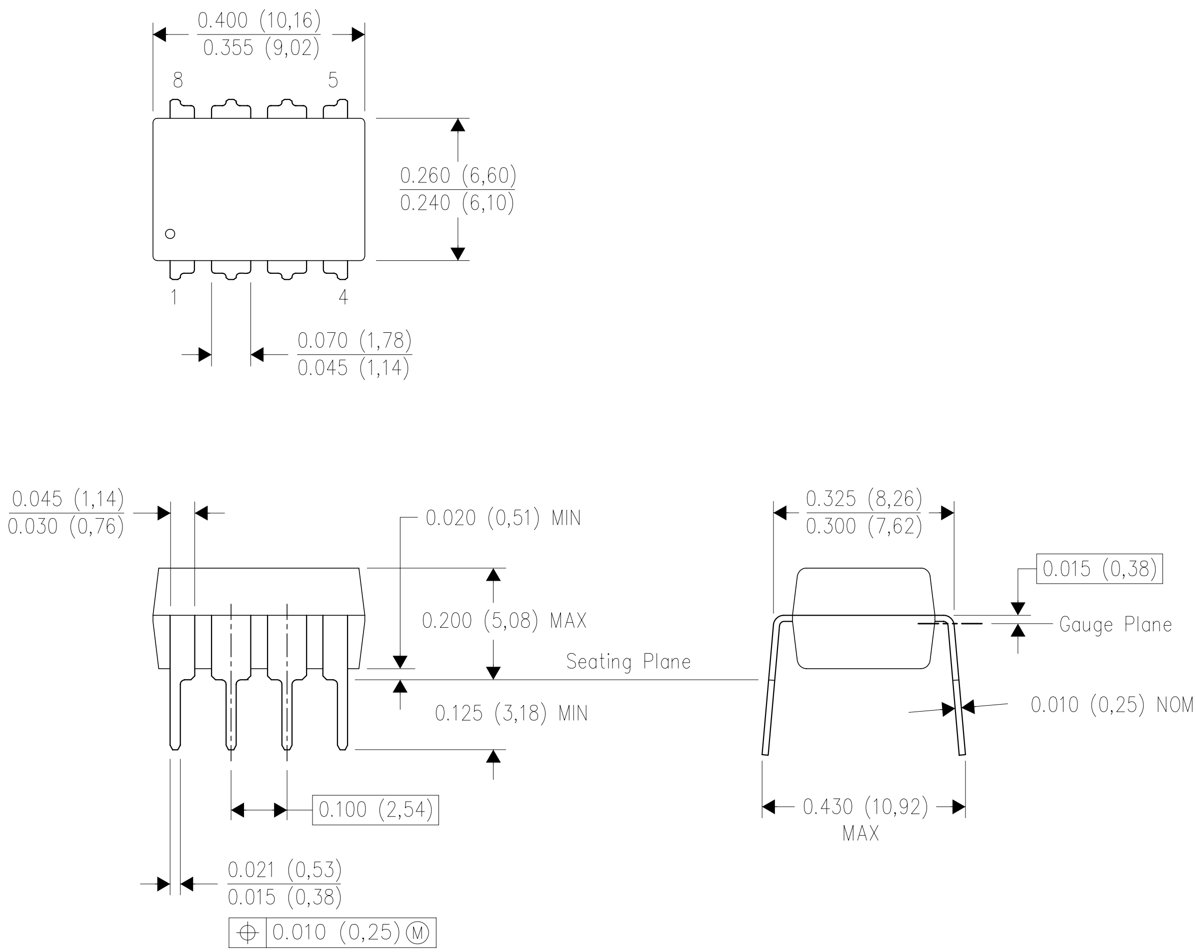
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM833DGKR	MSOP	DGK	8	2500	346.0	346.0	35.0
LM833DGKT	MSOP	DGK	8	250	203.0	203.0	35.0
LM833DR	SOIC	D	8	2500	340.5	338.1	20.6
LM833DR	SOIC	D	8	2500	346.0	346.0	29.0

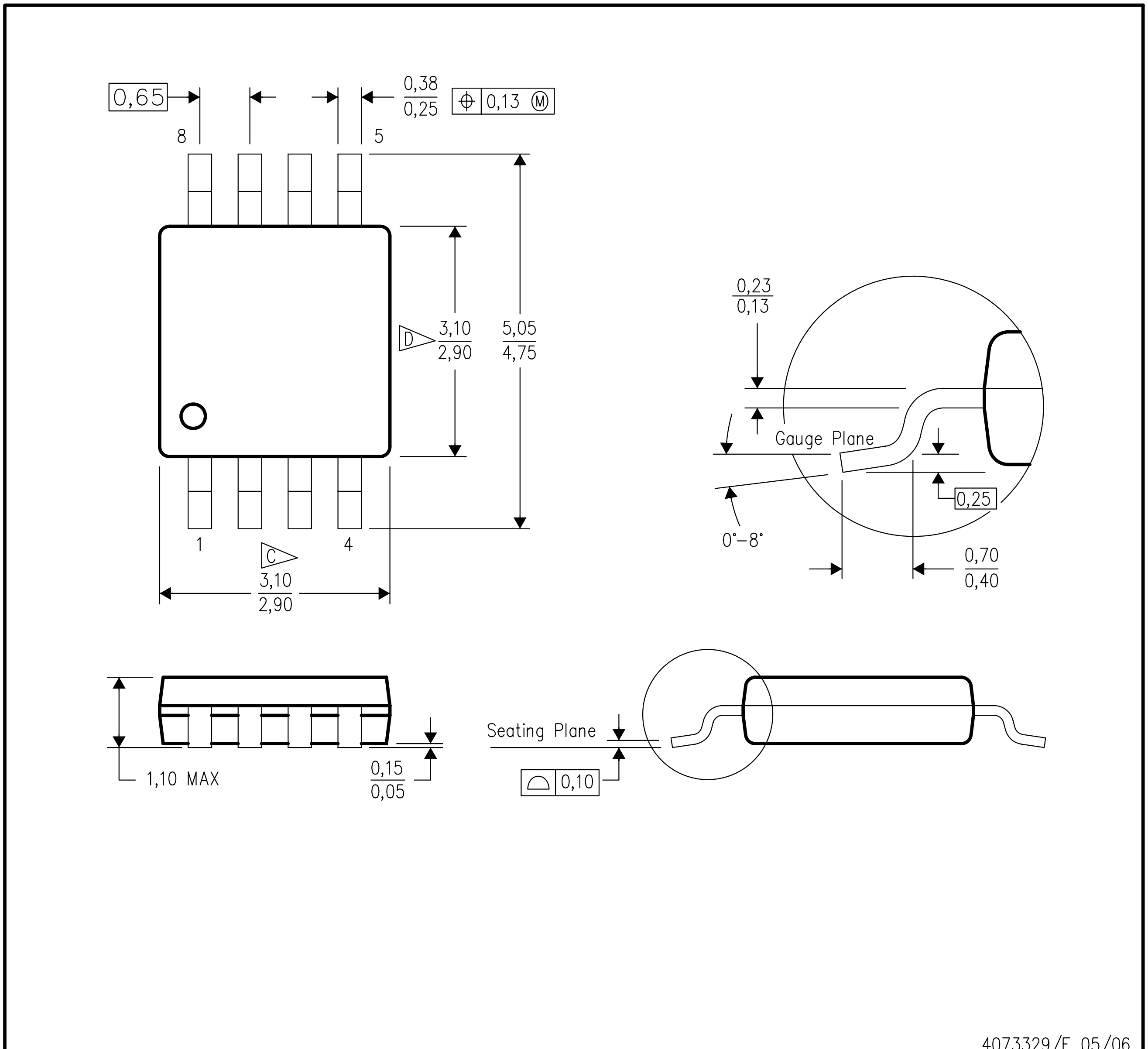
P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



4040082/E 04/2010

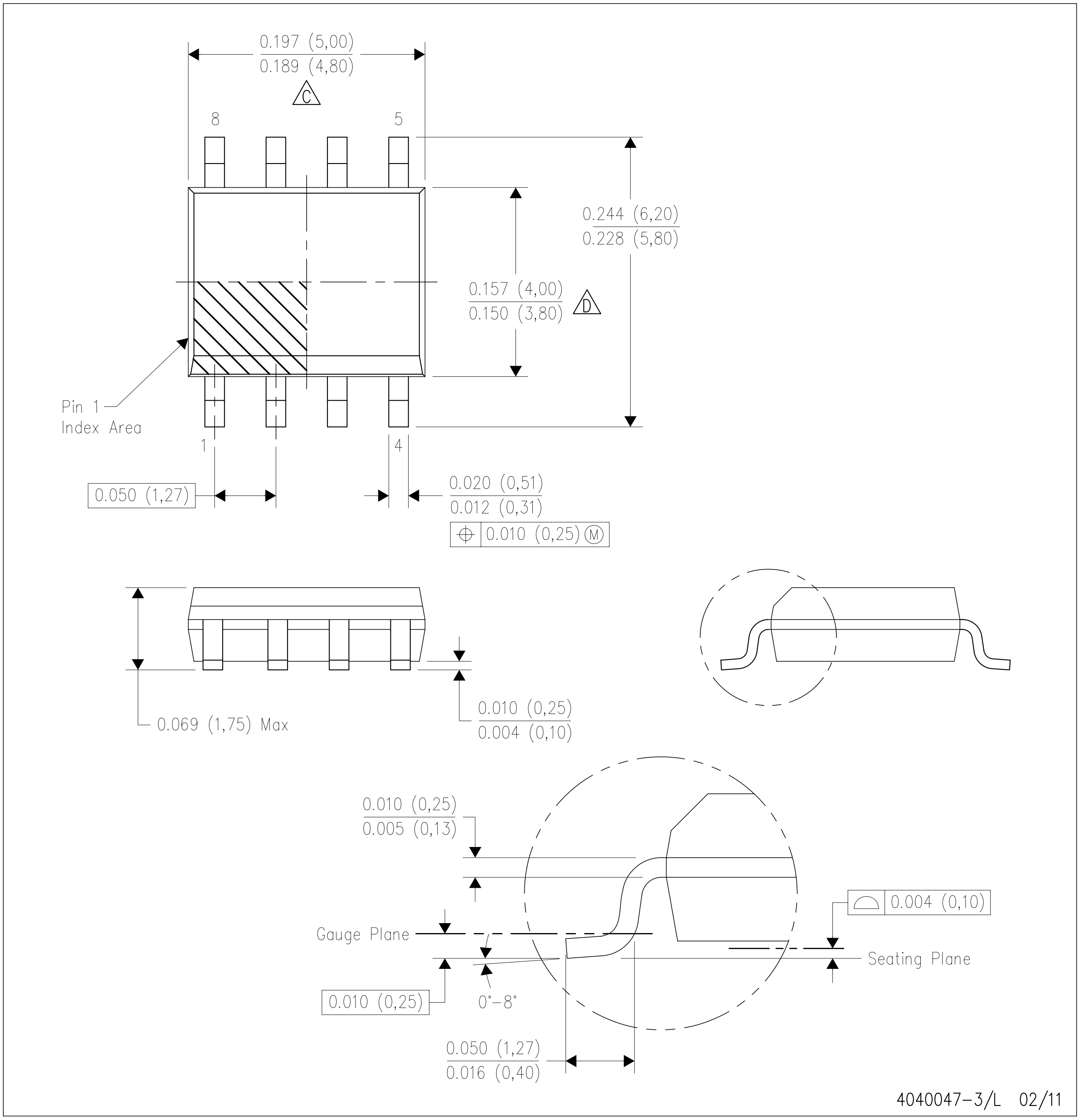
NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

DGK (S-PDSO-G8) PLASTIC SMALL-OUTLINE PACKAGE



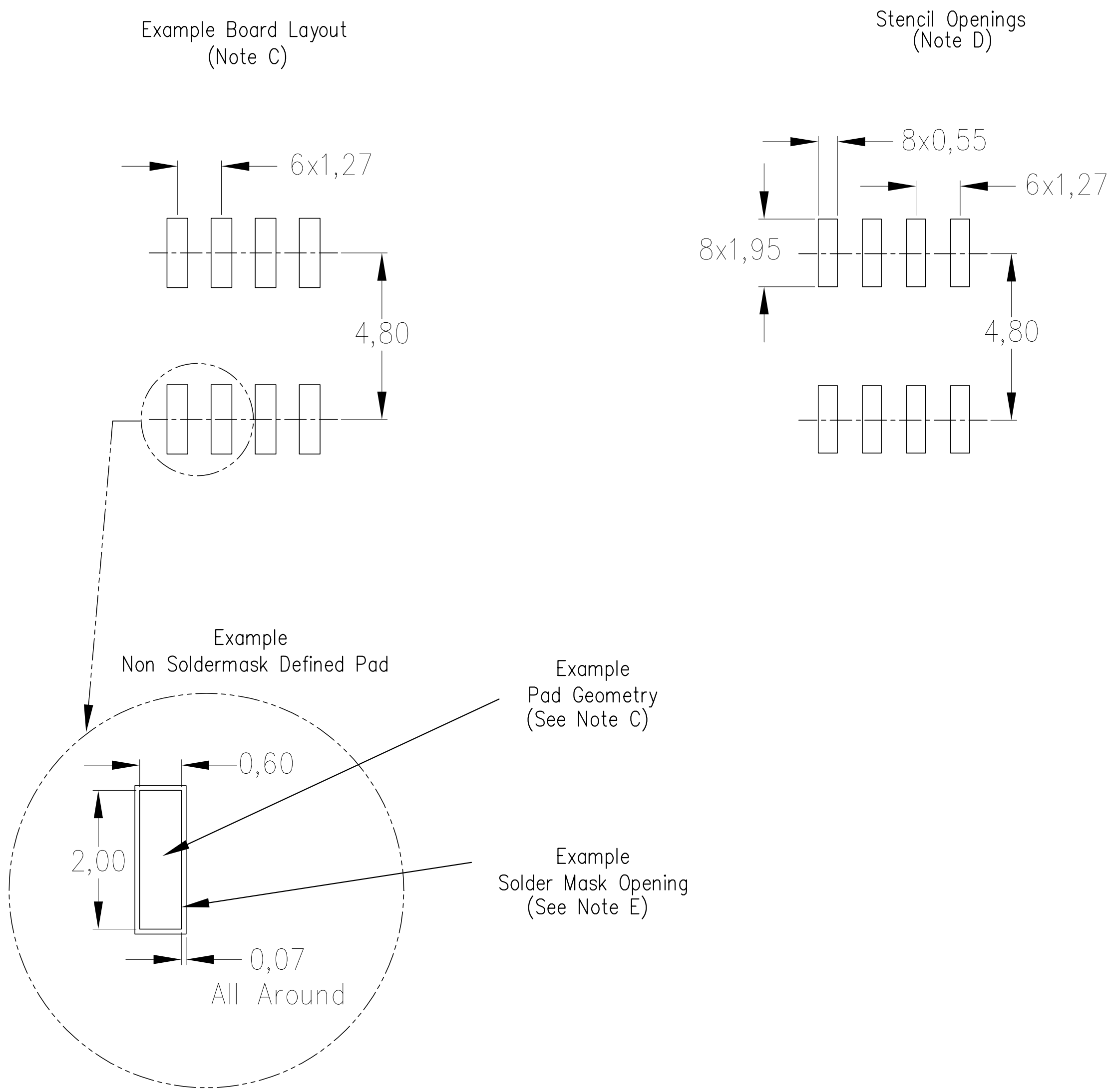
NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
- E. Falls within JEDEC MO-187 variation AA, except interlead flash.

D (R-PDSO-G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS-012 variation AA.

D (R-PDSO-G8) PLASTIC SMALL OUTLINE



4211283-2/C 02/11

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC-7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

IMPORTANT NOTICE

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		**Applications**	
Audio	www.ti.com/audio	Communications and Telecom	www.ti.com/communications
Amplifiers	amplifier.ti.com	Computers and Peripherals	www.ti.com/computers
Data Converters	dataconverter.ti.com	Consumer Electronics	www.ti.com/consumer-apps
DLP® Products	www.dlp.com	Energy and Lighting	www.ti.com/energy
DSP	dsp.ti.com	Industrial	www.ti.com/industrial
Clocks and Timers	www.ti.com/clocks	Medical	www.ti.com/medical
Interface	interface.ti.com	Security	www.ti.com/security
Logic	logic.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Power Mgmt	power.ti.com	Transportation and Automotive	www.ti.com/automotive
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com	Wireless	www.ti.com/wireless-apps
RF/IF and ZigBee® Solutions	www.ti.com/lprf		
	TI E2E Community Home Page		e2e.ti.com

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265