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FDP2D3N10C / FDPF2D3N10C

N-Channel Shielded Gate PowerTrench[®] MOSFET 100 V, 222 A, 2.3 m Ω

Features

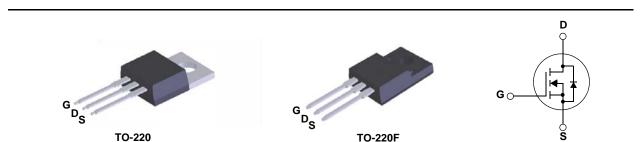
- Max $r_{DS(on)}$ = 2.3 m Ω at V_{GS} = 10 V, I_D = 100 A
- Extremely Low Reverse Recovery Charge, Qrr
- 100% UIL Tested
- RoHS Compliant

General Description

This N-Channel MV MOSFET is produced using ON Semiconductor's advanced PowerTrench[®] process that incorporates Shielded Gate technology. This process has been optimized to minimize on-state resistance and yet maintain superior switching performance with best in class soft body diode.

Applications

- Synchronous Rectification for ATX / Server / Telecom PSU
- Motor drives and Uninterruptible Power Supplies
- Micro Solar Inverter



MOSFET Maximum Ratings T_C = 25 °C unless otherwise noted.

Cumbed.	Parameter		Rat	Unite			
Symbol			FDP2D3N10C	FDPF2D3N10C	Units		
V _{DS}	Drain to Source Voltage			100	100	V	
V _{GS}	Gate to Source Voltage			±20	±20	V	
	Drain Current -Continuous	T _C = 25°C	(Note 3)	222*	222*		
I _D	-Continuous	T _C = 100°C	(Note 3)	157*	157*	А	
	-Pulsed		(Note 1)	888	888		
E _{AS}	Single Pulse Avalanche Energy (Note 2)		(Note 2)	1176		mJ	
P _D	Power Dissipation	T _C = 25°C		214	45	14/	
	Power Dissipation	T _A = 25°C		2.4	2.4	W	
T _J , T _{STG}	Operating and Storage Junction Temperature Range			-55 to	+175	°C	

* Drain current limited by maximum junction temperature. Package limitation current is 120A.

Thermal Characteristics

Symbol	Parameter	FDP2D3N10C	FDPF2D3N10C	Units
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	0.7	3.3	°C/W
$R_{ ext{ heta}JA}$	Thermal Resistance, Junction to Ambient, Max.	62.5	62.5	C/VV

Package Marking and Ordering Information

Device Marking	Device	Package	Packing Method	Quantity
FDP2D3N10C	FDP2D3N10C	TO-220	Tube	50 units
FDPF2D3N10C	FDPF2D3N10C	TO-220F	Tube	50 units

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FDPF2D3N10C N
N-Channel Shie
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3N10C N-Channel Shielded Gate PowerTrench [®] MOSFET

	Parameter	Test Conditions	Min.	Тур.	Max.	Units
Off Chara	octeristics					
BV _{DSS}	Drain to Source Breakdown Voltage	I _D = 250 μA, V _{GS} = 0 V	100			V
ΔBV _{DSS} ΔTJ	Breakdown Voltage Temperature Coefficient	$I_D = 250 \ \mu$ A, referenced to 25 °C		70		mV/°C
1	Zero Gate Voltage Drain Current	V _{DS} = 80 V, V _{GS} = 0 V			1	μA
DSS		V _{DS} = 80 V, T _J = 150°C			500	μA
I _{GSS}	Gate to Source Leakage Current	$V_{GS} = \pm 20 \text{ V}, V_{DS} = 0 \text{ V}$			±100	nA
	cteristics	N/ N/ 1 1				
V _{GS(th)}	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$, $I_D = 700 \ \mu A$	2.0	3.0	4.0	V
r _{DS(on)}	Static Drain to Source On Resistance	$V_{GS} = 10 \text{ V}, \text{ I}_{D} = 100 \text{ A}$		2.1	2.3	mΩ
9fs	Forward Transconductance	$V_{DS} = 5 V, I_{D} = 100 A$		222		S
Dynamic	Characteristics					
C _{iss}	Input Capacitance	V 50.V.V. 0.V.		7980	11180	pF
C _{oss}	Output Capacitance	V _{DS} = 50 V, V _{GS} = 0 V, f = 1 MHz		4490	6290	pF
C _{rss}	Reverse Transfer Capacitance			40	75	pF
	Gate Resistance		0.1	0.8	1.8	Ω
Rg						
	g Characteristics					
Switching	g Characteristics			42	67	ns
Switching t _{d(on)}		V _{DD} = 50 V, I _D = 100 A,		42 35	67 56	ns ns
t _{d(on)} t _r	Turn-On Delay Time	V _{DD} = 50 V, I _D = 100 A, V _{GS} = 10 V, R _{GEN} = 6 Ω			-	-
Switching t _{d(on)} t _r t _{d(off)}	Turn-On Delay Time Rise Time	$V_{GS} = 10 \text{ V}, \text{ R}_{GEN} = 6 \Omega$		35	56	ns
Switching t _{d(on)} t _r t _{d(off)} t _f Q _g	Turn-On Delay Time Rise Time Turn-Off Delay Time	$V_{GS} = 10 \text{ V}, \text{ R}_{GEN} = 6 \Omega$		35 74	56 118	ns ns
Switching t _{d(on)} t _r t _{d(off)} t _f Q _g Q _{gs}	Turn-On Delay Time Rise Time Turn-Off Delay Time Fall Time	$V_{GS} = 10 \text{ V}, \text{ R}_{GEN} = 6 \Omega$ $V_{GS} = 0 \text{ V to } 10 \text{ V}$ $V_{DD} = 50 \text{ V},$		35 74 32	56 118 57	ns ns ns
Switching t _{d(on)} t _r t _{d(off)}	Turn-On Delay TimeRise TimeTurn-Off Delay TimeFall TimeTotal Gate Charge	$V_{GS} = 10 \text{ V}, \text{ R}_{GEN} = 6 \Omega$		35 74 32 108	56 118 57	ns ns ns nC

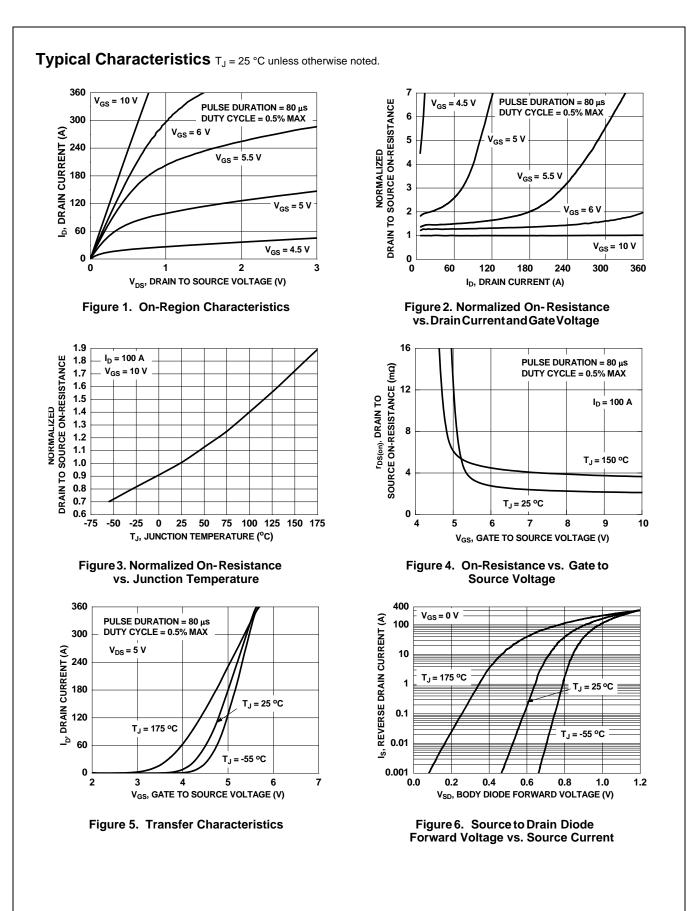
I _S	Maximum Continuous Drain to Source Diode Forward Current		-	-	222	А
I _{SM}	Maximum Pulsed Drain to Source Diode Forward Current		-	-	888	А
V _{SD}	Source to Drain Diode Forward Voltage	V _{GS} = 0 V, I _{SD} = 100 A		0.9	1.3	V
t _{rr}	Reverse Recovery Time	V _{GS} = 0 V, V _{DD} = 50 V,		107	172	ns
Q _{rr}	Reverse Recovery Charge	$I_F = 100 \text{ A}, \text{ d}I_F/\text{d}t = 100 \text{ A}/\mu\text{s}$		191	306	nC
t _{rr}	Reverse Recovery Time	V _{GS} = 0 V, V _{DD} = 50 V,		97	155	ns
Q _{rr}	Reverse Recovery Charge	$I_F = 100 \text{ A}, \text{ dI}_F/\text{dt} = 300 \text{ A}/\mu\text{s}$		492	788	nC

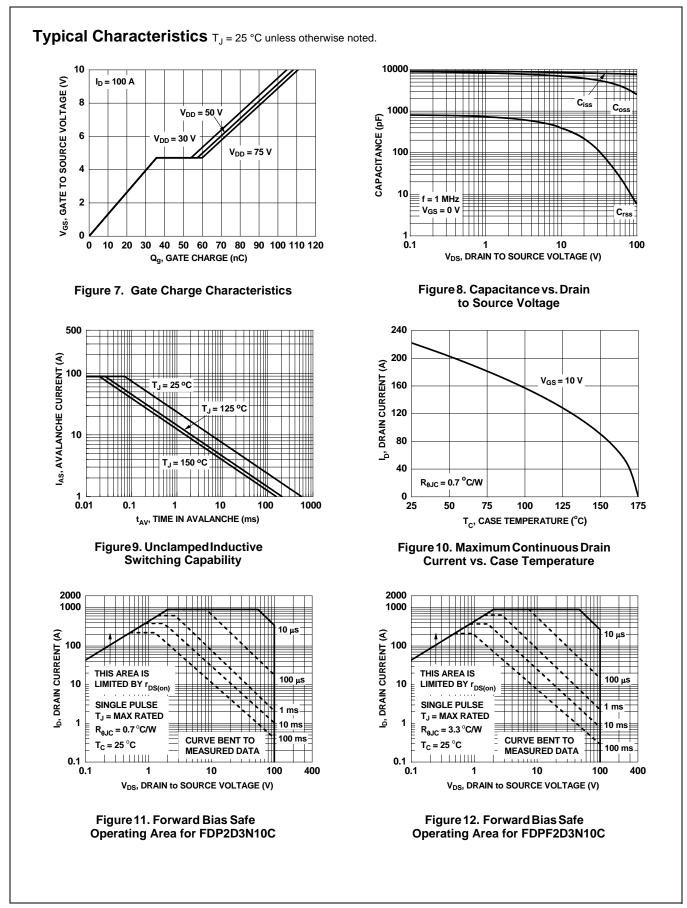
Notes:

1. Pulsed Id please refer to Figure.11 and Figure.12 "Forward Bias Safe Operating Area" for more details.

2. E_{AS} of 1176 mJ is based on starting T_J = 25 °C, L = 3 mH, I_{AS} = 28 A, V_{DD} = 90 V, V_{GS} = 10 V. 100% test at L = 0.1 mH, I_{AS} = 89 A.

3. Computed continuous current limited to Max Junction Temperature only, actual continuous current will be limited by thermal & electro-mechanical application board design.





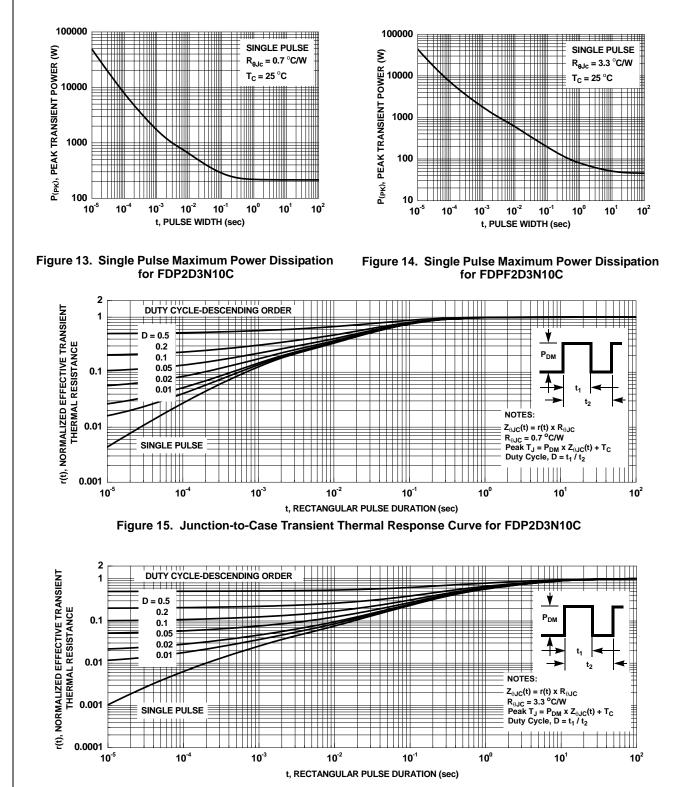
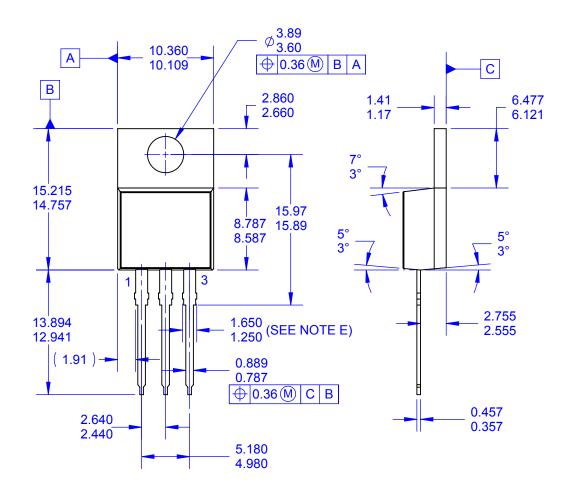


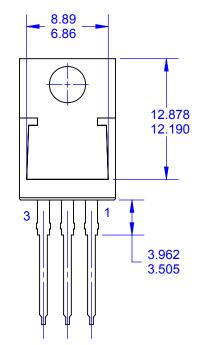
Figure 16. Junction-to-Case Transient Thermal Response Curve for FDPF2D3N10C

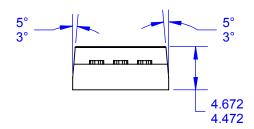
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Typical Characteristics T_J = 25 °C unless otherwise noted.

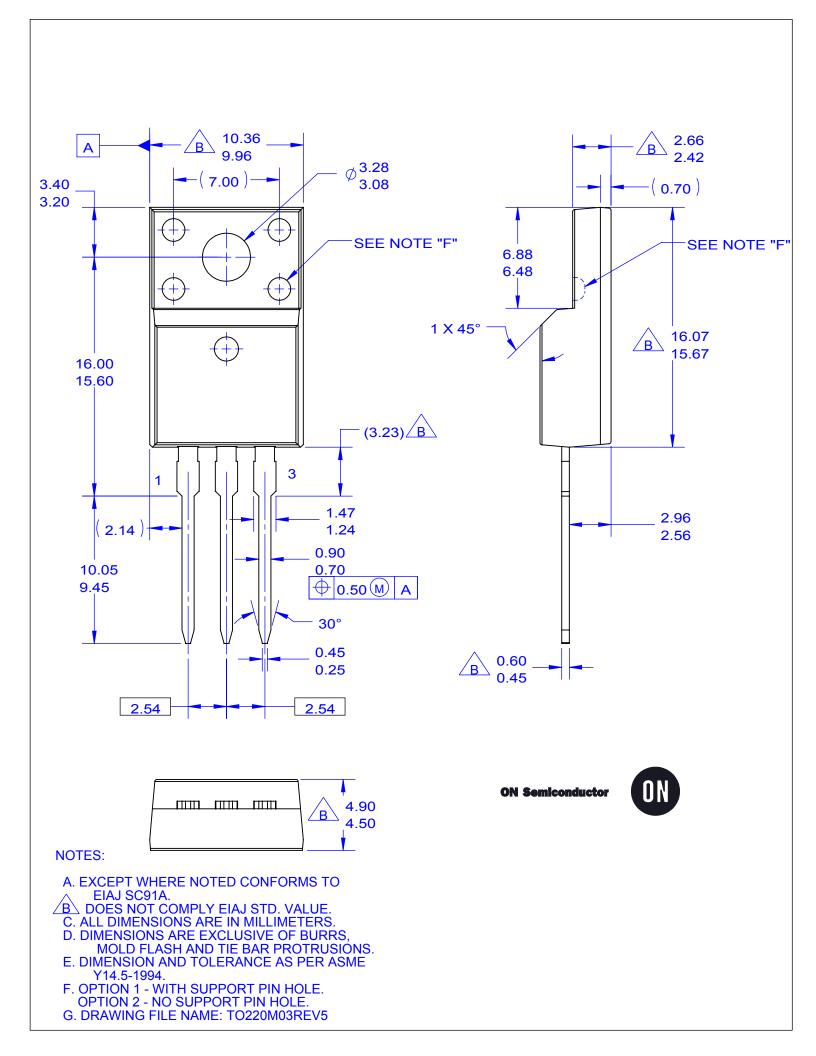






NOTES:

- A. PACKAGE REFERENCE: JEDEC TO220 VARIATION AB
- B. ALL DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSION AND TOLERANCE AS PER ASME Y14.5-2009.
- D. DIMENSIONS ARE EXCLUSIVE OF BURRS,
 - MOLD FLASH AND TIE BAR PROTRUSIÓNS.
- E. MAX WIDTH FOR F102 DEVICE = 1.35mm. F. DRAWING FILE NAME: TO220T03REV4.
- G. FAIRCHILD SEMICONDUCTOR.



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