PESD3V3Z1BSF

Extremely low capacitance bidirectional ESD protection diode

Rev. 2 — 16 January 2017 Product data sheet

1. Product profile

1.1 General description

Extremely low capacitance bidirectional ElectroStatic Discharge (ESD) protection diode, which is part of the TrEOS protection family. The device is housed in a DSN0603-2 (SOD962-2) leadless ultra small Surface-Mounted Device (SMD) package designed to protect one signal line from damage caused by ESD and other transients.

1.2 Features and benefits

- Bidirectional ESD protection of one line
- Extremely low diode capacitance C_d = 0.28 pF
- Extremely low clamping voltage to protect sensitive I/Os
- Extremely low inductance protection path to ground
- ESD protection up to 20 kV according to IEC 61000-4-2
- Ultra small SMD package
- 9.5 A maximum 8/20 µs peak pulse current

1.3 Applications

- Cellular handsets and accessories
- Portable electronics
- Communication systems
- Computers and peripherals

1.4 Quick reference data

Table 1. Quick reference data

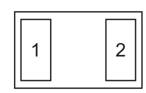
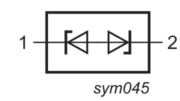
T_{amb} = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{RWM}	reverse standoff voltage		–3.3	-	+3.3	V
C_d	diode capacitance	f = 1 MHz; V_R = 0 V	-	0.28	-	pF

nexperia

2. Pinning information

Table 2. Pinning

Pin	Description	Simplified outline	Graphic symbol
1	cathode 1 [1]	 Transparent top view	
2	cathode 2		

[1] The marking bar indicates pin 1.

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PESD3V3Z1BSF	DSN0603-2	leadless ultra small package; 2 terminals; body 0.6 × 0.3 × 0.3 mm	SOD962-2

4. Marking

Table 4. Marking codes

Type number	Marking code
PESD3V3Z1BSF	U

5. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{RWM}	reverse standoff voltage		–3.3	+3.3	V
I_{PPM}	rated peak pulse current	t_p = 8/20 µs [1]	–9.5	+9.5	A
T_j	junction temperature		-	150	°C
T_{amb}	ambient temperature		–40	+125	°C
T_{stg}	storage temperature		–65	+150	°C

[1] Non-repetitive current pulse 8/20 µs exponentially decaying waveform according to IEC 61000-4-5.

Table 6. ESD maximum ratings

Symbol	Parameter	Conditions	Min	Max	Unit
V_{ESD}	electrostatic discharge voltage	IEC 61000-4-2 (contact discharge) [1]	–20	+20	kV
		IEC 61000-4-2 (air discharge) [1]	–20	+20	kV

[1] Device stressed with ten non-repetitive ESD pulses.

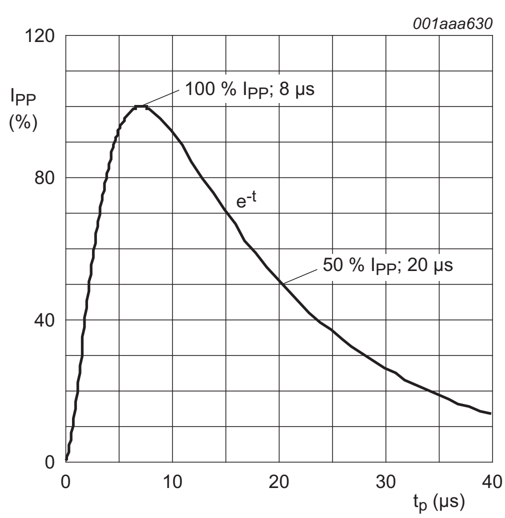


Fig 1. 8/20 µs pulse waveform according to IEC 61000-4-5

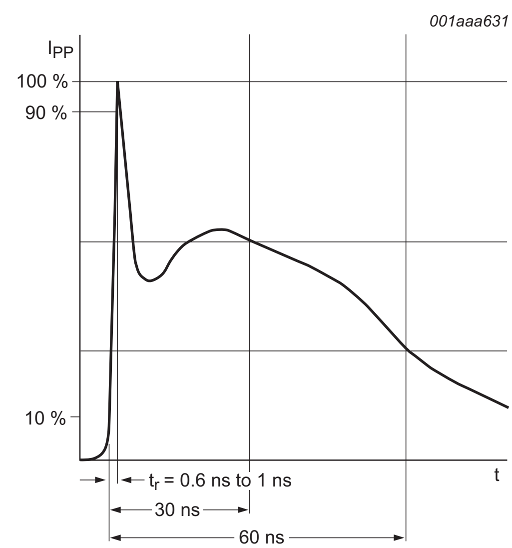


Fig 2. ESD pulse waveform according to IEC 61000-4-2

6. Characteristics

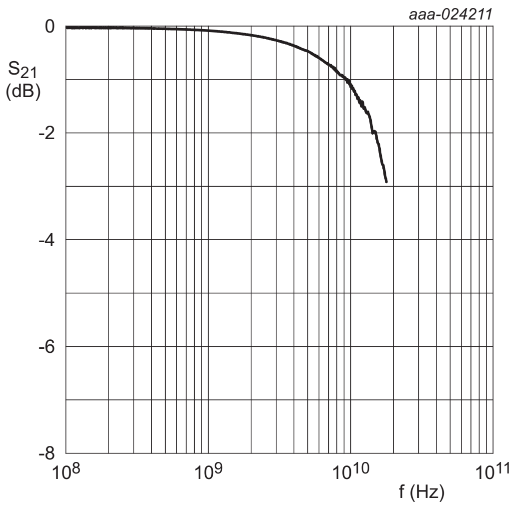
Table 7. Characteristics

T_{amb} = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
C_d	diode capacitance	f = 1 MHz; V_R = 0 V		-	0.28	0.35	pF
		f = 1 MHz; V_R = 1.5 V		-	0.25	-	pF
f_{-3dB}	cut-off frequency	normalized to attenuation at 1 MHz		-	17	-	GHz
V_{BR}	breakdown voltage	I_R = 1 mA		-	6.9	-	V
I_{RM}	reverse leakage current	V_{RWM} = 3.3 V		-	1	50	nA
r_{dyn}	dynamic resistance	I_R = 4 A to 16 A	[1]	-	0.19	-	Ω
		I_R = −4 A to −16 A	[1]	-	0.19	-	Ω
V_{CL}	clamping voltage	I_{PP} = 4 A	[2]	-	3.7	-	V
		I_{PP} = 9.5 A	[2]	-	5.3	-	V

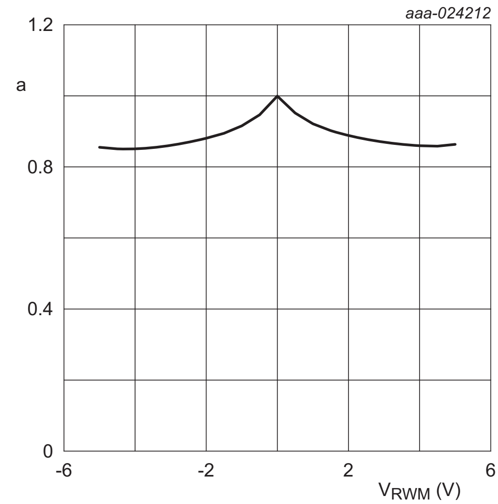
[1] Non-repetitive current pulse, Transmission Line Pulse (TLP) t_p = 100 ns; square pulse; pulser at 70 ns to 90 ns; ANSI/ESD STM5.5.1-2008.

[2] Non-repetitive current pulse 8/20 μs exponential decay waveform according to IEC 61000-4-5.



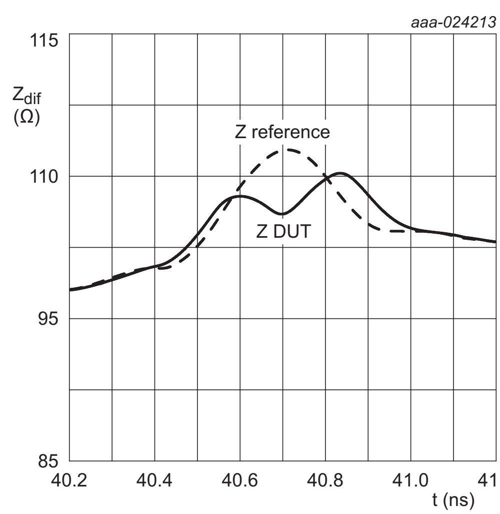
f = 1 MHz; T_{amb} = 25 °C

Fig 3. Insertion loss; typical values



$$a = \frac{C_d}{C_d(V_{RWM} = 0\ \mathrm{V})}$$

Fig 4. Relative capacitance as a function of reverse standoff voltage; typical values



Rise time = 200 ps

Fig 5. Differential Time Domain Reflectometer (TDR) plot; typical values

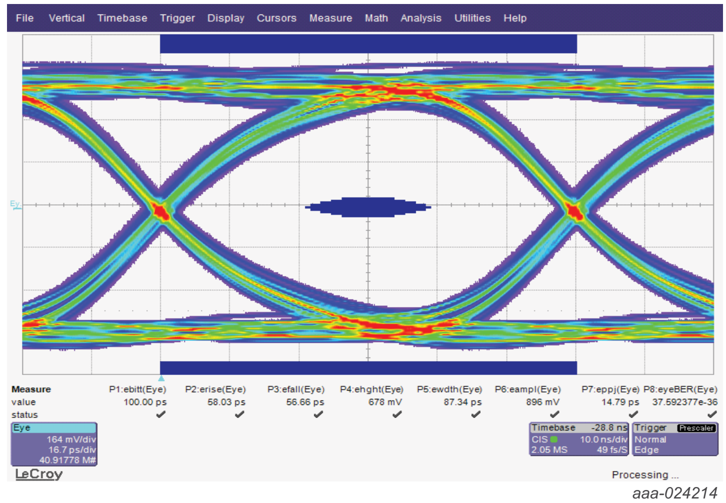


Fig 6. USB3.1 eye diagram 10 Gbit/s, test board with PESD3V3Z1BSF; typical values

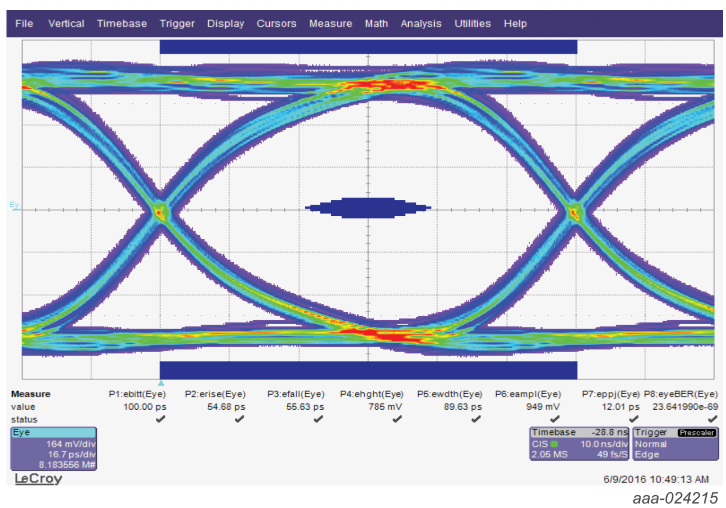
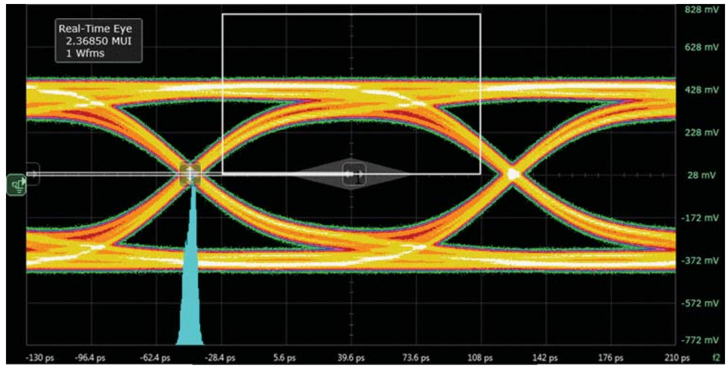


Fig 7. USB3.1 eye diagram 10 Gbit/s, test board without device; typical values



aaa-025117

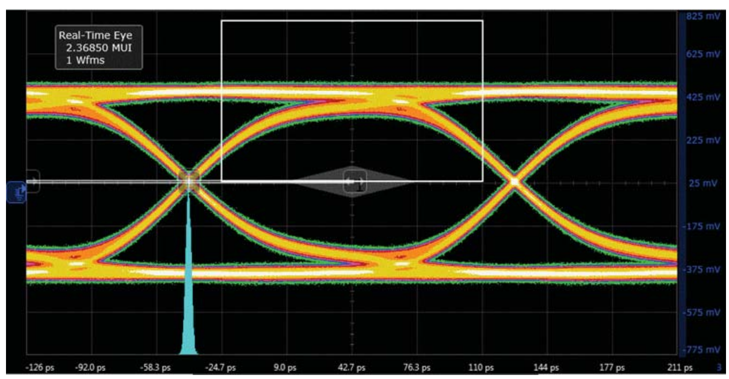
Pixel clock 148.5 MHz

Differential swing voltage 845 mV

Horizontal scale: 34 ps/div

Vertical scale: 200 mV/div

Fig 8. HDMI 2.0 eye diagram TP1, test board with PESD3V3Z1BSF; typical values



aaa-025119

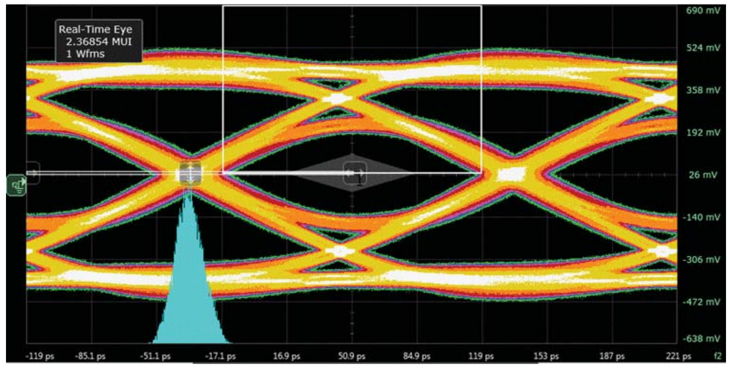
Pixel clock 148.5 MHz

Differential swing voltage 844 mV

Horizontal scale: 34 ps/div

Vertical scale: 200 mV/div

Fig 9. HDMI 2.0 eye diagram TP1, test board without device; typical values



aaa-025126

Pixel clock 148.5 MHz

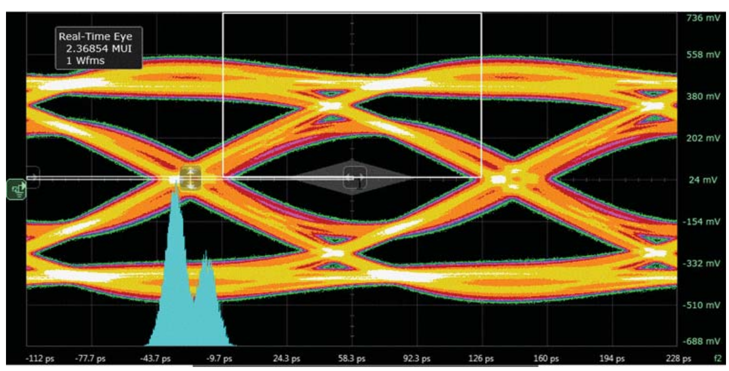
Differential swing voltage 806 mV

Horizontal scale: 34 ps / div

Vertical scale: 166 mV / div

Remark: Measured at Test Point 2 (TP2) worst cable emulator, reference cable equalizer and worst case positive skew

Fig 10. HDMI 2.0 eye diagram TP2, test board with PESD3V3Z1BSF; typical values



aaa-025127

Pixel clock 148.5 MHz

Differential swing voltage 823 mV

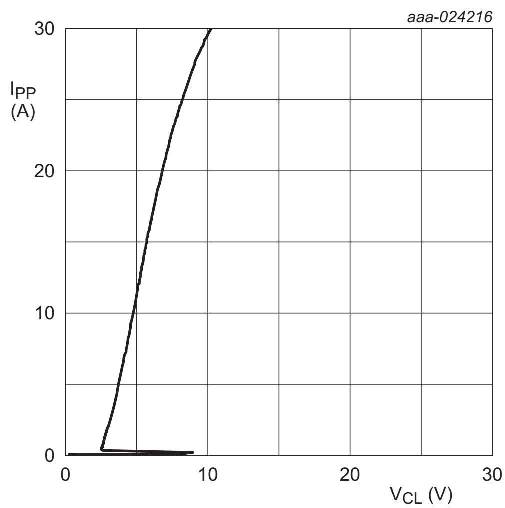
Horizontal scale: 34 ps / div

Vertical scale: 178 mV / div

Remark: Measured at Test Point 2 (TP2) worst cable emulator, reference cable equalizer and worst case positive skew

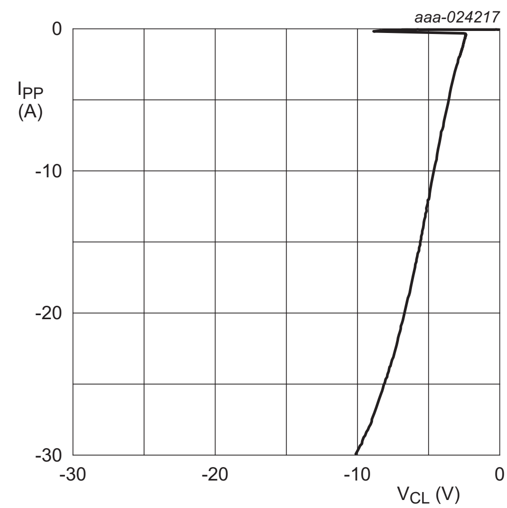
Fig 11. HDMI 2.0 eye diagram TP2, test board without device; typical values

6.1 Dynamic resistance



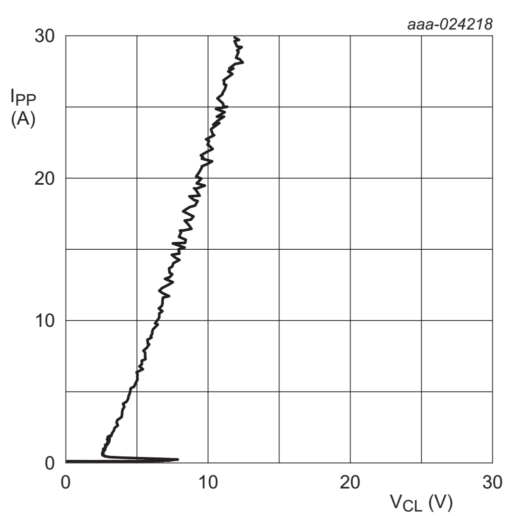
Transmission Line Pulse (TLP) = 100 ns; rise time = 1 ns

Fig 12. Dynamic resistance with positive clamping; typical values



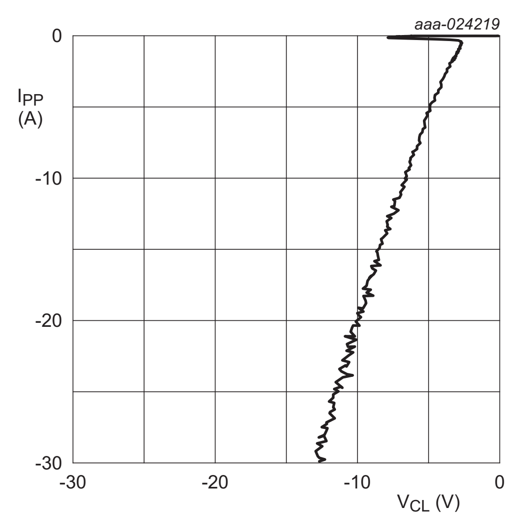
Transmission Line Pulse (TLP) = 100 ns; rise time = 1 ns

Fig 13. Dynamic resistance with negative clamping; typical values



Very Fast Transmission Line Pulse (VF-TLP) = 5 ns

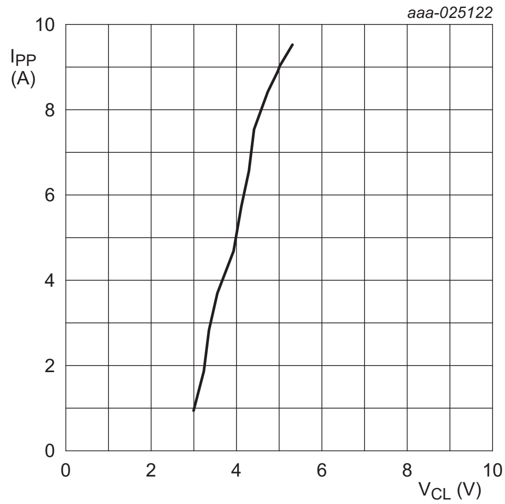
Fig 14. Dynamic resistance with positive clamping; typical values



Very Fast Transmission Line Pulse (VF-TLP) = 5 ns

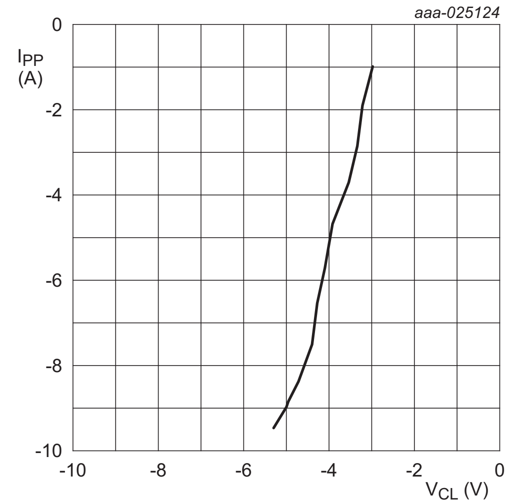
Fig 15. Dynamic resistance with negative clamping; typical values

The device uses an advanced clamping structure showing a negative dynamic resistance. This snapback behavior strongly reduces the clamping voltage to the system behind the ESD protection during an ESD event. Do not connect unlimited DC current sources to the data lines to avoid keeping the ESD protection device in snapback state after exceeding breakdown voltage (due to an ESD pulse for instance).



IEC61000-4-5; t_p = 8/20 µs; positive pulse

Fig 16. Dynamic resistance with positive clamping; typical values



IEC61000-4-5; t_p = 8/20 µs; negative pulse

Fig 17. Dynamic resistance with negative clamping; typical values

7. Application information

The device is designed for the protection of one bidirectional data or signal line from surge pulses and ESD damage. The device is suitable on lines where the signal polarities are both, positive and negative with respect to ground.

Do not connect unlimited current sources to the data lines. Refer to Section 6.1 "Dynamic resistance" for details.

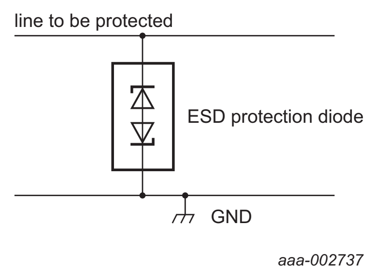


Fig 18. Application diagram

Circuit board layout and protection device placement

Circuit board layout is critical for the suppression of ESD, Electrical Fast Transient (EFT) and surge transients. The following guidelines are recommended:

1. Place the device as close to the input terminal or connector as possible.
2. Minimize the path length between the device and the protected line.
3. Keep parallel signal paths to a minimum.
4. Avoid running protected conductors in parallel with unprotected conductors.
5. Minimize all Printed-Circuit Board (PCB) conductive loops including power and ground loops.
6. Minimize the length of the transient return path to ground.
7. Avoid using shared transient return paths to a common ground point.
8. Use ground planes whenever possible. For multilayer PCBs, use ground vias.

8. Package outline

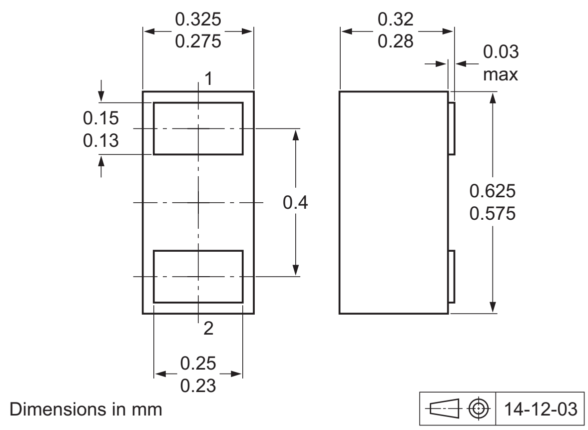


Fig 19. Package outline DSN0603-2 (SOD962-2)

9. Soldering

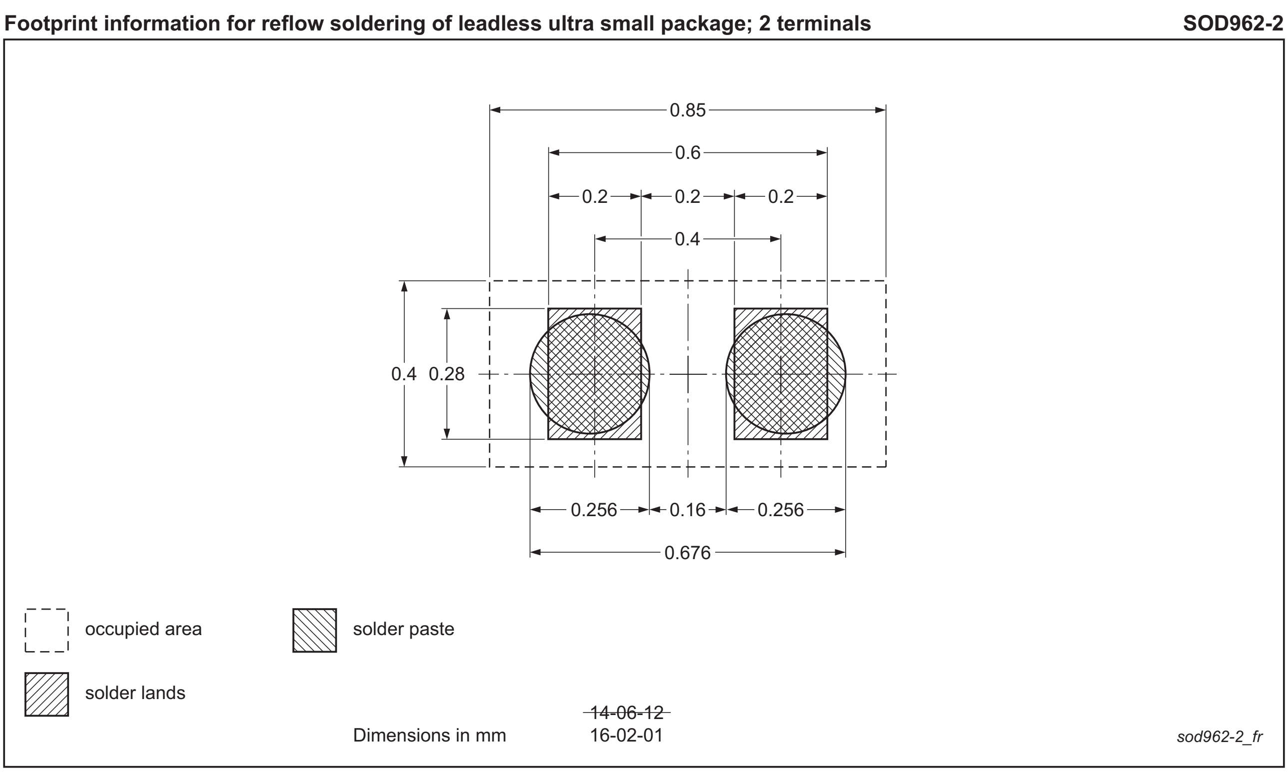


Fig 20. Reflow soldering footprint DSN0603-2 (SOD962-2)

10. Revision history

Table 8. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PESD3V3Z1BSF v.2	20170116	Products data sheet	-	PESD3V3Z1BSF v.1
Modification:	• Product status changed			
PESD3V3Z1BSF v.1	20161031	Preliminary data sheet	-	-

11. Legal information

11.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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