Source/Sink Dual ±25A or Single ±50A µModule Regulator with Input Overvoltage Protection

FEATURES

- **Dual ±25A or Single ±50A Output Source/Sink**
- **Input Voltage Range: 4.5V to 18V (20V Abs Max)**
- **Output Voltage Range: 0.6V to 7.5V (8V Abs Max)**
- **±1.5% Maximum Total DC Output Error Over Line, Load and Temperature**
- **Adjustable Control Loop Compensation**
- **Differential Remote Sense Amplifier**
- **Current Mode Control/Fast Transient Response**
- **Multiphase Parallel Current Sharing Up to ±300A**
- **Internal Temperature Monitor**
- Adjustable Switching Frequency or Synchronization
- Overcurrent Foldback Protection
- Selectable Pulse-Skipping Mode Operation
- Soft-Start/Voltage Tracking
- Input and Output Overvoltage Protection
- 16mm × 16mm × 4.92mm BGA Package

APPLICATIONS

- Test and Measurement Instrumentation
- Telecom and Networking Equipment
- Industrial Equipment

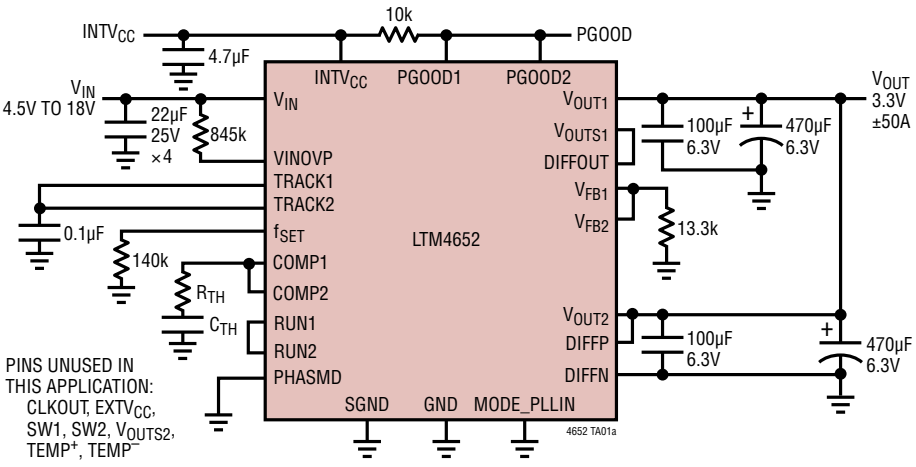
DESCRIPTION

The LTM®4652 is a source/sink dual ±25A or single ±50A output switching mode step-down DC/DC µModule® (micromodule) regulator with ±1.5% total DC output error. Included in the package are the switching controllers, power MOSFETs, inductors and all supporting components. Operating from an input voltage range of 4.5V to 18V, the LTM4652 supports two outputs with an output voltage range of 0.6V to 7.5V, each set by a single external resistor. Its high efficiency design delivers up to ±25A continuous current for each output. Only a few input and output capacitors are needed. Adjustable control loop compensation allows for fast transient response to minimize output capacitance when powering FPGAs, ASICs, and processors.

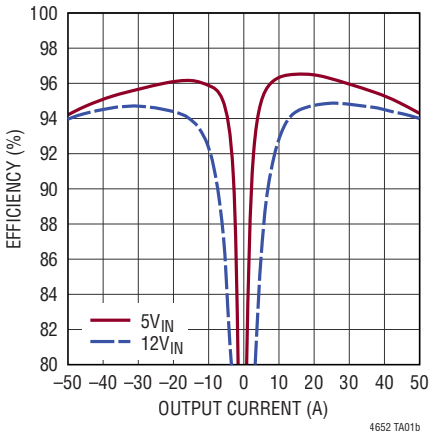
Fault protection features include input and output overvoltage and bidirectional overcurrent protection. The LTM4652 is offered in a 16mm × 16mm × 4.92mm BGA package.

TYPICAL APPLICATION

±50A, 3.3V Bidirectional Output DC/DC µModule Regulator with Input Overvoltage Protection



3.3V_{OUT} Efficiency vs I_{OUT}



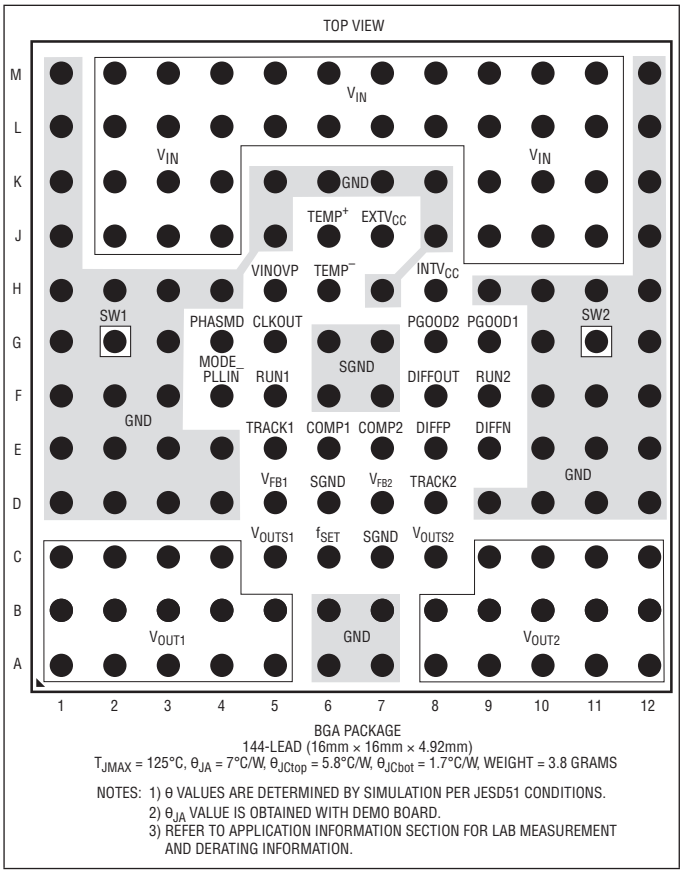
Rev. A

ABSOLUTE MAXIMUM RATINGS

(Note 1)

V_{IN} ..... –0.3V to 20V
PGOOD1, PGOOD2, RUN1, RUN2,
$INTV_{CC}$, $EXTV_{CC}$..... –0.3V to 6V
MODE_PLLIN, f_{SET}, TRACK1, TRACK2,
DIFFOUT, PHASMD ..... –0.3V to $INTV_{CC}$
V_{OUT1}, V_{OUT2}, V_{OUTS1}, V_{OUTS2} (Note 5)..... –0.3V to 8V
DIFFP, DIFFN, VINOVP..... –0.3V to $INTV_{CC}$
COMP1, COMP2, V_{FB1}, V_{FB2} (Note 5)..... –0.3V to 2.7V
$INTV_{CC}$ Peak Output Current.....50mA
Internal Operating Temperature Range
(Note 2)..... –40°C to 125°C
Storage Temperature Range ..... –55°C to 125°C
Peak Package Body Temperature..... 245°C

PIN CONFIGURATION



BGA PACKAGE
144-LEAD (16mm × 16mm × 4.92mm)
T_{JMAX} = 125°C, θ_{JA} = 7°C/W, θ_{JCtop} = 5.8°C/W, θ_{JCbot} = 1.7°C/W, WEIGHT = 3.8 GRAMS

NOTES: 1) θ VALUES ARE DETERMINED BY SIMULATION PER JESD51 CONDITIONS.
2) θ_{JA} VALUE IS OBTAINED WITH DEMO BOARD.
3) REFER TO APPLICATION INFORMATION SECTION FOR LAB MEASUREMENT AND DERATING INFORMATION.

ORDER INFORMATION

PART NUMBER	PAD OR BALL FINISH	PART MARKING		PACKAGE TYPE	MSL RATING	TEMPERATURE RANGE (NOTE 2)
		DEVICE	FINISH CODE			
LTM4652EY#PBF	SAC305 (RoHS)	LTM4652Y	e1	BGA	4	–40°C to 125°C
LTM4652IY#PBF						

- Contact the factory for parts specified with wider operating temperature ranges. Pad or ball finish code is per IPC/JEDEC J-STD-609.
- Recommended LGA and BGA PCB Assembly and Manufacturing Procedures
- LGA and BGA Package and Tray Drawings

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified internal operating temperature range. Specified as each individual output channel (Note 3). T_A = 25°C (Note 2), V_{IN} = 12V, V_{RUN1}, V_{RUN2} at 5V and I_{OUT1}, I_{OUT2} at 0A unless otherwise noted. Per the typical application in Figure 31.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN}	Input DC Voltage		●	4.5		18	V
V_{OUT}	Output Voltage		●	0.6		7.5	V
$V_{OUT1(DC)}$, $V_{OUT2(DC)}$	Output Voltage, Total DC Variation with Line and Load (Note 7)	C_{IN} = 22µF ×3, C_{OUT} = 100µF ×1 Ceramic, 470µF POSCAP, V_{IN} = 4.5V to 18V, V_{OUT} = 1.2V, I_{OUT} = 0A to ±25A	●	1.182	1.2	1.218	V
Input Specifications							
V_{RUN1}, V_{RUN2}	RUN Pin Off Threshold	RUN Rising		1.1	1.22	1.4	V
$V_{RUN1HYS}$, $V_{RUN2HYS}$	RUN Pin On Hysteresis				135		mV
V_{VINOVP}	VINOVP Pin OVP Inception Threshold	VINOVP Rising		1.1	1.22	1.4	V
V_{OVP_HYS}	VINOVP Pin OVP Inception Hysteresis				10		mV
$I_{INRUSH(VIN)}$	Input Inrush Current at Start-Up	I_{OUT} = 0A, C_{IN} = 22µF ×3, C_{SS} = 0.01µF, C_{OUT} = 100µF ×3, V_{OUT1} = 1.2V, V_{OUT2} = 1.2V, V_{IN} = 12V			1		A
$I_{Q(VIN)}$	Input Supply Bias Current (Both Channels On)	V_{IN} = 12V, V_{OUT} = 1.2V, Pulse-Skipping Mode V_{IN} = 12V, V_{OUT}= 1.2V, Switching Continuous Shutdown, RUN = 0, V_{IN} = 12V			22 135 35		mA mA µA
$I_{S(VIN)}$	Input Supply Current	V_{IN} = 4.5V, V_{OUT} = 1.2V, I_{OUT} = 25A V_{IN} = 12V, V_{OUT} = 1.2V, I_{OUT} = 25A V_{IN} = 4.5V, V_{OUT} = 1.2V, I_{OUT} = –25A V_{IN} = 12V, V_{OUT} = 1.2V, I_{OUT} = –25A			8.0 3.0 –5.2 –1.9		A A A A
Output Specifications							
$I_{OUT1(DC)}$, $I_{OUT2(DC)}$	Output Continuous Current Range	V_{IN} = 12V, V_{OUT} = 1.2V (Note 6)		–25		25	A
$\Delta V_{OUT1(LINE)}/V_{OUT1}$ $\Delta V_{OUT2(LINE)}/V_{OUT2}$	Line Regulation Accuracy	For Each Output, V_{OUT} = 1.2V, I_{OUT} = 0A, V_{IN} from 4.5V to 18V	●		0.02	0.1	%/V
$\Delta V_{OUT1}/V_{OUT1}$ $\Delta V_{OUT2}/V_{OUT2}$	Load Regulation Accuracy	For Each Output, V_{IN} = 12V, V_{OUT} = 1.2V, I_{OUT} from 0A to ±25A	●		0.2	0.75	%
$V_{OUT1(AC)}$, $V_{OUT2(AC)}$	Output Ripple Voltage	For Each Output, V_{IN} = 12V, V_{OUT} = 1.2V, Frequency = 450kHz, I_{OUT} = 0A, C_{OUT} = 100µF ×3 Ceramic, 470µF POSCAP			15		mV_{P-P}
f_{SW} (Each Channel)	Output Ripple Voltage Frequency	V_{IN} = 12V, V_{OUT} = 1.2V, f_{SET} = 1.2V (Note 4)			500		kHz
f_{SYNC} (Each Channel)	Phase-Locked Loop Synchronization Capture Range	(Note 4)		400		750	kHz
$\Delta V_{OUTSTART}$ (Each Channel)	Turn-On Overshoot	C_{OUT} = 100µF ×3 Ceramic, 470µF POSCAP, V_{IN} = 12V , V_{OUT} = 1.2V, I_{OUT} = 0A			10		mV
t_{START} (Each Channel)	Turn-On Time	C_{OUT} = 100µF ×4 Ceramic, V_{IN} = 12V, No Load, TRACK with 0.01µF to GND			5		ms
$\Delta V_{OUT(LS)}$ (Each Channel)	Peak Deviation for Dynamic Load	Load: 0% to 50% to 0% of Full Load, C_{OUT} = 100µF ×3 Ceramic, 470µF POSCAP, V_{IN} = 12V, V_{OUT} = 1.2V (Note 8)			30		mV
t_{SETTLE} (Each Channel)	Settling Time for Dynamic Load Step	Load: 0% to 50% to 0% of Full Load, V_{IN} = 12V, C_{OUT} = 100µF ×3 Ceramic, 470µF POSCAP (Note 8)			20		µs
$I_{OUT(PK)}$ (Each Channel)	Output Current Limit	V_{IN} = 12V, V_{OUT} = 1.2V			35		A

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified internal operating temperature range. Specified as each individual output channel (Note 3). T_A = 25°C (Note 2), V_{IN} = 12V, V_{RUN1}, V_{RUN2} at 5V and I_{OUT1}, I_{OUT2} at 0A unless otherwise noted. Per the typical application in Figure 31.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Control Section							
V_{FB1}, V_{FB2}	Voltage at V_{FB} Pins	I_{OUT} = 0A, V_{OUT} = 1.2V	●	0.594	0.600	0.606	V
I_{FB}		(Note 5)			–5	–30	nA
V_{OVL}	Feedback Overvoltage Lockout		●	0.64	0.66	0.68	V
I_{TRACK1}, I_{TRACK2}	Track Pin Soft-Start Pull-Up Current	TRACK1, TRACK2 Start at 0V		1	1.25	1.5	µA
UVLO	Undervoltage Lockout (Falling)				3.4		V
UVLO Hysteresis					0.6		V
$t_{ON(MIN)}$	Minimum On-Time	(Note 5)			90		ns
R_{FBHI1}, R_{FBHI2}	Resistor Between V_{OUTS1}, V_{OUTS2} and V_{FB1}, V_{FB2} Pins for Each Output			60.05	60.4	60.75	kΩ
V_{PGOOD1}, V_{PGOOD2} Low	PGOOD Voltage Low	I_{PGOOD} = 2mA			0.1	0.3	V
I_{PGOOD}	PGOOD Leakage Current	V_{PGOOD} = 5V				±5	µA
V_{PGOOD}	PGOOD Trip Level	V_{FB} with Respect to Set Output Voltage V_{FB} Ramping Negative V_{FB} Ramping Positive			 –10 10		 % %
$INTV_{CC}$ Linear Regulator							
V_{INTVCC}	Internal V_{CC} Voltage	6V < V_{IN} < 18V		4.75	5	5.2	V
V_{INTVCC} Load Regulation	$INTV_{CC}$ Load Regulation	I_{CC} = 0mA to 50mA			0.5	2	%
V_{EXTVCC}	$EXTV_{CC}$ Switchover Voltage	$EXTV_{CC}$ Ramping Positive		4.5	4.7		V
$V_{EXTVCC(DROP)}$	$EXTV_{CC}$ Dropout	I_{CC} = 20mA, V_{EXTVCC} = 5V			50	100	mV
$V_{EXTVCC(HYST)}$	$EXTV_{CC}$ Hysteresis				220		mV
Oscillator							
Frequency Nominal	Nominal Frequency	f_{SET} = 1.2V		450	500	550	kHz
Frequency Low	Lowest Frequency	f_{SET} = 0.93V f_{SET} = 0V (Note 5)			400 250		kHz kHz
Frequency High	Highest Frequency	f_{SET} > 2.4V, Up to $INTV_{CC}$			780		kHz
f_{SET}	Frequency Set Current			8.5	9.5	11	µA
R_{MODE_PLLIN}	MODE_PLLIN Input Resistance				250		kΩ
CLKOUT	Phase (Relative to V_{OUT1})	PHASMD = GND PHASMD = Float PHASMD = $INTV_{CC}$			60 90 120		Deg Deg Deg
CLK High CLK Low	Clock High Output Voltage Clock Low Output Voltage			2		 0.4	V V
Differential Amplifier							
A_V Differential Amp	Gain				1		V/V
R_{IN}	Input Resistance	Measured at DIFFP Input			80		kΩ
V_{OS}	Input Offset Voltage	V_{DIFFP} = $V_{DIFFOUT}$ = 1.5V, $I_{DIFFOUT}$ = 100µA				3	mV
PSRR Differential Amp	Power Supply Rejection Ratio	4.5V < V_{IN} < 18V			90		dB
I_{CL}	Maximum Output Current				3		mA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified internal operating temperature range. Specified as each individual output channel (Note 3). T_A = 25°C (Note 2), V_{IN} = 12V, V_{RUN1}, V_{RUN2} at 5V and I_{OUT1}, I_{OUT2} at 0A unless otherwise noted. Per the typical application in Figure 31.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$V_{OUT(MAX)}$	Maximum Output Voltage	$I_{DIFFOUT}$ = 300µA		$INTV_{CC}$ – 1.4			V
GBW	Gain Bandwidth Product				3		MHz
ΔV_{TEMP}	Diode Connected PNP	I_{TEMP}^+ = 100µA, I_{TEMP}^- = –100µA			0.6		V
T_C	Temperature Coefficient		●		–2.2		mV/C
η	Ideality Factor				1.004		

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTM4652 is tested under pulsed-load conditions such that $T_J \approx T_A$. The LTM4652E is guaranteed to meet performance specifications over the 0°C to 125°C internal operating temperature range. Specifications over the –40°C to 125°C internal operating temperature range are assured by design, characterization and correlation with statistical process controls. The LTM4652I is guaranteed to meet specifications over the full –40°C to 125°C internal operating temperature range. Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal resistance and other environmental factors.

Note 3: Two outputs are tested separately and the same testing condition is applied to each output.

Note 4: The LTM4652 device is designed to operate best from 400kHz to 780kHz. For some applications such as $1V_{OUT}$, operation at 300kHz is acceptable—but not ATE-tested in production.

Note 5: These parameters are tested at wafer sort.

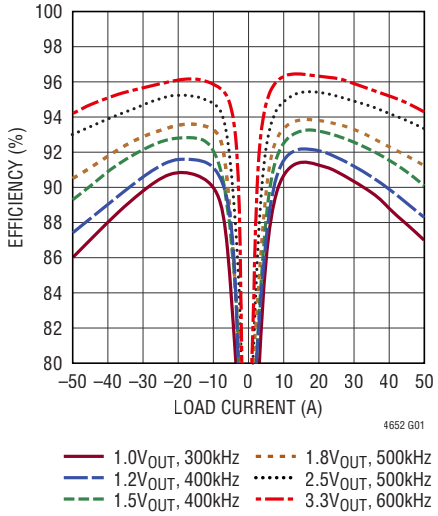
Note 6: See output current derating curve for different ambient temperature.

Note 7: Total DC output voltage error includes all errors over temperature—reference, line and load regulation as well as the tolerance of the integrated top feedback resistor.

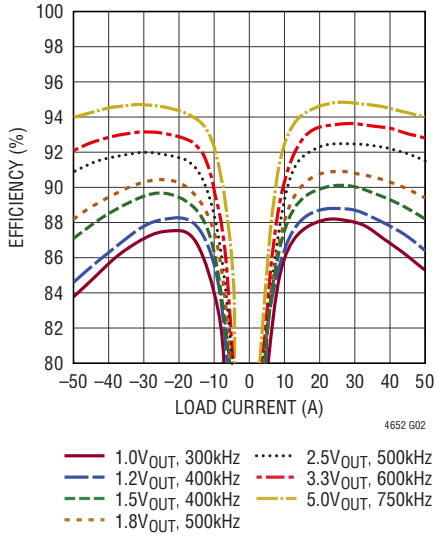
Note 8: Transient response and load step performance are layout dependent and thus application-specific. Typical values are reported from lab Demo Board evaluation. Evaluation in application demonstrates capability.

TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

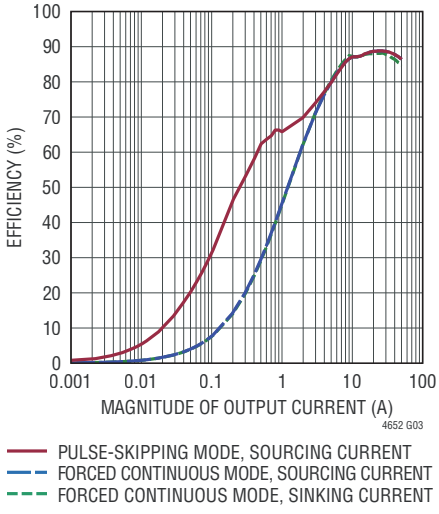
Efficiency vs Output Current, V_{IN} = 5V, Outputs Paralleled



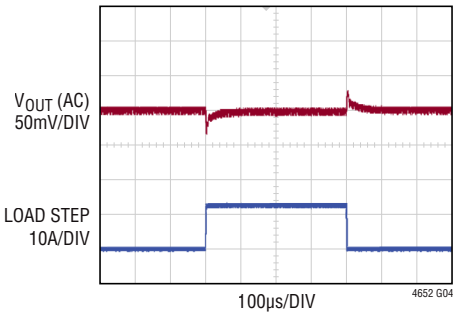
Efficiency vs Output Current, V_{IN} = 12V, Outputs Paralleled



Pulse-Skipping Mode Efficiency V_{IN} = 12V, V_{OUT} = 1.2V, f_S = 400kHz, Outputs Paralleled

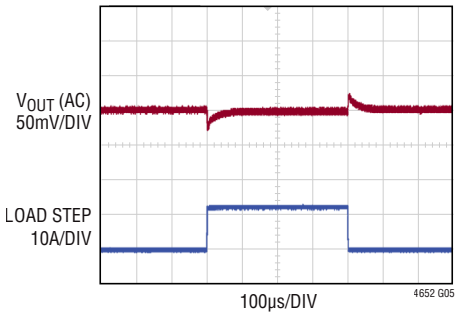


1V Dual Phase Single Output Load Transient Response (Ceramic Output Capacitor Only)



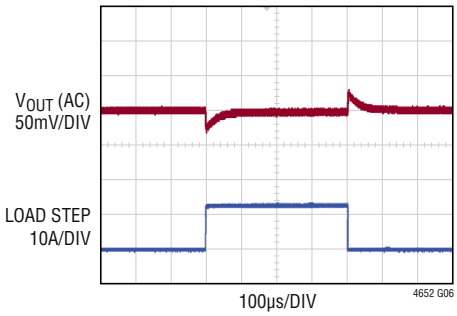
$12V_{IN}$, $1V_{OUT}$, 300kHz
25%, 12.5A LOAD STEP-UP AND
STEP-DOWN, 10A/µs SLEW RATE
C_{OUT} = 220µF ×8 CERAMIC CAP
R_{TH} = 3.32k, C_{TH} = 6800pF, C_{FF} = 68pF

1.2V Dual Phase Single Output Load Transient Response (Ceramic Output Capacitor Only)



$12V_{IN}$, $1.2V_{OUT}$, 400kHz
25%, 12.5A LOAD STEP-UP AND
STEP-DOWN, 10A/µs SLEW RATE
C_{OUT} = 220µF ×8 CERAMIC CAP
R_{TH} = 3.32k, C_{TH} = 6800pF, C_{FF} = 68pF

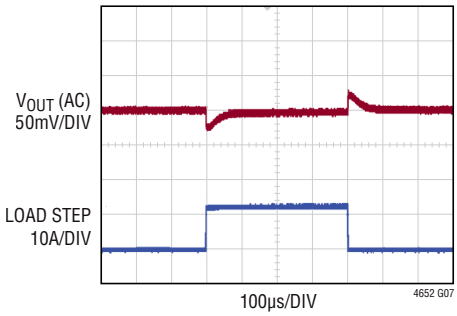
1.5V Dual Phase Single Output Load Transient Response (Ceramic Output Capacitor Only)



$12V_{IN}$, $1.5V_{OUT}$, 400kHz
25%, 12.5A LOAD STEP-UP AND
STEP-DOWN, 10A/µs SLEW RATE
C_{OUT} = 220µF ×8 CERAMIC CAP
R_{TH} = 3.32k, C_{TH} = 6800pF, C_{FF} = 68pF

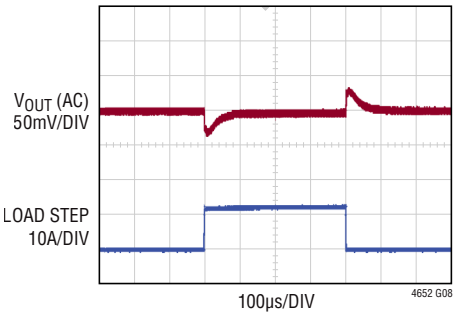
TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

1.8V Dual Phase Single Output Load Transient Response (Ceramic Output Capacitor Only)



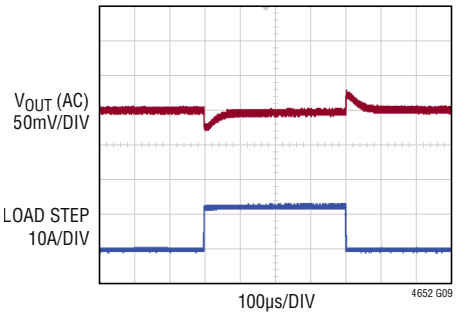
$12V_{IN}$, $1.8V_{OUT}$, 500kHz
25%, 12.5A LOAD STEP-UP AND
STEP-DOWN, 10A/µs SLEW RATE
C_{OUT} = 220µF ×8 CERAMIC CAP
R_{TH} = 3.32k, C_{TH} = 6800pF, C_{FF} = 68pF

2.5V Dual Phase Single Output Load Transient Response (Ceramic Output Capacitor Only)



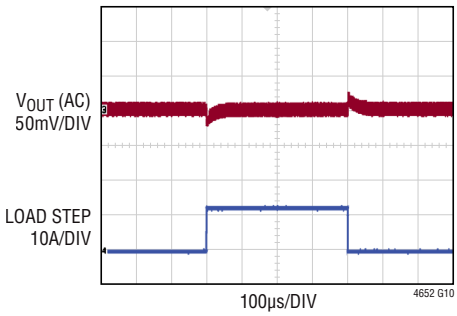
$12V_{IN}$, $2.5V_{OUT}$, 500kHz
25%, 12.5A LOAD STEP-UP AND
STEP-DOWN, 10A/µs SLEW RATE
C_{OUT} = 220µF ×8 CERAMIC CAP
R_{TH} = 3.32k, C_{TH} = 6800pF, C_{FF} = 68pF

3.3V Dual Phase Single Output Load Transient Response (Ceramic Output Capacitor Only)



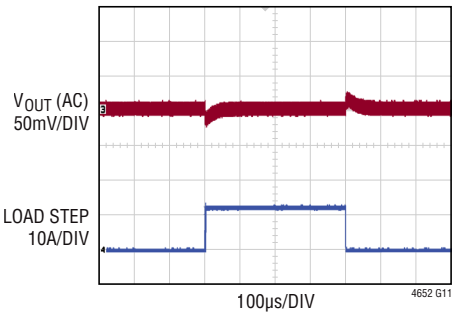
$12V_{IN}$, $3.3V_{OUT}$, 600kHz
25%, 12.5A LOAD STEP-UP AND
STEP-DOWN, 10A/µs SLEW RATE
C_{OUT} = 220µF ×8 CERAMIC CAP
R_{TH} = 3.32k, C_{TH} = 6800pF, C_{FF} = 68pF

1V Dual Phase Single Output Load Transient Response (Bulk Output Capacitor)



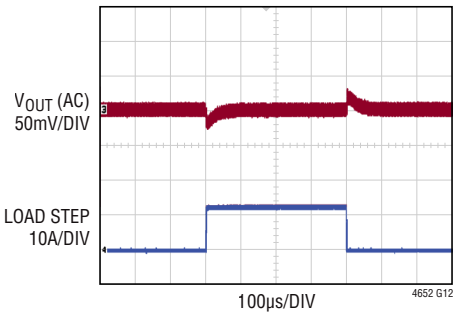
$12V_{IN}$, $1V_{OUT}$, 300kHz
25%, 12.5A LOAD STEP-UP AND
STEP-DOWN, 10A/µs SLEW RATE
C_{OUT} = 220µF ×4 CERAMIC CAP
+ 470µF ×2, 2.5V SPCAP
C_{THP} = 10pF, R_{TH} = 4.65k
C_{TH} = 4700pF, C_{FF} = 10pF

1.2V Dual Phase Single Output Load Transient Response (Bulk Output Capacitor)



$12V_{IN}$, $1.2V_{OUT}$, 400kHz
25%, 12.5A LOAD STEP-UP AND
STEP-DOWN, 10A/µs SLEW RATE
C_{OUT} = 220µF ×4 CERAMIC CAP
+ 470µF ×2, 2.5V SPCAP
C_{THP} = 10pF, R_{TH} = 4.65k
C_{TH} = 4700pF, C_{FF} = 10pF

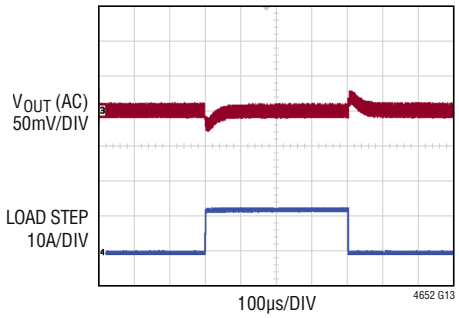
1.5V Dual Phase Single Output Load Transient Response (Bulk Output Capacitor)



$12V_{IN}$, $1.5V_{OUT}$, 400kHz
25%, 12.5A LOAD STEP-UP AND
STEP-DOWN, 10A/µs SLEW RATE
C_{OUT} = 220µF ×4 CERAMIC CAP
+ 470µF ×2, 2.5V SPCAP
C_{THP} = 10pF, R_{TH} = 4.65k
C_{TH} = 4700pF, C_{FF} = 10pF

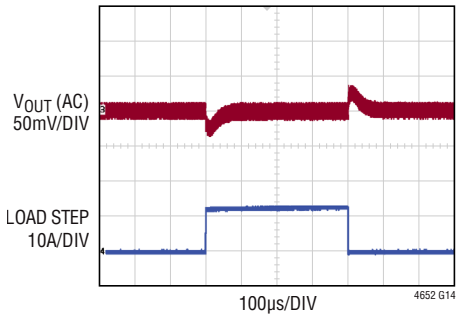
TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

1.8V Dual Phase Single Output Load Transient Response (Bulk Output Capacitor)



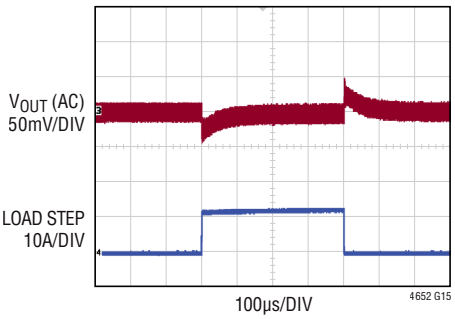
$12V_{IN}$, $1.8V_{OUT}$, 500kHz
25%, 12.5A LOAD STEP-UP AND STEP-DOWN, 10A/µs SLEW RATE
C_{OUT} = 220µF ×4 CERAMIC CAP + 470µF ×2, 2.5V SPCAP
C_{THP} = 10pF, R_{TH} = 4.65k
C_{TH} = 4700pF, C_{FF} = 10pF

2.5V Dual Phase Single Output Load Transient Response (Bulk Output Capacitor)



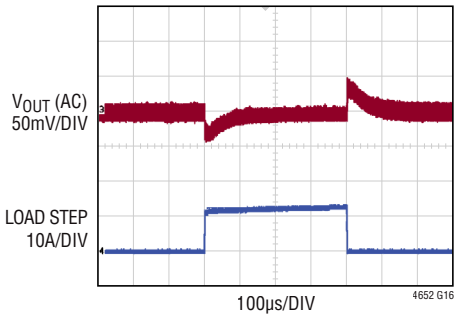
$12V_{IN}$, $2.5V_{OUT}$, 500kHz
25%, 12.5A LOAD STEP-UP AND STEP-DOWN, 10A/µs SLEW RATE
C_{OUT} = 220µF ×4 CERAMIC CAP + 470µF ×2, 2.5V SPCAP
C_{THP} = 10pF, R_{TH} = 4.65k
C_{TH} = 4700pF, C_{FF} = 10pF

3.3V Dual Phase Single Output Load Transient Response (Bulk Output Capacitor)



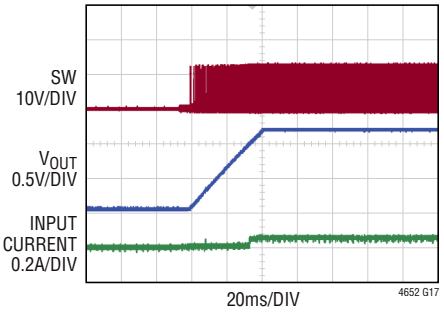
$12V_{IN}$, $3.3V_{OUT}$, 600kHz
25%, 12.5A LOAD STEP-UP AND STEP-DOWN, 10A/µs SLEW RATE
C_{OUT} = 220µF ×4 CERAMIC CAP + 470µF ×2, 6.3V POSCAP
C_{THP} = 10pF, R_{TH} = 9.09k
C_{TH} = 4700pF, C_{FF} = NONE

5V Dual Phase Single Output Load Transient Response (Bulk Output Capacitor)



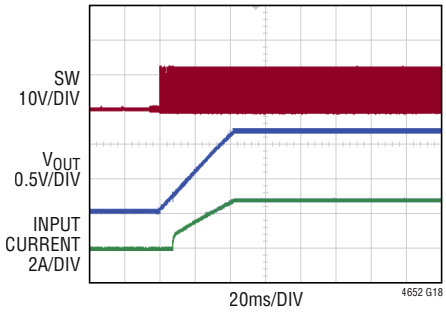
$12V_{IN}$, $5V_{OUT}$, 750kHz
25%, 12.5A LOAD STEP-UP/ STEP-DOWN, 10A/µs SLEW RATE, C_{OUT} = 220µF ×4 CERAMIC CAP + 470µF ×2, 6.3V POSCAP
C_{THP} = 10pF, R_{TH} = 9.09k
C_{TH} = 4700pF, C_{FF} = NONE

Single Phase Start-Up with No Load



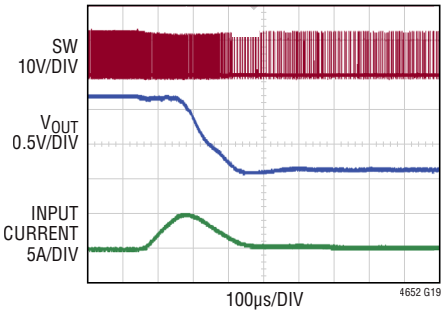
$12V_{IN}$, $1.2V_{OUT}$, 400kHz
C_{OUT} = 470µF ×2
SPCAP + 100µF ×4 CERAMIC CAP
C_{SS} = 0.1µF

Single Phase Start-Up with 25A Load



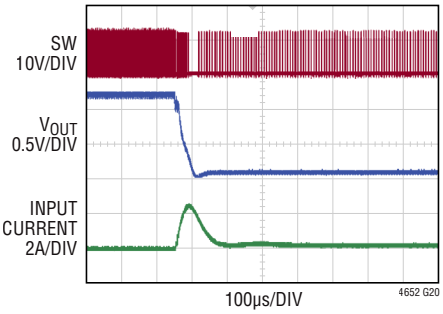
$12V_{IN}$, $1.2V_{OUT}$, 400kHz
C_{OUT} = 470µF ×2
SPCAP + 100µF ×4 CERAMIC CAP, C_{SS} = 0.1µF

Single Phase Short-Circuit Protection with No Load



$12V_{IN}$, $1.2V_{OUT}$, 400kHz
C_{OUT} = 470µF ×2
SPCAP + 100µF ×4 CERAMIC CAP

Single Phase Short-Circuit Protection with 25A Load



$12V_{IN}$, $1.2V_{OUT}$, 400kHz
C_{OUT} = 470µF ×2
SPCAP + 100µF ×4 CERAMIC CAP

Rev. A

PIN FUNCTIONS (Recommended to use test points to monitor signal pin connections.)

PACKAGE ROW AND COLUMN LABELING MAY VARY AMONG µModule PRODUCTS. REVIEW EACH PACKAGE LAYOUT CAREFULLY.

V_{OUT1} (Pins A1–A5, B1–B5, C1–C4): Power Output Pins. Apply output load between these pins and GND pins. Recommend placing output decoupling capacitance directly between these pins and GND pins. Review Table 6.

GND (Pins A6–A7, B6–B7, D1–D4, D9–D12, E1–E4, E10–E12, F1–F3, F10–F12, G1, G3, G10, G12, H1–H4, H7, H9–H12, J1, J5, J8, J12, K1, K5–K8, K12, L1, L12, M1, M12): Power Ground Pins for Both Input and Output Returns.

V_{OUT2} (Pins A8–A12, B8–B12, C9–C12): Power Output Pins. Apply output load between these pins and GND pins. Recommend placing output decoupling capacitance directly between these pins and GND pins. Review Table 6.

V_{OUTS1}, V_{OUTS2} (Pins C5, C8): This pin is connected to the top of the internal top feedback resistor for each output. The pin can be directly connected to its specific output, or connected to DIFFOUT when the remote sense amplifier is used. In paralleling modules, one of the V_{OUTS} pins is connected to the DIFFOUT pin in remote sensing or directly to V_{OUT} with no remote sensing. It is very important to connect these pins to either the DIFFOUT or V_{OUT} since this is the feedback path, and cannot be left open. See the Applications Information section.

f_{SET} (Pin C6): Frequency Set Pin. A 9.5µA current is sourced from this pin. A resistor from this pin to ground sets a voltage that in turn programs the operating frequency. Alternatively, this pin can be driven with a DC voltage that can set the operating frequency. See the Applications Information section.

SGND (Pins C7, D6, G6–G7, F6–F7): Signal Ground Pin. Return ground path for all analog and low power circuitry. Tie a single connection to the output capacitor GND in the application. See layout guidelines in Figure 30.

V_{FB1}, V_{FB2} (Pins D5, D7): The Negative Input of the Error Amplifier for Each Channel. Internally, this pin is connected to V_{OUTS1} or V_{OUTS2} with a 60.4k precision resistor. Different output voltages can be programmed with an additional resistor between V_{FB} and GND pins. In PolyPhase® operation, tying the V_{FB} pins together allows for parallel operation. See the Applications Information section for details. Do not drive this pin.

TRACK1, TRACK2 (Pins E5, D8): Output Voltage Tracking Pin and Soft-Start Inputs. Each channel has a 1.25µA pull-up current source. When one channel is configured to be the main of the two channels, then a capacitor from this pin to ground will set a soft-start ramp rate. The remaining channel can be set up as the subordinate, and have the main's output applied through a voltage divider to the subordinate output's TRACK pin. This voltage divider is equal to the subordinate output's feedback divider for coincidental tracking. See the Applications Information section.

COMP1, COMP2 (Pins E6, E7): Current control threshold and error amplifier compensation point for each channel. The current comparator threshold increases with this control voltage. COMP pin internal has 10pF filter cap to SGND. An external RC filter circuit is required for control loop compensation. See Applications Information section. Tie the COMP pins together for parallel operation. Do not drive this pin.

DIFFP (Pin E8): Positive input of the remote sense amplifier. This pin is connected to the remote sense point of the output voltage. Diffamp can be used for ≤3.3V outputs. See the Applications Information section.

DIFFN (Pin E9): Negative input of the remote sense amplifier. This pin is connected to the remote sense point of the output GND. Diffamp can be used for ≤3.3V outputs. See the Applications Information section.

MODE_PLLIN (Pin F4): Forced Continuous Mode or Pulse-Skipping Mode Selection Pin and External Synchronization Input to Phase Detector Pin. Connect this pin to SGND to force both channels into forced continuous mode of operation. Connect to $INTV_{CC}$ to enable pulse-skipping mode of operation. A clock on the pin will force both channels into continuous mode of operation and synchronized to the external clock applied to this pin.

Note that this module is designed to conduct bidirectional output current. When pulse-skipping mode is selected, there is no way for the control loop to command

PIN FUNCTIONS (Recommended to use test points to monitor signal pin connections.)

instantaneous inductor current below 0A except by deliberately allowing the output voltage to rise high enough (~10% above nominal regulation) to induce an output overvoltage response. Transient and sustained operation in this manner is strongly not recommended.

Thus, in applications where transient and/or sustained negative (sinking) output current is expected, the LTM4652 must be operated in forced continuous mode.

RUN1, RUN2 (Pins F5, F9): Run Control Pin. A voltage above 1.22V will turn on each channel in the module. A voltage below 1.085V (135mV hysteresis, typ.) on the RUN pin will turn off the related channel. Each RUN pin has a 1µA pull-up current, once the RUN pin reaches 1.22V an additional 4.5µA pull-up current is added to this pin.

DIFFOUT (Pin F8): Internal Remote Sense Amplifier Output. Connect this pin to V_{OUTS1} or V_{OUTS2} depending on which output is using remote sense. In parallel operation connect one of the V_{OUTS} pin to DIFFOUT for remote sensing.

SW1, SW2 (Pins G2, G11): Switching node of each channel that is used for testing purposes. Also an R-C snubber network can be applied to reduce or eliminate switch node ringing, or otherwise leave floating. See the Applications Information section.

PHASMD (Pin G4): Connect this pin to SGND, $INTV_{CC}$, or floating this pin to select the phase of CLKOUT to 60 degrees, 120 degrees, and 90 degrees respectively.

CLKOUT (Pin G5): Clock output with phase control using the PHASMD pin to enable multiphase operation between devices. See the Applications Information section.

PGOOD1, PGOOD2 (Pins G9, G8): Output Voltage Power Good Indicator. Open drain logic output that is pulled to ground when the output voltage is not within ±10% of the regulation point.

VINOVP (Pin H5): V_{IN} Overvoltage Protection (OVP) Comparator Input. Internally, this pin connects to SGND through a 60.4k resistor. If desired, apply resistor R_{VINOVP} from V_{IN} to VINOVP to set $V_{IN(OVP)}$, the V_{IN} overvoltage inception threshold. $V_{IN(OVP)}$ is given by Equation 1.

$$V_{IN(OVP)} = 1.22V \bullet \left(1 + \frac{R_{VINOVP}}{60.4k}\right) \quad (1)$$

See Figure 1 and the Applications Information section.

When VINOVP is detected (V_{VINOVP} > 1.22V), all power MOSFETs in both channels are turned off and remain off until the module is restarted. The module can be restarted by either cycling the RUN pins below their RUN thresholds or cycling the TRACK pins to SGND. Leave VINOVP open circuit or connect to SGND when this feature is not used.

$TEMP^-$ (Pin H6): Temperature Monitor, Negative Terminal. See $TEMP^+$.

$INTV_{CC}$ (Pin H8): Internal 5V Regulator Output. The control circuits and internal gate drivers are powered from this voltage. Decouple this pin to PGND with a 4.7µF low ESR tantalum or ceramic. $INTV_{CC}$ is activated when either RUN1 or RUN2 is activated.

$TEMP^+$ (Pin J6): Temperature Monitor, Positive Terminal. An internal diode-configured PNP transistor connected between $TEMP^+$ and $TEMP^-$ pins. See the Applications Information section.

$EXTV_{CC}$ (Pin J7): External power input that is enabled through a switch to $INTV_{CC}$ whenever $EXTV_{CC}$ is greater than 4.7V. Do not exceed 6V on this input, and connect this pin to V_{IN} when operating V_{IN} on 5V. An efficiency increase will occur, corresponding to a power loss reduction of (V_{IN} – $INTV_{CC}$) multiplied by power MOSFET driver current. Typical current requirement is 30mA. V_{IN} must be applied before $EXTV_{CC}$, and $EXTV_{CC}$ must be removed before V_{IN}.

V_{IN} (Pins M2–M11, L2–L11, J2–J4, J9–J11, K2–K4, K9–K11): Power Input Pins. Apply input voltage between these pins and GND pins. Recommend placing input decoupling capacitance directly between V_{IN} pins and GND pins.

Heat Sink (Top Exposed Metal): The top exposed metal is electrically unconnected.

SIMPLIFIED BLOCK DIAGRAM

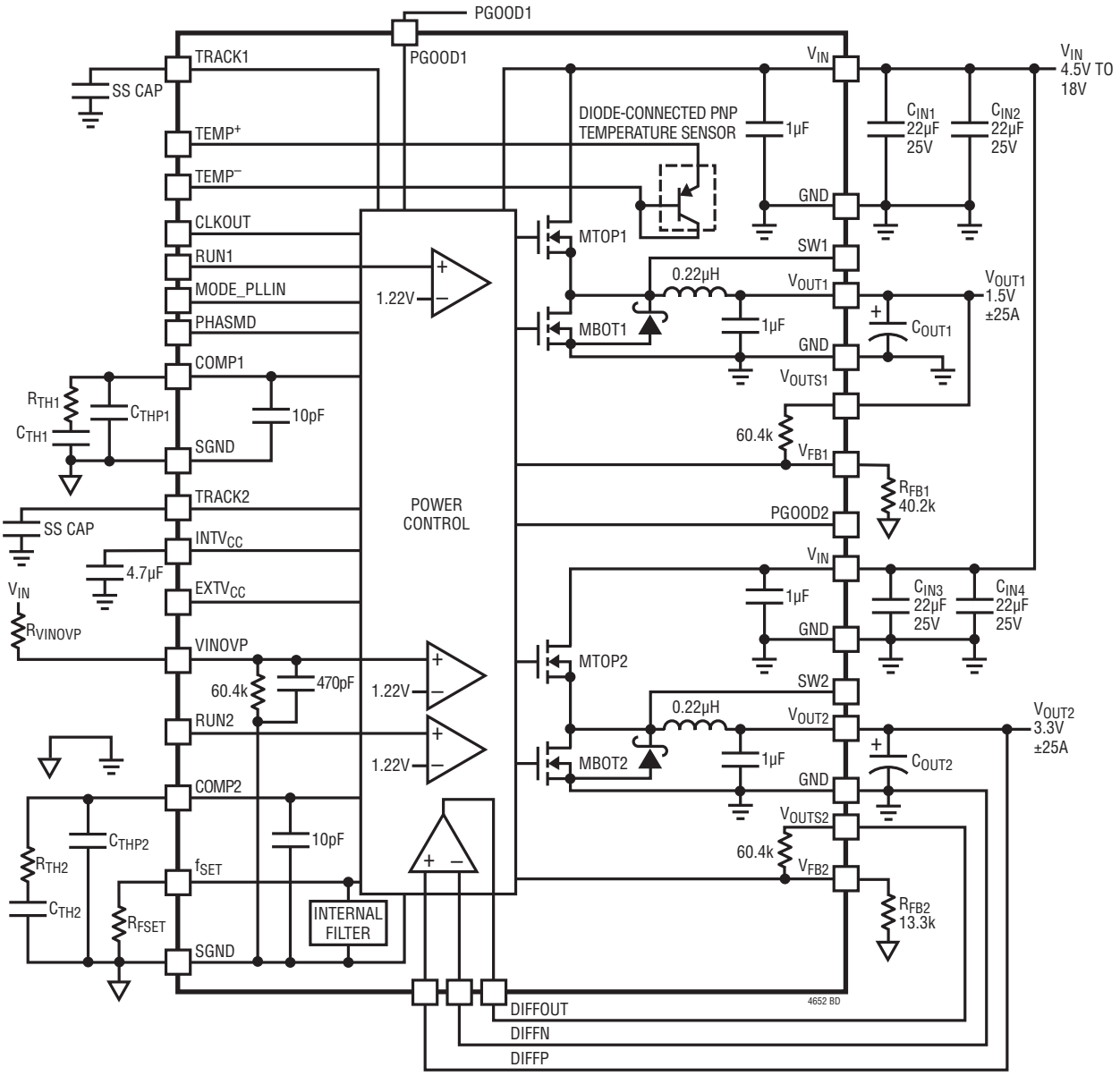


Figure 1. Simplified LTM4652 Block Diagram

DECOUPLING REQUIREMENTS

T_A = 25°C. Use Figure 1 configuration.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
	External Input Capacitor Requirement					
C_{IN1}, C_{IN2}	(V_{IN1} = 4.5V to 18V, V_{OUT1} = 1.2V)	I_{OUT1} = ±25A	22	66		µF
C_{IN3}, C_{IN4}	(V_{IN2} = 4.5V to 18V, V_{OUT2} = 3.3V)	I_{OUT2} = ±25A	22	66		µF
	External Output Capacitor Requirement					
C_{OUT1}	(V_{IN1} = 4.5V to 18V, V_{OUT1} = 1.2V)	I_{OUT1} = ±25A	300	600		µF
C_{OUT2}	(V_{IN2} = 4.5V to 18V, V_{OUT2} = 3.3V)	I_{OUT2} = ±25A	300	600		µF

OPERATION

Power Module Description

The LTM4652 is a bidirectional dual-output standalone nonisolated switching mode DC/DC power supply with ±1.5% total DC output error over line, load and temperature variation. It can provide two ±25A outputs or single ±50A output with few external input and output capacitors and setup components. This module provides precisely regulated output voltages programmable via external resistors from 0.6VDC to 7.5VDC over 4.5V to 18V input voltages. The typical application schematic is shown in Figure 31.

The LTM4652 has dual integrated constant-frequency current mode regulators and built-in power MOSFET devices with fast switching speed. The typical switching frequency is 300kHz* to 780kHz depending on different input and output conditions. For switching-noise sensitive applications, it can be externally synchronized from 300kHz* to 780kHz. A resistor can be used to program a free run frequency on the f_{SET} pin. See the Applications Information section.

With current mode control, multiple LTM4652s can be easily paralleled to provide up to ±300A current with excellent current sharing. Also, with current mode control, the LTM4652 module is able to achieve sufficient stability margins and a very fast ±3% output transient response with a minimum number of output capacitors, even with all ceramic output capacitors. This makes LTM4652 the best candidate when powering FPGAs, ASICs and processors in terms of DC accuracy, AC transient response, high output current and accuracy current sharing. See Applications Information section.

Current mode control provides cycle-by-cycle fast current limit and foldback current limit in an overcurrent condition. Internal overvoltage and undervoltage comparators pull the open-drain PGOOD outputs low if the output feedback voltage exits a ±10% window around the regulation point. As the output voltage exceeds 10% above regulation, the bottom MOSFET will turn on to clamp the output voltage. The top MOSFET will be turned off. This overvoltage protection is feedback voltage referred.

If desired, latch-off input overvoltage protection can be implemented by connecting an appropriate resistor, R_{VINOVP}, from V_{IN} to VINOVP. When the VINOVP pin exceeds 1.22V, switching action ceases, i.e., both the top MOSFET and bottom MOSFET are latched off. The module can be restarted by cycling the RUN pins below their RUN thresholds, or by cycling the TRACK pins to SGND or by cycling V_{IN} altogether.

Pulling the RUN pins below 1.1V forces the regulators into a shutdown state, by turning off both MOSFETs. The TRACK pins are used for programming the output voltage ramp and voltage tracking during start-up or used for soft-starting the regulator. See the Applications Information section.

The LTM4652 has a built-in 10pF high frequency filter cap from COMP to SGND for each channel. An external RC filtering circuit is required to achieve fast Type II control loop compensation. Table 6 provides a guide line for input, output capacitances and R-C values on COMP pin for several operating conditions. The Analog Devices µModule Power Design Tool (LTpowerCAD®) provides for transient and stability analysis. The V_{FB} pin is used to program the output voltage with a single external resistor to ground. A differential remote sense amplifier is available for sensing the output voltage accurately on one of the outputs at the load point, or in parallel operation sensing the output voltage at the load point.

High efficiency at light loads can be accomplished with selectable pulse-skipping operation using the MODE_PLLIN pin. This light load feature will accommodate battery operation. Efficiency graphs are provided for light load operation in the Typical Performance Characteristics section. See the Applications Information section for details.

A general purpose diode-configured PNP temperature sensor is included inside the module to monitor the temperature of the module. See the Applications Information section for details.

The switch pins, SW1 and SW2, are available for functional operation monitoring and a resistor-capacitor snubber circuit can be careful placed on the switch pin to ground to dampen any high frequency ringing on the transition edges. See the Applications Information section for details.

*Note that synchronization below 400kHz is not tested in ATE.

APPLICATIONS INFORMATION

The typical LTM4652 application circuit is shown in Figure 31. External component selection is primarily determined by the maximum load current and output voltage. Refer to Table 6 for specific external capacitor requirements for a 25% or a 50% load step application.

Output Total DC Accuracy and AC Transient Performance

In modern ASIC and FPGA power supply designs, a tight total voltage regulation window, ±3% for example, is required of the supply powering the core and periphery. To meet this requirement, the supply's DC voltage variance plus any AC voltage variation which may occur during any load step transient must fall within this allowed window. The DC voltage variance is determined by the accuracies of the supply's reference voltage, resistor divider, load regulation and line regulation over the operating temperature range. The AC voltage variance is determined by the supply's output voltage overshoot and undershoots in response to a load transient condition for a given output capacitor network.

Figure 2 shows a typical load step transient response waveform together with DC voltage accuracy variance. For a given allowable voltage regulation window, a tighter DC voltage accuracy allows more margin for the AC variation due to a load transient response. This increased margin for AC variation allows for a reduction in the total output capacitance required to meet the regulation window requirement. This allows for a reduced total solution cost and footprint area.

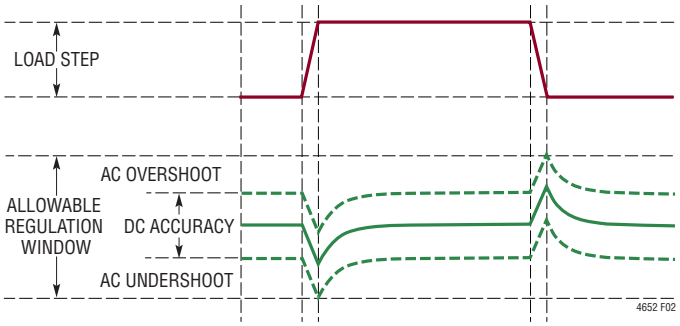


Figure 2. Typical Load Step Transient Response with DC Voltage Accuracy Variance

For example, in an FPGA core voltage application, for a 12V input, 1.0V output at 100A design, a total overall ±3% total voltage regulation window is required in responding to a 25% load step transient. Figure 3 illustrates the benefit of overall output capacitor reduction versus improved total DC accuracy by using 100µF ceramic output capacitors.

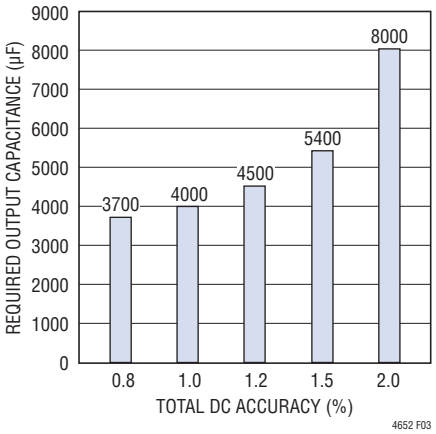


Figure 3. Overall Output Capacitor vs Total DC Accuracy

V_{IN} to V_{OUT} Step-Down Ratios

There are restrictions in the maximum V_{IN} and V_{OUT} step-down ratio that can be achieved for a given input voltage. Each output of the LTM4652 is capable of 98% duty cycle, but the V_{IN} to V_{OUT} minimum dropout is still shown as a function of its load current and will limit output current capability related to high duty cycle on the top side switch. Minimum on-time $t_{ON(MIN)}$ is another consideration in operating at a specified duty cycle while operating at a certain frequency due to the fact that $t_{ON(MIN)} < D/f_{SW}$, where D is duty cycle and f_{SW} is the switching frequency. $t_{ON(MIN)}$ is specified in the electrical parameters as 90ns.

Output Voltage Programming

The PWM controller has an internal 0.6V reference voltage. As shown in the Figure 1 (Simplified Block Diagram), a 60.4k internal feedback resistor connects between the V_{OUTS1} to V_{FB1} and V_{OUTS2} to V_{FB2}. It is very important that these pins be connected to their respective outputs for proper feedback regulation. Overvoltage can occur if these V_{OUTS1} and V_{OUTS2} pins are left floating when used as individual regulators, or at least one of them is used

APPLICATIONS INFORMATION

in paralleled regulators. The output voltage will default to 0.6V with no feedback resistor on either V_{FB1} or V_{FB2}. Adding a resistor R_{FB} from V_{FB} pin to GND programs the output voltage given by Equation 2. (See Table 1.)

$$V_{OUT} = 0.6V \bullet \frac{60.4k + R_{FB}}{R_{FB}} \quad (2)$$

Table 1. V_{FB} Resistor Table vs Various Output Voltages

V_{OUT}	0.6V	1.0V	1.2V	1.5V	1.8V	2.5V	3.3V	5V
R_{FB}	Open	90.9k	60.4k	40.2k	30.2k	19.1k	13.3k	8.25k

For parallel operation of multiple channels the same feedback setting resistor can be used for the parallel design. This is done by connecting the V_{OUTS1} to the output as shown in Figure 4, thus tying one of the internal 60.4k resistors to the output. All of the V_{FB} pins tie together with one programming resistor as shown in Figure 4.

In parallel operation, the V_{FB} pins have an I_{FB} current of 30nA per channel, maximum. To reduce output voltage error due to this current, an additional V_{OUTS} pin can be tied to V_{OUT}, and an additional R_{FB} resistor can be used to lower the total Thevenin equivalent resistance seen by this current. For example in Figure 4, the total Thevenin equivalent resistance of the V_{FB} pin is (60.4k//R_{FB}), which is 30.2k where R_{FB} is equal to 60.4k for a 1.2V output. Four phases connected in parallel equates to a worse case feedback current of 4 • I_{FB} = 120nA maximum. The voltage error is 120nA • 30.2k = 3.6mV. If V_{OUTS2} is connected, as shown in Figure 4, to V_{OUT}, and another 60.4k resistor is connected from V_{FB2} to ground, then the voltage error is reduced to 1.8mV. If the voltage error is acceptable then no additional connections are necessary. The onboard 60.4k resistor is 0.5% accurate and the V_{FB} resistor can be chosen by the user to be as accurate as needed. All COMP pins are tied together for current sharing between the phases. The TRACK pins can be tied together and a single soft-start capacitor can be used to soft-start the regulator. Equation 6 in the Soft-Start And Output Voltage Tracking section will need to have the soft-start current parameter increased by the number of paralleled channels.

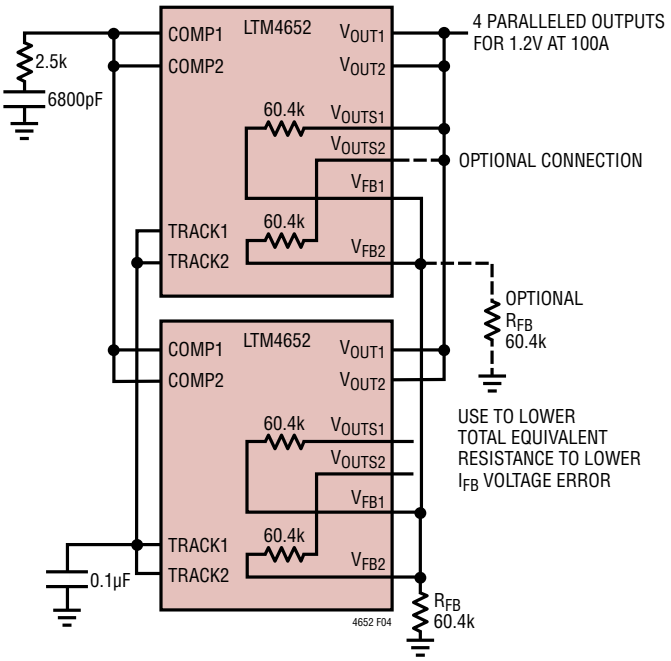


Figure 4. 4-Phase Parallel Configurations

Input Capacitors

The LTM4652 module should be connected to a low AC-impedance DC source. For each channel input, two 22µF input ceramic capacitors are used for RMS ripple current. A 47µF to 100µF surface mount aluminum electrolytic bulk capacitor can be used for more input bulk capacitance. This bulk input capacitor is only needed if the input source impedance is compromised by long inductive leads, traces or not enough source capacitance. If low impedance power planes are used, then this bulk capacitor is not needed.

For a buck converter, the switching duty-cycle can be estimated using Equation 3.

$$D = \frac{V_{OUT}}{V_{IN}} \quad (3)$$

Without considering the inductor current ripple, for each output, the RMS current of the input capacitor can be estimated using Equation 4.

$$I_{CIN(RMS)} = \frac{I_{OUT(MAX)}}{\eta\%} \bullet \sqrt{D \bullet (1-D)} \quad (4)$$

APPLICATIONS INFORMATION

In Equation 4, η% is the estimated efficiency of the power module. The bulk capacitor can be a switcher-rated electrolytic aluminum capacitor, Polymer capacitor.

Output Capacitors

The LTM4652 is designed for low output voltage ripple noise and good transient response. The bulk output capacitors defined as C_{OUT} are chosen with low enough effective series resistance (ESR) to meet the output voltage ripple and transient requirements. C_{OUT} can be a low ESR tantalum capacitor, the low ESR polymer capacitor or ceramic capacitor. The typical output capacitance range for each output is from 300µF to 800µF per output channel. Additional output filtering may be required by the system designer, if further reduction of output ripples or dynamic transient spikes is required. Table 6 shows a matrix of different output voltages and output capacitors to minimize the voltage droop and overshoot during a 25% load step. In multi LTM4652 paralleling applications, Table 6 RC compensation value is still valid in terms of having one set of RC filters on each of the paralleling modules while connecting all the COMP, FB and V_{OUT} pins together. See Figure 34 and Multiphase Operation section. The table optimizes total equivalent ESR and total bulk capacitance to optimize the transient performance. Stability criteria are considered in the Table 6 matrix, and the Analog Devices LTpowerCAD Design Tool provides for stability analysis. Multiphase operation will reduce effective output ripple as a function of the number of phases. Application Note 77 discusses this noise reduction versus output ripple current cancellation, but the output capacitance should be considered carefully as a function of stability and transient response. The Analog Devices µModule Power Design Tool can calculate the output ripple reduction as the number of implemented phases increases by N times. A small value 10Ω to 50Ω resistor can be placed in series from V_{OUT} to the V_{OUTS} pin to allow for a bode plot analyzer to inject a signal into the control loop and validate the regulator stability. The same resistor could be placed in series from V_{OUT} to DIFFP and a bode plot analyzer could inject a signal into the control loop and validate the regulator stability.

Pulse-Skipping Mode Operation

In applications where low output ripple and high efficiency at intermediate currents are desired, pulse-skipping mode should be used. Pulse-skipping operation allows the LTM4652 to skip cycles at low output loads, thus increasing efficiency by reducing switching loss. Tying the MODE_PLLIN pin to $INTV_{CC}$ enables pulse-skipping operation. At light loads the internal current comparator may remain tripped for several cycles and force the top MOSFET to stay off for several cycles, thus skipping cycles. The inductor current does not reverse in this mode.

Applications with transient and/or sustained negative (sinking) output current should operate the LTM4652 in forced continuous mode, since there is no way for the control loop to command reverse (negative) inductor current in pulse-skipping operation except by deliberately allowing the output voltage to rise high enough (~10% above nominal regulation) to activate an output overvoltage response.

Forced Continuous Operation

In applications where fixed frequency operation is more critical than low current efficiency, and where the lowest output ripple is desired, forced continuous operation should be used. Forced continuous operation can be enabled by tying the MODE_PLLIN pin to SGND. In this mode, inductor current is allowed to reverse during low output loads, the COMP voltage is in control of the current comparator threshold throughout, and the top MOSFET always turns on with each oscillator pulse. During start-up, forced continuous mode is disabled and inductor current is prevented from reversing until the LTM4652's output voltage is in regulation. Either regulator can be configured for forced continuous mode.

Multiphase Operation

For output loads that demand more than ±25A of current, two outputs in LTM4652 or even multiple LTM4652s can be paralleled to run out of phase to provide more output current without increasing input and output voltage ripples. The MODE_PLLIN pin allows the LTM4652 to synchronize to an external clock (between 300kHz* and 780kHz) and the internal phase-locked-loop allows the LTM4652 to lock

*Note that synchronization below 400kHz is not tested in ATE.

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onto incoming clock phase as well. The CLKOUT signal can be connected to the MODE_PLLIN pin of the following stage to line up both the frequency and the phase of the entire system. Tying the PHASMD pin to $INTV_{CC}$, SGND, or (floating) generates a phase difference (between MODE_PLLIN and CLKOUT) of 120 degrees, 60 degrees, or 90 degrees respectively. A total of 12 phases can be cascaded to run simultaneously with respect to each other by programming the PHASMD pin of each LTM4652 channel to different levels. Figure 5 shows a 2-phase design, 4-phase design and a 6-phase design example for clock phasing with the PHASMD table.

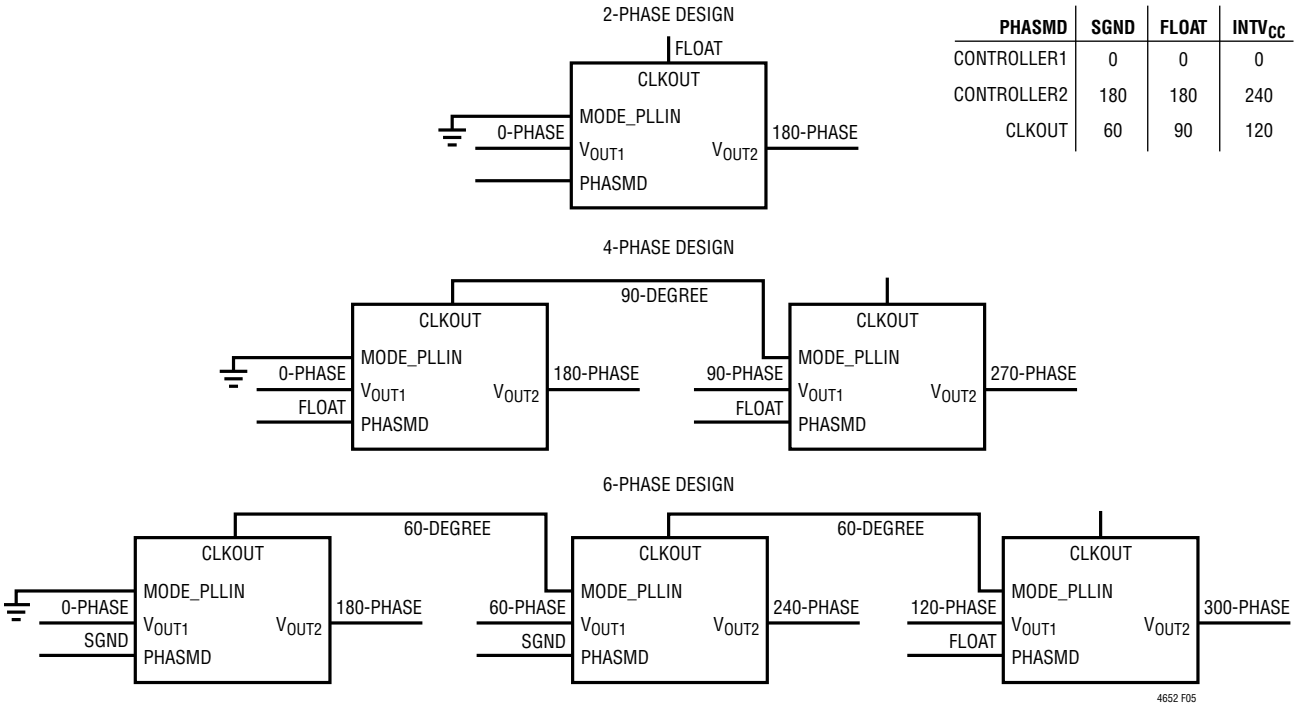
A multiphase power supply significantly reduces the amount of ripple current in both the input and output capacitors. The RMS input ripple current is reduced by, and the effective ripple frequency is multiplied by, the number of phases used (assuming that the input voltage is greater than the number of phases used times the output voltage). The output ripple amplitude is also reduced by the number of phases used when all of the outputs are tied together to achieve a single high output current design.

In multi LTM4652s parallel applications, C_{TH} and R_{TH} values in Table 6 are still valid to achieve transient response in a 25% load step. Connect one set of RC (R_{TH} and C_{TH}) network to the COMP pin of each paralleling module like a dual phase single output setup. Then connect the COMP pins, FB pins, TRACK pins and V_{OUT} pins from different modules together. See Figure 32, Figure 34 and Figure 35 for examples of parallel operation. LTpowerCAD Power Design Tool can also be used to optimize loop compensation and transient performance if only one set of RC (R_{TH} and C_{TH}) network is to be added to the common COMP pins.

The LTM4652 device is an inherently current mode controlled device, so parallel modules will have very good current sharing. This will balance the thermals on the design.

Input RMS Ripple Current Cancellation

Application Note 77 provides a detailed explanation of multiphase operation. The input RMS ripple current cancellation mathematical derivations are presented, and a graph is displayed representing the RMS ripple current reduction as a function of the number of interleaved phases. Figure 6 shows this graph.



PHASMD	SGND	FLOAT	$INTV_{CC}$
CONTROLLER1	0	0	0
CONTROLLER2	180	180	240
CLKOUT	60	90	120

Figure 5. Examples of 2-Phase, 4-Phase, and 6-Phase Operation with PHASMD Table

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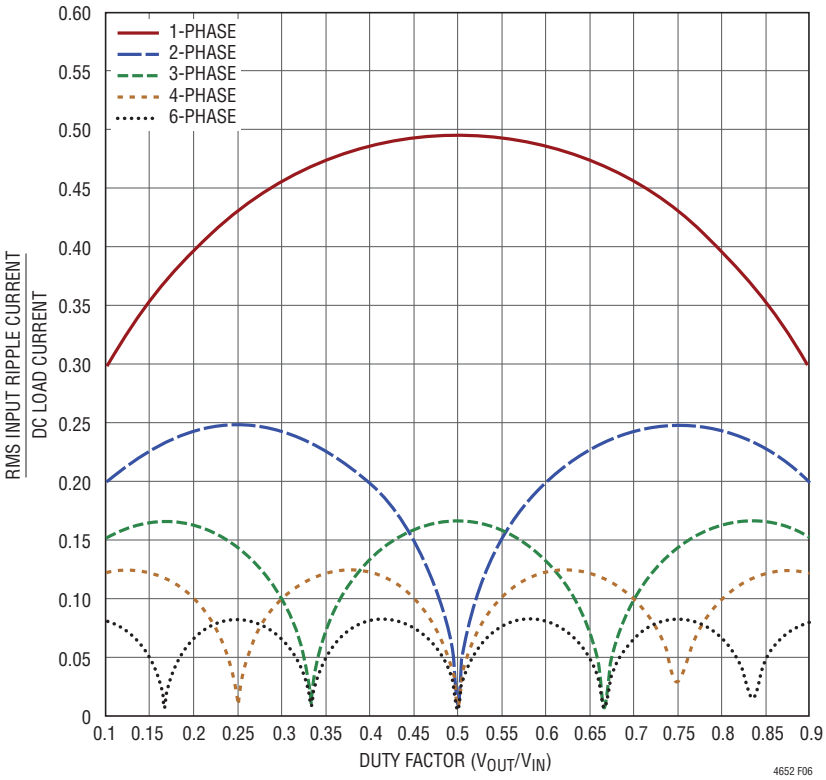

Figure 6. Input RMS Current Ratios to DC Load Current as a Function of Duty Cycle

Frequency Selection and Phase-Lock Loop (MODE_PLLIN and f_{SET} Pins)

The LTM4652 device is operated over a range of frequencies to improve power conversion efficiency. It is recommended to operate the module at 300kHz* to 780kHz over different input and output range for the best efficiency and inductor current ripple.

The LTM4652 switching frequency can be set with an external resistor from the f_{SET} pin to SGND. An accurate 9.5µA current source into the resistor will set a voltage that programs the frequency or a DC voltage can be applied. Figure 7 shows a graph of frequency setting verses programming voltage. An external clock can be applied to the MODE_PLLIN pin from 0V to $INTV_{CC}$ over a frequency range of 300kHz* to 780kHz. The clock input

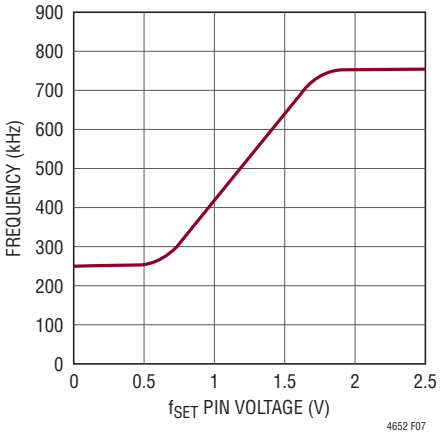

Figure 7. Operating Frequency vs f_{SET} Pin Voltage

*Note that synchronization below 400kHz is not tested in ATE.

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high threshold is 1.6V and the clock input low threshold is 1V. The LTM4652 has the PLL loop filter components on board. The frequency setting resistor should always be present to set the initial switching frequency before locking to an external clock. Both regulators will operate in forced continuous mode while being externally clocked.

The output of the PLL phase detector has a pair of complementary current sources that charge and discharge the internal filter network. When the external clock is applied then the f_{SET} frequency resistor is disconnected with an internal switch, and the current sources control the frequency adjustment to lock to the incoming external clock. When no external clock is applied, then the internal switch is on, thus connecting the external f_{SET} frequency set resistor for free run operation.

Minimum On-Time

Minimum on-time t_{ON} is the smallest time duration that the LTM4652 is capable of turning on the top MOSFET on either channel. It is determined by internal timing delays, and the gate charge required turning on the top MOSFET. Low duty cycle applications may approach this minimum on-time limit and care should be taken to ensure Equation 5.

$$\frac{V_{OUT}}{V_{IN} \bullet FREQ} > t_{ON(MIN)} \quad (5)$$

If the duty cycle falls below what can be accommodated by the minimum on-time, the controller will begin to skip cycles. The output voltage will continue to be regulated, but the output ripple and current will increase. The on-time can be increased by lowering the switching frequency. A good rule of thumb is to keep on-time longer than 110ns.

Soft-Start And Output Voltage Tracking

The TRACK pin provides a means to either soft-start the regulator or track it to a different power supply. A capacitor on the TRACK pin will program the ramp rate of the output voltage. An internal 1.25µA current source will charge up the external soft-start capacitor towards $INTV_{CC}$ voltage. When the TRACK voltage is below 0.6V, it will take over the internal 0.6V reference voltage to control the output voltage. The total soft-start time can be calculated using Equation 6.

$$t_{SS} = 0.6V \bullet \frac{C_{SS}}{1.25\mu A} \quad (6)$$

where C_{SS} is the capacitance on the TRACK pin. Current foldback and forced continuous mode are disabled during the soft-start process.

Output voltage tracking can also be programmed externally using the TRACK pin. The output can be tracked up and down with another regulator. Figure 8 shows an example waveform where the subordinate regulator's output slew rate is proportional to the main's.

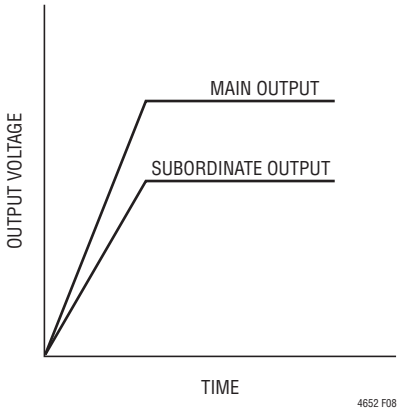

Figure 8. Output Ratiometric Tracking Waveform

Since the subordinate regulator's TRACK is connected to the main's output through a $R_{TR(TOP)}/R_{TR(BOT)}$ resistor divider and its voltage used to regulate the subordinate output voltage when TRACK voltage is below 0.6V, the subordinate output voltage and the main output voltage should satisfy Equation 7 during start-up:

$$V_{OUT(SL)} \bullet \frac{R_{FB(SL)}}{R_{FB(SL)} + 60.4k} = V_{OUT(MA)} \bullet \frac{R_{TR(BOT)}}{R_{TR(TOP)} + R_{TR(BOT)}} \quad (7)$$

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The $R_{FB(SL)}$ is the feedback resistor and the $R_{TR(TOP)}$/$R_{TR(BOT)}$ is the resistor divider on the TRACK pin of the subordinate regulator, as shown in Figure 9.

Following Equation 7, the ratio of the main's output slew rate (MR) to the subordinate's output slew rate (SR) is determined by Equation 8.

$$\frac{MR}{SR} = \frac{\frac{R_{FB(SL)}}{R_{FB(SL)} + 60.4k}}{\frac{R_{TR(BOT)}}{R_{TR(TOP)} + R_{TR(BOT)}}} \quad (8)$$

For example, $V_{OUT(MA)}$=1.5V, MR = 1.5V/1ms and $V_{OUT(SL)}$ = 3.3V, SR = 3.3V/1ms. From Equation 8, we could solve that $R_{TR(TOP)}$ = 60.4k and $R_{TR(BOT)}$ = 40.2k are a good combination for the ratiometric tracking.

The TRACK pin will have the 1.25µA current source on when a resistive divider is used to implement tracking on the subordinate regulator. This will impose an offset on the TRACK pin input. Smaller value resistors with the same ratios as the resistor values calculated from the Equation 8 can be used. For example, where the 60.4k is used then a 6.04k can be used to reduce the TRACK pin offset to a negligible value.

Coincident output tracking can be recognized as a special ratiometric output tracking in which the main's output slew rate (MR) is the same as the subordinate's output slew rate (SR), waveform as shown in Figure 10.

From Equation 8, we could easily find that, in coincident tracking, the subordinate regulator's TRACK pin resistor divider is always the same as its feedback divider given by Equation 9.

$$\frac{R_{FB(SL)}}{R_{FB(SL)} + 60.4k} = \frac{R_{TR(BOT)}}{R_{TR(TOP)} + R_{TR(BOT)}} \quad (9)$$

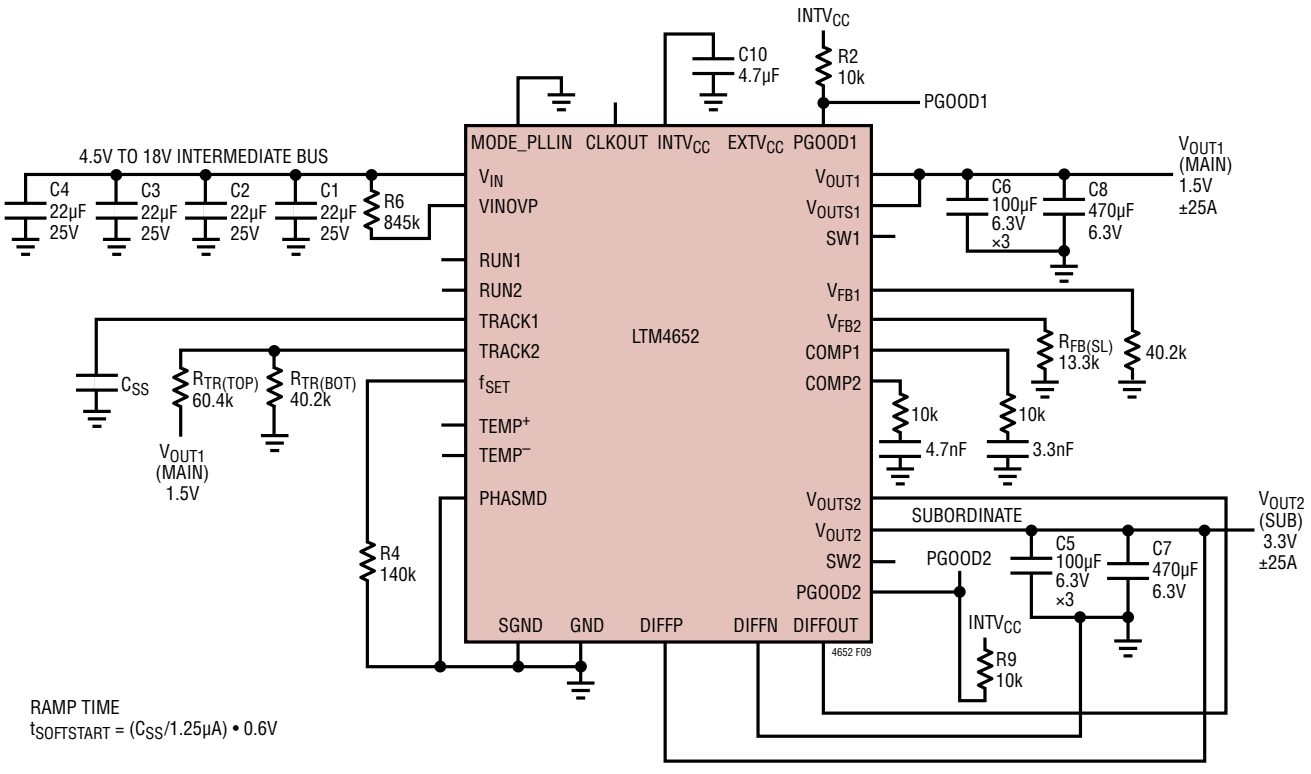

Figure 9. Example of Output Tracking Application Circuit

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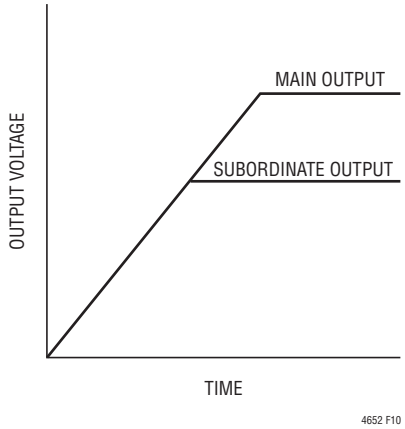

Figure 10. Output Coincident Tracking Waveform

For example, $R_{TR(TOP)}$ = 60.4k and $R_{TR(BOT)}$ = 13.3k is a good combination for coincident tracking for a $V_{OUT(MA)}$ = 1.5V and $V_{OUT(SL)}$ = 3.3V application.

Power Good

The PGOOD pins are open drain pins that can be used to monitor valid output voltage regulation. This pin monitors a 10% window around the regulation point. A resistor can be pulled up to a particular supply voltage no greater than 6V maximum for monitoring.

Stability Compensation

The LTM4652 has a built-in 10pF high frequency filter capacitor from COMP to SGND on each output channel. An external R-C filtering circuit is required to add from COMP to SGND to achieve fast Type II control loop compensation. Table 6 is provided for most application requirements. The Analog Devices µModule Power Design Tool (LTpowerCAD) provides for other control loop optimization.

Run Enable

The RUN pins have an enable threshold of 1.4V maximum, typically 1.22V with 135mV of hysteresis. They control the turn on of each of the channels and $INTV_{CC}$. These pins can be pulled up to V_{IN} for 5V operation, or a 5V Zener diode can be placed on the pins and a 10k to 100k resistor can be placed up to higher than 5V input for enabling the channels. There is 1µA pull-up current for each RUN pin. The LTM4652 will turn on with RUN floating. Please note RUN has a 6V Abs Max voltage rating. The RUN pins can also be used for output voltage sequencing. In parallel operation the RUN pins can be tied together and controlled from a single control. See the Typical Application circuits in Figure 31.

$INTV_{CC}$ and $EXTV_{CC}$

The LTM4652 module has an internal 5V low dropout regulator that is derived from the input voltage. This regulator is used to power the control circuitry and the power MOSFET drivers. This regulator can source up to 50mA, and typically uses ~30mA for powering the device at the maximum frequency. This internal 5V supply is enabled by either RUN1 or RUN2.

$EXTV_{CC}$ allows an external 5V supply to power the LTM4652 and reduce power dissipation from the internal low dropout 5V regulator. The power loss savings can be calculated using Equation 10.

$$(V_{IN} – 5V) • 30mA = PLOSS \quad (10)$$

$EXTV_{CC}$ has a threshold of 4.7V for activation, and a maximum rating of 6V. When using a 5V input, connect this 5V input to $EXTV_{CC}$ also to maintain a 5V gate drive level. $EXTV_{CC}$ must sequence on after V_{IN}, and $EXTV_{CC}$ must sequence off before V_{IN}.

Differential Remote Sense Amplifier

An accurate differential remote sense amplifier is provided to sense low output voltages accurately at the remote load points. This is especially true for high current loads. The amplifier can be used on one of the two channels, or on a single parallel output. It is very important that the DIFFP and DIFFN are connected properly at the output, and DIFFOUT is connected to either V_{OUTS1} or V_{OUTS2}. In parallel operation, the DIFFP and DIFFN are connected properly at the output, and DIFFOUT is connected to one of the V_{OUTS} pins. Review the parallel schematics in Figure 32 and Figure 34 and review Figure 4. Please note the differential amplifier can be used for ≤3.3V outputs.

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SW Pins

The SW pins are generally for testing purposes by monitoring these pins. These pins can also be used to dampen out switch node ringing caused by LC parasitic in the switched current paths. Usually a series R-C combination is used called a snubber circuit. The resistor will dampen the resonance and the capacitor is chosen to only affect the high frequency ringing across the resistor. If the stray inductance or capacitance can be measured or approximated then a somewhat analytical technique can be used to select the snubber values. The inductance is usually easier to predict. It combines the power path board inductance in combination with the MOSFET interconnect bond wire inductance.

First the SW pin can be monitored with a wide bandwidth scope with a high frequency scope probe. The ring frequency can be measured for its value. The impedance Z can be calculated using Equation 11.

$$Z_{(L)} = 2\pi fL, \quad (11)$$

where f is the resonant frequency of the ring, and L is the total parasitic inductance in the switch path. If a resistor is selected that is equal to Z, then the ringing should be dampened. The snubber capacitor value is chosen so that its impedance is equal to the resistor at the ring frequency. Calculated by: $Z_{(C)} = 1/(2\pi fC)$. These values are a good place to start with. Modification to these components should be made to attenuate the ringing with the least amount of power loss.

Temperature Monitoring

A diode connected PNP transistor is used for the TEMP+/TEMP– monitor function by monitoring its voltage over temperature. The temperature dependence of this diode voltage can be understood in Equation 12.

$$V_D = nV_T \ln\left(\frac{I_D}{I_S}\right) \quad (12)$$

where V_T is the thermal voltage (k_T/q), and n, the ideality factor, is 1 for the diode connected PNP transistor being used in the LTM4652. I_S is expressed by the typical empirical Equation 13.

$$I_S = I_0 \exp\left(\frac{-V_{G0}}{V_T}\right) \quad (13)$$

where I_0 is a process and geometry dependent current, (I_0 is typically around 20k orders of magnitude larger than I_S at room temperature) and V_{G0} is the band gap voltage of 1.2V extrapolated to absolute zero or –273°C.

If we take the I_S Equation 13 and substitute into the Equation 14, then we get:

$$V_D = V_{G0} - \left(\frac{kT}{q}\right)\ln\left(\frac{I_0}{I_D}\right),\ V_T = \frac{kT}{q} \quad (14)$$

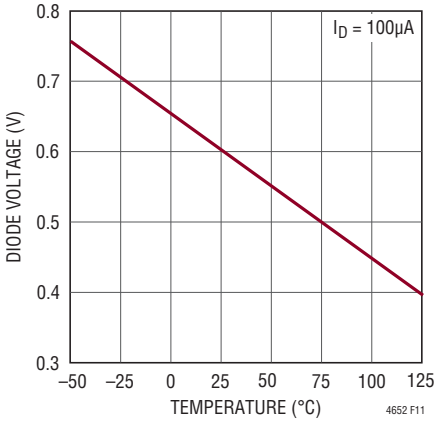

Figure 11. Diode Voltage V_D vs Temperature T(K) for Different Bias Currents

The expression shows that the diode voltage decreases (linearly if I_0 were constant) with increasing temperature and constant diode current. Figure 11 shows a plot of V_D vs Temperature over the operating temperature range of the LTM4652.

If we take Equation 14 and differentiate it with respect to temperature T, then Equation 15 gives:

$$\frac{dV_D}{dT} = -\frac{V_{G0} - V_D}{T} \quad (15)$$

This dV_D/d_T term is the temperature coefficient equal to about –2mV/K or –2mV/°C. Equation 15 is simplified for the first order derivation.

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Solving for T, $T = -(V_{G0} - V_D)/(dV_D/d_T)$ provides the temperature.

1st Example: Figure 11 for 27°C, or 300K the diode voltage is 0.598V, thus, 300K = –(1200mV – 598mV)/–2.0mV/K).

2nd Example: Figure 11 for 75°C, or 350K the diode voltage is 0.50V, thus, 350K = –(1200mV – 500mV)/–2.0mV/K).

Converting the Kelvin scale to Celsius is simply taking the Kelvin temp and subtracting 273 from it.

A typical forward voltage is given in the electrical characteristics section of the data sheet, and Figure 11 is the plot of this forward voltage. Measure this forward voltage at 27°C to establish a reference point. Then using the above expression while measuring the forward voltage over temperature will provide a general temperature monitor. A bias current on the order of 100µA is appropriate for generating a typical forward voltage. If preferred, LTC2997 and similar temperature-monitoring ICs can be used, instead (see Figure 33).

Thermal Considerations and Output Current Derating

The thermal resistances reported in the Pin Configuration section of the data sheet are consistent with those parameters defined by JESD51-9 and are intended for use with finite element analysis (FEA) software modeling tools that leverage the outcome of thermal modeling, simulation, and correlation to hardware evaluation performed on a µModule package mounted to a hardware test board—also defined by JESD51-9 (Test Boards for Area Array Surface Mount Package Thermal Measurements). The motivation for providing these thermal coefficients is found in JESD51-12 (Guidelines for Reporting and Using Electronic Package Thermal Information).

Many designers may opt to use laboratory equipment and a test vehicle such as the demo board to anticipate the µModule regulator's thermal performance in their application at various electrical and environmental operating conditions to compliment any FEA activities. Without FEA software, the thermal resistances reported in the Pin Configuration section are in-and-of themselves not relevant to providing guidance of thermal performance; instead, the derating curves provided in the data sheet can be used in a manner that yields insight and guidance pertaining to one's application-usage, and can be adapted to correlate thermal performance to one's own application.

The Pin Configuration section typically gives three thermal coefficients explicitly defined in JESD51-12; these coefficients are quoted or paraphrased below:

1. θ_{JA}, the thermal resistance from junction to ambient, is the natural convection junction-to-ambient air thermal resistance measured in a one cubic foot sealed enclosure. This environment is sometimes referred to as "still air" although natural convection causes the air to move. This value is determined with the part mounted to a Demo Board.
2. θ_{JCbot}, the thermal resistance from junction to the bottom of the product case, is the junction-to-board thermal resistance with all of the component power dissipation flowing through the bottom of the package. In the typical µModule, the bulk of the heat flows out the bottom of the package, but there is always heat flow out into the ambient environment. As a result, this thermal resistance value may be useful for comparing packages but the test conditions don't generally match the user's application.
3. θ_{JCtop}, the thermal resistance from junction to top of the product case, is determined with nearly all of the component power dissipation flowing through the top of the package. As the electrical connections of the typical µModule are on the bottom of the package, it is rare for an application to operate such that most of the heat flows from the junction to the top of the part. As in the case of θ_{JCbot}, this value may be useful for comparing packages but the test conditions don't generally match the user's application.

A graphical representation of the aforementioned thermal resistances is given in Figure 12; blue resistances are contained within the µModule regulator, whereas green resistances are external to the µModule.

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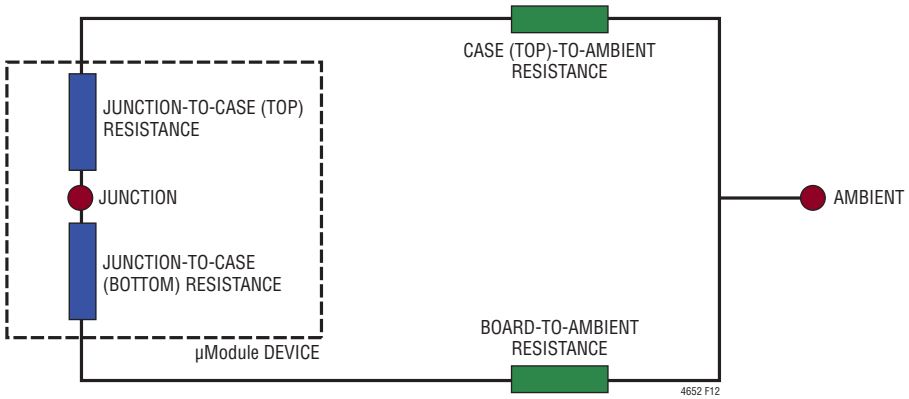

Figure 12. Graphical Representation of JESD51-12 Thermal Coefficients

As a practical matter, it should be clear to the reader that no individual or sub-group of the four thermal resistance parameters defined by JESD51-12 or provided in the Pin Configuration section replicates or conveys normal operating conditions of a µModule. For example, in normal board-mounted applications, never does 100% of the device's total power loss (heat) thermally conduct exclusively through the top or exclusively through bottom of the µModule—as the standard defines for θ_{JCtop} and θ_{JCbot}, respectively. In practice, power loss is thermally dissipated in both directions away from the package—granted, in the absence of a heat sink and airflow, a majority of the heat flow is into the board.

Within a SIP (system-in-package) module, be aware there are multiple power devices and components dissipating power, with a consequence that the thermal resistances relative to different junctions of components or die are not exactly linear with respect to total package power loss. To reconcile this complication without sacrificing modeling simplicity—but also, not ignoring practical realities—an approach has been taken using FEA software modeling along with laboratory testing in a controlled-environment chamber to reasonably define and correlate the thermal resistance values supplied in this data sheet: (1) Initially, FEA software is used to accurately build the mechanical geometry of the µModule and the specified PCB with all of the correct material coefficients along with accurate power loss source definitions; (2) this model simulates a software-defined JEDEC environment consistent with JESD51-9 to predict power loss heat flow and temperature readings at different interfaces that enable the calculation of the JEDEC-defined thermal resistance values; (3) the model and FEA software is used to evaluate the µModule with heat sink and airflow; (4) having solved for and analyzed these thermal resistance values and simulated various operating conditions in the software model, a thorough laboratory evaluation replicates the simulated conditions with thermocouples within a controlled-environment chamber while operating the device at the same power loss as that which was simulated. The outcome of this process and due diligence yields the set of derating curves provided in later sections of this data sheet, along with well-correlated JESD51-12-defined θ values provided in the Pin Configuration section of this data sheet. Each system has its own thermal characteristics, therefore thermal analysis must be performed by the user in a particular system.

The LTM4652 module has been designed to effectively remove heat from both the top and bottom of the package. The bottom substrate material has very low thermal resistance to the printed circuit board. An external heat sink can be applied to the top of the device for excellent heat sinking with airflow.

Figure 13 shows the thermal image of the LTM4652, without airflow, without heat sink, running paralleled from 12V to 1V at 50A with around 85.3% efficiency and 8.6W power loss. Figure 14 shows the thermal image of the LTM4652, with 200LFM airflow, without heat sink, running paralleled from 12V to 3.3V at 50A with around 92.2% efficiency and 14W power loss.

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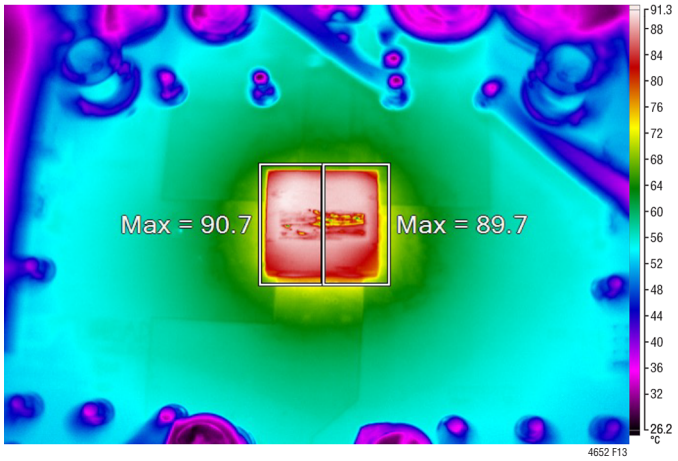

Figure 13. Thermal Image 12V to 1.0V, 50A with No Airflow without Heat Sink

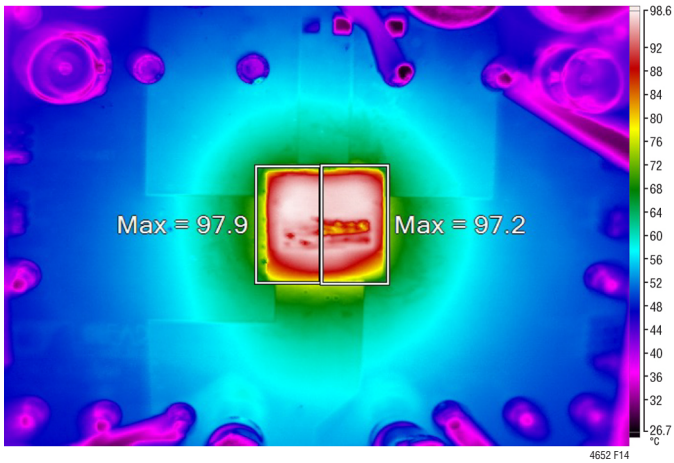

Figure 14. Thermal Image 12V to 3.3V, 50A with 200LFM Airflow without Heat Sink

Safety Considerations

The LTM4652 modules do not provide isolation from V_{IN} to V_{OUT}. There is no internal fuse. If required, a slow blow fuse with a rating twice the maximum input current needs to be provided to protect each unit from catastrophic failure. The device does support over current protection. A temperature diode is provided for monitoring internal temperature, and can be used to detect the need for thermal shutdown that can be done by controlling the RUN pin.

Power Derating

The 1.0V, 1.8V, 3.3V and 5V power loss curves in Figure 15 to Figure 17 can be used in coordination with the load current derating curves in Figure 18 to Figure 29 for calculating an approximate θ_{JA} thermal resistance for the LTM4652 with various heat sinking and airflow conditions. The power loss curves are taken at room temperature, and are increased with a 1.2 multiplicative factor at 125°C.

The derating curves are plotted with CH1 and CH2 in parallel single output operation starting at ±50A of load with low ambient temperature. The output voltages are 1V to 3.3V. These are chosen to include the lower and higher output voltage ranges for correlating the thermal resistance. Thermal models are derived from several temperature measurements in a controlled temperature chamber along with thermal modeling analysis.

The junction temperatures are monitored while ambient temperature is increased with and without airflow. The power loss increase with ambient temperature change is factored into the derating curves. The junctions are maintained at ~120°C maximum while lowering output current or power while increasing ambient temperature. The decreased output current will decrease the internal module loss as ambient temperature is increased.

The monitored junction temperature of 120°C minus the ambient operating temperature specifies how much module temperature rise can be allowed. As an example in Figure 26, the load current is derated to ~36A at ~50°C with no air or heat sink and the power loss for the 12V to 3.3V at 36A output is a ~8.8W loss. The 8.8W loss is calculated with the ~8.4W room temperature loss from the 12V to 3.3V power loss curve at 36A, and applying a 1.05 multiplying factor at 50°C ambient (see Figure 17). If the 50°C ambient temperature is subtracted from the 120°C junction temperature, then the difference of 70°C divided by 8.8W yields a 7.95°C/W θ_{JA} thermal resistance. Table 2 specifies a 7.9°C/W value which is pretty close. The airflow graphs are more accurate due to the fact that the ambient temperature environment is controlled better with airflow. Table 2 to Table 4 provide equivalent thermal resistances for 1.0V to 3.3V outputs with and without airflow and heat sinking.

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Switching frequency set per Table 6.

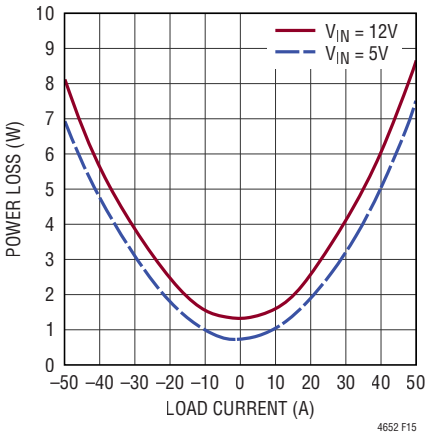


Figure 15. 1.0V_{OUT} Power Loss Curve

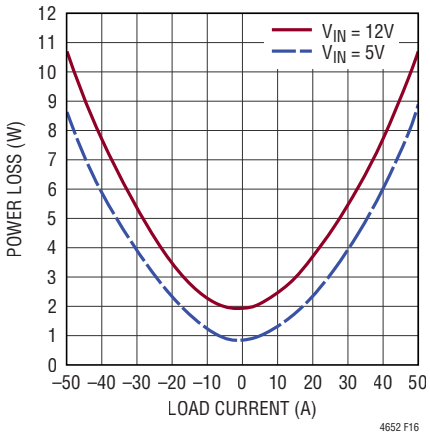


Figure 16. 1.8V_{OUT} Power Loss Curve

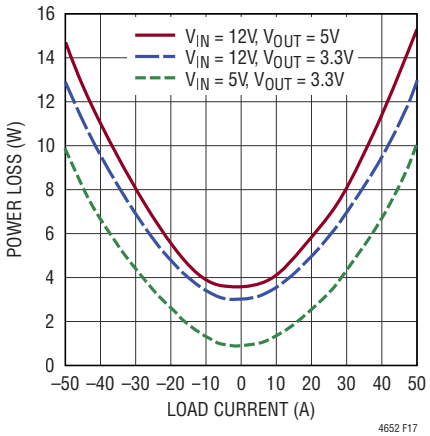


Figure 17. 3.3V_{OUT} and 5V_{OUT} Power Loss Curves

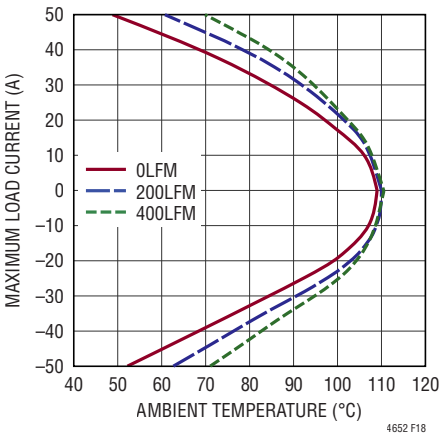


Figure 18. 12V to 1V Derating Curve, No Heat Sink

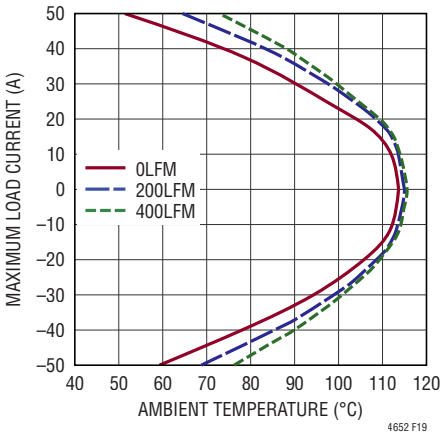


Figure 19. 5V to 1V Derating Curve, No Heat Sink

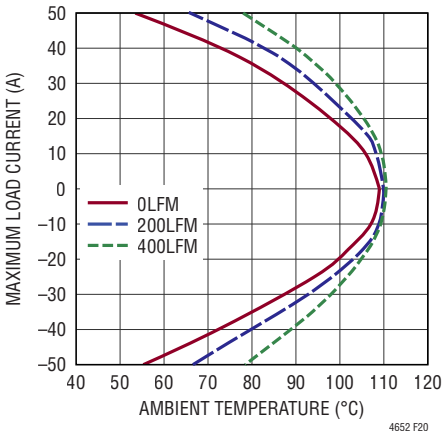


Figure 20. 12V to 1V Derating Curve, BGA Heat Sink

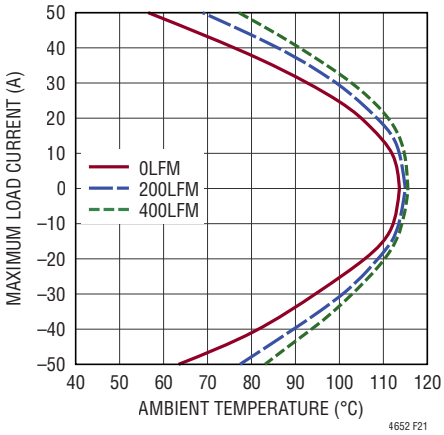


Figure 21. 5V to 1V Derating Curve, BGA Heat Sink

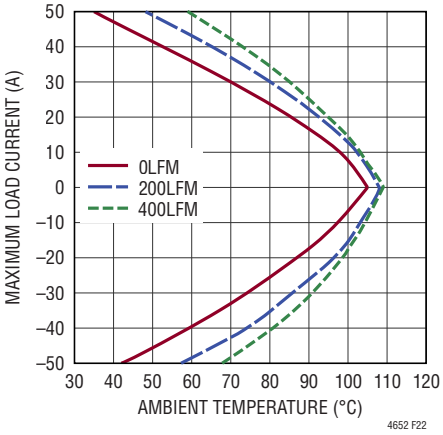


Figure 22. 12V to 1.8V Derating Curve, No Heat Sink

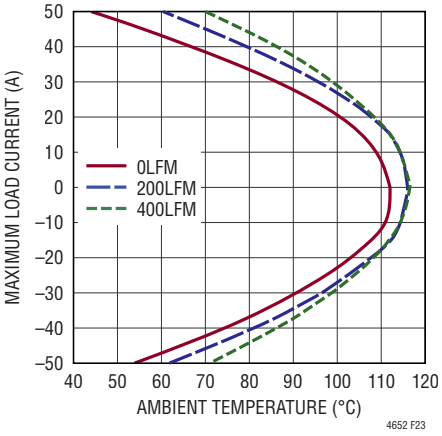


Figure 23. 5V to 1.8V Derating Curve, No Heat Sink

APPLICATIONS INFORMATION

Switching frequency set per Table 6.

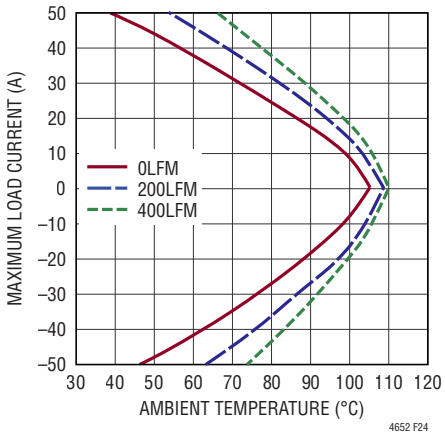


Figure 24. 12V to 1.8V Derating Curve, BGA Heat Sink

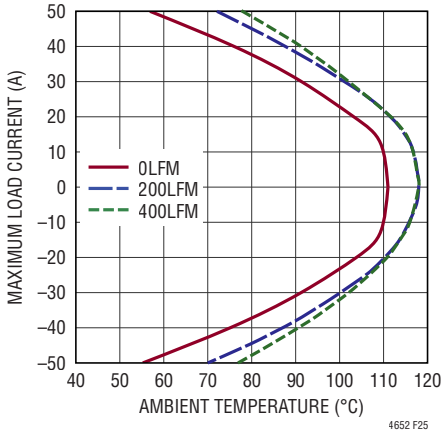


Figure 25. 5V to 1.8V Derating Curve, BGA Heat Sink

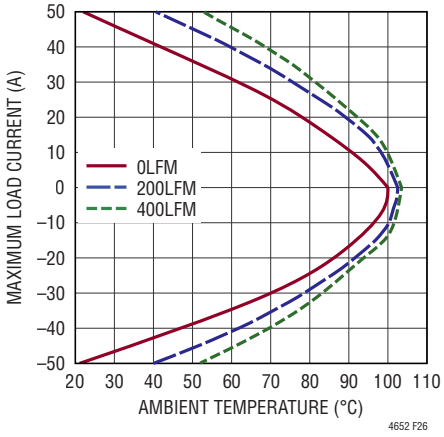


Figure 26. 12V to 3.3V Derating Curve, No Heat Sink

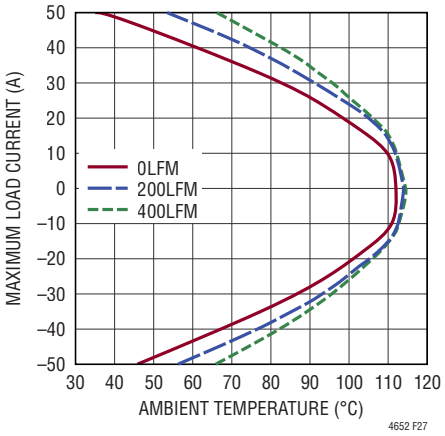


Figure 27. 5V to 3.3V Derating Curve, No Heat Sink

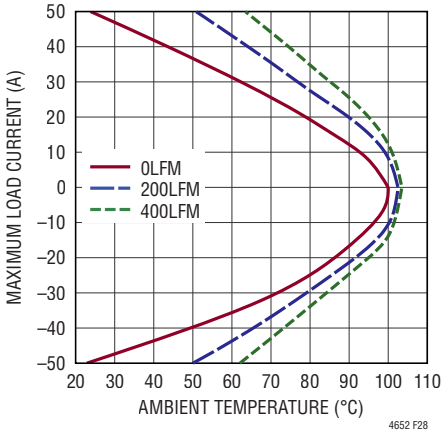


Figure 28. 12V to 3.3V Derating Curve, BGA Heat Sink

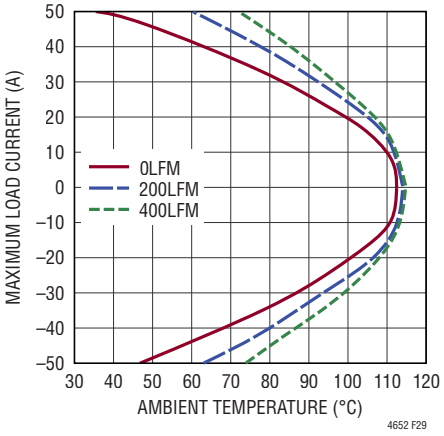


Figure 29. 5V to 3.3V Derating Curve, BGA Heat Sink

APPLICATIONS INFORMATION

The derived thermal resistances in Table 2 to Table 4 for the various conditions can be multiplied by the calculated power loss as a function of ambient temperature to derive temperature rise above ambient, thus maximum junction temperature. Room temperature power loss can be derived from the efficiency curves and adjusted with the above ambient temperature multiplicative factors. The printed circuit board is a 1.6mm thick four layer board with two ounce copper for all four layers. The PCB dimensions are 101mm × 114mm. The BGA heat sinks are listed in Table 5.

Layout Checklist/Example

The high integration of LTM4652 makes the PCB board layout very simple and easy. However, to optimize its electrical and thermal performance, some layout considerations are still necessary.

- Use large PCB copper areas for high current paths, including V_{IN}, GND, V_{OUT1} and V_{OUT2}. It helps to minimize the PCB conduction loss and thermal stress.
- Place high frequency ceramic input and output capacitors next to the V_{IN}, PGND and V_{OUT} pins to minimize high frequency noise.
- Place a dedicated power ground layer underneath the unit.
- To minimize the via conduction loss and reduce module thermal stress, use multiple vias for interconnection between top layer and other power layers.
- Do not put via directly on the pad, unless they are capped or plated over.
- Use a separated SGND ground copper area for components connected to signal pins. Connect the SGND to GND underneath the unit.
- For parallel modules, tie the V_{OUT}, V_{FB}, and COMP pins together. Use an internal layer to closely connect these pins together. The TRACK pin can be tied a common capacitor for regulator soft-start.
- Bring out test points on the signal pins for monitoring.

Figure 30 gives a good example of the recommended layout.

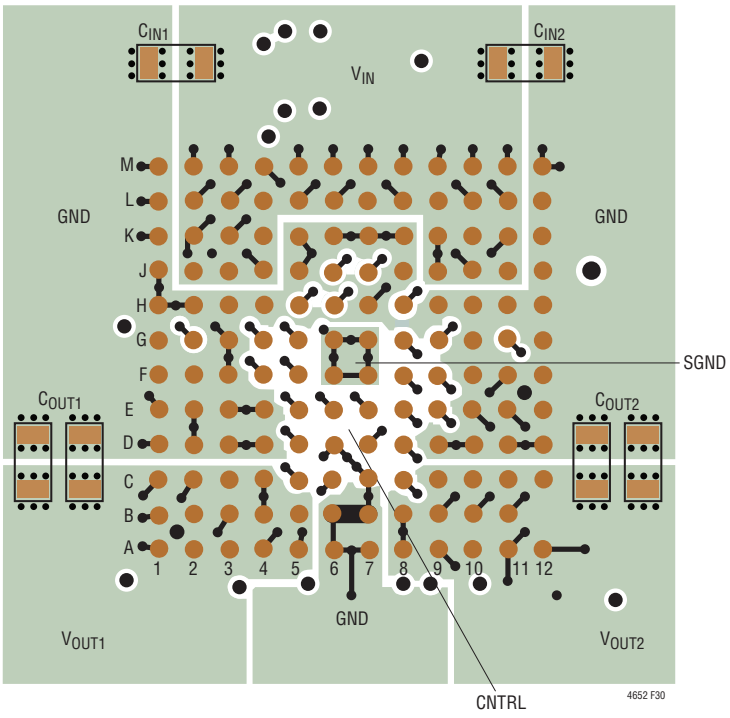


Figure 30. Recommended PCB Layout

APPLICATIONS INFORMATION

Table 2. 1.0V Output

DERATING CURVE	V_{IN} (V)	POWER LOSS CURVE	AIRFLOW (LFM)	HEAT SINK	θ_{JA} (°C/W)
Figure 18, Figure 19	5, 12	Figure 15	0	None	8.0
Figure 18, Figure 19	5, 12	Figure 15	200	None	6.6
Figure 18, Figure 19	5, 12	Figure 15	400	None	5.6
Figure 20, Figure 21	5, 12	Figure 15	0	BGA Heat Sink	7.6
Figure 20, Figure 21	5, 12	Figure 15	200	BGA Heat Sink	5.9
Figure 20, Figure 21	5, 12	Figure 15	400	BGA Heat Sink	5.0

Table 3. 1.8V Output

DERATING CURVE	V_{IN} (V)	POWER LOSS CURVE	AIRFLOW (LFM)	HEAT SINK	θ_{JA} (°C/W)
Figure 22, Figure 23	5, 12	Figure 16	0	None	8.0
Figure 22, Figure 23	5, 12	Figure 16	200	None	6.3
Figure 22, Figure 23	5, 12	Figure 16	400	None	5.3
Figure 24, Figure 25	5, 12	Figure 16	0	BGA Heat Sink	7.6
Figure 24, Figure 25	5, 12	Figure 16	200	BGA Heat Sink	5.5
Figure 24, Figure 25	5, 12	Figure 16	400	BGA Heat Sink	4.6

Table 4. 3.3V Output

DERATING CURVE	V_{IN} (V)	POWER LOSS CURVE	AIRFLOW (LFM)	HEAT SINK	θ_{JA} (°C/W)
Figure 26, Figure 27	5, 12	Figure 17	0	None	7.9
Figure 26, Figure 27	5, 12	Figure 17	200	None	6.0
Figure 26, Figure 27	5, 12	Figure 17	400	None	5.1
Figure 28, Figure 29	5, 12	Figure 17	0	BGA Heat Sink	7.6
Figure 28, Figure 29	5, 12	Figure 17	200	BGA Heat Sink	5.4
Figure 28, Figure 29	5, 12	Figure 17	400	BGA Heat Sink	4.2

Table 5. Heat Sink and Thermally Conductive Adhesive Tape Part Numbers

MANUFACTURER	DEVICE	PART NUMBER	WEBSITE
Boyd Corp.	Heat Sink	375424B00034G	www.boydcorp.com
Chomerics	Tape	T411	www.chomerics.com

APPLICATIONS INFORMATION

Table 6. Output Voltage Response vs Component Matrix (Refer to Figure 31) Load Step Typical Measured Values (2-Phase Single Output Solution)

C_{IN} (CERAMIC)			C_{OUT} (CERAMIC)			C_{OUT} (BULK)		
VENDOR	VALUE	PART NUMBER	VENDOR	VALUE	PART NUMBER	VENDOR	VALUE	PART NUMBER
Murata	22µF, 16V, X5R, 1210	GRM32ER61C226KE20L	Murata	100µF, 6.3V, X5R, 1210	GRM32ER60J107ME20L	Panasonic	470µF, 2.5V, 3mΩ	EEFGX0E4TIR
Murata	22µF, 16V, X5R, 1206	GRM31CR61C226KE15K	Murata	220µF, 4V, X5R, 1206	GRM31CR60G227M	Panasonic	470µF, 6.3V, 10mΩ	6TPF470MAH
TDK	22µF, 16V, X5R, 1210	C3225X5R1C226M250AA	Taiyo Yuden	100µF, 6.3V, X5R, 1210	JMK325BJ107MM-T			
			Taiyo Yuden	220µF, 4V, X5R, 1210	AMK325ABJ227MM-T			

25% Load Step (0A to 12.5A) Ceramic Output Capacitor Only Solutions

V_{IN} (V)	V_{OUT} (V)	C_{IN}** BULK (µF)	C_{IN} CERAMIC (µF)	C_{OUT} (BULK)	C_{OUT} CERAMIC (µF)	COMP PIN RESISTOR R_{TH} (kΩ)	COMP PIN CAPACITOR C_{TH} (pF)	COMP PIN PARALLELING CAPACITOR C_{THP} (pF)	FEED-FORWARD CAPACITOR C_{FF} (pF)	PEAK-PEAK DEVIATION (mV)	SETTLING TIME t_{SETTLE} (µs)	LOAD STEP (A)	LOAD STEP SLEW RATE (A/µs)	R_{FB} (kΩ)	FREQ (kHz)
12	1	150	22 ×4	None	220 ×8	3.32	6800	None	68	62	40	12.5	10	90.9	300
12	1.2	150	22 ×4	None	220 ×8	3.32	6800	None	68	51	40	12.5	10	60.4	400
12	1.5	150	22 ×4	None	220 ×8	3.32	6800	None	68	61	40	12.5	10	40.2	400
12	1.8	150	22 ×4	None	220 ×8	3.32	6800	None	68	58	40	12.5	10	30.2	500
12	2.5	150	22 ×4	None	220 ×8	3.32	6800	None	68	70	50	12.5	10	19.1	500
12	3.3	150	22 ×4	None	220 ×8	3.32	6800	None	68	70	60	12.5	10	13.3	600
12	5	Suggest to Use POSCAP + Ceramic Cap													

25% Load Step (0A to 12.5A) Bulk + Ceramic Output Capacitor Solutions

V_{IN} (V)	V_{OUT} (V)	C_{IN}** BULK (µF)	C_{IN} CERAMIC (µF)	C_{OUT} (BULK)	C_{OUT} CERAMIC (µF)	COMP PIN RESISTOR R_{TH} (kΩ)	COMP PIN CAPACITOR C_{TH} (pF)	COMP PIN PARALLELING CAPACITOR C_{THP} (pF)	FEED-FORWARD CAPACITOR C_{FF} (pF)	PEAK-PEAK DEVIATION (mV)	SETTLING TIME t_{SETTLE} (µs)	LOAD STEP (A)	LOAD STEP SLEW RATE (A/µs)	R_{FB} (kΩ)	FREQ (kHz)
12	1	150	22 ×4	470 ×2	100 ×4	4.64	4700	10	68	54	30	12.5	10	90.9	300
12	1.2	150	22 ×4	470 ×2	100 ×4	4.64	4700	10	68	50	30	12.5	10	60.4	400
12	1.5	150	22 ×4	470 ×2	100 ×4	4.64	4700	10	68	57	30	12.5	10	40.2	400
12	1.8	150	22 ×4	470 ×2	100 ×4	4.64	4700	10	68	57	40	12.5	10	30.2	500
12	2.5	150	22 ×4	470 ×2	100 ×4	4.64	4700	10	68	72	50	12.5	10	19.1	500
12	3.3	150	22 ×4	470 ×2	100 ×4	9.09	4700	10	None	89	60	12.5	10	13.3	600
12	5	150	22 ×4	470 ×2	100 ×4	9.09	4700	10	None	90	60	12.5	10	8.25	750

*Different Bulk C_{OUT1} used. See Part Number above.

**C_{IN} (BULK) may be required with long PCB traces.

TYPICAL APPLICATION

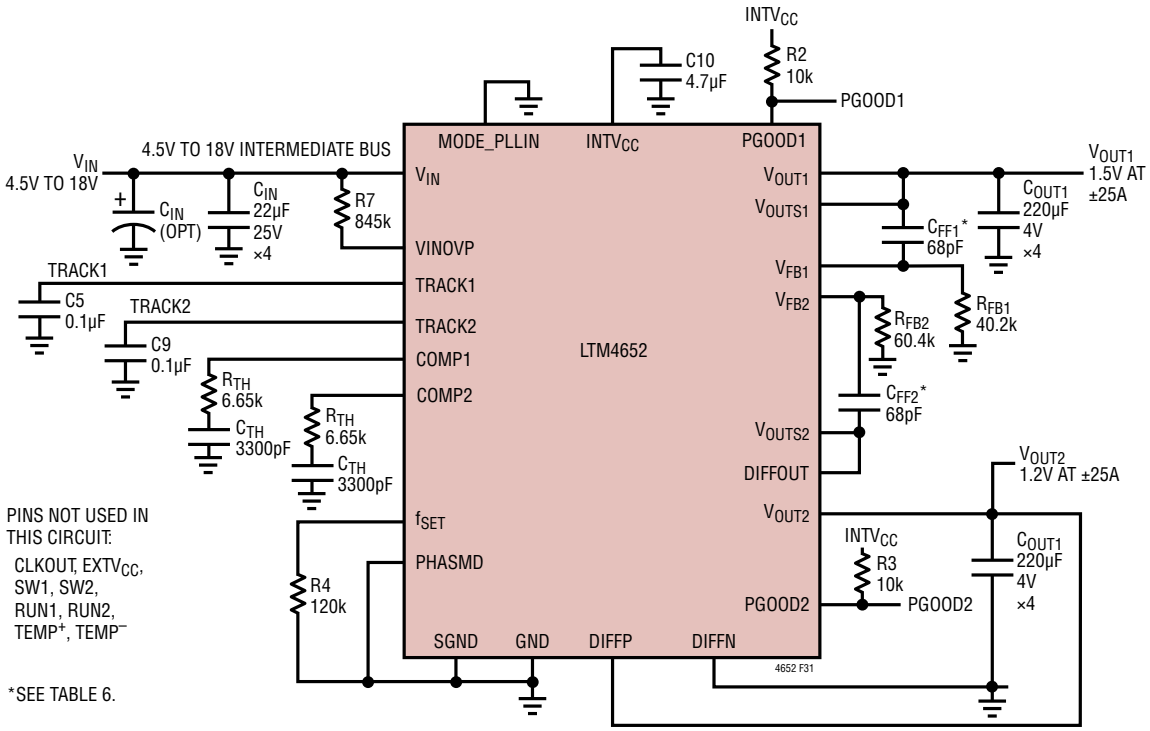
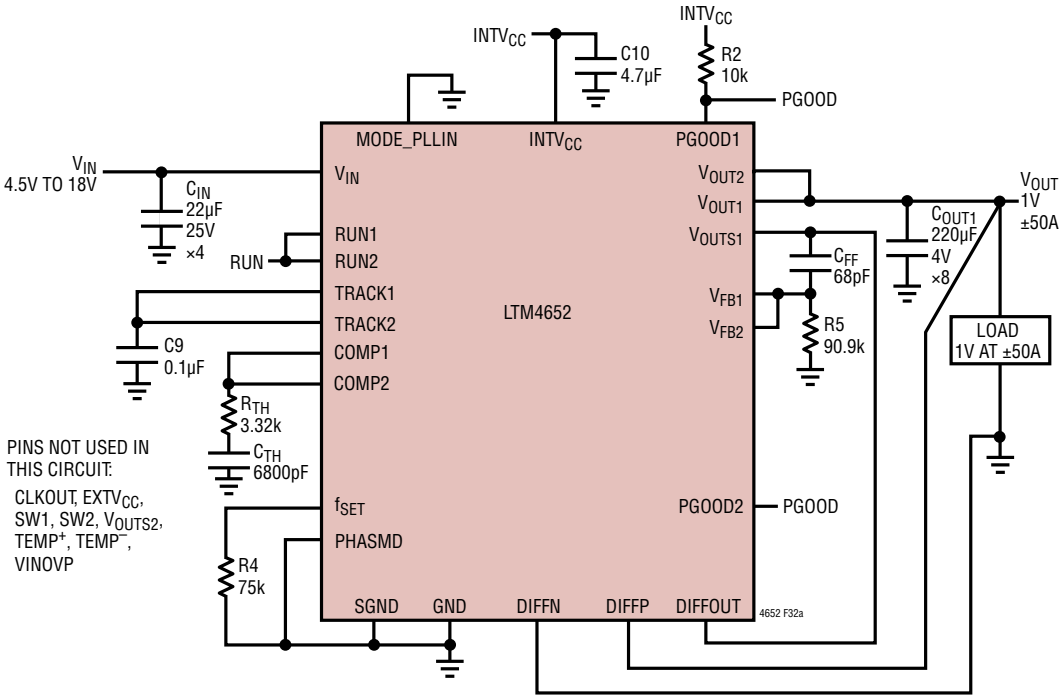
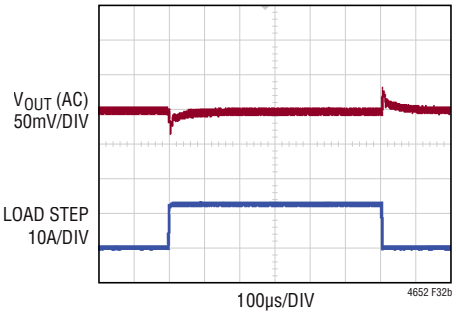


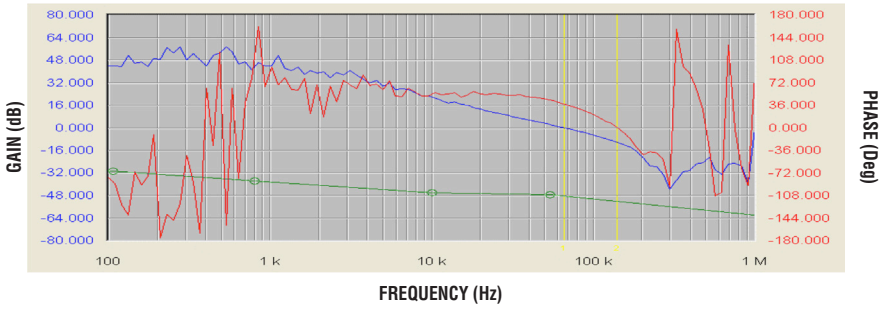
Figure 31. Typical 4.5V_{IN} to 18V_{IN}, 1.5V and 1.2V at ±25A Outputs

TYPICAL APPLICATION





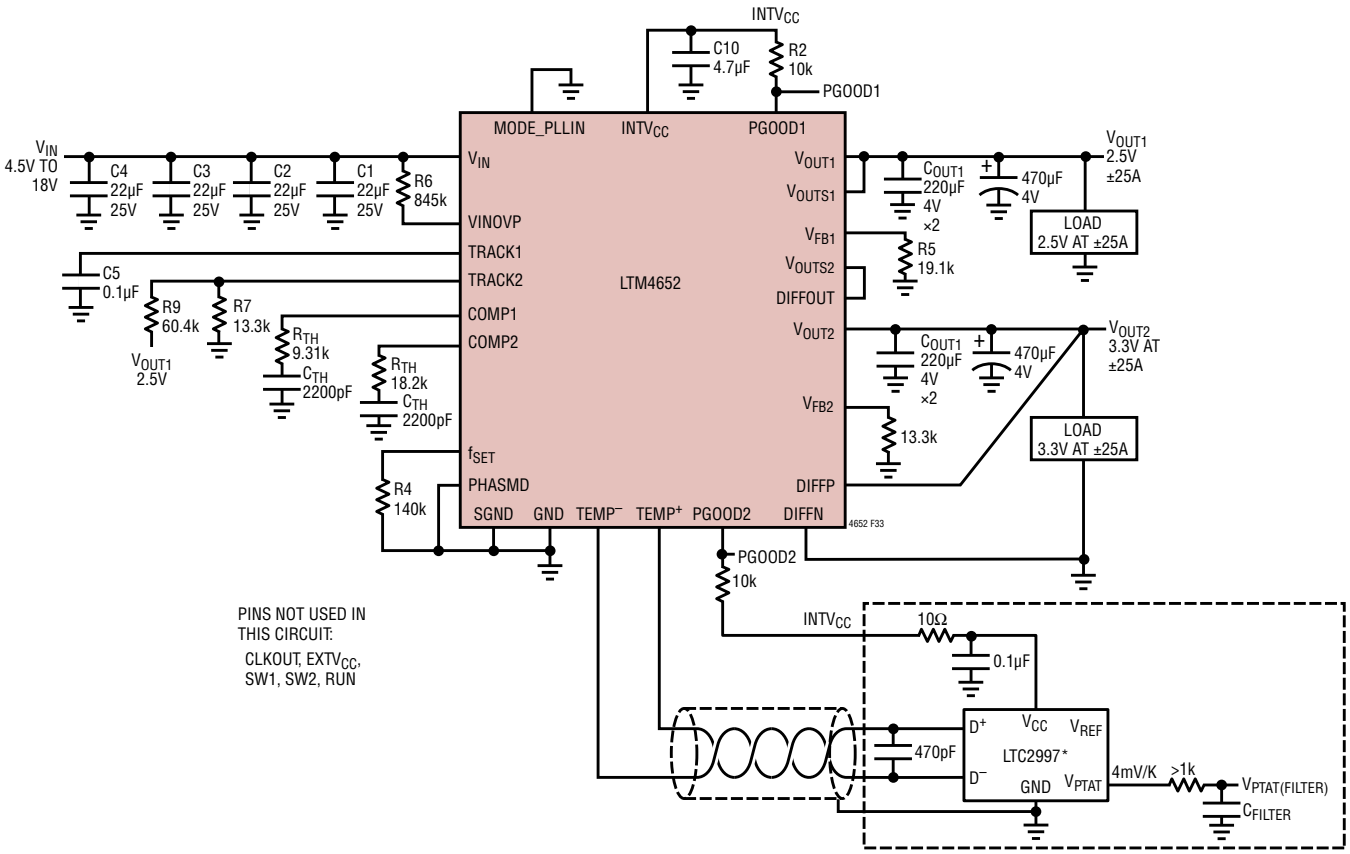
(b) 25% Load Step Transient Response; 12V_{IN}, 1.0V_{OUT}, 50A per Above Circuit



(c) 12V_{IN}, 1.0V_{OUT}, 50A Bode Plot per Above Circuit

Figure 32. LTM4652 2-Phase, 1V at 50A

TYPICAL APPLICATION



*PLACE 470pF DIRECTLY ACROSS THE LTC2997'S D^+/D^- PINS.
ROUTE $TEMP^+/TEMP^-$ DIFFERENTIALLY TO D^+/D^- AND PROTECT FROM NOISE WITH GROUND SHIELDING.
TERMINATE (CONNECT) THE D^+/D^- GROUND SHIELD AT THE LTC2997 GND PIN, ONLY.
FOR BEST V_{PTAT} PERFORMANCE, THE V_{CC} PIN OF THE LTC2997 MUST BE LOCALLY BYPASSED AND QUIET.
SEE LTC2997 DATA SHEET AND APRIL 2017 LT JOURNAL TECHNICAL ARTICLES.

Figure 33. LTM4652 2.5V and 3.3V Output with Tracking Function

TYPICAL APPLICATION

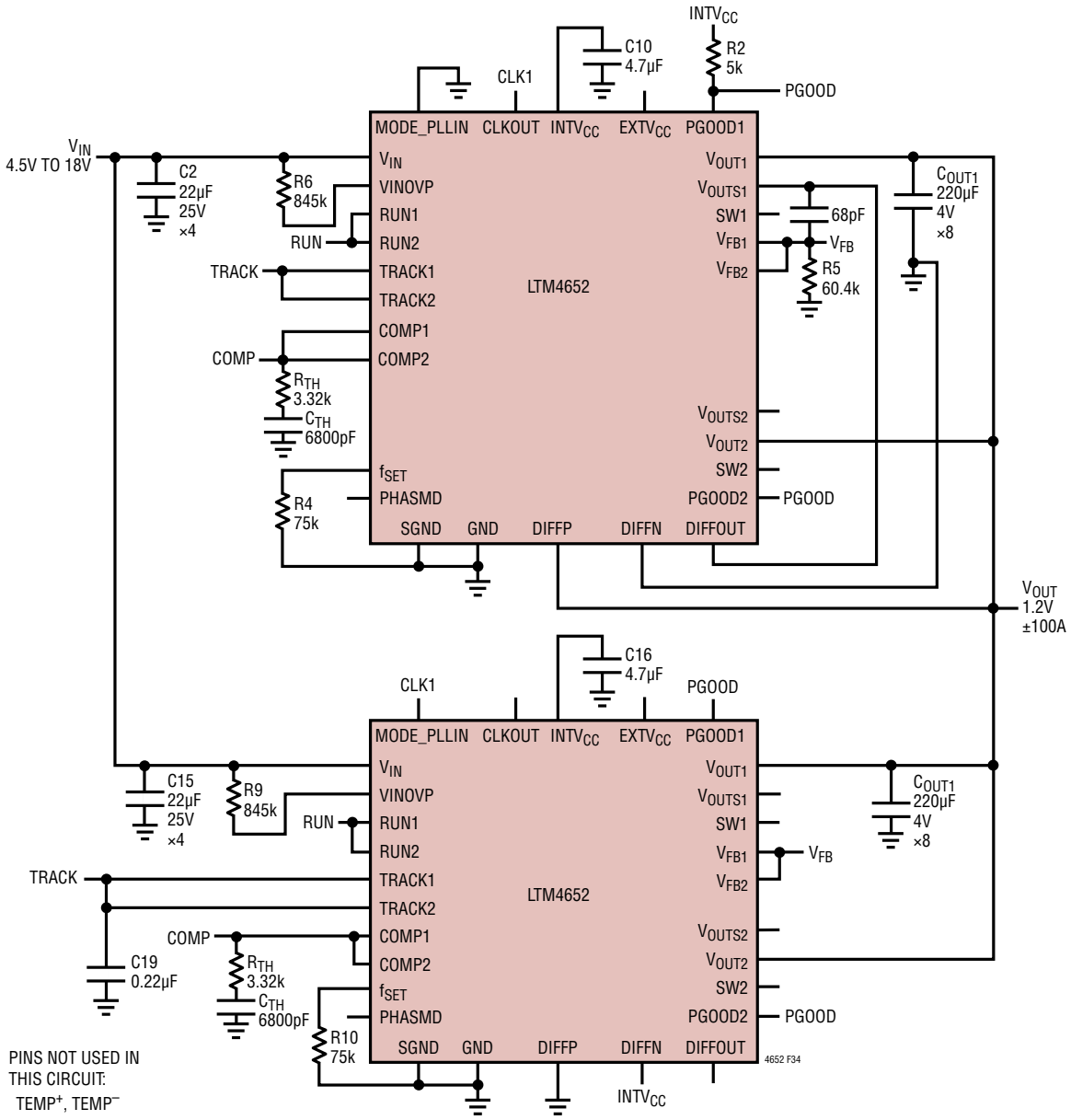
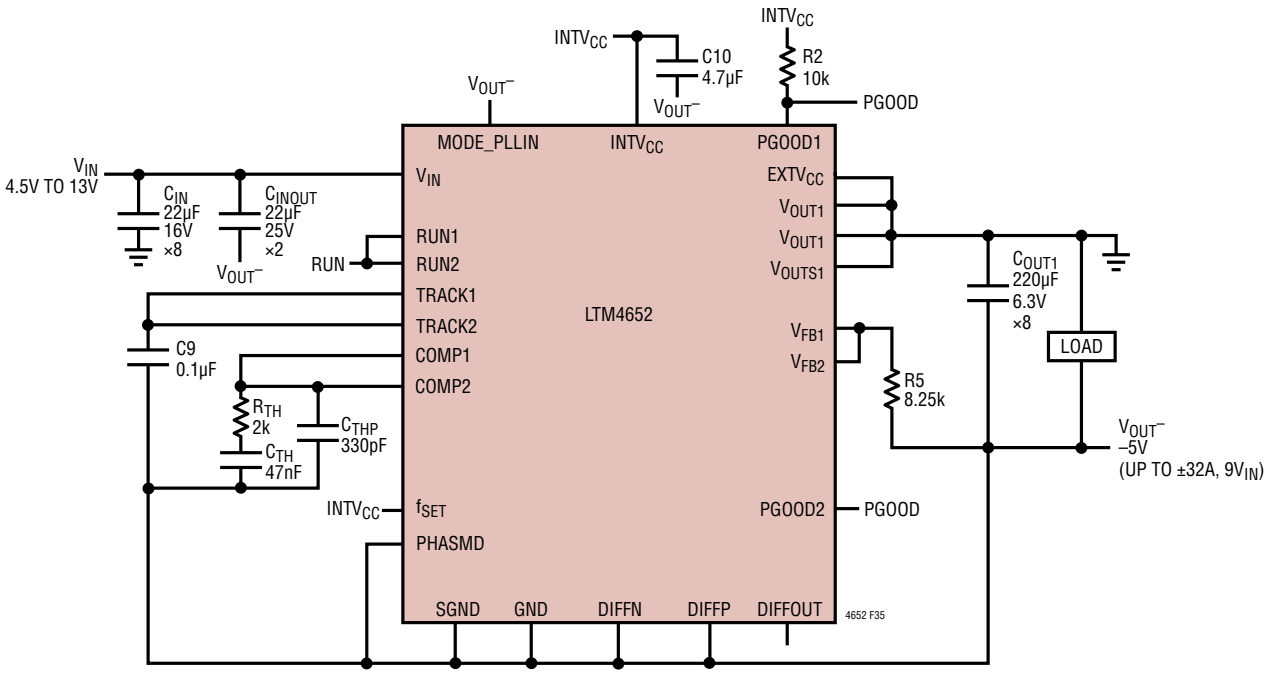


Figure 34. LTM4652 4-Phase, 1.2V at 100A

TYPICAL APPLICATION



PINS NOT USED IN THIS CIRCUIT:
CLKOUT, SW1, SW2, V_{OUTS2}, $TEMP^+$, $TEMP^-$, VINOVP

Figure 35. LTM4652 Regulating –5V at Up to ±32A (at $9V_{IN}$); See Demo Boards DC3230A and DC3195A for More Details (Including Performance of PolyPhase and Multimodule Parallel Applications)

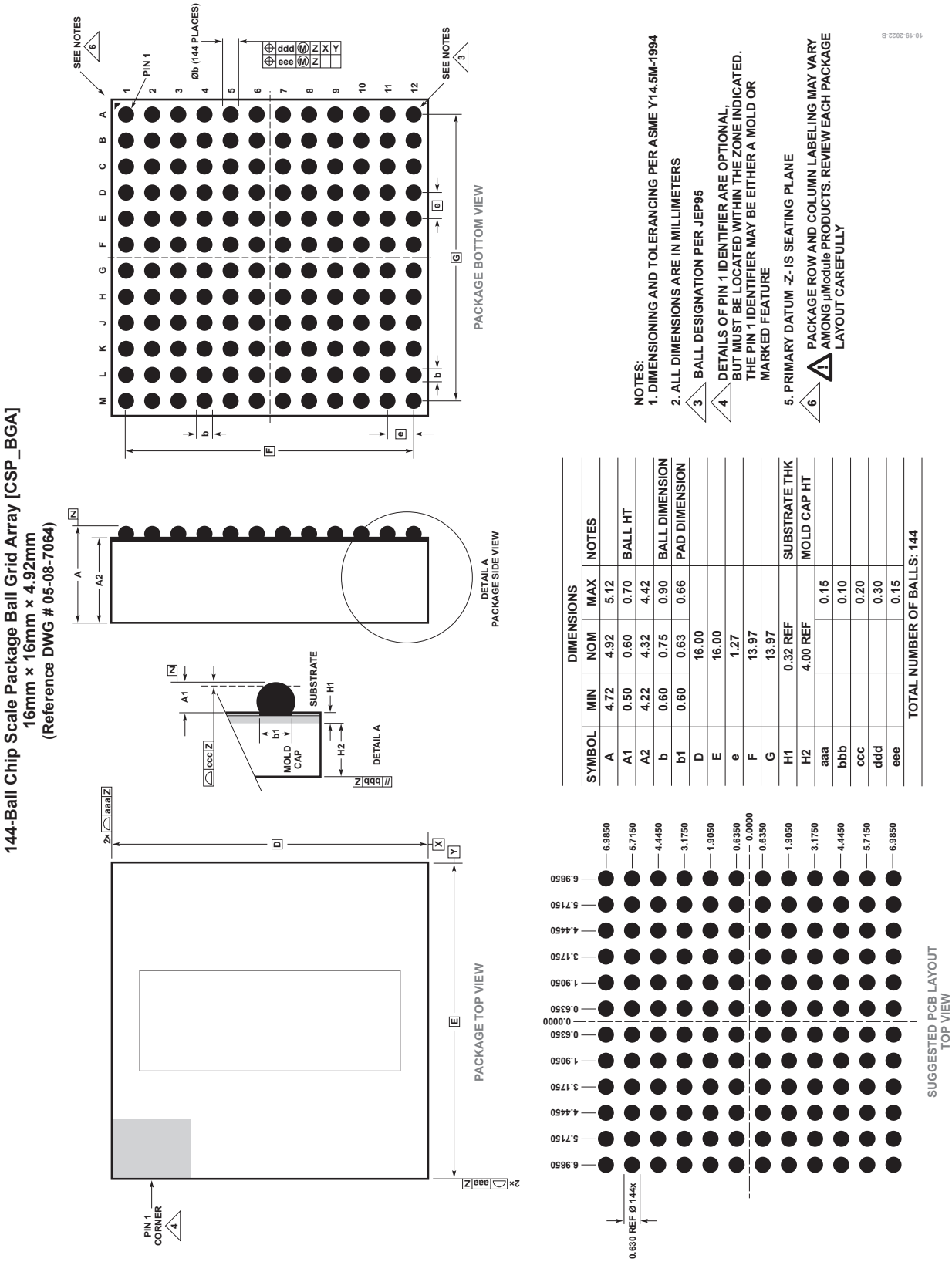
PACKAGE DESCRIPTION

LTM4652 Component BGA Pinout

PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION
A1	V_{OUT1}	B1	V_{OUT1}	C1	V_{OUT1}	D1	GND	E1	GND	F1	GND
A2	V_{OUT1}	B2	V_{OUT1}	C2	V_{OUT1}	D2	GND	E2	GND	F2	GND
A3	V_{OUT1}	B3	V_{OUT1}	C3	V_{OUT1}	D3	GND	E3	GND	F3	GND
A4	V_{OUT1}	B4	V_{OUT1}	C4	V_{OUT1}	D4	GND	E4	GND	F4	MODE_PLLIN
A5	V_{OUT1}	B5	V_{OUT1}	C5	V_{OUTS1}	D5	VFB1	E5	TRACK1	F5	RUN1
A6	GND	B6	GND	C6	f_{SET}	D6	SGND	E6	COMP1	F6	SGND
A7	GND	B7	GND	C7	SGND	D7	VFB2	E7	COMP2	F7	SGND
A8	V_{OUT2}	B8	V_{OUT2}	C8	V_{OUTS2}	D8	TRACK2	E8	DIFFP	F8	DIFFOUT
A9	V_{OUT2}	B9	V_{OUT2}	C9	V_{OUT2}	D9	GND	E9	DIFFN	F9	RUN2
A10	V_{OUT2}	B10	V_{OUT2}	C10	V_{OUT2}	D10	GND	E10	GND	F10	GND
A11	V_{OUT2}	B11	V_{OUT2}	C11	V_{OUT2}	D11	GND	E11	GND	F11	GND
A12	V_{OUT2}	B12	V_{OUT2}	C12	V_{OUT2}	D12	GND	E12	GND	F12	GND

PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION	PIN ID	FUNCTION
G1	GND	H1	GND	J1	GND	K1	GND	L1	GND	M1	GND
G2	SW1	H2	GND	J2	V_{IN}	K2	V_{IN}	L2	V_{IN}	M2	V_{IN}
G3	GND	H3	GND	J3	V_{IN}	K3	V_{IN}	L3	V_{IN}	M3	V_{IN}
G4	PHASMD	H4	GND	J4	V_{IN}	K4	V_{IN}	L4	V_{IN}	M4	V_{IN}
G5	CLKOUT	H5	VINOVP	J5	GND	K5	GND	L5	V_{IN}	M5	V_{IN}
G6	SGND	H6	$TEMP^-$	J6	$TEMP^+$	K6	GND	L6	VIN	M6	V_{IN}
G7	SGND	H7	GND	J7	$EXTV_{CC}$	K7	GND	L7	V_{IN}	M7	V_{IN}
G8	PGOOD2	H8	$INTV_{CC}$	J8	GND	K8	GND	L8	V_{IN}	M8	V_{IN}
G9	PGOOD1	H9	GND	J9	V_{IN}	K9	V_{IN}	L9	V_{IN}	M9	V_{IN}
G10	GND	H10	GND	J10	V_{IN}	K10	V_{IN}	L10	V_{IN}	M10	V_{IN}
G11	SW2	H11	GND	J11	V_{IN}	K11	V_{IN}	L11	V_{IN}	M11	V_{IN}
G12	GND	H12	GND	J12	GND	K12	GND	L12	GND	M12	GND

PACKAGE DESCRIPTION



DIMENSIONS				
SYMBOL	MIN	NOM	MAX	NOTES
A	4.72	4.92	5.12	
A1	0.50	0.60	0.70	BALL HT
A2	4.22	4.32	4.42	
b	0.60	0.75	0.90	BALL DIMENSION
b1	0.60	0.63	0.66	PAD DIMENSION
D		16.00		
E		16.00		
e		1.27		
F		13.97		
G		13.97		
H1		0.32 REF		SUBSTRATE THK
H2		4.00 REF		MOLD CAP HT
aaa			0.15	
bbb			0.10	
ccc			0.20	
ddd			0.30	
eee			0.15	
TOTAL NUMBER OF BALLS: 144				

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
2. ALL DIMENSIONS ARE IN MILLIMETERS
3. BALL DESIGNATION PER JEP95
4. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE PIN 1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE
5. PRIMARY DATUM -Z- IS SEATING PLANE
6. PACKAGE ROW AND COLUMN LABELING MAY VARY AMONG µModule PRODUCTS. REVIEW EACH PACKAGE LAYOUT CAREFULLY

10-19-2022-B

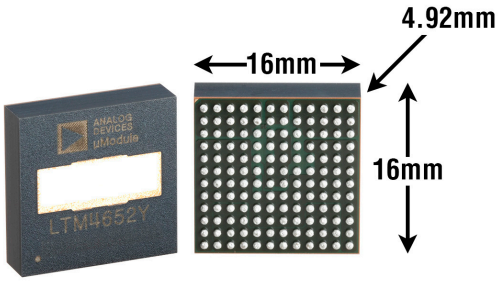
Rev. A

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	3/23	Changed master to main and slave to subordinate.	All
		Updated Electrical Characteristics (f_{SYNC}, Each Channel)	3
		Corrected pin function names for PHASMD, V_{OUTS1} and V_{OUTS2} in Figure 1 (Block Diagram) and Pinout table.	11, 35
		Updated package drawing.	36

PACKAGE PHOTOS

Part marking is either ink mark or laser mark



DESIGN RESOURCES

SUBJECT	DESCRIPTION	
µModule Design and Manufacturing Resources	Design: • Selector Guides • Demo Boards and Gerber Files • Free Simulation Tools	Manufacturing: • Quick Start Guide • PCB Design, Assembly and Manufacturing Guidelines • Package and Board Level Reliability
µModule Regulator Products Search	1. Sort table of products by parameters and download the result as a spread sheet. 2. Search using the Quick Power Search parametric table. Quick Power Search INPUT | V_{in}(Min) V V_{in}(Max) V OUTPUT | V_{Out} V I_{out} A FEATURES | Low EMI Ultrathin Internal Heat Sink Multiple Outputs Search	
Digital Power System Management	Analog Devices' family of digital power supply management ICs are highly integrated solutions that offer essential functions, including power supply monitoring, supervision, margining and sequencing, and feature EEPROM for storing user configurations and fault logging.	

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTM8064	58V_{IN}, ±6A, CV_{CC} µModule Regulator	6V ≤ V_{IN} ≤ 58V, 1.2V ≤ V_{OUT} ≤ 36V; 16mm × 11.9mm × 4.92mm (BGA)
LTM8052	36V_{IN}, ±5A, CV_{CC} µModule Regulator	6V ≤ V_{IN} ≤ 36V, 1.2V ≤ V_{OUT} ≤ 24V; 15mm × 11.25mm × 2.82mm (LGA) and 15mm × 11.25mm × 3.42mm (BGA)
LTM4650	Dual 25A or Single 50A µModule Regulator	4.5V ≤ V_{IN} ≤ 15V, 0.6V ≤ V_{OUT} ≤ 1.8V; 16mm × 16mm × 5.01mm (BGA)
LTM4650A	Dual 25A or Single 50A µModule Regulator, Up to 5.5V_{OUT}	4.5V ≤ V_{IN} ≤ 16V, 0.6V ≤ V_{OUT} ≤ 5.5V; 16mm × 16mm × 5.01mm (BGA)
LTM4650A-1	Dual 25A or Single 50A µModule Regulator, Up to 5.5V_{OUT} and External Compensation	4.5V ≤ V_{IN} ≤ 16V, 0.6V ≤ V_{OUT} ≤ 5.5V; 16mm × 16mm × 5.01mm (BGA)
LTM4630A	Lower Current and Higher V_{OUT} than LTM4650, Up to 5.3V_{OUT}, Dual 18A or Single 36A	Pin Compatible with LTM4650; 4.5V ≤ V_{IN} ≤ 18V, 0.6V ≤ V_{OUT} ≤ 8V, 16mm × 16mm × 4.41mm (LGA), 16mm × 16mm × 5.01mm (BGA)
LTM4620A	Lower Current and Higher V_{OUT} than LTM4650, Up to 5.3V_{OUT}, Dual 13A or Single 26A	Pin Compatible with LTM4650; 4.5V ≤ V_{IN} ≤ 16V, 0.6V ≤ V_{OUT} ≤ 5.3V, 15mm 15mm × 4.41mm (LGA) and 15mm × 15mm × 5.01mm (BGA)