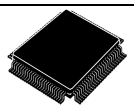
SPC58xN

32-bit Power Architecture® microcontroller for automotive ASIL-D and security applications

Data brief

LFBGA292 (17 x 17 x 1.7 mm)



eLQFP176 (24 x 24 x 1.4 mm)

Features

- AEC-Q100 qualified
- 32-bit Power Architecture VLE compliant CPU cores:
  - Five enhanced main e200z4256n3 cores, dual issue, two paired in lockstep
  - Floating Point, End-to-End Error Correction
- 6576 KB (6288 KB code flash + 288 KB data flash) on-chip flash memory:
  - supports read during program and erase operations, and multiple blocks allowing EEPROM emulation
  - Supports read while read between the two code Flash partitions.
- 128 KB on-chip general-purpose SRAM (in addition to 384 KB included in the CPUs)
- 96-channel direct memory access controller (eDMA)
- Comprehensive new generation ASIL-D safety concept
  - ASIL-D of ISO 26262
  - FCCU for collection and reaction to failure notifications
  - Memory Error Management Unit (MEMU) for collection and reporting of error events in memories
  - Cyclic redundancy check (CRC) unit
- Junction temperature range -40 °C to 165 °C
- Dual-channel FlexRay controller
- Hardware Security Module (HSM)
- GTM344 - generic timer module
  - Intelligent complex timer module
  - 144 channels (48 input and 96 output)
  - 5 programmable fine grain multi-threaded cores
  - 61 KB of dedicated RAM
  - 24-bit wide channels
- Enhanced analog-to-digital converter system with:
  - 1 supervisor 12-bit SAR analog converter
  - 2 separate 10-bit SAR analog converter
  - 4 separate fast 12-bit SAR analog converters
  - 6 separate 16-bit Sigma-Delta analog converter with programmable decimation filters
- SAR ADC Queued digital interfaces for individual channel ordering and command sequencing
- Communication interfaces
  - 7 LINFlexD modules
  - 8 deserial serial peripheral interface (DSPI) modules
  - 7 modular controller area network (MCAN) modules, and one time-triggered controller area network (M-TTCAN), all supporting flexible data rate (ISO CAN-FD)
- One Ethernet controller 10/100 Mbps, compliant IEEE 802.3-2008
- Flexible Power Supply options:
  - External Regulators (1.2 V core, 3.3 V - 5 V IO)
  - Single internal SMPS regulator
- Nexus development interface (NDI) per IEEEISTO 5001-2003 standard, with some support for 2010 standard
- Boot assist Flash (BAF) supports factory programming using a serial bootload through the asynchronous CAN or LIN/UART

Contents

1 Description

SPC58 N line MCU, based on Power Architecture® Technology, is designed for mission-critical automotive applications where most stringent safety standards and real-time performance really matters.

SPC58 N line high performance and real time capabilities, combined with ISO26262 ASIL D functional safety compliance and embedded security, address high and mid powertrain applications, Electric vehicles.

2 SPC58 N line main benefits

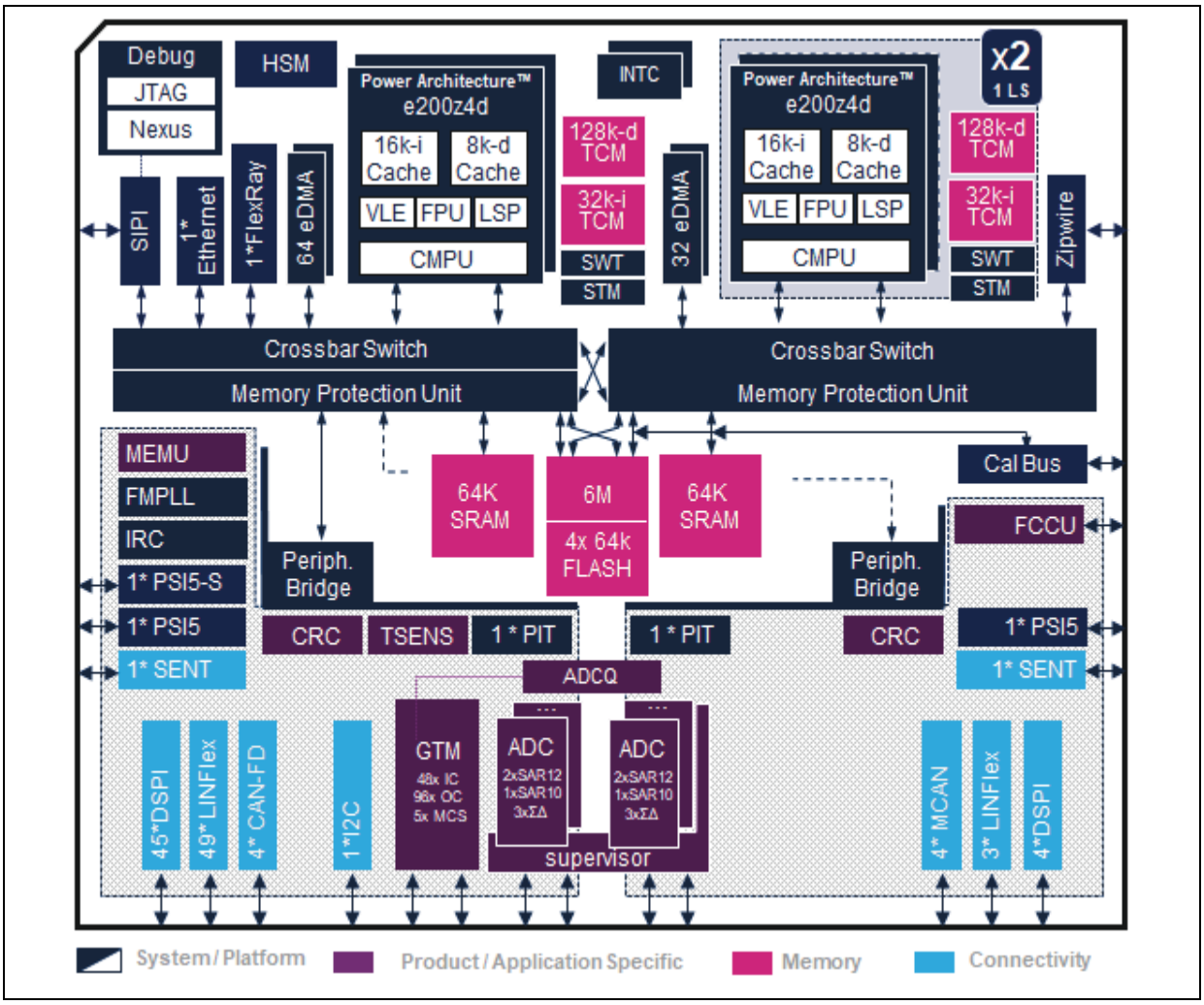
The SPC58 N line family system benefits are the followings:

- Optimized platform architecture (dedicated Multi-cores, Local memories, etc...) for best-in-class system performance MCU
- True ASIL-D Safety Element out of Context (SEooC) concept relying on HW measures for reduced SW overhead
- Generic Timer Module (GTM) optimized for Powertrain use while minimizing CPU load
- Hardware Security Module (HSM)
- Hardware Sensor Interface (SENT, PSI5)
- Enhanced Communication (LFAST, Ethernet, Micro Second Bus (MSB), etc...)
- Increased high dynamic signals acquisition through SD-ADC
- Innovative built-in concept allowing on-chip emulation with production-compatible package (176-pin eLQFP and 292-pin LFBGA)

3 Block diagram

Figure 1 shows the top-level block diagram.

Figure 1. SPC58 N line family block diagram



4 ECOPACK

In order to meet environmental requirements, ST offers these devices in different grades of *ECOPACK* packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK is an ST trademark.

5 Ordering information

Table 1. Device summary

Reference	Part number
SPC58xN	SPC58NN84C3, SPC58NN84E7, SPC58NN80C3, SPC58NN80E7

6 Revision history

Table 2. Document revision history

Date	Revision	Changes
17-Sep-2015	1	Initial release.
29-Jan-2020	2	Updated: – RPN; – Features.