Isolated Compact IGBT Gate Driver with Current Sense

NCD57085, NCV57085

NCx57085 is a high current single channel IGBT gate driver with 2.5 kVrms internal galvanic isolation designed for high system efficiency and reliability in high power applications. The driver includes Current Sense function with soft turn off and fault reporting in a narrow body SOIC − 8 package. NCx57085 accommodates wide range of input bias voltage and signal levels from 3.3 V to 20 V, and wide range of output bias voltage up to 30 V.

Features

- High Peak Output Current (+7A/−7 A)
- Low Output Impedance for Enhanced IGBT Driving
- Short Propagation Delays with Accurate Matching
- IGBT Over Current Protection
- Negative Voltage (Down to −9 V) Capability for CS Pin
- IGBT Gate Clamping during Short Circuit
- IGBT Gate Active Pull Down
- Soft Turn Off During IGBT Over Current
- Tight UVLO Thresholds for Bias Flexibility
- Output Partial Pulse Avoidance During UVLO/CS (Restart)
- 3.3. V, 5 V, and 15 V Logic Input
- 2.5 kVrms Galvanic Isolation
- High Transient Immunity
- High Electromagnetic Immunity
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable
- This Device is Pb−Free, Halogen Free/BFR Free and is RoHS Compliant

Typical Applications

- Motor Control
- Automotive Applications
- Uninterruptible Power Supplies (UPS)
- Industrial Power Supplies
- HVAC
- Industrial Pumps and Fans
- PTC Heater

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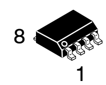
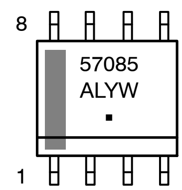


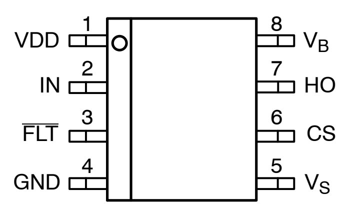
SOIC−8 NB
CASE 751−07

MARKING DIAGRAM



57085	= Specific Device Code
A	= Assembly Location
L	= Wafer Lot
Y	= Year
W	= Work Week
▪	= Pb−Free Package

PIN CONNECTIONS



NCx57085
x = D or V

ORDERING INFORMATION

See detailed ordering and shipping information on page 12 of this data sheet.

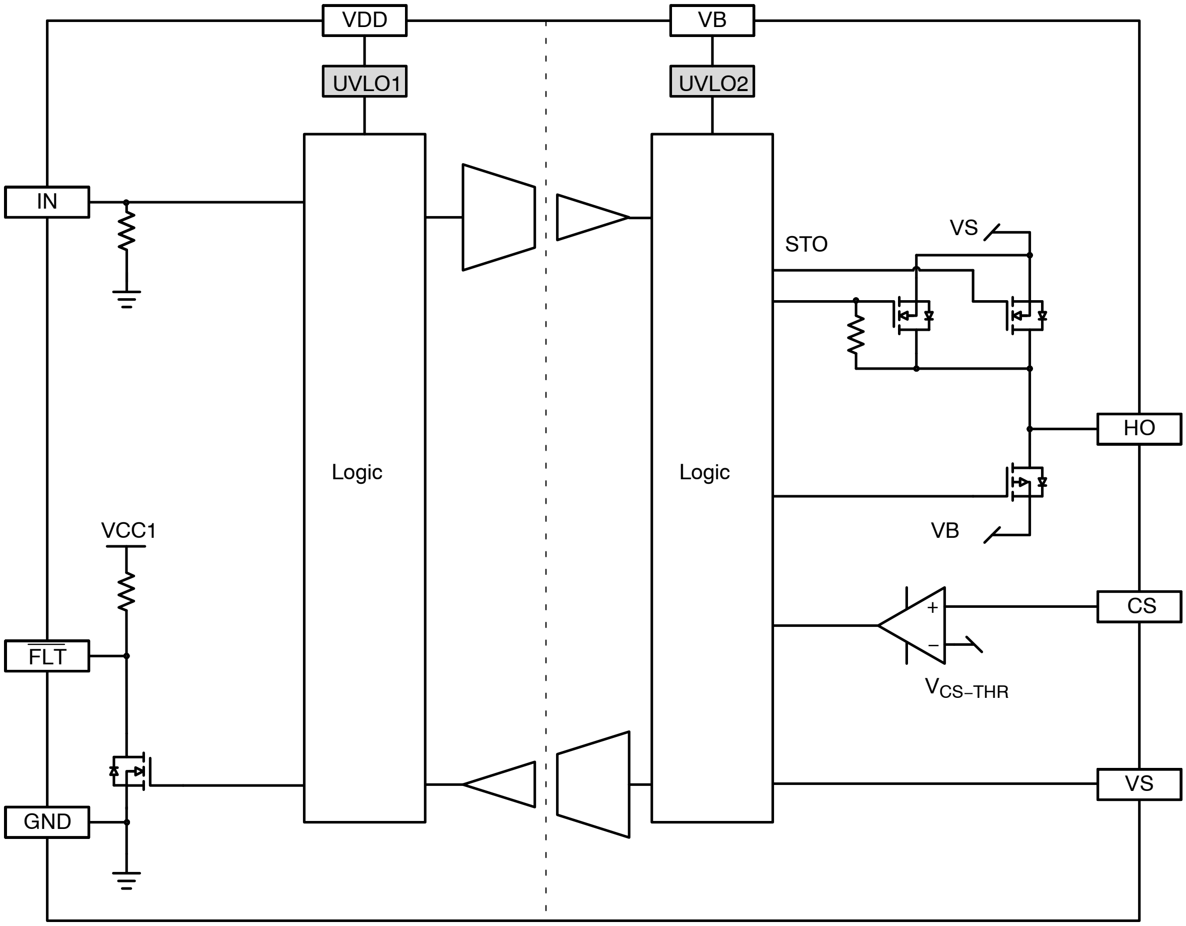


Figure 1. Simplified Block Diagram

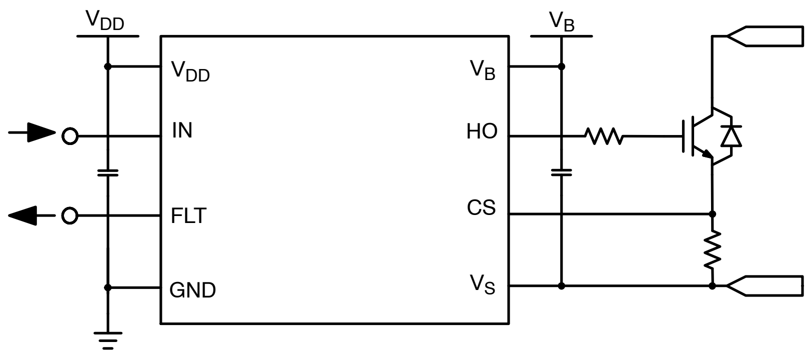


Figure 2. Simplified Application Schematics, Current Sense Using Shunt Resistor

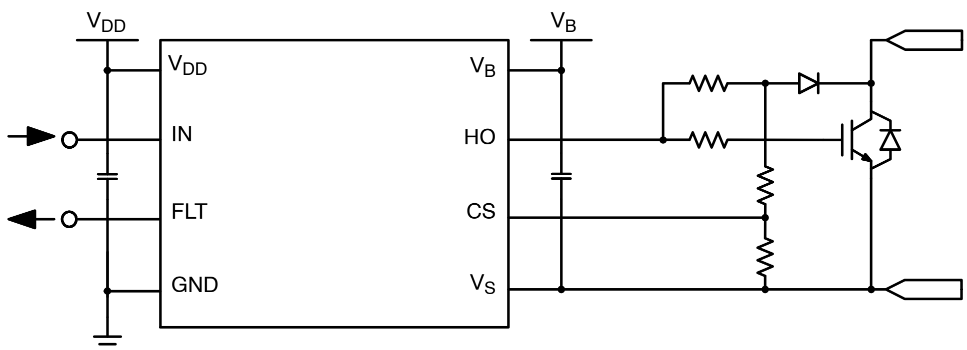


Figure 3. Simplified Application Schematics, Current Sense Using IGBT Vce

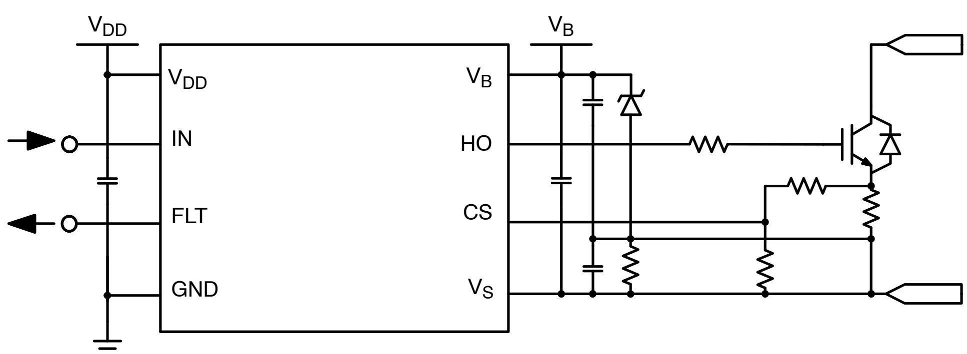


Figure 4. Simplified Application Schematics, Current Sense Using Shunt Resistor and Negative Gate Drive

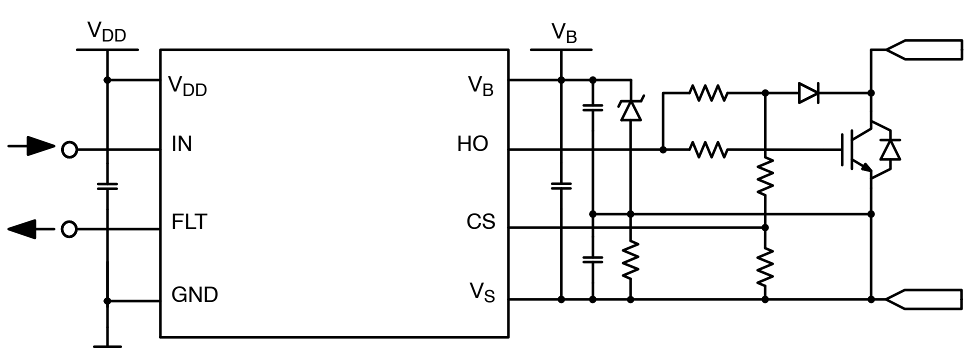


Figure 5. Simplified Application Schematics, Current Sense Using IGBT Vce and Negative Gate Drive

FUNCTION DESCRIPTION

Pin Name	No.	I/O	Description
V_{DD}	1	Power	Input side power supply. A good quality bypassing capacitor is required from this pin to GND and should be placed close to the pins for best results. The under voltage lockout (UVLO) circuit enables the device to operate at power on when a typical supply voltage higher than $V_{UVLO1-OUT-ON}$ is present. Please see Figure 7 for more details.
IN	2	I	Non−inverted gate driver input. The equivalent input pull down resistance is about 100 kΩ when the input voltage is below 5.5 V. The input adapter circuitry will work once the input voltage is higher than 5.5 V, and will keep the input current at the level when the input voltage is 5.5 V even though it is higher than that. A minimum pulse width is required at IN before HO responds.
$\overline{FLT}$	3	O	Fault output (active low) that allows communication to the main controller that the driver has encountered a Over Current, or UVLO1, or UVLO2 condition and has deactivated the output. There is an internal 50 kΩ pull−up resistor connected to this pin. Multiple of them from different drivers can be “OR”ed together. /FLT and HO will go high automatically after t_{MUTE} expires along with a rising edge of IN to avoid partial output pulse on HO. This is a feature called “Re−start”.
GND	4	Power	Input side ground reference.
V_S	5	Power	Output side ground reference.
CS	6	I/O	Input for detecting over current of IGBT. The current sense threshold has to be met uninterruptedly for a fixed period of t_{FILTER} before HO and /FLT are set low. Please refer to Figure 9 and Figure 10. $\overline{FLT}$ and HO will be kept low (including soft turn off time) at least for a period defined by t_{MUTE}.
HO	7	O	Driver output that provides the appropriate drive voltage and source/sink current to the IGBT/FET gate. HO is actively pulled low during start−up.
V_B	8	Power	Output side positive power supply. The operating range for this pin is from UVLO2 to its maximum allowed value. A good quality bypassing capacitor is required from this pin to V_S and should be placed close to the pins for best results. The under voltage lockout (UVLO) circuit enables the device to operate at power on when a typical supply voltage higher than $V_{UVLO2-OUT-ON}$ is present. Please see Figure 8 for more details.

SAFETY AND INSULATION RATINGS

Symbol	Parameter		Value	Unit
	Installation Classifications per DIN VDE 0110/1.89 Table 1 Rated Mains Voltage	< 150 V_{RMS}	I–IV	
		< 300 V_{RMS}	I–IV	
		< 450 V_{RMS}	I–IV	
		< 600 V_{RMS}	I–IV	
		< 1000 V_{RMS}	I–III	
	Climatic Classification		40/100/21	
	Pollution Degree (DIN VDE 0110/1.89)		2	
CTI	Comparative Tracking Index (DIN IEC 112/VDE 0303 Part 1)		600	
V_{PR}	Input−to−Output Test Voltage, Method B, $V_{IORM} \times 1.875 = V_{PR}$, 100% Production Test with t_m = 1 s, Partial Discharge < 5 pC		2250	V_{PK}
V_{IORM}	Maximum Repetitive Peak Voltage		1200	V_{PK}
V_{IOWM}	Maximum Working Insulation Voltage		870	V_{RMS}
V_{IOTM}	Highest Allowable Over Voltage		4200	V_{PK}
E_{CR}	External Creepage		4.0	mm
E_{CL}	External Clearance		4.0	mm
DTI	Insulation Thickness		8.65	μm
T_{Case}	Safety Limit Values – Maximum Values in Failure; Case Temperature		150	°C
$P_{S,INPUT}$	Safety Limit Values – Maximum Values in Failure; Input Power		132	mW
$P_{S,OUTPUT}$	Safety Limit Values – Maximum Values in Failure; Output Power		1128	mW
R_{IO}	Insulation Resistance at TS, V_{IO} = 500 V		10^9	Ω

ISOLATION CHARACTERISTICS

Symbol	Parameter	Conditions	Value	Unit
$V_{ISO,}$ INPUT− OUTPUT	Input−Output Isolation Voltage	T_A = 25°C, Relative Humidity < 50%, t = 1.0 minute, I_{I-O} < 30 μA, 50 Hz (Notes 1, 2, 3)	2500	V_{RMS}
R_{ISO}	Isolation Resistance	V_{I-O} = 500 V (Note 1)	10^{11}	Ω

1. Device is considered a two−terminal device: pins 1 to 4 are shorted together and pins 5 to 8 are shorted together.
2. 2,500 VRMS for 1−minute duration is equivalent to 3,000 VRMS for 1−second duration.
3. The input−output isolation voltage is a dielectric voltage rating per UL1577. It should not be regarded as an input−output continuous voltage rating. For the continuous working voltage rating, refer to equipment−level safety specification or DIN VDE V 0884−11 Safety and Insulation Ratings Table.

ABSOLUTE MAXIMUM RATINGS (Note 4) Over operating free−air temperature range unless otherwise noted.

Symbol	Parameter	Minimum	Maximum	Unit
V_{DD} − GND	Supply Voltage, Input Side	−0.3	22	V
$V_B - V_S$	Supply Voltage, Output Side	−0.3	32	V
$V_{HO} - V_S$	Gate−driver Output Voltage	−0.3	V_{BS} + 0.3	V
I_{PK-SRC}	Gate−driver Output Sourcing Current (maximum pulse width = 10 μs, maximum duty cycle = 0.2%, $V_D - V_S$ = 15 V)	−	7	A
I_{PK-SNK}	Gate−driver Output Sinking Current (maximum pulse width = 10 μs, maximum duty cycle = 0.2%, $V_D - V_S$ = 15 V)	−	7.5	A
V_{IN} − GND	Voltage at IN, $\overline{FLT}$	−0.3	V_{DD} + 0.3	V
I_{FLT}	Output current of $\overline{FLT}$	−	10	mA
$V_{CS} - V_S$	Voltage at CS (Note 5)	−9	V_{BS} + 0.3	V
PD	Power Dissipation (Note 6)	−	1123	mW
ESD_{HBM}	ESD Capability, Human Body Model (Note 7)	−	± 2	kV
ESD_{CDM}	ESD Capability, Charged Device Model (Note 7)	−	± 2	kV
MSL	Moisture Sensitivity Level	−	1	−
T_J(max)	Maximum Junction Temperature	−40	150	°C
T_{STG}	Storage Temperature Range	−65	150	°C
T_{SLD}	Lead Temperature Soldering Reflow, Pb−Free (Note 8)	−	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

4. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.
5. The minimum value is verified by characterization with a single pulse of 1.5 mA for 300 μs.
6. The value is estimated for ambient temperature 25°C and junction temperature 150°C, 650 mm², 1 oz copper, 2 surface layers and 2 internal power plane layers. Power dissipation is affected by the PCB design and ambient temperature.
7. This device series incorporates ESD protection and is tested by the following methods:
   ESD Human Body Model tested per AEC−Q100−002 (EIA/JESD22−A114).
   ESD Charged Device Model tested per AEC−Q100−011 (EIA/JESD22−C101).
   Latchup Current Maximum Rating: ≤100 mA per JEDEC standard: JESD78, 125°C.
8. For information, please refer to our Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

THERMAL CHARACTERISTICS

Symbol	Parameter	Conditions	Value	Unit
$R_{\theta JA}$	Thermal Resistance, Junction−to−Air	100 mm², 1 oz Copper, 1 Surface Layer	179	°C/W
		100 mm², 1 oz Copper, 2 Surface Layers and 2 Internal Power Plane Layers	110	

9. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.
10. Values based on copper area of 100 mm² (or 0.16 in²) of 1 oz copper thickness and FR4 PCB substrate.

OPERATING RANGES (Note 11)

Symbol	Parameter	Min	Max	Unit
V_{DD}−GND	Supply Voltage, Input Side	UVLO1	20	V
V_B−V_S	Supply Voltage, Output Side	UVLO2	30	V
V_{IN}	Logic Input Voltage at IN	GND	V_{DD}	V
$\lvert dV_{ISO}/dt \rvert$	Common Mode Transient Immunity	100	−	kV/μs
T_A	Ambient Temperature	−40	125	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

11. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.

ELECTRICAL CHARACTERISTICS V_{DD} = 5 V, V_{BS} = 15 V.
For typical values T_A = 25°C, for min/max values, T_A is the operating ambient temperature range that applies, unless otherwise noted.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
VOLTAGE SUPPLY						
$V_{UVLO1-OUT-ON}$	UVLO1 Output Enabled		–	–	3.1	V
$V_{UVLO1-OUT-OFF}$	UVLO1 Output Disabled		2.4	–	–	V
$V_{UVLO1-HYST}$	UVLO1 Hysteresis		0.1	–	–	V
$V_{UVLO2-OUT-ON}$	UVLO2 Output Enabled		12.4	12.9	13.4	V
$V_{UVLO2-OUT-OFF}$	UVLO2 Output Disabled		11.5	12	12.5	V
$V_{UVLO2-HYST}$	UVLO2 Hysteresis		0.7	1	–	V
$I_{DD-0-3.3}$	Input Supply Quiescent Current	IN = Low, V_{DD} = 3.3 V, $\overline{FLT}$ = High	–	–	2	mA
I_{DD-0-5}		IN = Low, V_{DD} = 5 V, $\overline{FLT}$ = High	–	–	2	mA
$I_{DD-0-15}$		IN = Low, V_{DD} = 15 V, $\overline{FLT}$ = High	–	–	2	mA
$I_{DD-100-5}$		IN = High, V_{DD} = 5 V, $\overline{FLT}$ = High	–	–	6	mA
I_{BS-0}	Output Supply Quiescent Current	IN = Low, no load	–	–	4	mA
I_{BS-100}		IN = High, no load	–	–	6	mA
LOGIC INPUT AND OUTPUT						
V_{IL}	Low Input Voltage (Note 12)				1.65	V
V_{IH}	High Input Voltage (Note 12)		0.7 x V_{DD}		2.1	V
$V_{IN-HYST}$	Input Hysteresis Voltage (Note 12)			0.15 x V_{DD}		V
I_{IN}	Input Current	V_{IN} = V_{DD}		50		μA
I_{FLT-L}	$\overline{FLT}$ Pull−up Current (50 kΩ pull−up resistor)	V_{FLT} = Low	–	100	–	μA
V_{FLT-L}	$\overline{FLT}$ Low Level Output Voltage	I_{FLT} = 5 mA	–	–	0.3	V
t_{MIN1}	Input Pulse Width of IN for No Response at Output		–	–	10	ns
t_{MIN2}	Input Pulse Width of IN for Guaranteed Response at Output		40	–	–	ns
DRIVER OUTPUT						
V_{HOL1}	Output Low State ($V_{HO} - V_S$)	I_{SNK} = 200 mA	–	0.1	0.22	V
V_{HOL2}		I_{SNK} = 1.0 A, T_A = 25°C	–	0.4	1	
V_{HOH1}	Output High State ($V_B - V_{HO}$)	I_{SRC} = 200 mA	–	0.2	0.35	V
V_{HOH2}		I_{SRC} = 1.0 A, T_A = 25°C	–	0.6	1.7	
$I_{PK-SNK1}$	Peak Driver Current, Sink (Note 13)		–	7.5	–	A
$I_{PK-SNK2}$	Peak Driver Current, Sink (Note 13)	V_{HO} = 9 V (near IGBT Miller Plateau)	–	7	–	A
$I_{PK-SRC1}$	Peak Driver Current, Source (Note 13)		–	7	–	A
$I_{PK-SRC2}$	Peak Driver Current, Source (Note 13)	V_{HO} = 9 V (near IGBT Miller Plateau)	–	5	–	A
OVER CURRENT PROTECTION						
V_{CS-THR}	CS Threshold Voltage		0.2	0.25	0.3	V
V_{CS-NEG}	CS Negative Voltage	I_{CS} = 1.5 mA	–	−8	–	V

ELECTRICAL CHARACTERISTICS V_{DD} = 5 V, V_{BS} = 15 V.
For typical values T_A = 25°C, for min/max values, T_A is the operating ambient temperature range that applies, unless otherwise noted.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
IGBT SHORT CIRCUIT CLAMPING						
V_{CLP-HO}	IGBT Short Circuit Clamping (V_{HO} – V_B)	IN = High, I_{HO} = 500 mA, t_{CLP} = 10 μs	–	0.7	1.5	V
DYNAMIC CHARACTERISTICS						
t_{PD-ON}	IN to HO High Propagation Delay	C_{LOAD} = 10 Nf V_{IH} to 10% of HO Change for PW > 150 ns	40	60	90	ns
t_{PD-OFF}	IN to HO Low Propagation Delay	C_{LOAD} = 10 nF V_{IL} to 90% of HO Change for PW > 150 ns	40	60	90	ns
$t_{DISTORT}$	Propagation Delay Distortion (= t_{PD-ON} – t_{PD-OFF})	T_A = 25°C, PW > 150 ns	–	0	–	ns
		T_A = –40°C to 125°C, PW > 150 ns	–25	–	25	
$t_{DISTORT\_TOT}$	Prop Delay Distortion between Parts	PW > 150 ns	–30	0	30	ns
t_{RISE}	Rise Time (see Figure 6) (Note 13)	C_{LOAD} = 1 nF, 10% to 90% of HO Change	–	10	–	ns
t_{FALL}	Fall Time (see Figure 6) (Note 13)	C_{LOAD} = 1 nF, 90% to 10% of HO Change	–	15	–	ns
t_{LEB}	CS Leading Edge Blanking Time (See Figure 9 and Figure 10)		200	450	700	ns
t_{FILTER}	CS Threshold Filtering Time (see Figure 9 and Figure 10)		–	600	700	ns
t_{STO}	Soft Turn Off Time (see Figure 9 and Figure 10)	C_{LOAD} = 10 nF, R_G = 10 Ω	1.2	1.8	3	μs
t_{FLT}	Delay after t_{FILTER} to $\overline{FLT}$ Low		100	450	700	ns
t_{FLT1}	Delay from $V_{UVLO1-OUT-OFF}$ Triggered to $\overline{FLT}$ Low		–	1.5	–	ns
t_{FLT2}	Delay from t_{UV2F} to $\overline{FLT}$ Low		–	2.4	–	μs
t_{MUTE}	IN Mute Time after t_{FILTER}, or UVLO1, UVLO2 Triggered		20	–	–	μs
t_{UVR1}	Delay from $V_{UVLO1-OUT-ON}$ Triggered to HO High (see Figure 7)	(Note 13)	–	770	–	ns
t_{UVF1}	Delay from $V_{UVLO1-OUT-OFF}$ Triggered to HO Low (see Figure 7)	(Note 13)	–	1500	–	ns
t_{UVR2}	Delay from $V_{UVLO2-OUT-ON}$ Triggered to HO High (see Figure 8)	(Note 13)	–	1000	–	ns
t_{UVF2}	Delay from $V_{UVLO2-OUT-OFF}$ Triggered to HO Low (see Figure 8)	(Note 13)	–	1000	–	ns

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.
12. Table values are valid for 3.3 V and 5 V V_{DD}, for higher V_{DD} voltages, the threshold values are maintained at the 5 V V_{DD} levels.
13. Values based on design and/or characterization.

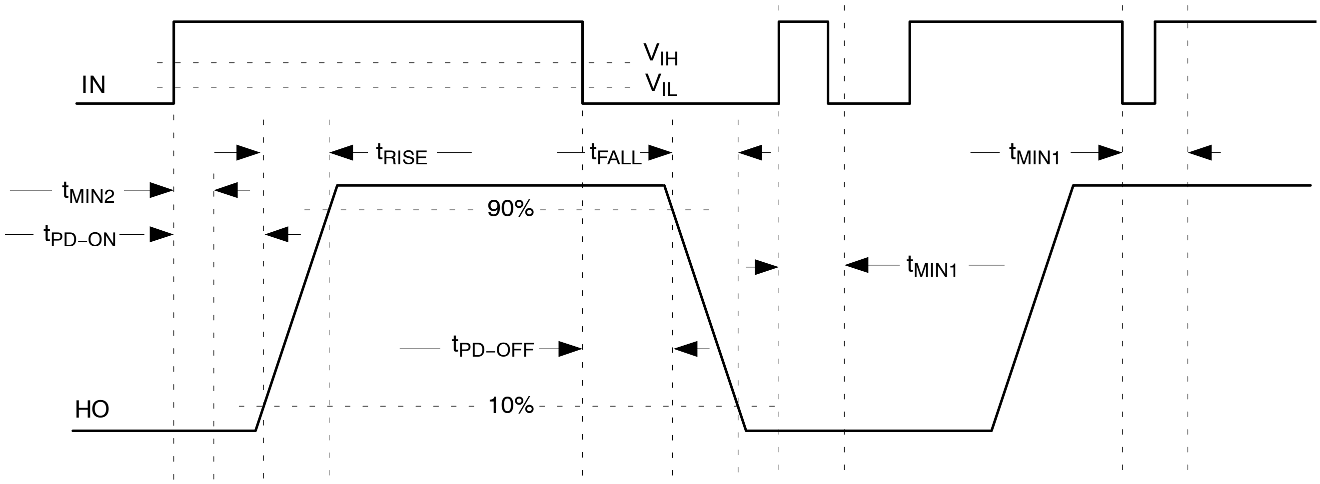


Figure 6. Propagation Delay, Rise and Fall Time

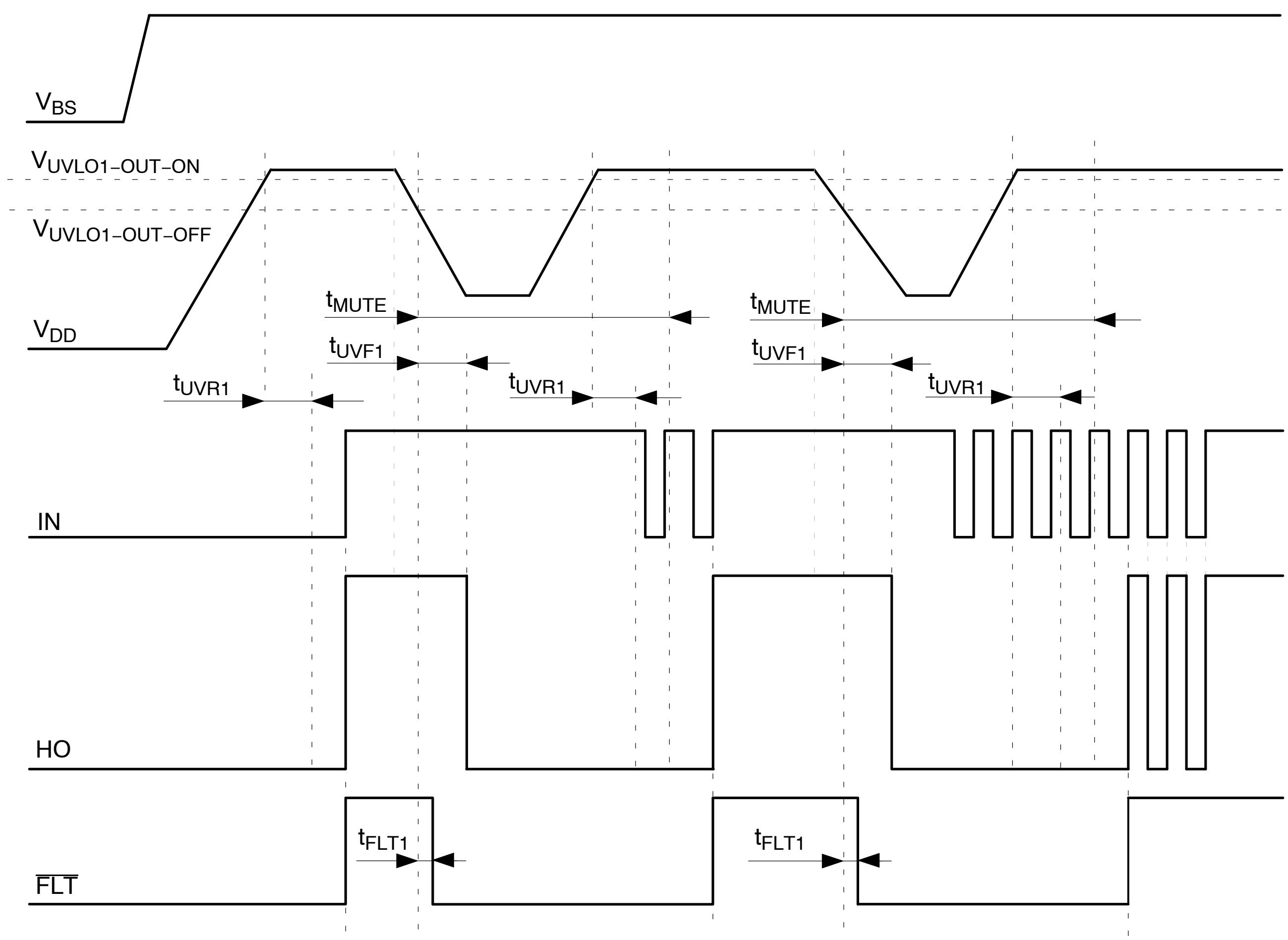


Figure 7. UVLO1 Waveform

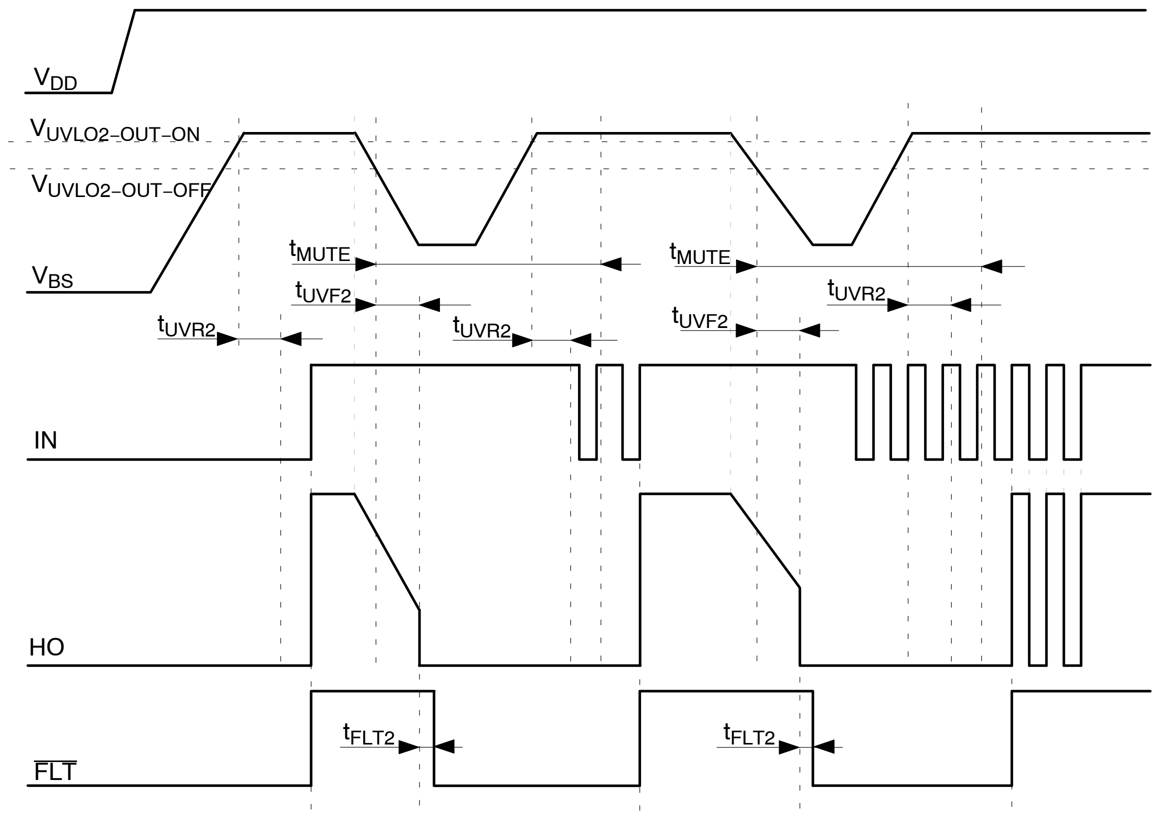


Figure 8. UVLO2 Waveform

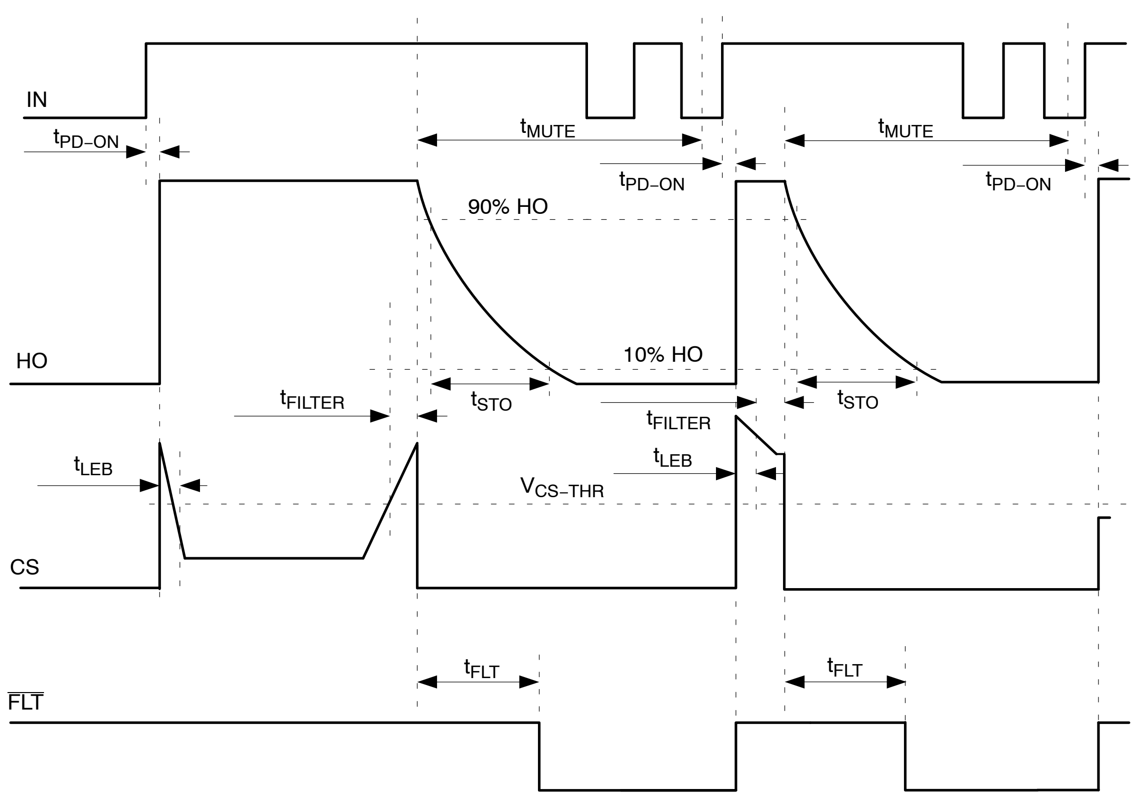


Figure 9. CS Response Waveform Using IGBT Vce

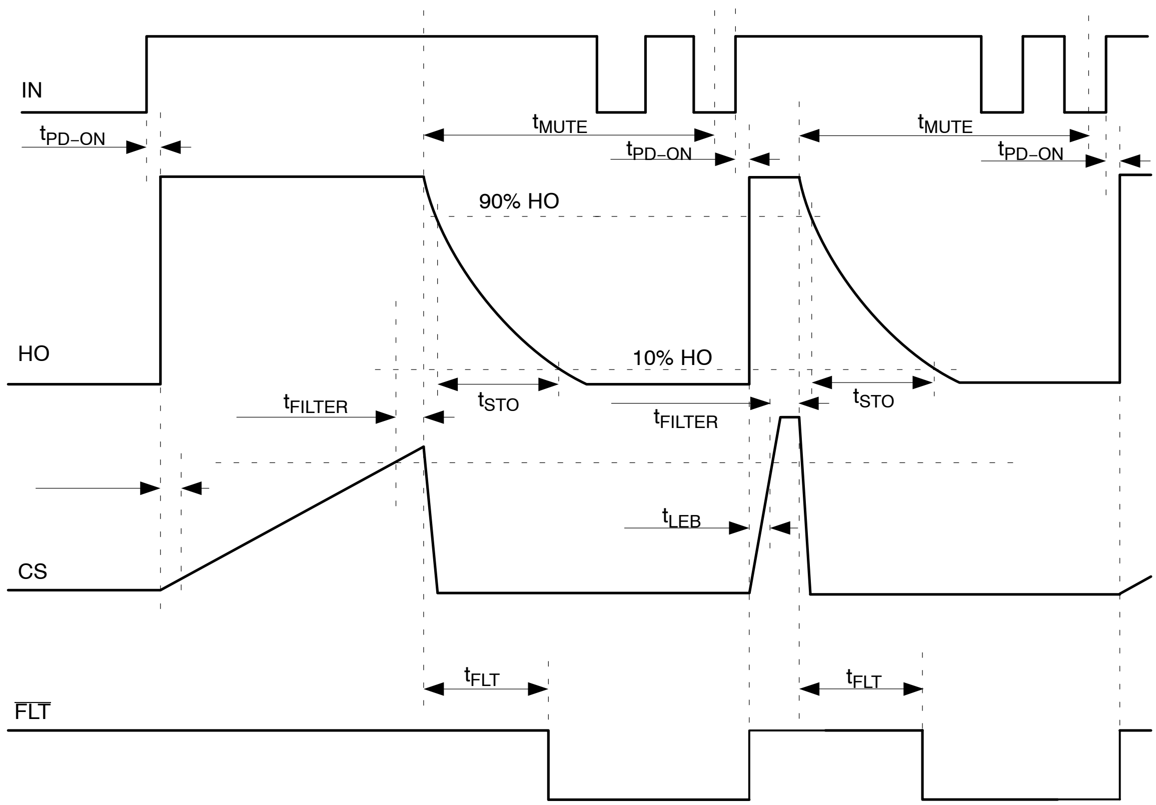


Figure 10. CS Response Waveform Using Shunt Resistor

TRUTH TABLE

IN	UVLO1	UVLO2	CS	HO	$\overline{FLT}$	Notes
H	Inactive	Inactive	L	L	L	Initial condition after power up V_{DD} and V_{BS}
↗	Inactive	Inactive	L	↗	↗	Initial condition – IN First Rising edge
H	Inactive	Inactive	L	H	H	Normal Operation – Output High
↘	Inactive	Inactive	L	↘	H	Normal Operation – Turn off Output
L	Inactive	Inactive	L	L	H	Normal Operation – Output Low
X	Active	Inactive	X	L	L	UVLO1 Activated – FLT Low (t_{FLT1}), Output Low
↗	Inactive	Inactive	L	↗	↗	FLT reset, UVLO1 conditions disappear
X	Inactive	Active	X	L	L	UVLO2 Activated – FLT Low (t_{FLT1}), Output Low
↗	Inactive	Inactive	L	↗	↗	FLT reset, UVLO2 conditions disappear
H	Inactive	Inactive	H (>t_{FILTER})	L	L	CS Activated – FLT Low (tFLT), Output Low
↗	Inactive	Inactive	L	↗	↗	FLT reset, CS conditions disappear

ORDERING INFORMATION

Device	Package	Shipping†
NCD57085DR2G	SOIC−8 Narrow Body, (Pb−Free)	2500 / Tape & Reel
NCV57085DR2G	SOIC−8 Narrow Body, (Pb−Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

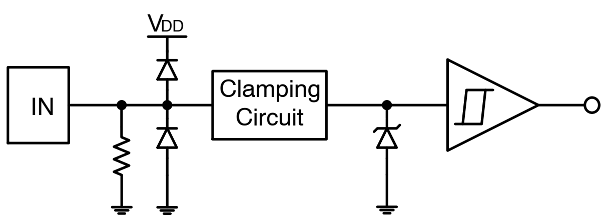
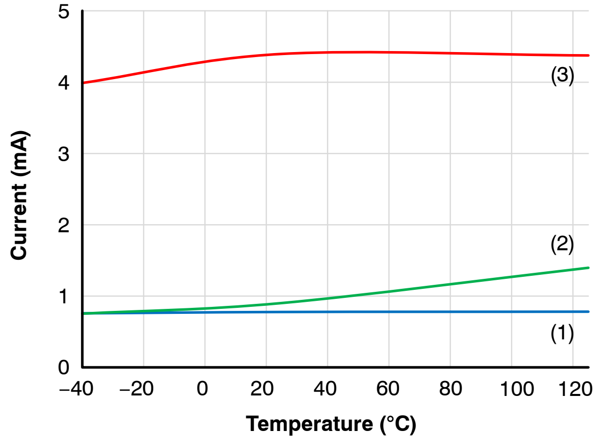


Figure 11. Input Pin Structure

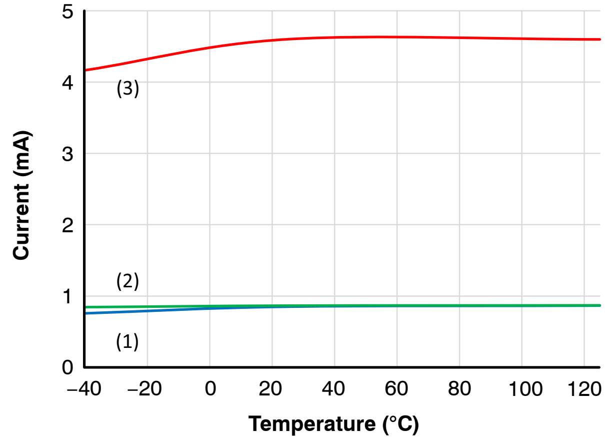
TYPICAL CHARACTERISTICS



(1) $I_{DD-0-3.3}$, I_N = 0 V
(2) $I_{DD-50-3.3}$, I_N = 3.3 V/1 MHz/50%,
(3) $I_{DD-100-3.3}$, I_N = 3.3 V

(Note: V_{DD} = 3.3 V, V_B = 15 V

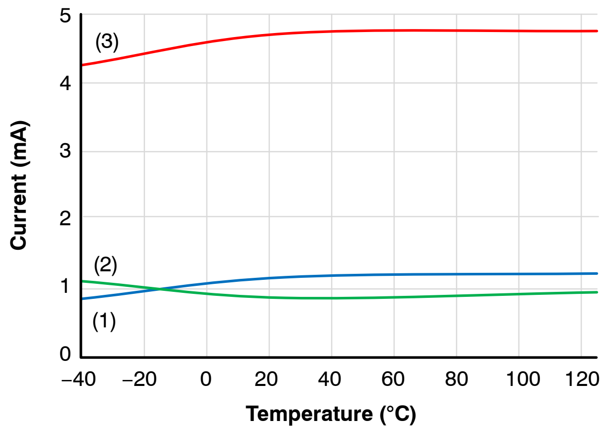
Figure 12. I_{DD} Supply Current, V_{DD} = 3.3 V



(1) I_{DD-0-5}, I_N = 0 V
(2) $I_{DD-50-5}$, I_N = 5 V/1 MHz/50%,
(3) $I_{DD-1000-5}$, I_N = 5 V

(Note: V_{DD} = 5 V, V_B = 15 V)

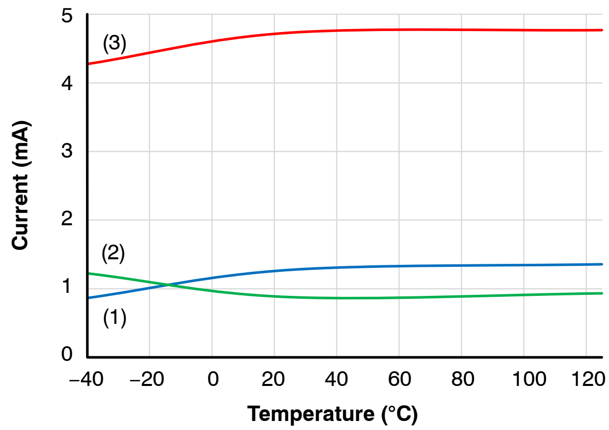
Figure 13. I_{DD} Supply Current, V_{BS} = 5 V



(1) $I_{DD-0-15}$, I_N = 0 V
(2) $I_{DD-50-15}$, I_N = 5 V/1 MHz/50%,
(3) $I_{DD-100-15}$, I_N = 5 V

(Note: V_{DD} = 15 V, V_B = 15 V)

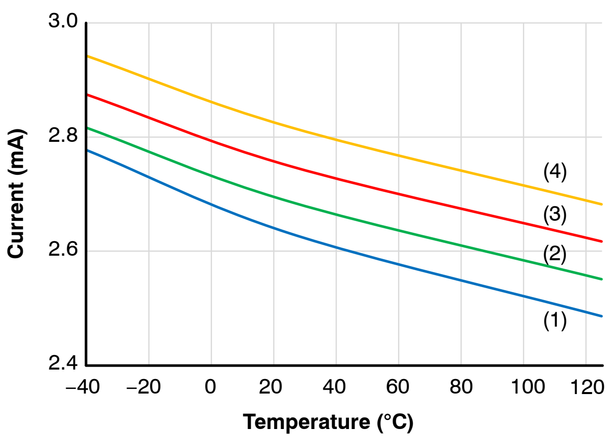
Figure 14. I_{DD} Supply Current, V_{DD} = 15 V



(1) $I_{DD-0-20}$, I_N = 0 V
(2) $I_{DD-50-20}$, I_N = 5 V/1 MHz/50%,
(3) $I_{DD-100-20}$, I_N = 5 V

(Note: V_{DD} = 20 V, V_B = 15 V)

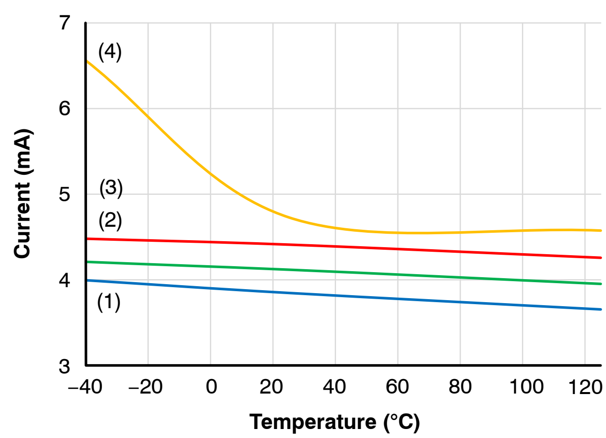
Figure 15. I_{DD} Supply Current, V_{DD} = 20 V



(1) $I_{BS-0-15}$, V_B = 15 V
(2) $I_{BS-0-20}$, V_B = 20 V
(3) $I_{BS-0-25}$, V_B = 25 V
(4) $I_{BS-0-30}$, V_B = 30 V

(Note: V_{DD} = 5 V, I_N = LOW, $\overline{FLT}$ = HIGH)

Figure 16. I_{BS} Supply Current, V_{DD} = 5 V

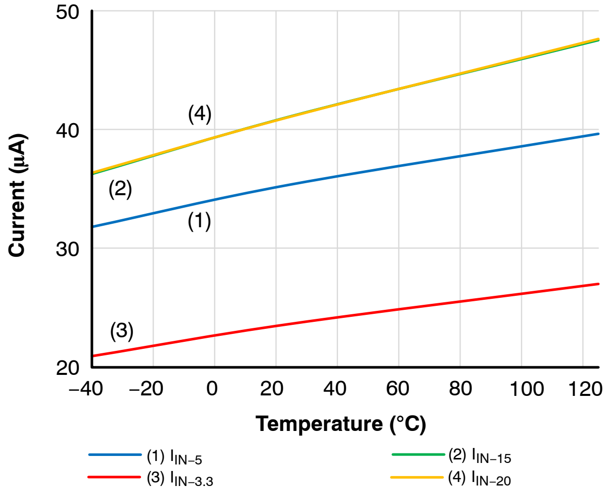


(1) $I_{BS-100-15}$, V_B = 15 V
(2) $I_{BS-100-20}$, V_B = 20 V
(3) $I_{BS-100-25}$, V_B = 25 V
(4) $I_{BS-100-30}$, V_B = 30 V

(Note: V_{DD} = 5 V, I_N = HIGH, $\overline{FLT}$ = HIGH)

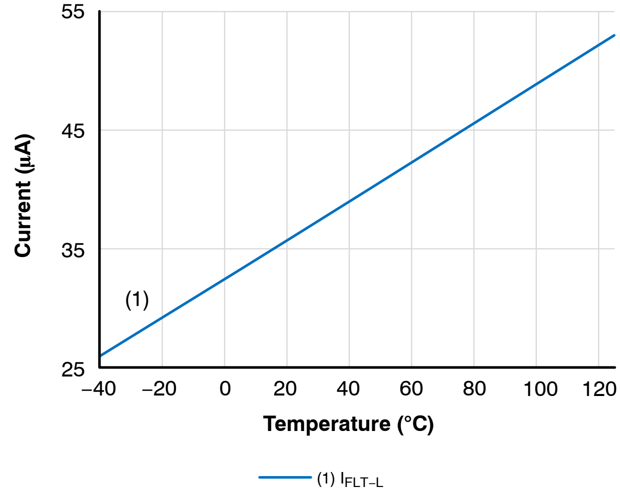
Figure 17. I_{BS} Supply Current, V_{DD} = 5 V

TYPICAL CHARACTERISTICS (continued)



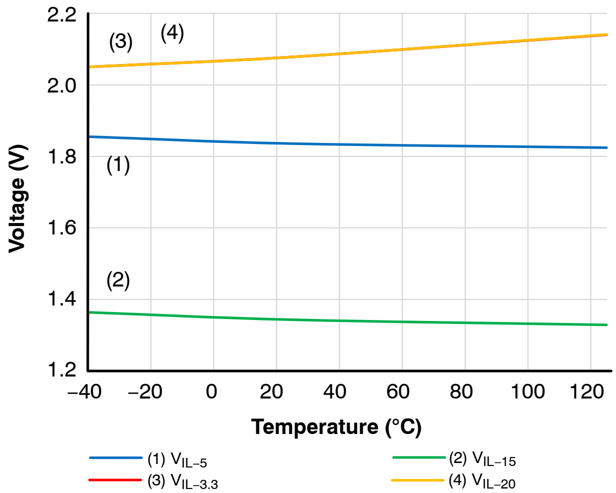
(Note: $V_{IN} = V_{DD}$, V_{BS} = 15 V)

Figure 18. Input Current – Logic "1"



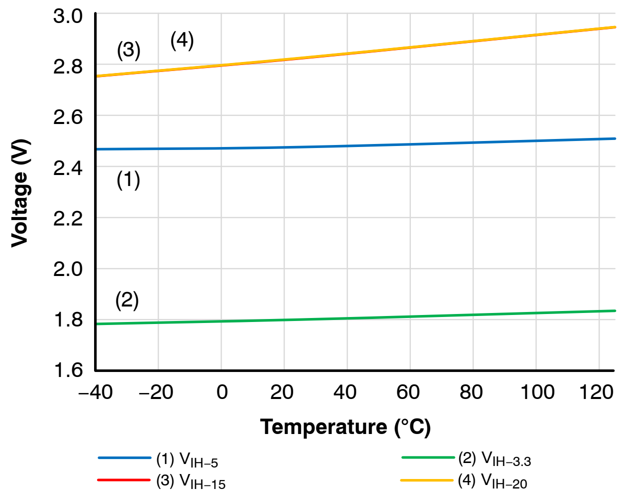
(Note: FLT = LOW, V_{DD} = 5 V)

Figure 19. FLT = Pull−up Current



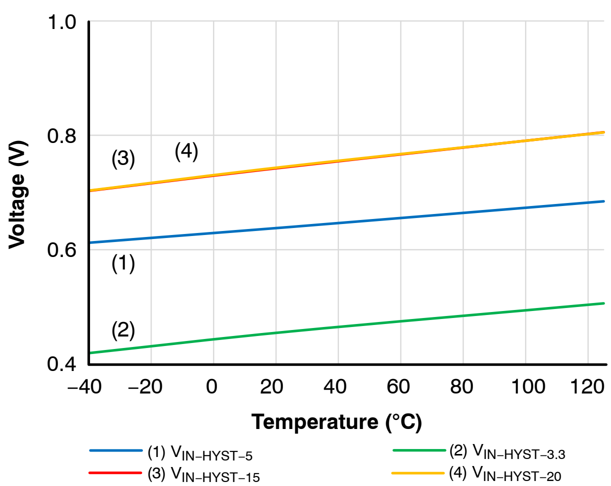
(Note: V_{BS} = 15 V)

Figure 20. Low Input Voltage



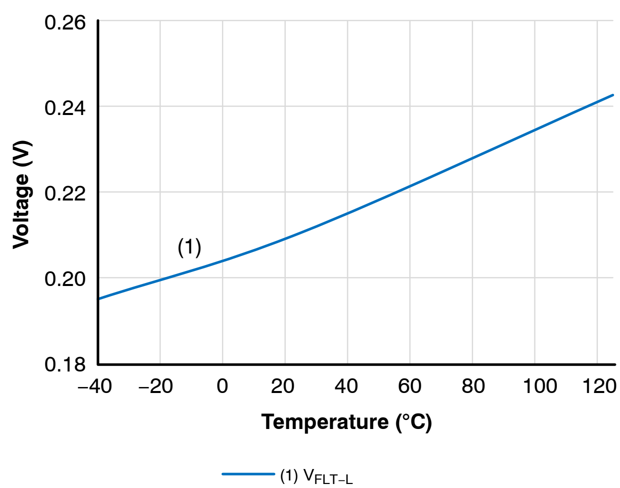
(Note: V_{BS} = 15 V)

Figure 21. High Input Voltage



(Note: V_{BS} = 15 V)

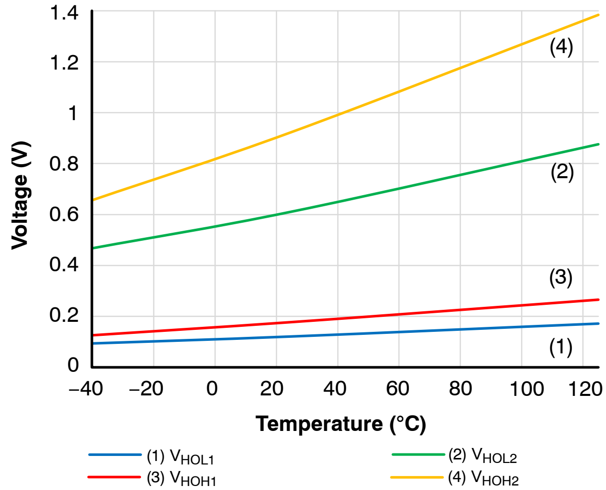
Figure 22. Input Hysteresis Voltage



(Note: I_{FLT} = 5 mA)

Figure 23. FLT Low Level Output Voltage

TYPICAL CHARACTERISTICS (continued)



(Note: V_{DD} = 5 V, V_{BS} = 15 V)

Figure 24. Output Voltage

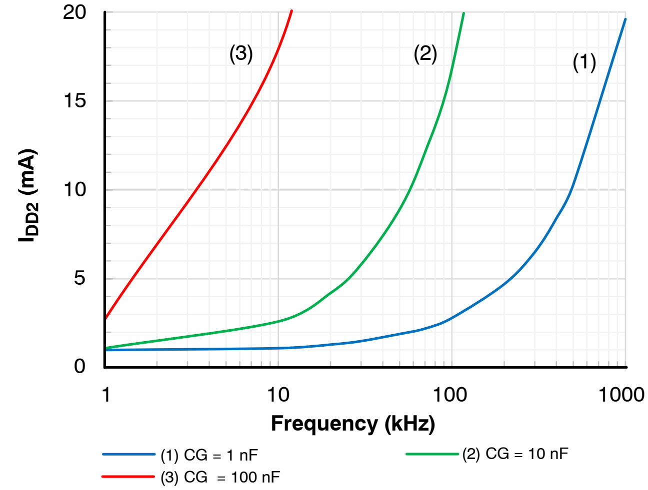


Figure 25. I_{BS} vs Switching Frequency

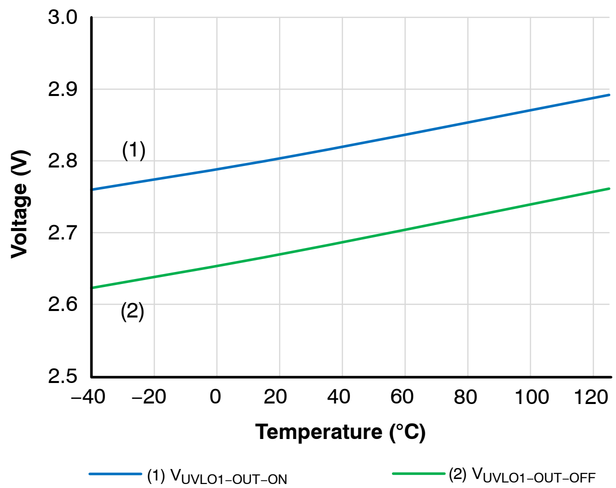


Figure 26. UVLO1 Threshold Voltage

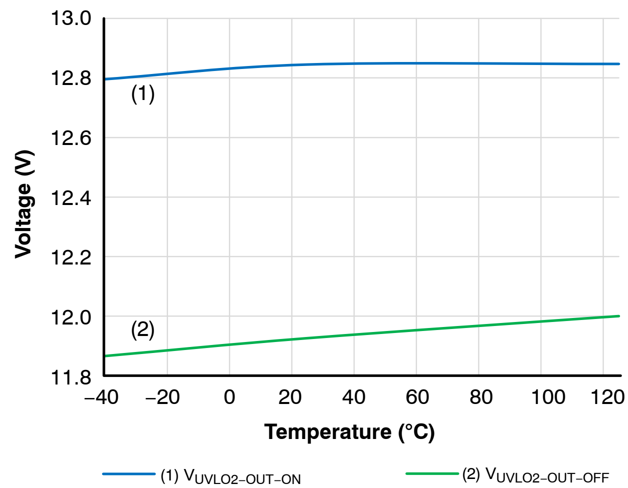


Figure 27. UVLO2 Threshold Voltage

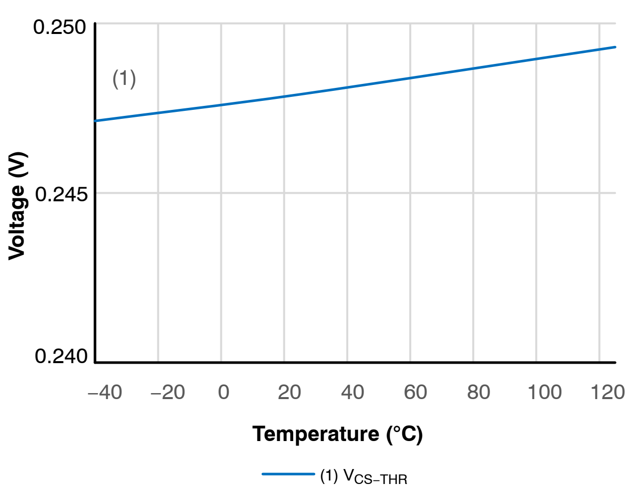


Figure 28. CS Threshold Voltage

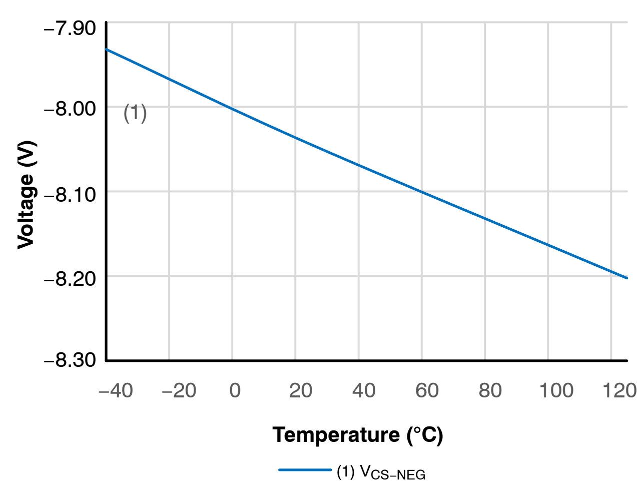


Figure 29. CS Negative Voltage

TYPICAL CHARACTERISTICS (continued)

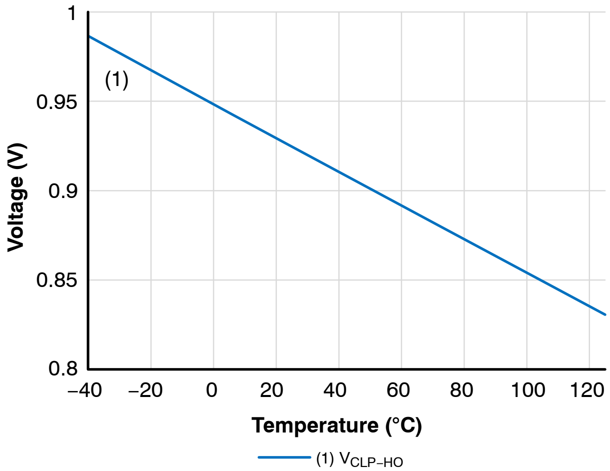
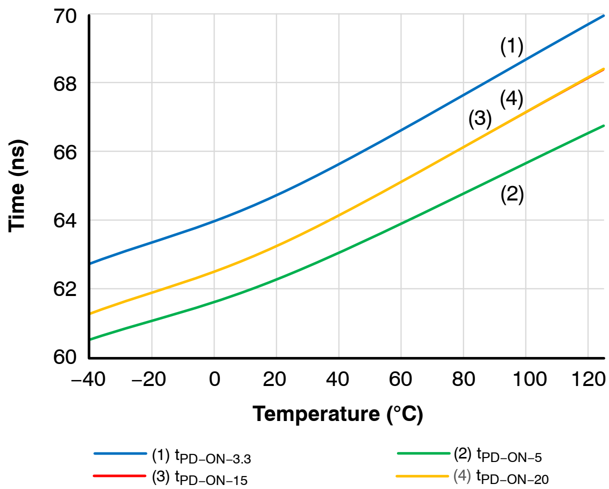
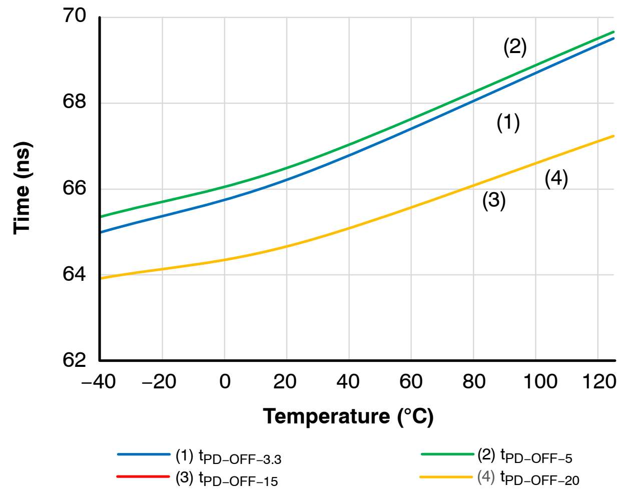


Figure 30. IGBT Short Circuit Clamping Voltage



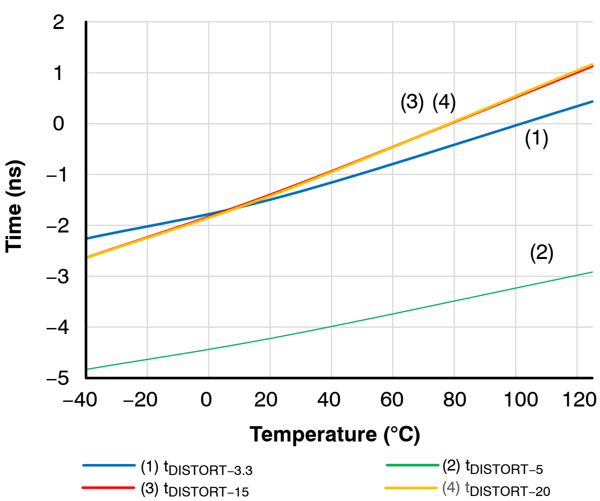
(Note: C_{LOAD} = 10 nF, V_{BS} = 15 V)

Figure 31. High Propagation Delay



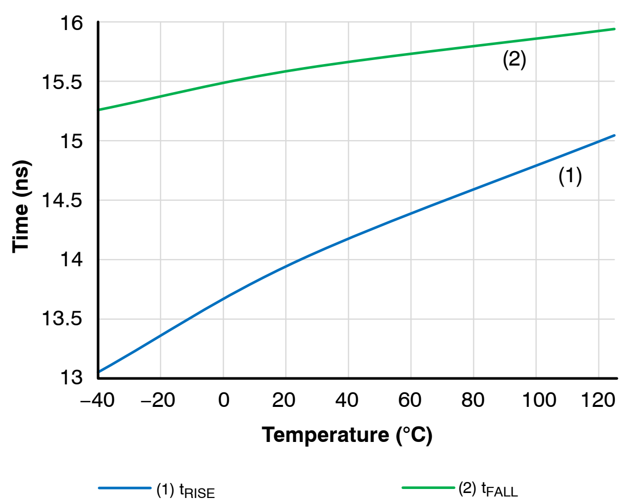
(Note: C_{LOAD} = 10 nF, V_{BS} = 15 V)

Figure 32. Low Propagation Delay



(Note: V_{BS} = 15 V)

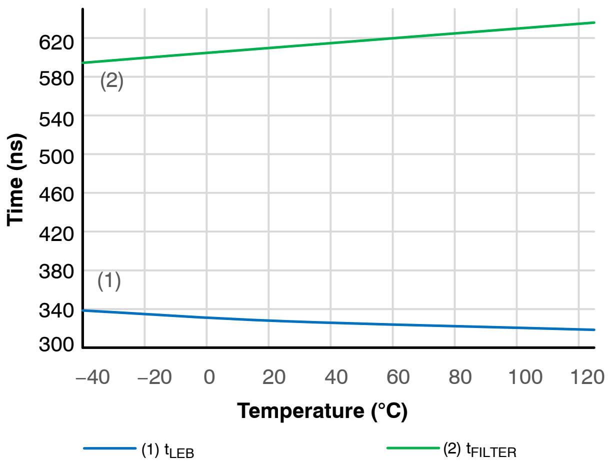
Figure 33. Propagation Delay Distortion



(Note: C_{LOAD} = 1 nF, V_{BS} = 15 V)

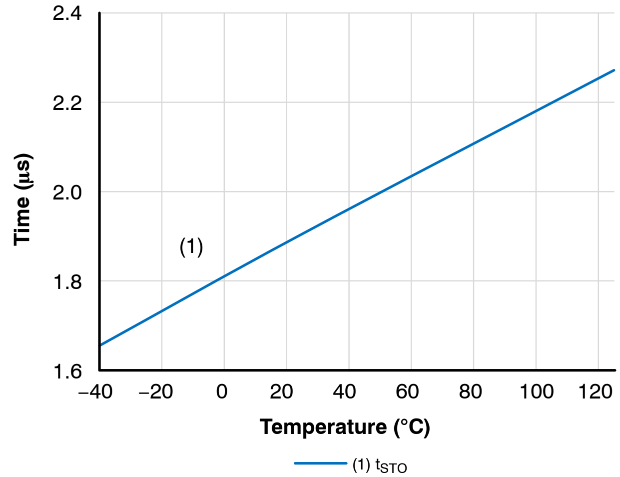
Figure 34. Rise / Fall Time

TYPICAL CHARACTERISTICS (continued)



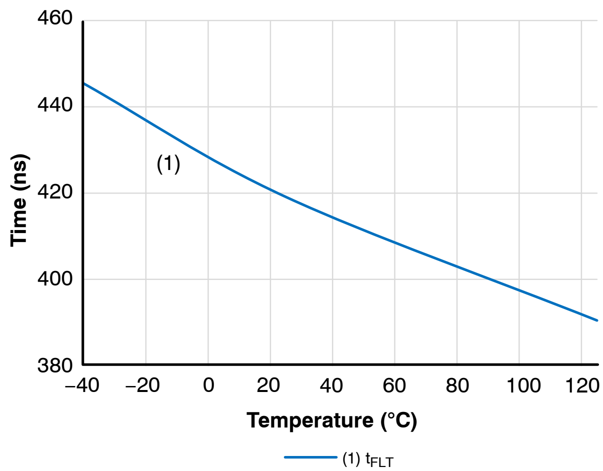
(Note: V_{DD} = 5 V, V_{BS} = 15 V)

Figure 35. CS Threshold Filtering Time, CS Leading Edge Blanking Time



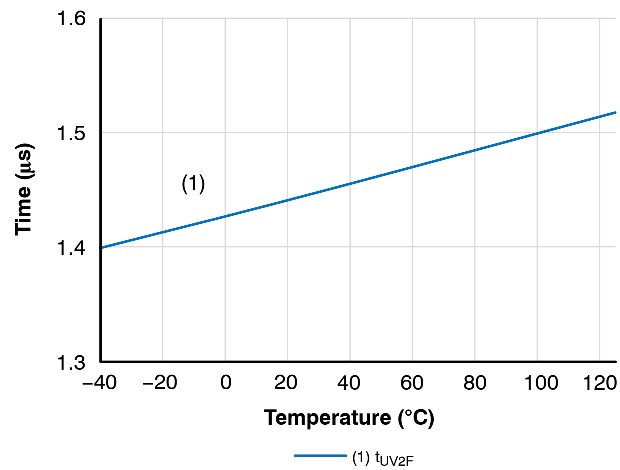
(Note: V_{DD} = 5 V, V_{BS} = 15 V)

Figure 36. Soft Turn Off Time



(Note: V_{DD} = 5 V, V_{BS} = 15 V)

Figure 37. FLT Delay Time



(Note: V_{DD} = 5 V, V_{BS} falls from HI to LOW)

Figure 38. UVLO2 Fall Delay

Under Voltage Lockout (UVLO)

UVLO ensures correct switching of IGBT connected to the driver output.

- The IGBT is turned−off and the output is disabled, if the supply V_{DD} drops below $V_{UVLO1-OUT-OFF}$ or V_{BS} drops below $V_{UVLO2-OUT-OFF}$.
- The driver output does not follow the input signal on V_{IN} until the V_{DD} / V_{BS} rises above the $V_{UVLOX-OUT-ON}$ and the input signal rising edge is applied to the V_{IN}.

With high loading gate capacitances over 10 nF it is important to follow the decoupling capacitor routing guidelines as shown on Figure 41. The decoupling capacitor value should be at least 10 μF. Also gate resistor of minimal value of 2 Ω has to be used in order to avoid interference of the high di/dt with internal circuitry (e.g. UVLO2).

After the power−on of the driver there has to be a rising edge applied to the IN in order for the output to start following the inputs. This serves as a protection against producing partial pulses at the output if the V_{DD} or V_B is applied in the middle of the input PWM pulse.

Power Supply (V_{DD}, V_{BS})

NCx57085 is designed to support unipolar power supply.

For reliable high output current the suitable external power capacitors required. Parallel combination of 100 nF + 4,7 μF ceramic capacitors is optimal for a wide range of applications using IGBT. For reliable driving IGBT modules (containing several parallel IGBT's) a higher capacity required (typically 100 nF + 10 μF). Capacitors should be as close as possible to the driver's power pins.

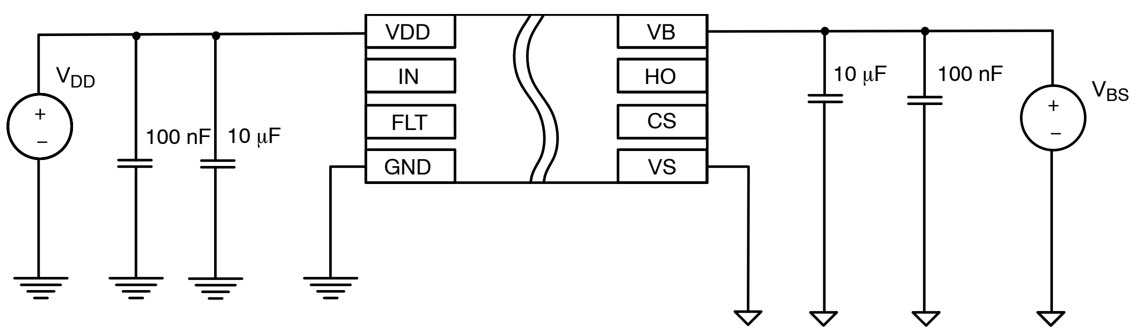
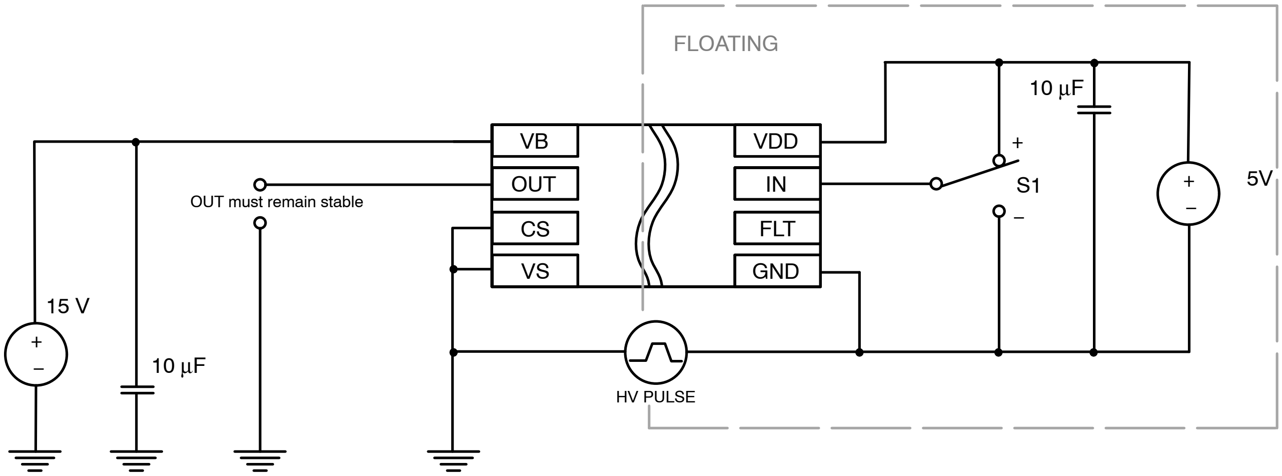


Figure 39. Power Supply

Current Sense (CS)

Current sense protection ensures the protection of IGBT at over current. When the V_{CESAT} or V_{SHUTN} voltage goes up and reaches the set limit, the output is driven low and FLT output is activated. To avoid false CS triggering , all CS circuit parts should be placed as close as possible to CS pin and wires from detecting circuit (V_{CESAT} or R_{SHUNT}) should be routed directly and without approaching the power paths.



(Test Conditions: HV Pulse ±1500 V, dV/dt = 1–100 V/ns, V_{DD} = 5 V, V_{BS} = 15 V)

Figure 40. CMTI Test Setup

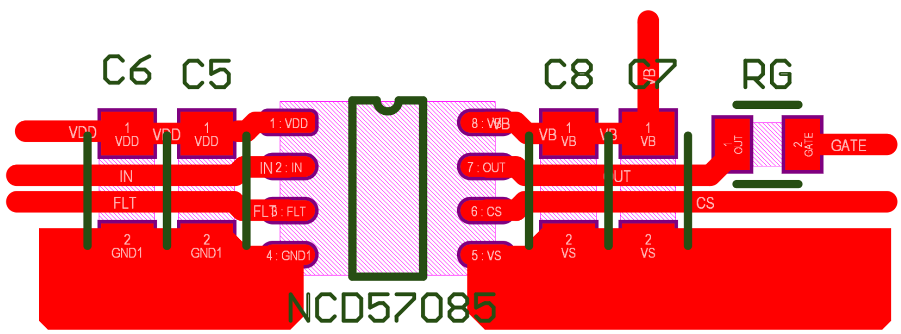


Figure 41. Recommended Layout

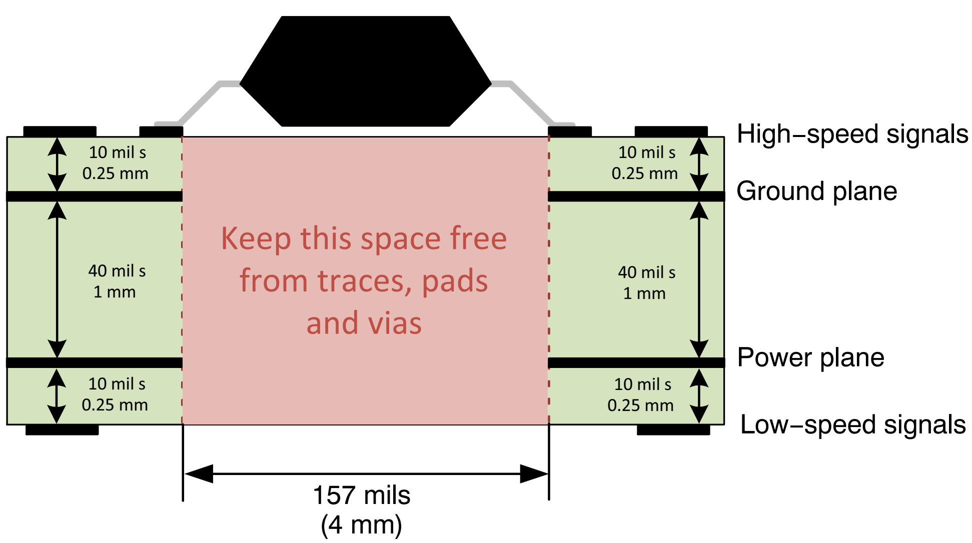
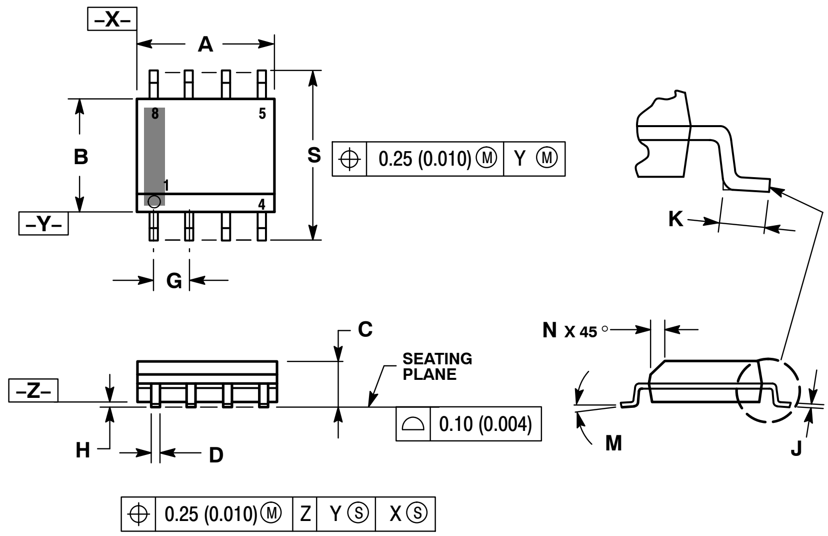


Figure 42. Recommended Layer Stack

PACKAGE DIMENSIONS

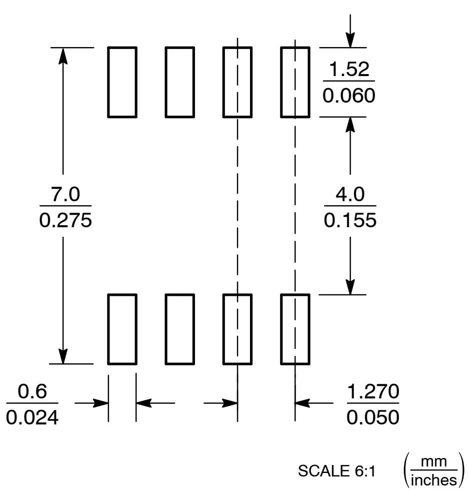
SOIC−8 NB
CASE 751−07
ISSUE AK



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

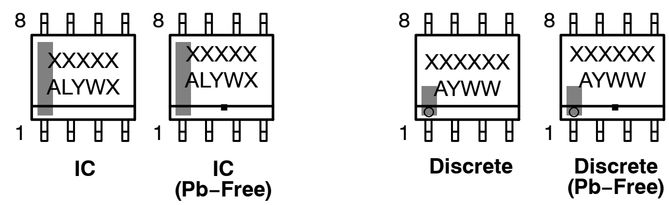
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0 °	8 °	0 °	8 °
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

SOIC−8 NB
CASE 751−07
ISSUE AK

DATE 16 FEB 2011

STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. COLLECTOR
4. EMITTER
5. EMITTER
6. BASE
7. BASE
8. EMITTER

STYLE 2:
PIN 1. COLLECTOR, DIE, #1
2. COLLECTOR, #1
3. COLLECTOR, #2
4. COLLECTOR, #2
5. BASE, #2
6. EMITTER, #2
7. BASE, #1
8. EMITTER, #1

STYLE 3:
PIN 1. DRAIN, DIE #1
2. DRAIN, #1
3. DRAIN, #2
4. DRAIN, #2
5. GATE, #2
6. SOURCE, #2
7. GATE, #1
8. SOURCE, #1

STYLE 4:
PIN 1. ANODE
2. ANODE
3. ANODE
4. ANODE
5. ANODE
6. ANODE
7. ANODE
8. COMMON CATHODE

STYLE 5:
PIN 1. DRAIN
2. DRAIN
3. DRAIN
4. DRAIN
5. GATE
6. GATE
7. SOURCE
8. SOURCE

STYLE 6:
PIN 1. SOURCE
2. DRAIN
3. DRAIN
4. SOURCE
5. SOURCE
6. GATE
7. GATE
8. SOURCE

STYLE 7:
PIN 1. INPUT
2. EXTERNAL BYPASS
3. THIRD STAGE SOURCE
4. GROUND
5. DRAIN
6. GATE 3
7. SECOND STAGE Vd
8. FIRST STAGE Vd

STYLE 8:
PIN 1. COLLECTOR, DIE #1
2. BASE, #1
3. BASE, #2
4. COLLECTOR, #2
5. COLLECTOR, #2
6. EMITTER, #2
7. EMITTER, #1
8. COLLECTOR, #1

STYLE 9:
PIN 1. EMITTER, COMMON
2. COLLECTOR, DIE #1
3. COLLECTOR, DIE #2
4. EMITTER, COMMON
5. EMITTER, COMMON
6. BASE, DIE #2
7. BASE, DIE #1
8. EMITTER, COMMON

STYLE 10:
PIN 1. GROUND
2. BIAS 1
3. OUTPUT
4. GROUND
5. GROUND
6. BIAS 2
7. INPUT
8. GROUND

STYLE 11:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

STYLE 12:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 13:
PIN 1. N.C.
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 14:
PIN 1. N−SOURCE
2. N−GATE
3. P−SOURCE
4. P−GATE
5. P−DRAIN
6. P−DRAIN
7. N−DRAIN
8. N−DRAIN

STYLE 15:
PIN 1. ANODE 1
2. ANODE 1
3. ANODE 1
4. ANODE 1
5. CATHODE, COMMON
6. CATHODE, COMMON
7. CATHODE, COMMON
8. CATHODE, COMMON

STYLE 16:
PIN 1. EMITTER, DIE #1
2. BASE, DIE #1
3. EMITTER, DIE #2
4. BASE, DIE #2
5. COLLECTOR, DIE #2
6. COLLECTOR, DIE #2
7. COLLECTOR, DIE #1
8. COLLECTOR, DIE #1

STYLE 17:
PIN 1. VCC
2. V2OUT
3. V1OUT
4. TXE
5. RXE
6. VEE
7. GND
8. ACC

STYLE 18:
PIN 1. ANODE
2. ANODE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. CATHODE
8. CATHODE

STYLE 19:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. MIRROR 2
7. DRAIN 1
8. MIRROR 1

STYLE 20:
PIN 1. SOURCE (N)
2. GATE (N)
3. SOURCE (P)
4. GATE (P)
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 21:
PIN 1. CATHODE 1
2. CATHODE 2
3. CATHODE 3
4. CATHODE 4
5. CATHODE 5
6. COMMON ANODE
7. COMMON ANODE
8. CATHODE 6

STYLE 22:
PIN 1. I/O LINE 1
2. COMMON CATHODE/VCC
3. COMMON CATHODE/VCC
4. I/O LINE 3
5. COMMON ANODE/GND
6. I/O LINE 4
7. I/O LINE 5
8. COMMON ANODE/GND

STYLE 23:
PIN 1. LINE 1 IN
2. COMMON ANODE/GND
3. COMMON ANODE/GND
4. LINE 2 IN
5. LINE 2 OUT
6. COMMON ANODE/GND
7. COMMON ANODE/GND
8. LINE 1 OUT

STYLE 24:
PIN 1. BASE
2. EMITTER
3. COLLECTOR/ANODE
4. COLLECTOR/ANODE
5. CATHODE
6. CATHODE
7. COLLECTOR/ANODE
8. COLLECTOR/ANODE

STYLE 25:
PIN 1. VIN
2. N/C
3. REXT
4. GND
5. IOUT
6. IOUT
7. IOUT
8. IOUT

STYLE 26:
PIN 1. GND
2. dv/dt
3. ENABLE
4. ILIMIT
5. SOURCE
6. SOURCE
7. SOURCE
8. VCC

STYLE 27:
PIN 1. ILIMIT
2. OVLO
3. UVLO
4. INPUT+
5. SOURCE
6. SOURCE
7. SOURCE
8. DRAIN

STYLE 28:
PIN 1. SW_TO_GND
2. DASIC_OFF
3. DASIC_SW_DET
4. GND
5. V_MON
6. VBULK
7. VBULK
8. VIN

STYLE 29:
PIN 1. BASE, DIE #1
2. EMITTER, #1
3. BASE, #2
4. EMITTER, #2
5. COLLECTOR, #2
6. COLLECTOR, #2
7. COLLECTOR, #1
8. COLLECTOR, #1

STYLE 30:
PIN 1. DRAIN 1
2. DRAIN 1
3. GATE 2
4. SOURCE 2
5. SOURCE 1/DRAIN 2
6. SOURCE 1/DRAIN 2
7. SOURCE 1/DRAIN 2
8. GATE 1

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