

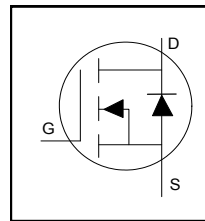
### Application

- Brushed Motor drive applications
- BLDC Motor drive applications
- Battery powered circuits
- Half-bridge and full-bridge topologies
- Synchronous rectifier applications
- Resonant mode power supplies
- OR-ing and redundant power switches
- DC/DC and AC/DC converters
- DC/AC Inverters

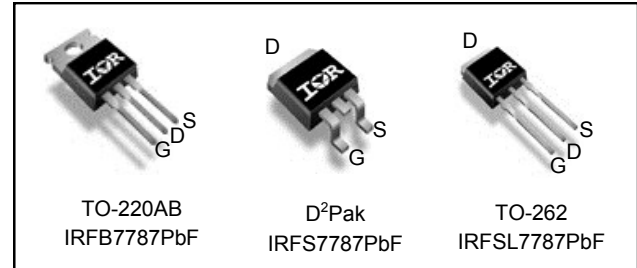
### Benefits

- Improved Gate, Avalanche and Dynamic dV/dt Ruggedness
- Fully Characterized Capacitance and Avalanche SOA
- Enhanced body diode dV/dt and dI/dt Capability
- Lead-Free, RoHS Compliant

HEXFET® Power MOSFET

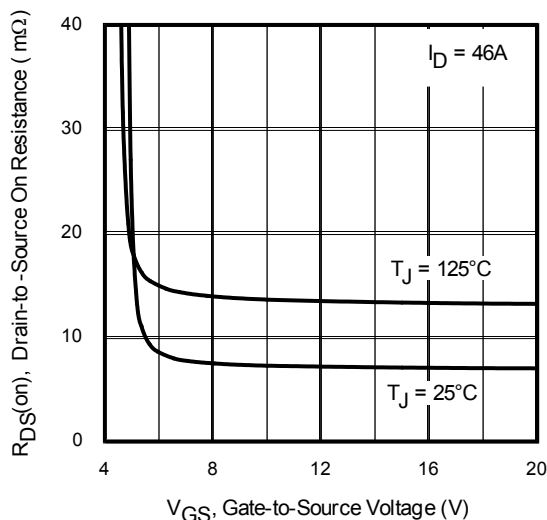


<b>V<sub>DSS</sub></b>	<b>75V</b>
<b>R<sub>DS(on)</sub> typ.</b>	<b>6.9mΩ</b>
	<b>8.4mΩ</b>
<b>I<sub>D</sub></b>	<b>76A</b>

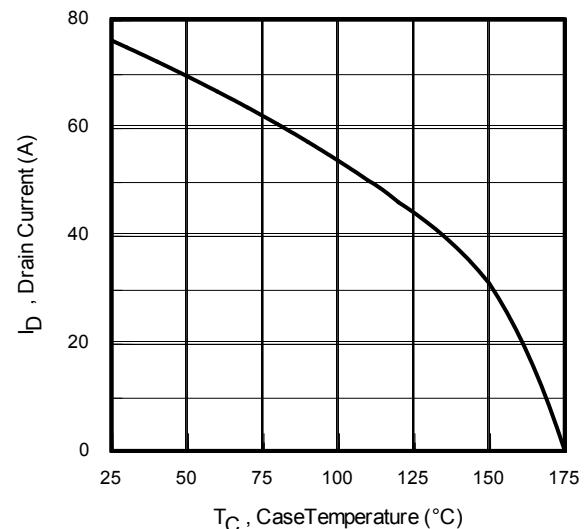


<b>G</b>	<b>D</b>	<b>S</b>
Gate	Drain	Source

Base part number	Package Type	Standard Pack		Orderable Part Number
		Form	Quantity	
IRFB7787PbF	TO-220	Tube	50	IRFB7787PbF
IRFSL7787PbF	TO-262	Tube	50	IRFSL7787PbF
IRFS7787PbF	D²-Pak	Tube	50	IRFS7787PbF
		Tape and Reel Left	800	IRFS7787TRLPbF



**Fig 1.** Typical On-Resistance vs. Gate Voltage



**Fig 2.** Maximum Drain Current vs. Case Temperature

**Absolute Maximum Rating**

Symbol	Parameter	Max.	Units
$I_D @ T_C = 25^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$	76	A
$I_D @ T_C = 100^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$	54	
$I_{DM}$	Pulsed Drain Current ②	280	
$P_D @ T_C = 25^\circ\text{C}$	Maximum Power Dissipation	125	W
	Linear Derating Factor	0.83	W/°C
$V_{GS}$	Gate-to-Source Voltage	$\pm 20$	V
$T_J$ $T_{STG}$	Operating Junction and Storage Temperature Range	-55 to + 175	°C
	Soldering Temperature, for 10 seconds (1.6mm from case)	300	
	Mounting Torque, 6-32 or M3 Screw	10 lbf-in (1.1 N·m)	

**Avalanche Characteristics**

$E_{AS}$ (Thermally limited)	Single Pulse Avalanche Energy ③	144	mJ
$E_{AS}$ (tested)	Single Pulse Avalanche Energy Tested Value ①	150	
$I_{AR}$	Avalanche Current ②	See Fig 15, 16, 23a, 23b	A
$E_{AR}$	Repetitive Avalanche Energy ②		mJ

**Thermal Resistance**

Symbol	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case ⑧	—	1.2	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat Greased Surface	0.50	—	
$R_{\theta JA}$	Junction-to-Ambient ⑧	—	62	

**Static @  $T_J = 25^\circ\text{C}$  (unless otherwise specified)**

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	75	—	—	V	$V_{GS} = 0\text{V}, I_D = 250\mu\text{A}$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.06	—	V/°C	Reference to $25^\circ\text{C}, I_D = 1\text{mA}$ ②
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	6.9	8.4	mΩ	$V_{GS} = 10\text{V}, I_D = 46\text{A}$
		—	8.2	—		$V_{GS} = 6.0\text{V}, I_D = 23\text{A}$
$V_{GS(th)}$	Gate Threshold Voltage	2.1	—	3.7	V	$V_{DS} = V_{GS}, I_D = 100\mu\text{A}$
$I_{DSS}$	Drain-to-Source Leakage Current	—	—	1.0	μA	$V_{DS} = 75\text{V}, V_{GS} = 0\text{V}$
		—	—	150		$V_{DS} = 75\text{V}, V_{GS} = 0\text{V}, T_J = 125^\circ\text{C}$
$I_{GSS}$	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 20\text{V}$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS} = -20\text{V}$
$R_G$	Gate Resistance	—	2.1	—	Ω	

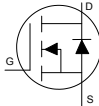
**Notes:**

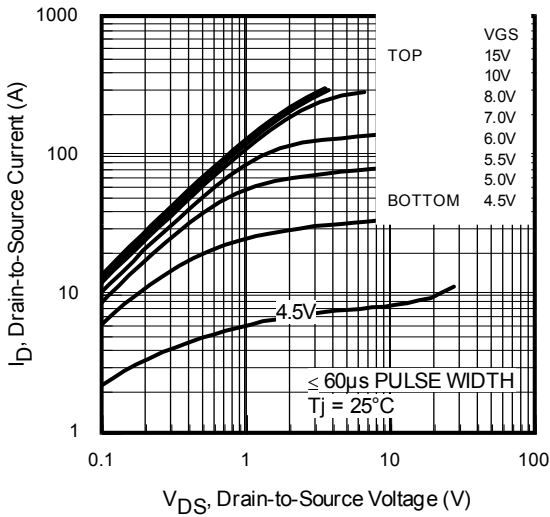
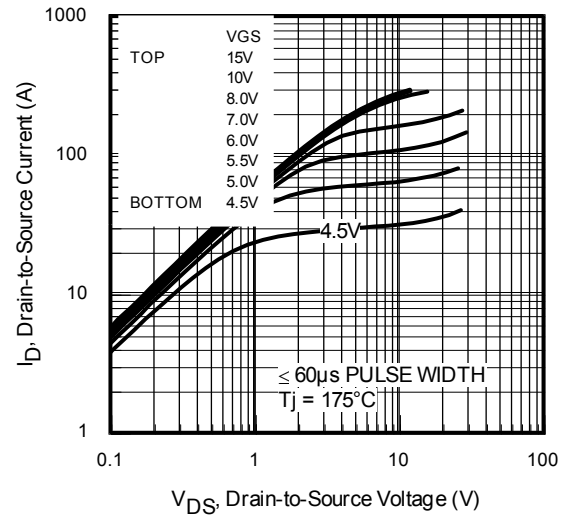
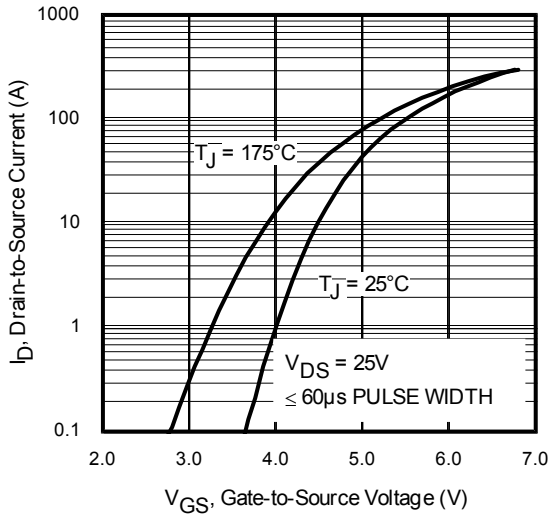
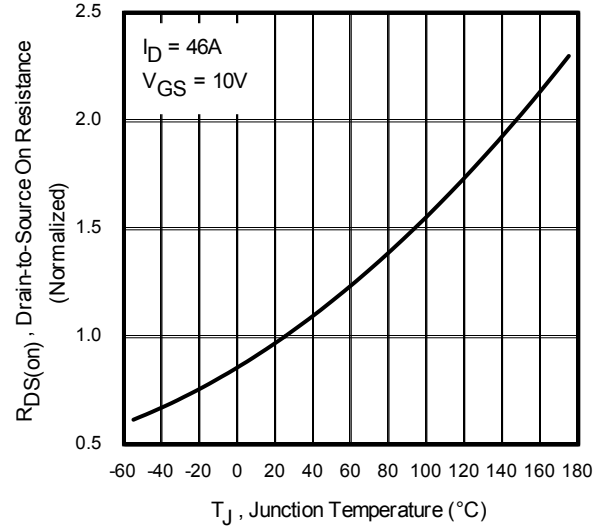
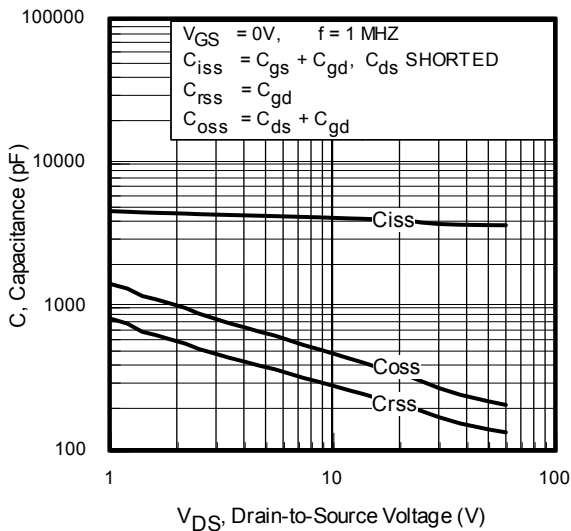
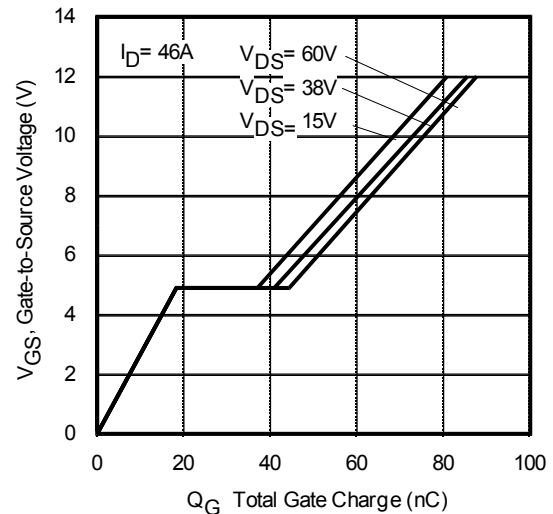
- ① This value determined from sample failure population, starting  $T_J = 25^\circ\text{C}$ ,  $L = 0.138\text{mH}$ ,  $R_G = 50\Omega$ ,  $I_{AS} = 46\text{A}$ ,  $V_{GS} = 10\text{V}$ .
- ② Repetitive rating; pulse width limited by max. junction temperature.
- ③ Limited by  $T_{Jmax}$ , starting  $T_J = 25^\circ\text{C}$ ,  $L = 0.138\text{mH}$ ,  $R_G = 50\Omega$ ,  $I_{AS} = 46\text{A}$ ,  $V_{GS} = 10\text{V}$ .
- ④  $I_{SD} \leq 46\text{A}$ ,  $di/dt \leq 425\text{A}/\mu\text{s}$ ,  $V_{DD} \leq V_{(BR)DSS}$ ,  $T_J \leq 175^\circ\text{C}$ .
- ⑤ Pulse width  $\leq 400\mu\text{s}$ ; duty cycle  $\leq 2\%$ .
- ⑥  $C_{oss}$  eff. (TR) is a fixed capacitance that gives the same charging time as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 80%  $V_{DSS}$ .
- ⑦  $C_{oss}$  eff. (ER) is a fixed capacitance that gives the same energy as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 80%  $V_{DSS}$ .
- ⑧  $R_\theta$  is measured at  $T_J$  approximately  $90^\circ\text{C}$ .

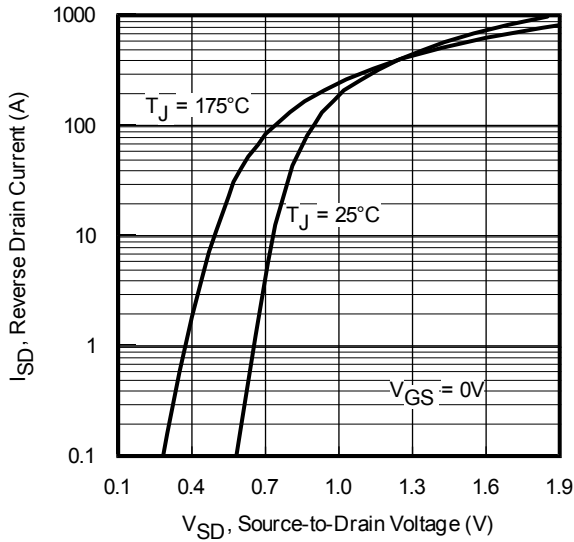
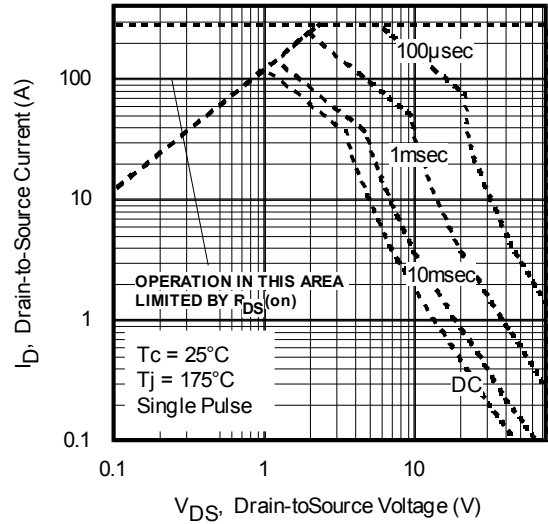
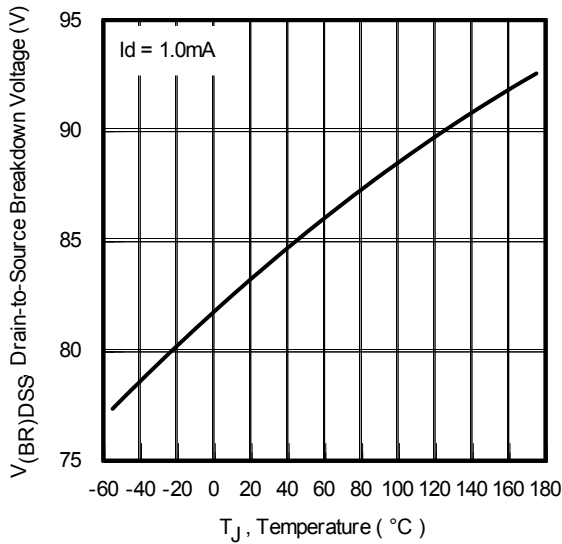
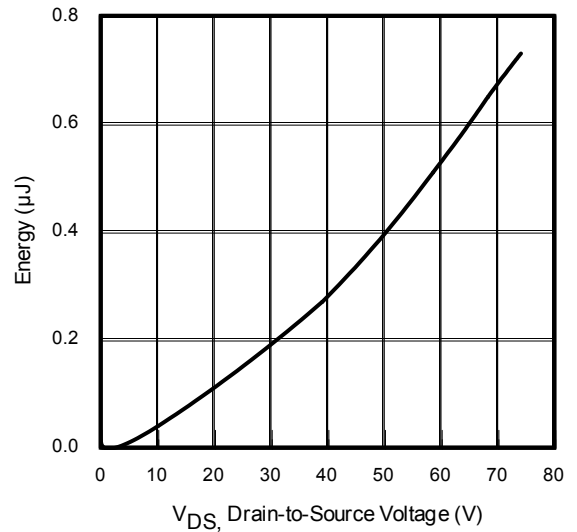
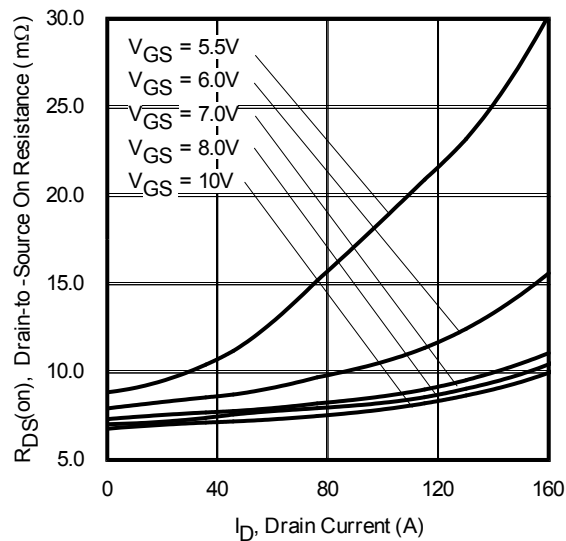
**Dynamic Electrical Characteristics @ T<sub>J</sub> = 25°C (unless otherwise specified)**

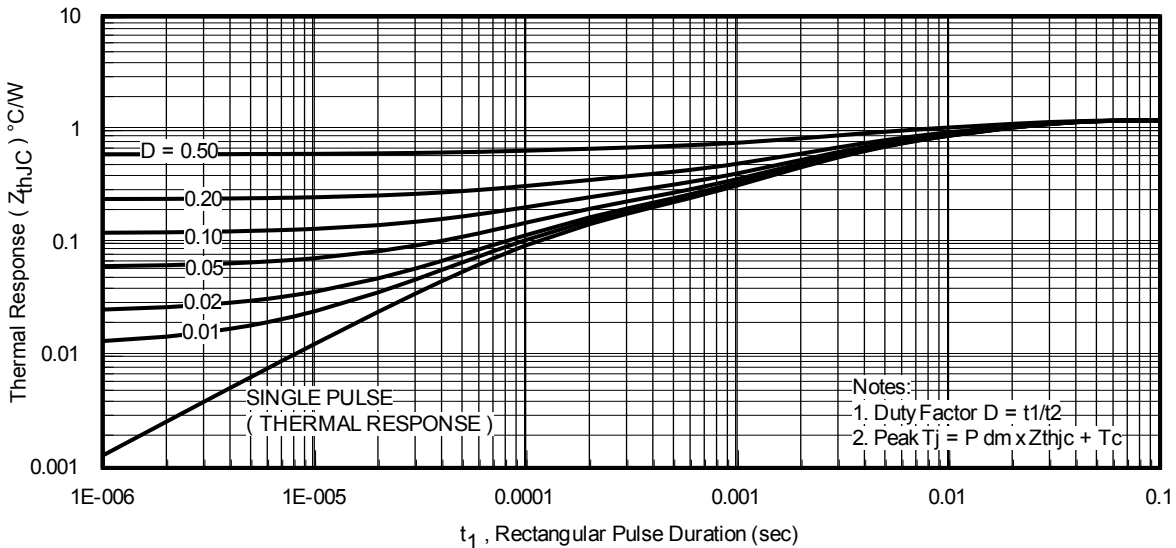
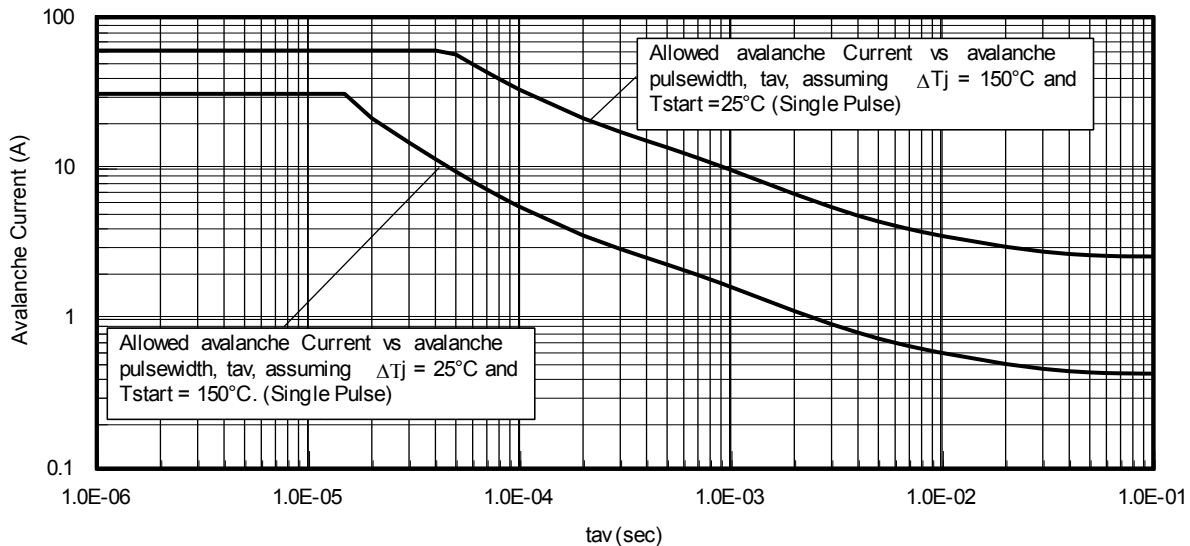
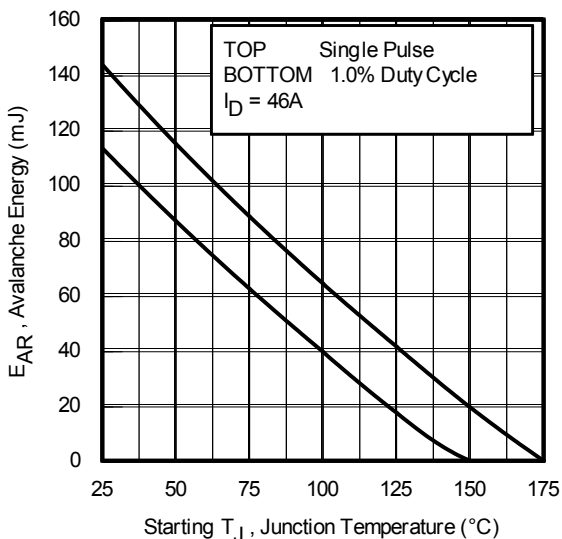
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g <sub>fs</sub>	Forward Transconductance	154	—	—	S	V <sub>DS</sub> = 10V, I <sub>D</sub> = 46A
Q <sub>g</sub>	Total Gate Charge	—	73	109	nC	I <sub>D</sub> = 46A V <sub>DS</sub> = 38V V <sub>GS</sub> = 10V
Q <sub>gs</sub>	Gate-to-Source Charge	—	18	—		
Q <sub>gd</sub>	Gate-to-Drain Charge	—	23	—		
Q <sub>sync</sub>	Total Gate Charge Sync. (Q <sub>g</sub> – Q <sub>gd</sub> )	—	50	—		
t <sub>d(on)</sub>	Turn-On Delay Time	—	11	—	ns	V <sub>DD</sub> = 38V I <sub>D</sub> = 46A R <sub>G</sub> = 2.7Ω V <sub>GS</sub> = 10V <sup>⑤</sup>
t <sub>r</sub>	Rise Time	—	48	—		
t <sub>d(off)</sub>	Turn-Off Delay Time	—	51	—		
t <sub>f</sub>	Fall Time	—	39	—		
C <sub>iss</sub>	Input Capacitance	—	4020	—	pF	V <sub>GS</sub> = 0V V <sub>DS</sub> = 25V f = 1.0MHz, See Fig.7 V <sub>GS</sub> = 0V, V <sub>DS</sub> = 0V to 60V <sup>⑦</sup> V <sub>GS</sub> = 0V, V <sub>DS</sub> = 0V to 60V <sup>⑥</sup>
C <sub>oss</sub>	Output Capacitance	—	330	—		
C <sub>riss</sub>	Reverse Transfer Capacitance	—	205	—		
C <sub>oss eff.(ER)</sub>	Effective Output Capacitance (Energy Related)	—	295	—		
C <sub>oss eff.(TR)</sub>	Output Capacitance (Time Related)	—	380	—		

**Diode Characteristics**

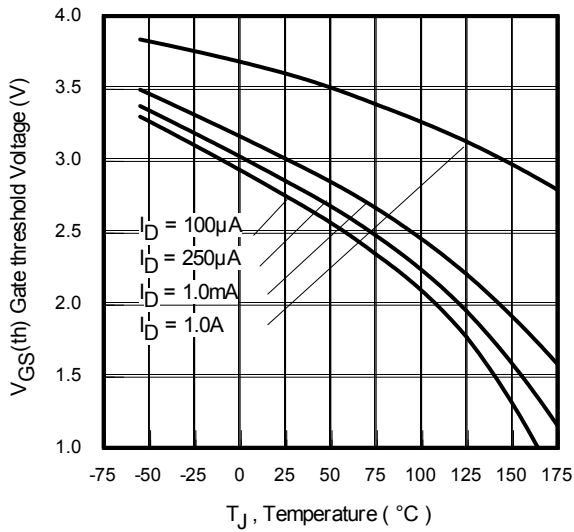
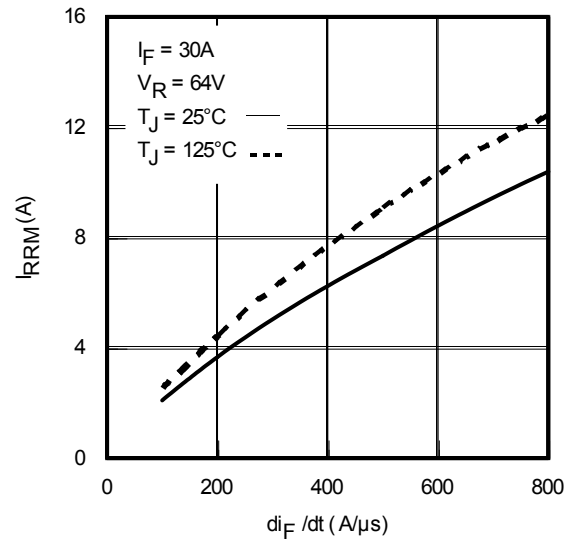
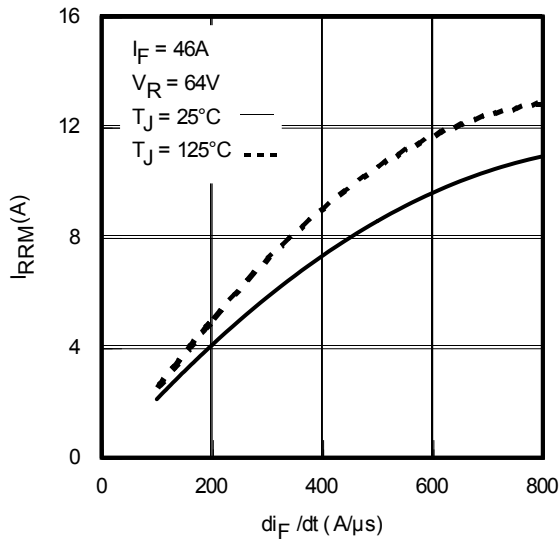
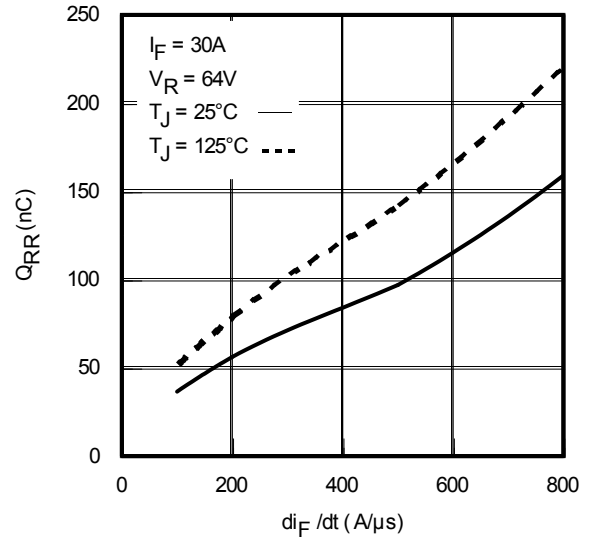
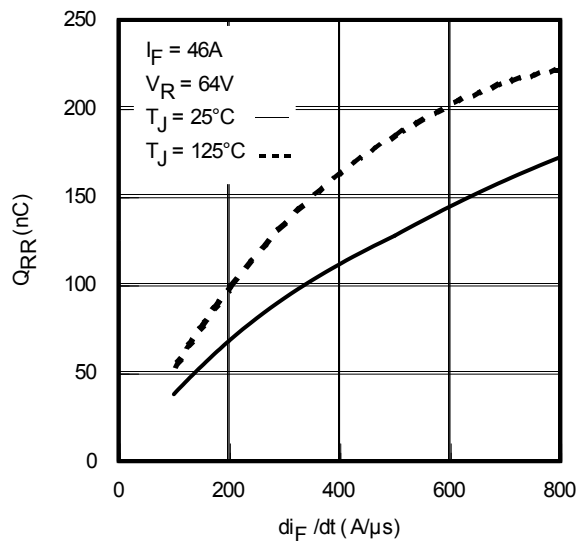
Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
I <sub>S</sub>	Continuous Source Current (Body Diode)	—	—	76	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I <sub>SM</sub>	Pulsed Source Current (Body Diode) <sup>②</sup>	—	—	280		
V <sub>SD</sub>	Diode Forward Voltage	—	—	1.2	V	T <sub>J</sub> = 25°C, I <sub>S</sub> = 46A, V <sub>GS</sub> = 0V <sup>⑤</sup>
dv/dt	Peak Diode Recovery dv/dt <sup>④</sup>	—	10	—	V/ns	T <sub>J</sub> = 175°C, I <sub>S</sub> = 46A, V <sub>DS</sub> = 75V <sup>⑤</sup>
t <sub>rr</sub>	Reverse Recovery Time	—	33	—	ns	T <sub>J</sub> = 25°C V <sub>DD</sub> = 64V
		—	39	—		T <sub>J</sub> = 125°C I <sub>F</sub> = 46A,
Q <sub>rr</sub>	Reverse Recovery Charge	—	42	—	nC	T <sub>J</sub> = 25°C di/dt = 100A/μs <sup>⑤</sup>
		—	61	—		T <sub>J</sub> = 125°C
I <sub>RRM</sub>	Reverse Recovery Current	—	2.2	—	A	T <sub>J</sub> = 25°C

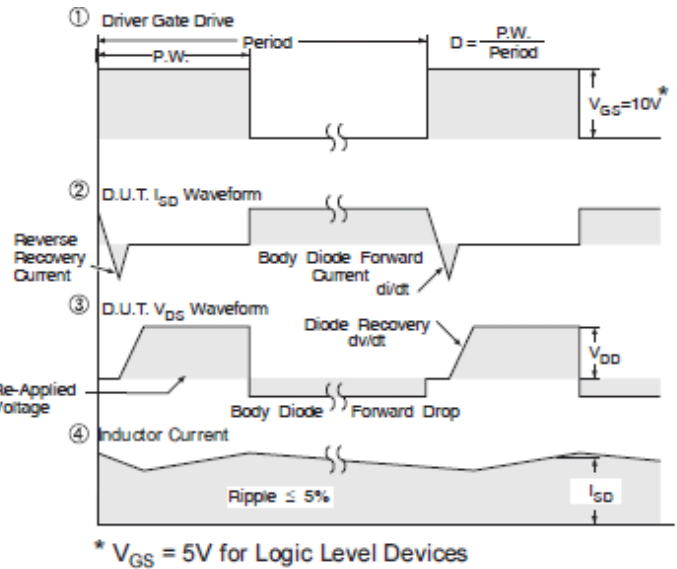
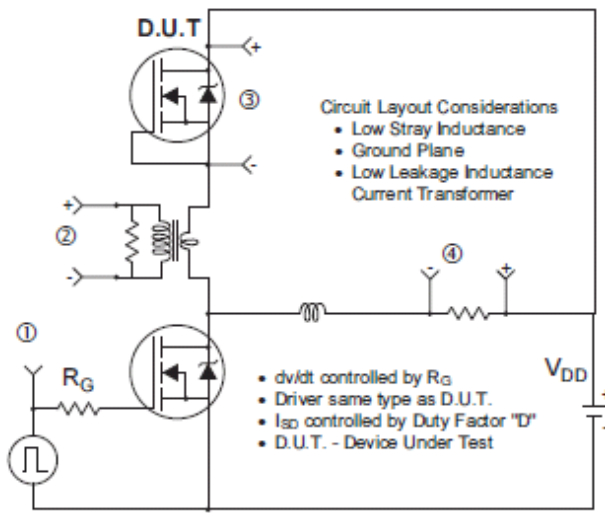
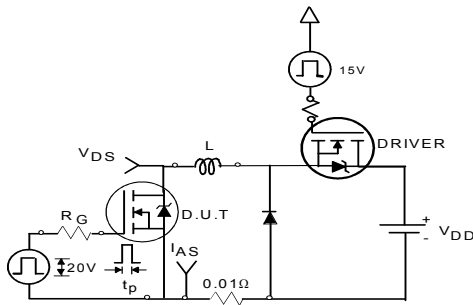
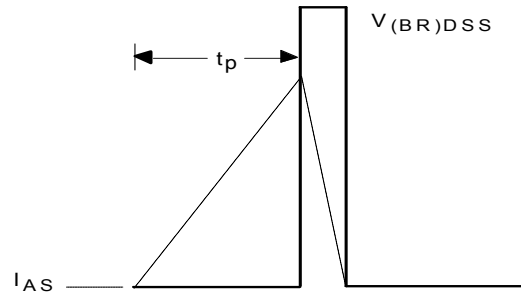
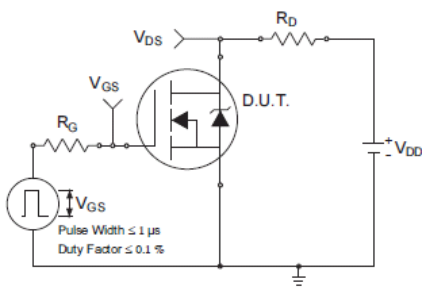
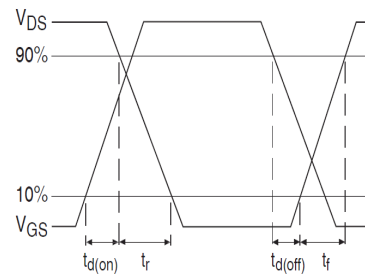
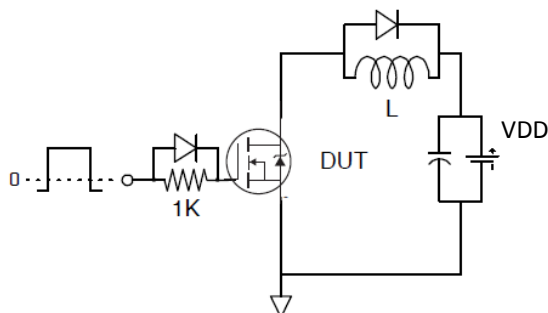
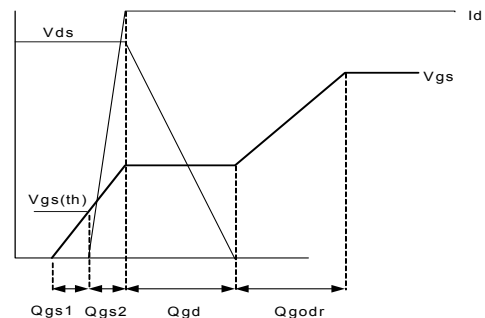

**Fig 3. Typical Output Characteristics**

**Fig 4. Typical Output Characteristics**

**Fig 5. Typical Transfer Characteristics**

**Fig 6. Normalized On-Resistance vs. Temperature**

**Fig 7. Typical Capacitance vs. Drain-to-Source Voltage**

**Fig 8. Typical Gate Charge vs. Gate-to-Source Voltage**


**Fig 9.** Typical Source-Drain Diode Forward Voltage

**Fig 10.** Maximum Safe Operating Area

**Fig 11.** Drain-to-Source Breakdown Voltage

**Fig 12.** Typical  $C_{oss}$  Stored Energy

**Fig 13.** Typical On-Resistance vs. Drain Current

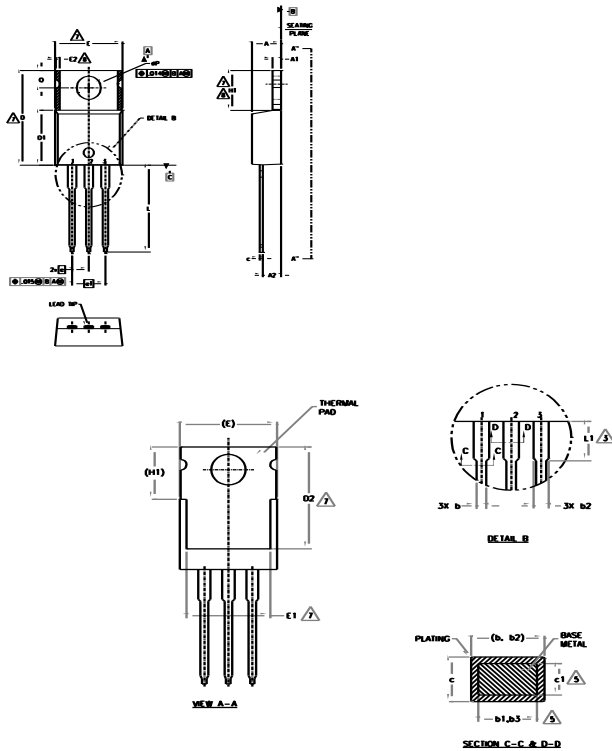

**Fig 14. Maximum Effective Transient Thermal Impedance, Junction-to-Case**

**Fig 15. Avalanche Current vs. Pulse Width**

**Fig 16. Maximum Avalanche Energy vs. Temperature**
**Notes on Repetitive Avalanche Curves , Figures 15, 16:  
(For further info, see AN-1005 at www.irf.com)**

1. Avalanche failures assumption:  
Purely a thermal phenomenon and failure occurs at a temperature far in excess of  $T_{jmax}$ . This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as  $T_{jmax}$  is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 23a, 23b.
4.  $P_{D(ave)}$  = Average power dissipation per single avalanche pulse.
5.  $BV$  = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6.  $I_{av}$  = Allowable avalanche current.
7.  $\Delta T$  = Allowable rise in junction temperature, not to exceed  $T_{jmax}$  (assumed as 25°C in Figure 15, 16).  
 $t_{av}$  = Average time in avalanche.  
 $D$  = Duty cycle in avalanche =  $t_{av} \cdot f$   
 $Z_{thJC}(D, t_{av})$  = Transient thermal resistance, see Figures 14)  
 $P_{D(ave)} = 1/2 ( 1.3 \cdot BV \cdot I_{av} ) = \Delta T / Z_{thJC}$   
 $I_{av} = 2\Delta T / [ 1.3 \cdot BV \cdot Z_{th} ]$   
 $E_{AS(AR)} = P_{D(ave)} \cdot t_{av}$


**Fig 17.** Threshold Voltage vs. Temperature

**Fig 18.** Typical Recovery Current vs. dif/dt

**Fig 19.** Typical Recovery Current vs. dif/dt

**Fig 20.** Typical Stored Charge vs. dif/dt

**Fig 21.** Typical Stored Charge vs. dif/dt


**Fig 22. Peak Diode Recovery  $dv/dt$  Test Circuit for N-Channel HEXFET® Power MOSFETs**

**Fig 23a. Unclamped Inductive Test Circuit**

**Fig 23b. Unclamped Inductive Waveforms**

**Fig 24a. Switching Time Test Circuit**

**Fig 24b. Switching Time Waveforms**

**Fig 25a. Gate Charge Test Circuit**

**Fig 25b. Gate Charge Waveform**



**TO-220AB Package Outline** (Dimensions are shown in millimeters (inches))


- NOTES:**
- 1- DIMENSIONING AND TOLERANCING AS PER ASME Y14.5 M- 1994.
  - 2- DIMENSIONS ARE SHOWN IN INCHES [MILLIMETERS].
  - 3- LEAD DIMENSION AND FINISH UNCONTROLLED IN L1.
  - 4- DIMENSION D, D1 & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
  - 5- DIMENSION b1, b3 & c1 APPLY TO BASE METAL ONLY.
  - 6- CONTROLLING DIMENSION : INCHES.
  - 7- THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS E1, D2 & E1
  - 8- DIMENSION E2 X HI DEFINE A ZONE WHERE STAMPING AND SINGULATION IRREGULARITIES ARE ALLOWED.
  - 9- OUTLINE CONFORMS TO JEDEC TO-220, EXCEPT A2 (max.) AND D2 (min.) WHERE DIMENSIONS ARE DERIVED FROM THE ACTUAL PACKAGE OUTLINE.

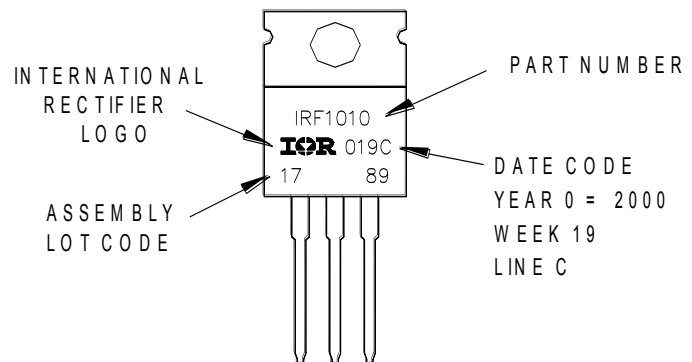
SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	3.56	4.83	.140	.190	
A1	0.51	1.40	.020	.055	
A2	2.03	2.92	.080	.115	
b	0.38	1.01	.015	.040	
b1	0.38	0.97	.015	.038	5
b2	1.14	1.78	.045	.070	
b3	1.14	1.73	.045	.068	5
c	0.36	0.61	.014	.024	
c1	0.36	0.56	.014	.022	5
D	14.22	16.51	.560	.650	4
D1	8.38	9.02	.330	.355	
D2	11.68	12.88	.460	.507	7
E	9.65	10.67	.380	.420	4,7
E1	6.86	8.89	.270	.350	7
E2	-	0.76	-	.030	8
e	2.54 BSC		.100 BSC		
e1	5.08 BSC		.200 BSC		
HI	5.84	6.86	.230	.270	7,8
L	12.70	14.73	.500	.580	
L1	3.56	4.06	.140	.160	3
ØP	3.54	4.06	.139	.161	
Q	2.54	3.42	.100	.135	

- LEAD ASSIGNMENTS**
- HERMETIC**
- 1- GATE
  - 2- COLLECTOR
  - 3- EMITTER
- HERMETIC PACKAGE**
- 1- GATE
  - 2- COLLECTOR
  - 3- EMITTER
- MARKS**
- 1- ANVIL
  - 2- CATHODE
  - 3- ANVIL

**TO-220AB Part Marking Information**

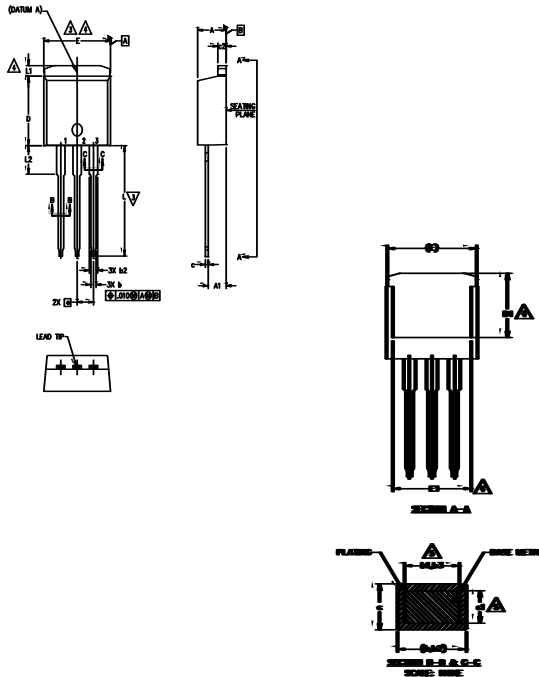
EXAMPLE: THIS IS AN IRF1010  
 LOT CODE 1789  
 ASSEMBLED ON WW 19, 2000  
 IN THE ASSEMBLY LINE "C"

Note: "P" in assembly line position indicates "Lead - Free"



TO-220AB packages are not recommended for Surface Mount Application.

Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

**TO-262 Package Outline (Dimensions are shown in millimeters (inches))**

**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
3. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 [.005"] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY.
4. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSION E, L1, D1 & E1.
5. DIMENSION b1 AND c1 APPLY TO BASE METAL ONLY.
6. CONTROLLING DIMENSION: INCH.
- 7.- OUTLINE CONFORM TO JEDEC TO-262 EXCEPT A1(max.), b(min.) AND D1(min.) WHERE DIMENSIONS DERIVED THE ACTUAL PACKAGE OUTLINE.

SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	4.06	4.83	.160	.190	
A1	2.03	3.02	.080	.119	
b	0.51	0.99	.020	.039	
b1	0.51	0.89	.020	.035	5
b2	1.14	1.78	.045	.070	
b3	1.14	1.73	.045	.068	5
c	0.38	0.74	.015	.029	
c1	0.38	0.58	.015	.023	5
c2	1.14	1.65	.045	.065	
D	8.38	9.65	.330	.380	3
D1	6.86	-	.270	-	4
E	9.65	10.67	.380	.420	3,4
E1	6.22	-	.245	-	4
e	2.54 BSC		.100 BSC		
L	13.46	14.10	.530	.555	
L1	-	1.65	-	.065	4
L2	3.56	3.71	.140	.146	

**LEAD ASSIGNMENTS**
**HEXFET**

- 1.- GATE
- 2.- DRAIN
- 3.- SOURCE
- 4.- DRAIN

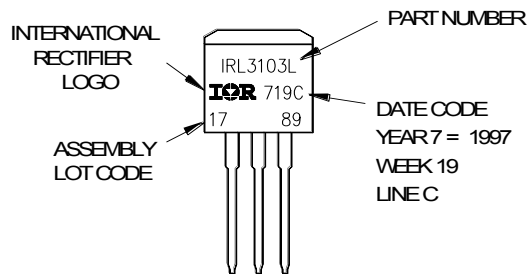
**IGBTs, CoPACK**

- 1.- GATE
- 2.- COLLECTOR
- 3.- EMITTER
- 4.- COLLECTOR

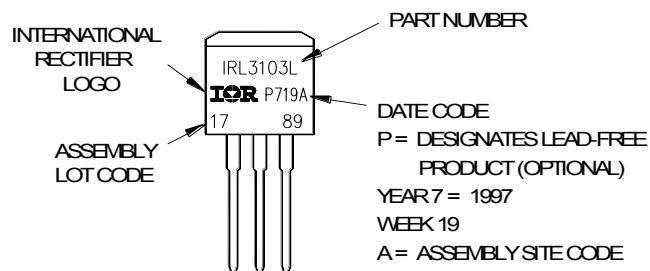
**TO-262 Part Marking Information**

EXAMPLE: THIS IS AN IRL3103L  
 LOT CODE 1789  
 ASSEMBLED ON VWV19, 1997  
 IN THE ASSEMBLY LINE "C"

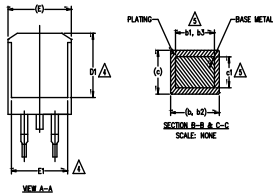
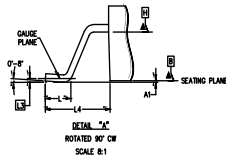
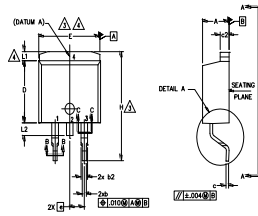
Note: "P" in assembly line position indicates "Lead - Free"



OR



Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

**D<sup>2</sup>Pak (TO-263AB) Package Outline (Dimensions are shown in millimeters (inches))**

**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
3. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 [0.005"] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY AT DATUM H.
4. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSION E, L1, D1 & E1.
5. DIMENSION b1 AND c1 APPLY TO BASE METAL ONLY.
6. DATUM A & B TO BE DETERMINED AT DATUM PLANE H.
7. CONTROLLING DIMENSION: INCH.
8. OUTLINE CONFORMS TO JEDEC OUTLINE TO-263AB.

SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	4.06	4.83	.160	.190	5
A1	0.00	0.254	.000	.010	
b	0.51	0.99	.020	.039	5
b1	0.51	0.89	.020	.035	
b2	1.14	1.78	.045	.070	5
b3	1.14	1.73	.045	.068	
c	0.38	0.74	.015	.029	5
c1	0.38	0.58	.015	.023	
c2	1.14	1.65	.045	.065	3
D	8.38	9.65	.330	.380	
D1	6.86	-	.270	-	4
E	9.65	10.67	.380	.420	3,4
E1	6.22	-	.245	-	4
e	2.54	BSC	.100	BSC	4
H	14.61	15.88	.575	.625	
L	1.78	2.79	.070	.110	4
L1	-	1.65	-	.066	
L2	1.27	1.78	-	.070	
L3	0.25	BSC	.010	BSC	
L4	4.78	5.28	.188	.208	

**LEAD ASSIGNMENTS**
**HEXFET**

- 1.- GATE
- 2, 4.- DRAIN
- 3.- SOURCE

**IGBTs, CoPACK**

- 1.- GATE
- 2, 4.- COLLECTOR
- 3.- EMITTER

**DIODES**

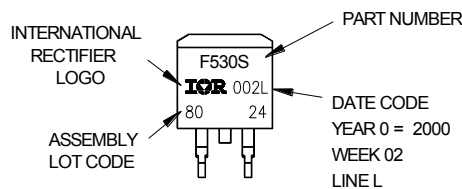
- 1.- ANODE \*
- 2, 4.- CATHODE
- 3.- ANODE

\* PART DEPENDENT.

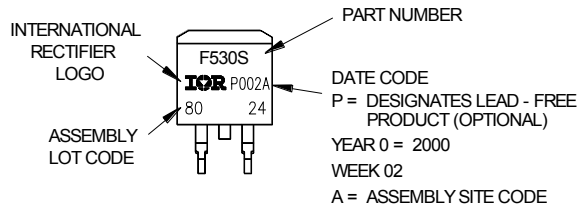
**D<sup>2</sup>Pak (TO-263AB) Part Marking Information**

EXAMPLE: THIS IS AN IRF530S WITH  
LOT CODE 8024  
ASSEMBLED ON VVW 02, 2000  
IN THE ASSEMBLY LINE "L"

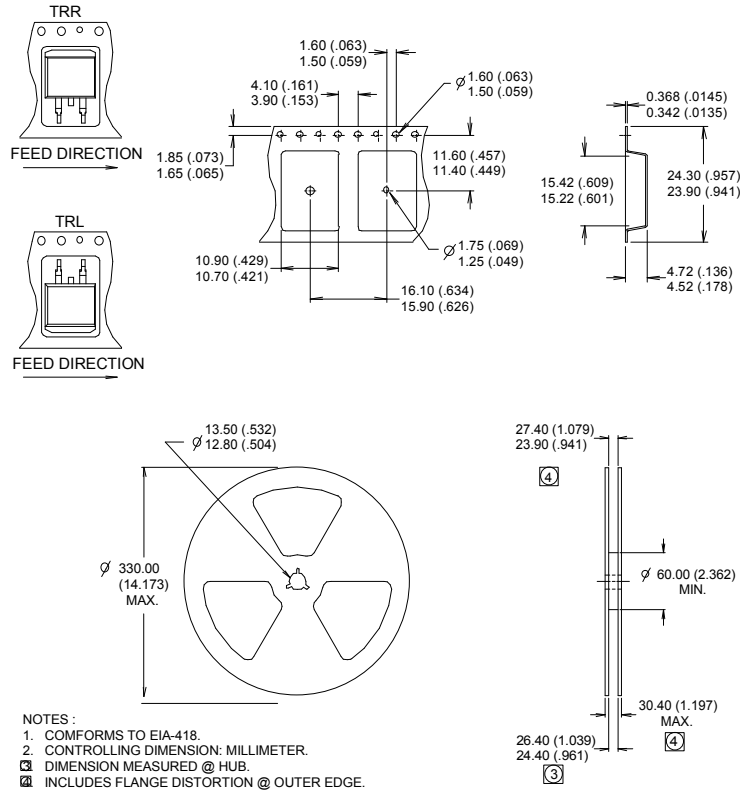
Note: "P" in assembly line position  
indicates "Lead - Free"



OR



Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

**D<sup>2</sup>Pak (TO-263AB) Tape & Reel Information** (Dimensions are shown in millimeters (inches))


Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

**Qualification Information<sup>†</sup>**

Qualification Level	Industrial (per JEDEC JESD47F) <sup>††</sup>	
Moisture Sensitivity Level	TO-220	N/A
	D <sup>2</sup> Pak	MSL 1
	TO-262	N/A
RoHS Compliant	Yes	

<sup>†</sup> Qualification standards can be found at International Rectifier's web site: <http://www.irf.com/product-info/reliability/>

<sup>††</sup> Applicable version of JEDEC standard at the time of product release.