

RMWV6416A Series

64Mb Advanced LPSRAM (4M word × 16bit / 8M word × 8bit)

R10DS0278EJ0100

Rev.1.00

2018.12.26

Description

The RMWV6416A Series is a family of 64-Mbit static RAMs organized 4,194,304-word × 16-bit, fabricated by Renesas's high-performance Advanced LPSRAM technologies. The RMWV6416A Series has realized higher density, higher performance and low power consumption. The RMWV6416A Series offers low power standby power dissipation; therefore, it is suitable for battery backup systems. It is offered in 48pin TSOP (I), 52pin μ TSOP (II) or 48-ball fine pitch ball grid array.

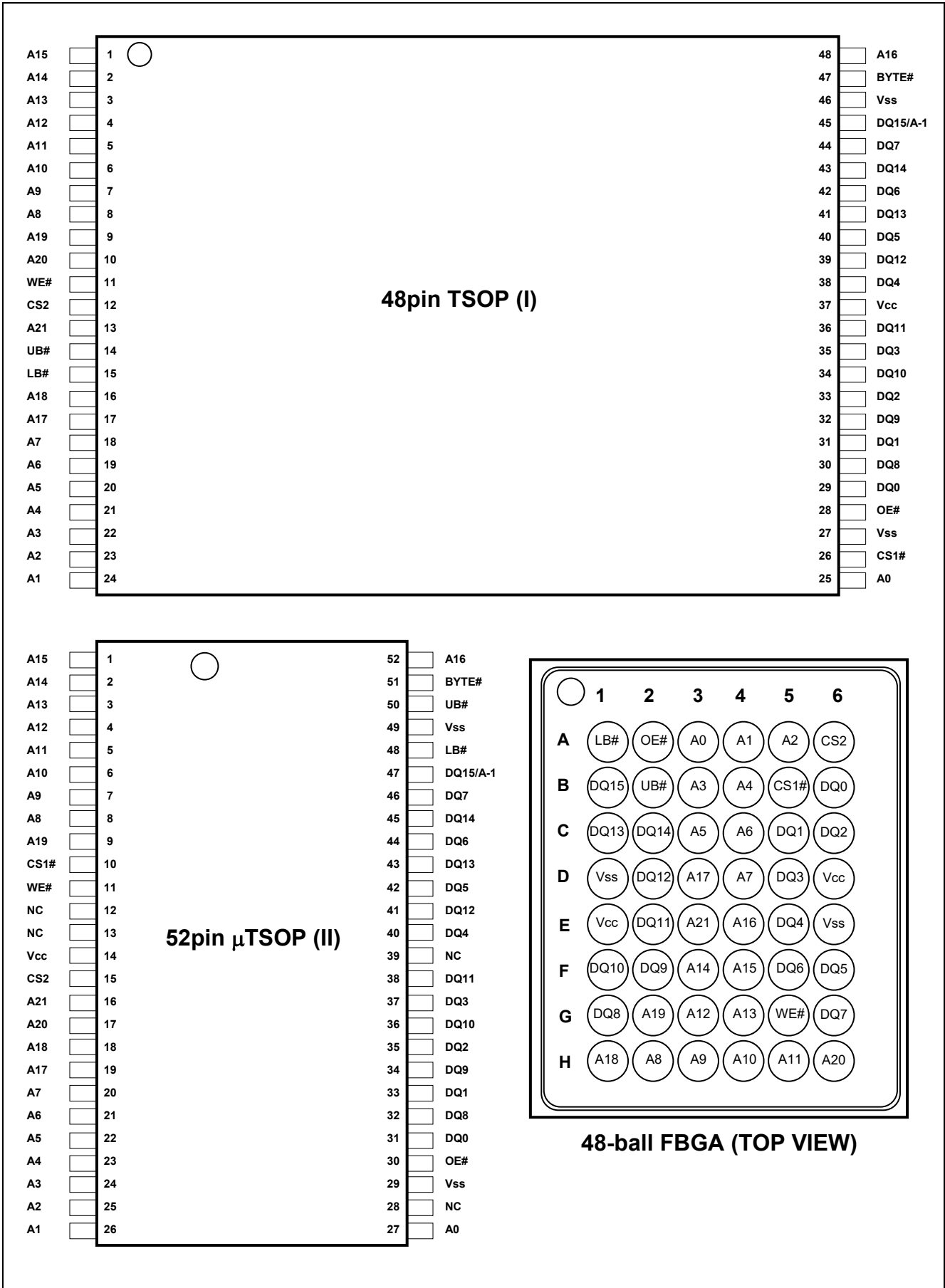
Features

- Single 3V supply: 2.7V to 3.6V
- Access time: 55ns (max.)
- Current consumption:
 - Standby: 1.2 μ A (typ.)
- Common data input and output
 - Three state output
- Directly TTL compatible
 - All inputs and outputs
- Battery backup operation

Part Name Information

Part Name	Access time	Temperature Range	Package
RMWV6416AGSA-5S2	55 ns	-40 ~ +85°C	12mm x 20mm 48pin plastic TSOP (I)
RMWV6416AGSD-5S2			10.79mm × 10.49mm 52pin plastic μ TSOP (II)
RMWV6416AGBG-5S2			48-ball FBGA with 0.75mm ball pitch

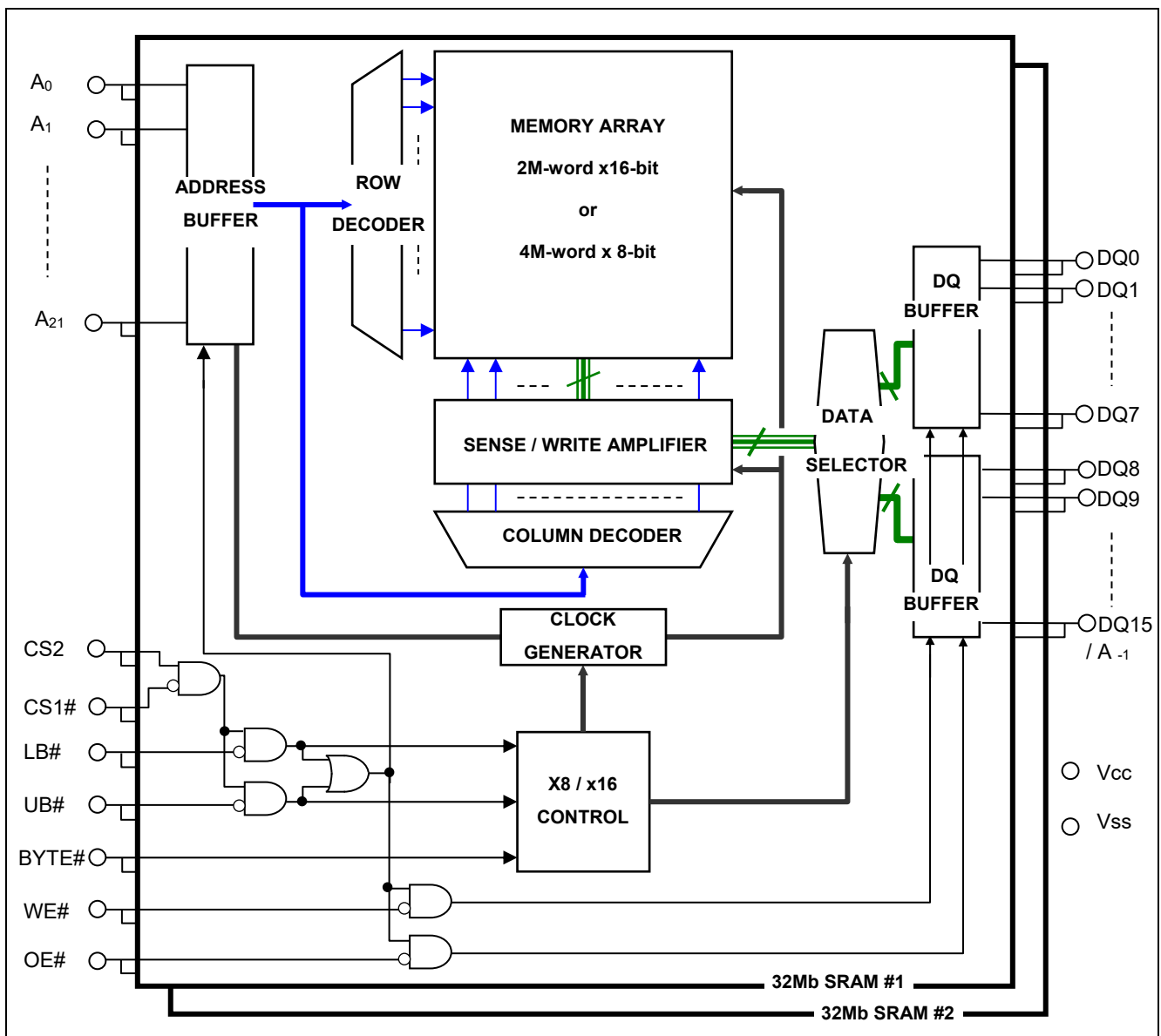
Pin Arrangement



Pin Description

Pin name	Function
Vcc	Power supply
Vss	Ground
A0 to A21	Address input (word mode)
A-1 to A21	Address input (byte mode)
DQ0 to DQ15	Data input/output
CS1#	Chip select 1
CS2	Chip select 2
OE#	Output enable
WE#	Write enable
LB#	Lower byte select
UB#	Upper byte select
BYTE#	Byte control mode enable
NC	No connection

Block Diagram



Note 1. BYTE# pin supported by only 48pin TSOP (I) and 52pin μTSOP (II) types.

Operation Table

CS1#	CS2	BYTE#	UB#	LB#	WE#	OE#	DQ0~7	DQ8~14	DQ15	Operation
H	X	X	X	X	X	X	High-Z	High-Z	High-Z	Stand-by
X	L	X	X	X	X	X	High-Z	High-Z	High-Z	Stand-by
X	X	H	H	H	X	X	High-Z	High-Z	High-Z	Stand-by
L	H	H	H	L	L	X	Din	High-Z	High-Z	Write in lower byte
L	H	H	H	L	H	L	Dout	High-Z	High-Z	Read in lower byte
L	H	H	H	L	H	H	High-Z	High-Z	High-Z	Output disable
L	H	H	L	H	L	X	High-Z	Din	Din	Write in upper byte
L	H	H	L	H	H	L	High-Z	Dout	Dout	Read in upper byte
L	H	H	L	H	H	H	High-Z	High-Z	High-Z	Output disable
L	H	H	L	L	L	X	Din	Din	Din	Word write
L	H	H	L	L	H	L	Dout	Dout	Dout	Word read
L	H	H	L	L	H	H	High-Z	High-Z	High-Z	Output disable
L	H	L	X	X	L	X	Din	High-Z	A-1	Byte write
L	H	L	X	X	H	L	Dout	High-Z	A-1	Byte read
L	H	L	X	X	H	H	High-Z	High-Z	A-1	Output disable

Note 2. H: V_{IH} L: V_{IL} X: V_{IH} or V_{IL}

3. BYTE# pin supported by only 48pin TSOP (I) and 52pin μ TSOP (II) types.
48-ball FBGA type equals BYTE#=H mode.

Absolute Maximum Ratings

Parameter	Symbol	Value	unit
Power supply voltage relative to V_{SS}	V_{CC}	-0.5 to +4.6	V
Terminal voltage on any pin relative to V_{SS}	V_T	-0.5^{*4} to $V_{CC}+0.3^{*5}$	V
Power dissipation	P_T	0.7	W
Operation temperature	T_{opr}	-40 to +85	°C
Storage temperature range	T_{stg}	-65 to +150	°C
Storage temperature range under bias	T_{bias}	-40 to +85	°C

Note 4. -2.0V for pulse \leq 30ns (full width at half maximum)

5. Maximum voltage is +4.6V.

DC Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Supply voltage	V_{CC}	2.7	3.0	3.6	V	
	V_{SS}	0	0	0	V	
Input high voltage	V_{IH}	2.2	—	$V_{CC}+0.3$	V	
Input low voltage	V_{IL}	-0.3	—	0.6	V	6
Ambient temperature range	T_a	-40	—	+85	°C	

Note 6. -2.0V for pulse \leq 30ns (full width at half maximum)

DC Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test conditions ⁷	
Input leakage current	$ I_{LI} $	—	—	1	μA	$V_{in} = V_{SS} \text{ to } V_{CC}$	
Output leakage current	$ I_{LO} $	—	—	1	μA	CS1# = V_{IH} or CS2 = V_{IL} or OE# = V_{IH} or WE# = V_{IL} or LB# = UB# = V_{IH} , $V_{I/O} = V_{SS} \text{ to } V_{CC}$	
Average operating current	I_{CC1}	—	29 ^{*8}	38	mA	Cycle = 55ns, duty = 100%, $I_{I/O} = 0\text{mA}$, CS1# = V_{IL} , CS2 = V_{IH} , Others = V_{IH}/V_{IL}	
	I_{CC2}	—	2.5 ^{*8}	5	mA	Cycle = 1 μs , duty = 100%, $I_{I/O} = 0\text{mA}$, CS1# $\leq 0.2\text{V}$, CS2 $\geq V_{CC}-0.2\text{V}$, $V_{IH} \geq V_{CC}-0.2\text{V}$, $V_{IL} \leq 0.2\text{V}$	
Standby current	I_{SB}	—	0.1 ^{*8}	0.3	mA	CS2 = V_{IL} , Others = $V_{SS} \text{ to } V_{CC}$	
Standby current	I_{SB1}	—	1.2 ^{*8}	8	μA	$\sim +25^{\circ}\text{C}$	$V_{in} = V_{SS} \text{ to } V_{CC}$, (1) CS2 $\leq 0.2\text{V}$ or (2) CS1# $\geq V_{CC}-0.2\text{V}$, CS2 $\geq V_{CC}-0.2\text{V}$ or (3) LB# = UB# $\geq V_{CC}-0.2\text{V}$, CS1# $\leq 0.2\text{V}$, CS2 $\geq V_{CC}-0.2\text{V}$
		—	2 ^{*9}	12	μA	$\sim +40^{\circ}\text{C}$	
		—	—	34	μA	$\sim +70^{\circ}\text{C}$	
		—	—	46	μA	$\sim +85^{\circ}\text{C}$	
Output high voltage	V_{OH}	2.4	—	—	V	$I_{OH} = -1\text{mA}$	
Output low voltage	V_{OL}	—	—	0.4	V	$I_{OL} = 2\text{mA}$	

Note 7. BYTE# pin supported by only 48pin TSOP (I) and 52pin μTSOP (II) types.

BYTE# $\geq V_{CC} - 0.2\text{V}$ or BYTE# $\leq 0.2\text{V}$

8. Typical parameter indicates the value for the center of distribution at 3.0V ($T_a=25^{\circ}\text{C}$), and not 100% tested.

9. Typical parameter indicates the value for the center of distribution at 3.0V ($T_a=40^{\circ}\text{C}$), and not 100% tested.

Capacitance

($T_a = 25^{\circ}\text{C}$, $f = 1\text{MHz}$)

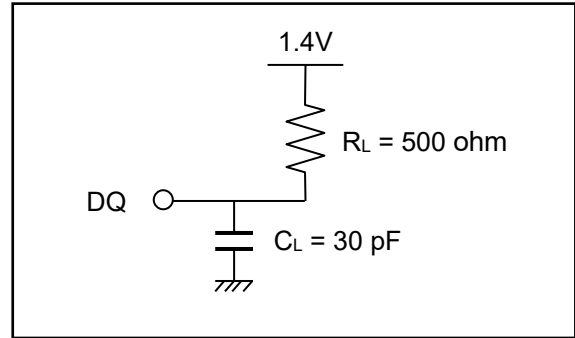
Parameter	Symbol	Min.	Typ.	Max.	Unit	Test conditions	Note
Input capacitance	C_{in}	—	—	20	pF	$V_{in} = 0\text{V}$	10
Input / output capacitance	$C_{I/O}$	—	—	20	pF	$V_{I/O} = 0\text{V}$	10

Note 10. This parameter is sampled and not 100% tested.

AC Characteristics

Test Conditions ($V_{CC} = 2.7V \sim 3.6V$, $T_a = -40 \sim +85^{\circ}C$)

- Input pulse levels:
 $V_{IL} = 0.4V$, $V_{IH} = 2.4V$
- Input rise and fall time: 5ns
- Input and output timing reference level: 1.4V
- Output load: See figures (Including scope and jig)



Read Cycle

Parameter	Symbol	Min.	Max.	Unit	Note
Read cycle time	t_{RC}	55		ns	
Address access time	t_{AA}	—	55	ns	
Chip select access time	t_{ACS1}	—	55	ns	
	t_{ACS2}	—	55	ns	
Output enable to output valid	t_{OE}	—	25	ns	
Output hold from address change	t_{OH}	10	—	ns	
LB#, UB# access time	t_{BA}	—	55	ns	
Chip select to output in low-Z	t_{CLZ1}	10	—	ns	11,12
	t_{CLZ2}	10	—	ns	11,12
LB#, UB# enable to low-Z	t_{BLZ}	5	—	ns	11,12
Output enable to output in low-Z	t_{OLZ}	5	—	ns	11,12
Chip deselect to output in high-Z	t_{CHZ1}	0	20	ns	11,12,13
	t_{CHZ2}	0	20	ns	11,12,13
LB#, UB# disable to high-Z	t_{BHZ}	0	20	ns	11,12,13
Output disable to output in high-Z	t_{OHZ}	0	20	ns	11,12,13

Note 11. This parameter is sampled and not 100% tested.

12. At any given temperature and voltage condition, t_{CHZ1} max is less than t_{CLZ1} min, t_{CHZ2} max is less than t_{CLZ2} min, t_{BHZ} max is less than t_{BLZ} min, and t_{OHZ} max is less than t_{OLZ} min, for any device.

13. t_{CHZ1} , t_{CHZ2} , t_{BHZ} and t_{OHZ} are defined as the time when the DQ pins enter a high-impedance state and are not referred to the DQ levels.

Write Cycle

Parameter	Symbol	Min.	Max.	Unit	Note
Write cycle time	t_{WC}	55	—	ns	
Address valid to write end	t_{AW}	45	—	ns	
Chip select to write end	t_{CW}	45	—	ns	
Write pulse width	t_{WP}	40	—	ns	14
LB#,UB# valid to write end	t_{BW}	45	—	ns	
Address setup time to write start	t_{AS}	0	—	ns	
Write recovery time from write end	t_{WR}	0	—	ns	
Data to write time overlap	t_{DW}	25	—	ns	
Data hold from write end	t_{DH}	0	—	ns	
Output enable from write end	t_{OW}	5	—	ns	15
Output disable to output in high-Z	t_{OHZ}	0	20	ns	15,16
Write to output in high-Z	t_{WHZ}	0	20	ns	15,16

Note 14. t_{WP} is the interval between write start and write end.

A write starts when all of (CS1#), (CS2), (WE#) and (one or both of LB# and UB#) become active.

A write is performed during the overlap of a low CS1#, a high CS2, a low WE# and a low LB# or a low UB#.

A write ends when any of (CS1#), (CS2), (WE#) or (one or both of LB# and UB#) becomes inactive.

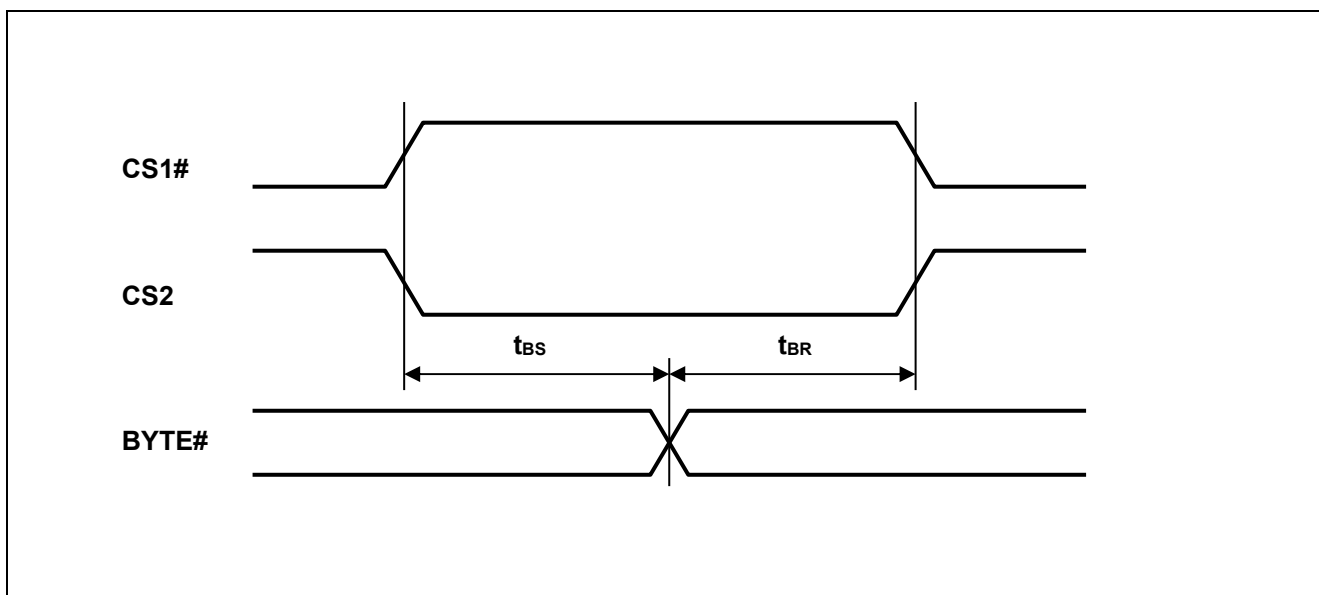
15. This parameter is sampled and not 100% tested.

16. t_{OHZ} and t_{WHZ} are defined as the time when the DQ pins enter a high-impedance state and are not referred to the DQ levels.

BYTE# Timing Conditions (BYTE# pin supported by only 48pin TSOP (I) and 52pin μ TSOP (II) types)

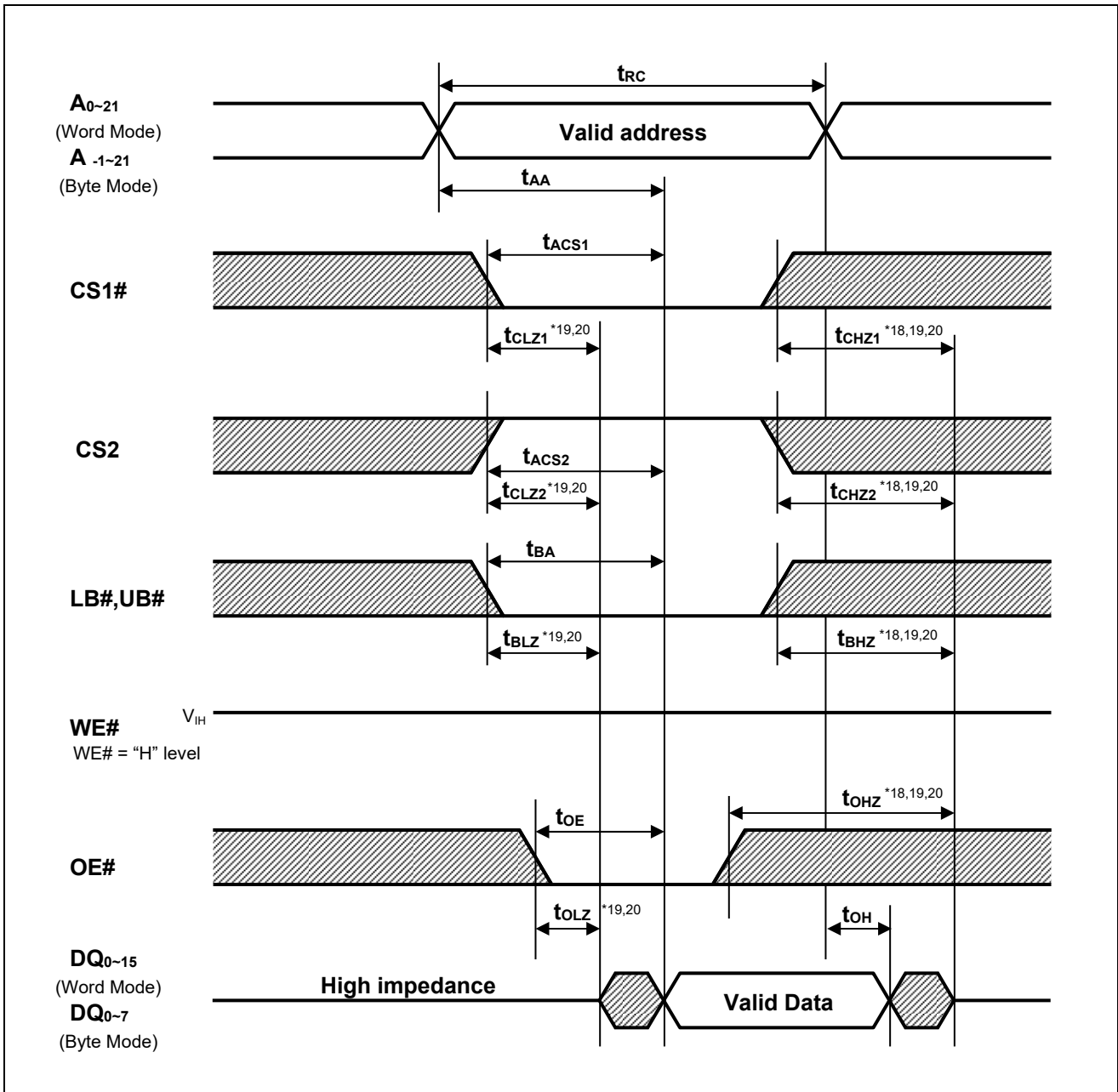
Parameter	Symbol	Min.	Max.	Unit	Note
Byte setup time	t_{BS}	5	-	ms	
Byte recovery time	t_{BR}	5	-	ms	

BYTE# Timing Waveforms



Timing Waveforms

Read Cycle^{*17}



Note 17. BYTE# pin supported by only 48pin TSOP (I) and 52pin μ TSOP (II) types.

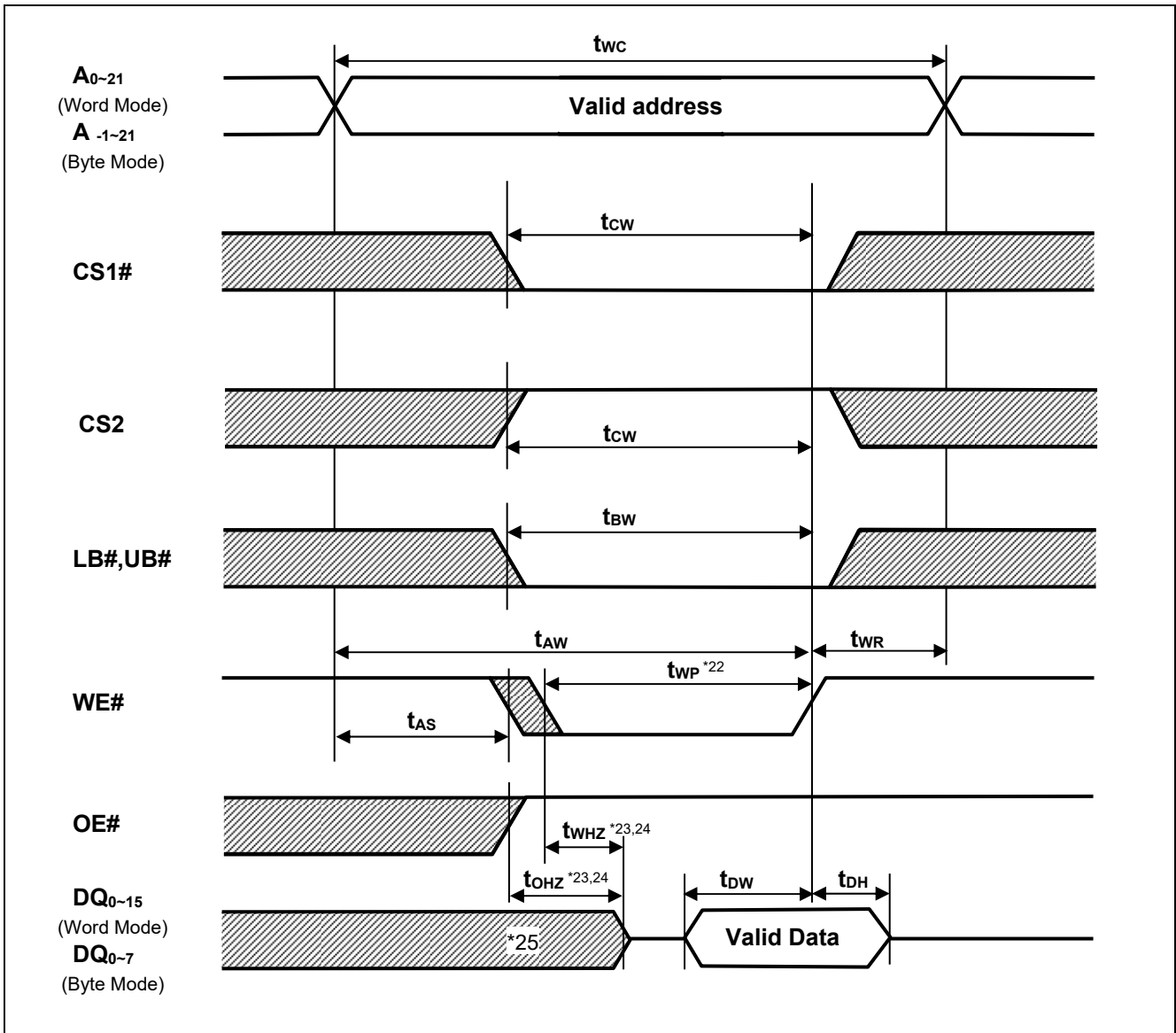
BYTE# $\geq V_{CC} - 0.2V$ (Word mode) or BYTE# $\leq 0.2V$ (Byte mode)

18. t_{CHZ1} , t_{CHZ2} , t_{BHZ} and t_{OHZ} are defined as the time when the DQ pins enter a high-impedance state and are not referred to the DQ levels.

19. This parameter is sampled and not 100% tested.

20. At any given temperature and voltage condition, t_{CHZ1} max is less than t_{CLZ1} min, t_{CHZ2} max is less than t_{CLZ2} min, t_{BHZ} max is less than t_{BLZ} min, and t_{OHZ} max is less than t_{OLZ} min, for any device.

Write Cycle (1)^{*21} (WE# CLOCK, OE#="H" while writing)



Note 21. BYTE# pin supported by only 48pin TSOP (I) and 52pin μ TSOP (II) types.

BYTE# $\geq V_{CC} - 0.2V$ (Word mode) or BYTE# $\leq 0.2V$ (Byte mode)

22. t_{WP} is the interval between write start and write end.

A write starts when all of (CS1#), (CS2), (WE#) and (one or both of LB# and UB#) become active.

A write is performed during the overlap of a low CS1#, a high CS2, a low WE# and a low LB# or a low UB#.

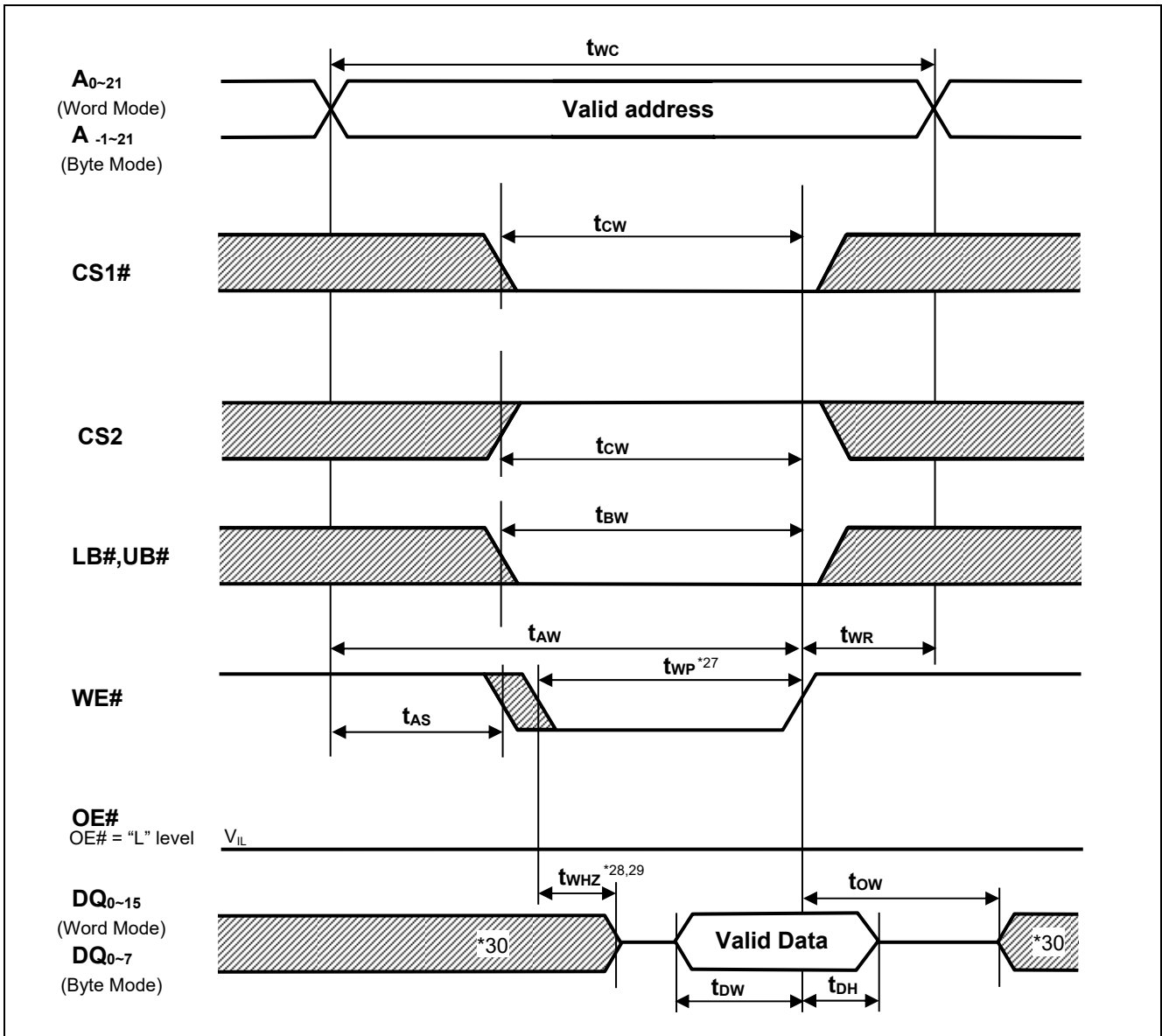
A write ends when any of (CS1#), (CS2), (WE#) or (one or both of LB# and UB#) becomes inactive.

23. t_{OHZ} and t_{WHZ} are defined as the time when the DQ pins enter a high-impedance state and are not referred to the DQ levels.

24. This parameter is sampled and not 100% tested.

25. During this period, DQ pins are in the output state so input signals must not be applied to the DQ pins.

Write Cycle (2)^{*26} (WE# CLOCK, OE# Low Fixed)



Note 26. BYTE# pin supported by only 48pin TSOP (I) and 52pin μ TSOP (II) types.

BYTE# $\geq V_{cc} - 0.2V$ (Word mode) or BYTE# $\leq 0.2V$ (Byte mode)

27. t_{WP} is the interval between write start and write end.

A write starts when all of (CS1#), (CS2), (WE#) and (one or both of LB# and UB#) become active.

A write is performed during the overlap of a low CS1#, a high CS2, a low WE# and a low LB# or a low UB#.

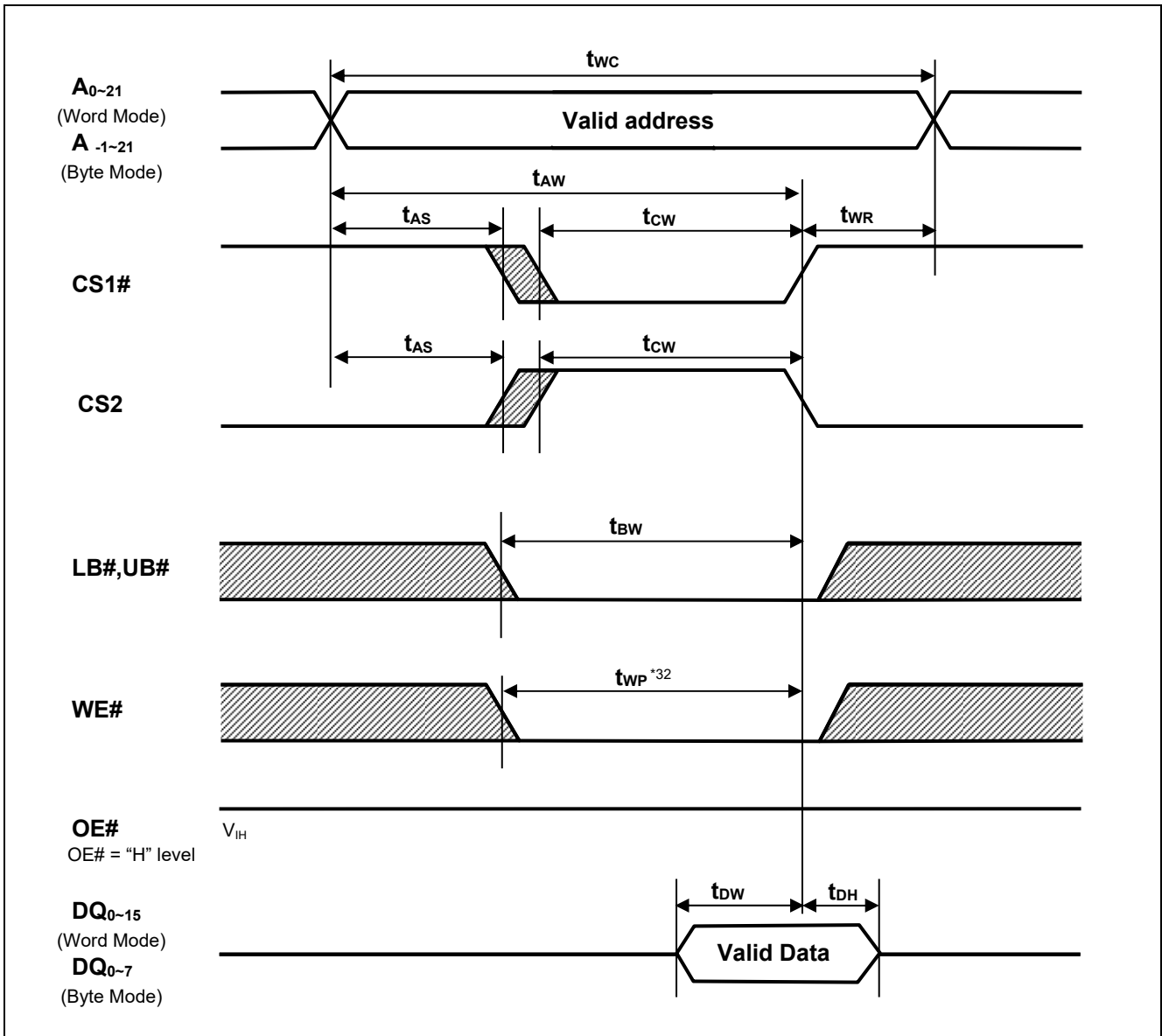
A write ends when any of (CS1#), (CS2), (WE#) or (one or both of LB# and UB#) becomes inactive.

28. t_{WHZ} is defined as the time when the DQ pins enter a high-impedance state and are not referred to the DQ levels.

29. This parameter is sampled and not 100% tested.

30. During this period, DQ pins are in the output state so input signals must not be applied to the DQ pins.

Write Cycle (3)^{*31} (CS1#, CS2 CLOCK)



Note 31. BYTE# pin supported by only 48pin TSOP (I) and 52pin μ TSOP (II) types.

BYTE# $\geq V_{CC} - 0.2V$ (Word mode) or BYTE# $\leq 0.2V$ (Byte mode)

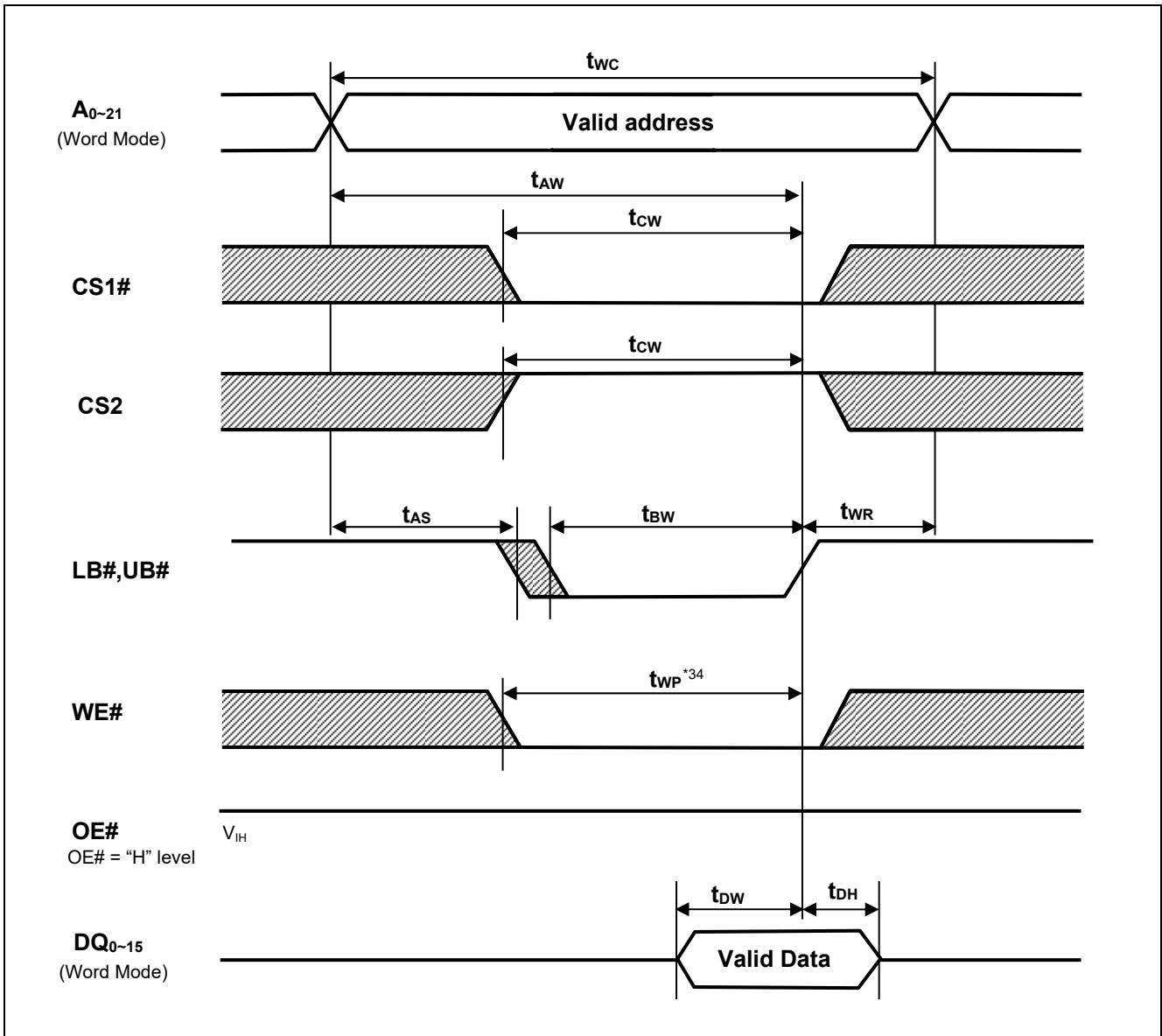
32. t_{WP} is the interval between write start and write end.

A write starts when all of (CS1#), (CS2), (WE#) and (one or both of LB# and UB#) become active.

A write is performed during the overlap of a low CS1#, a high CS2, a low WE# and a low LB# or a low UB#.

A write ends when any of (CS1#), (CS2), (WE#) or (one or both of LB# and UB#) becomes inactive.

Write Cycle (4)^{*33} (LB#, UB# CLOCK, Word Mode)



Note 33. BYTE# pin supported by only 48pin TSOP (I) and 52pin μ TSOP (II) types.
 BYTE# $\geq V_{CC} - 0.2V$ (Word mode)

34. t_{WP} is the interval between write start and write end.
 A write starts when all of (CS1#), (CS2), (WE#) and (one or both of LB# and UB#) become active.
 A write is performed during the overlap of a low CS1#, a high CS2, a low WE# and a low LB# or a low UB#.
 A write ends when any of (CS1#), (CS2), (WE#) or (one or both of LB# and UB#) becomes inactive.

Low V_{CC} Data Retention Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test conditions ^{*35,36}	
V _{CC} for data retention	V _{DR}	1.5	—	3.6	V	Vin ≥ 0V (1) CS2 ≤ 0.2V or (2) CS1# ≥ V _{CC} -0.2V, CS2 ≥ V _{CC} -0.2V or (3) LB# = UB# ≥ V _{CC} -0.2V, CS1# ≤ 0.2V, CS2 ≥ V _{CC} -0.2V	
Data retention current	I _{CCDR}	—	1.2 ^{*37}	8	μA	~+25°C	Vin ≥ 0V (1) CS2 ≤ 0.2V or (2) CS1# ≥ V _{CC} -0.2V, CS2 ≥ V _{CC} -0.2V or (3) LB# = UB# ≥ V _{CC} -0.2V, CS1# ≤ 0.2V, CS2 ≥ V _{CC} -0.2V
		—	2 ^{*38}	12	μA	~+40°C	
		—	—	34	μA	~+70°C	
		—	—	46	μA	~+85°C	
Chip deselect time to data retention	t _{CDR}	0	—	—	ns	See retention waveform.	
Operation recovery time	t _R	5	—	—	ms		

Note 35. BYTE# pin supported by only 48pin TSOP (I) and 52pin μTSOP (II) types.

BYTE# ≥ V_{CC} - 0.2V or BYTE# ≤ 0.2V

36. CS2 controls address buffer, WE# buffer, CS1# buffer, OE# buffer, LB# buffer, UB# buffer and DQ buffer.

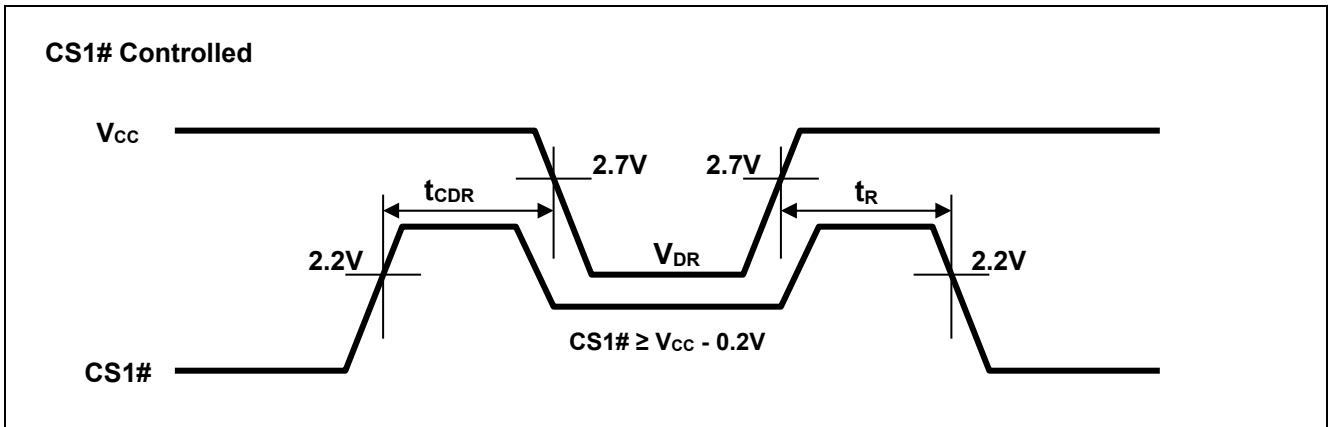
If CS2 controls data retention mode, Vin levels (address, WE#, CS1#, OE#, LB#, UB#, DQ) can be in the high impedance state. If CS1# controls data retention mode, CS2 must be CS2 ≥ V_{CC}-0.2V or CS2 ≤ 0.2V.

The other inputs levels (address, WE#, OE#, LB#, UB#, DQ) can be in the high-impedance state.

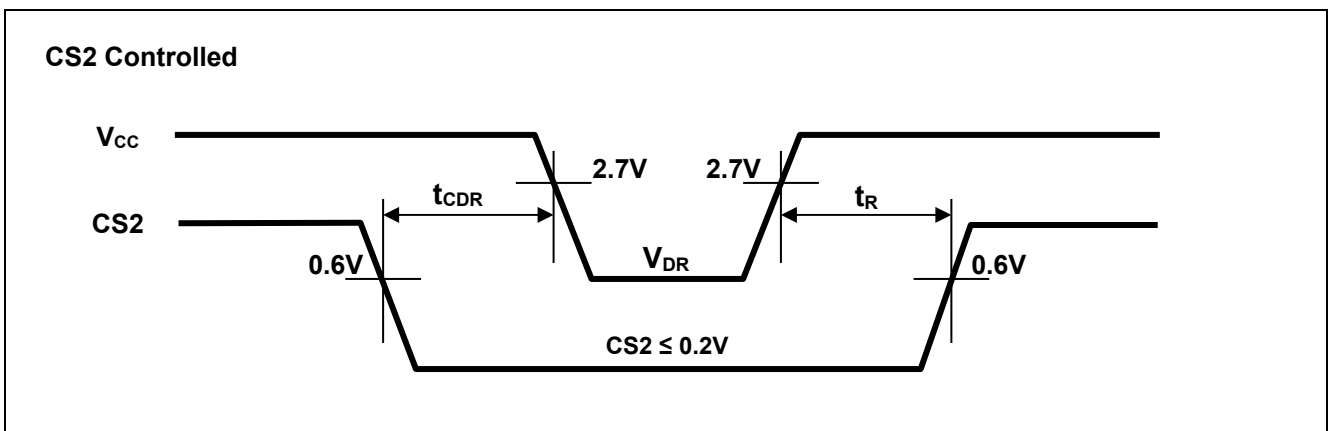
37. Typical parameter indicates the value for the center of distribution at 3.0V (Ta=25°C), and not 100% tested.

38. Typical parameter indicates the value for the center of distribution at 3.0V (Ta=40°C), and not 100% tested.

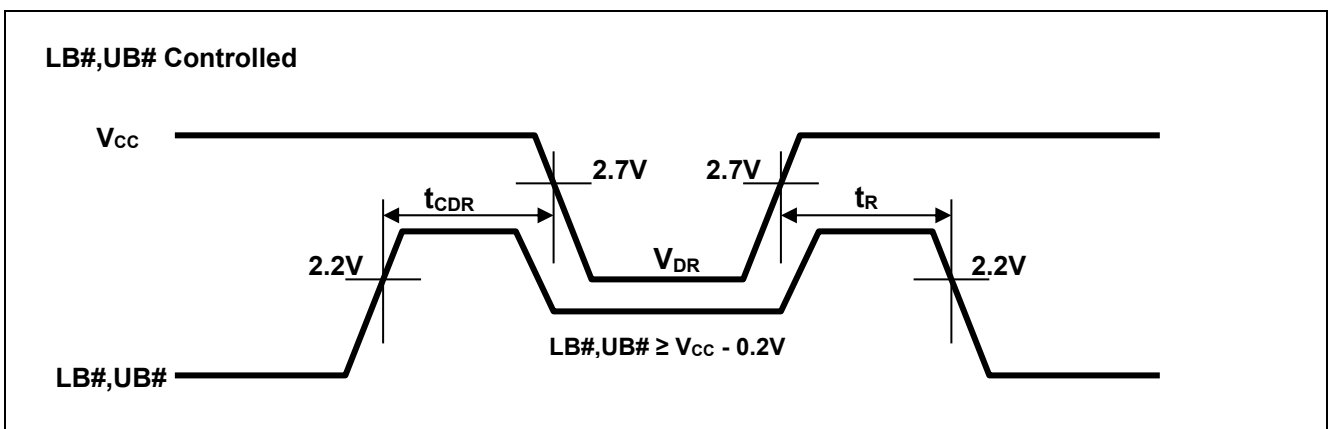
Low Vcc Data Retention Timing Waveforms (CS1# controlled)^{*39}



Low Vcc Data Retention Timing Waveforms (CS2 controlled)^{*39}



Low Vcc Data Retention Timing Waveforms (LB#,UB# controlled, Word Mode)^{*40}



Note 39. BYTE# pin supported by only 48pin TSOP (I) and 52pin μ TSOP (II) types.
 BYTE# ≥ V_{CC} - 0.2V or BYTE# ≤ 0.2V

40. BYTE# pin supported by only 48pin TSOP (I) and 52pin μ TSOP (II) types.
 BYTE# ≥ V_{CC} - 0.2V (Word mode)

Revision History	RMWV6416A Series Data Sheet
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Rev.	Date	Description	
		Page	Summary
1.00	2018.12.26	—	First Edition issued

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